Dr Chris McCarthy

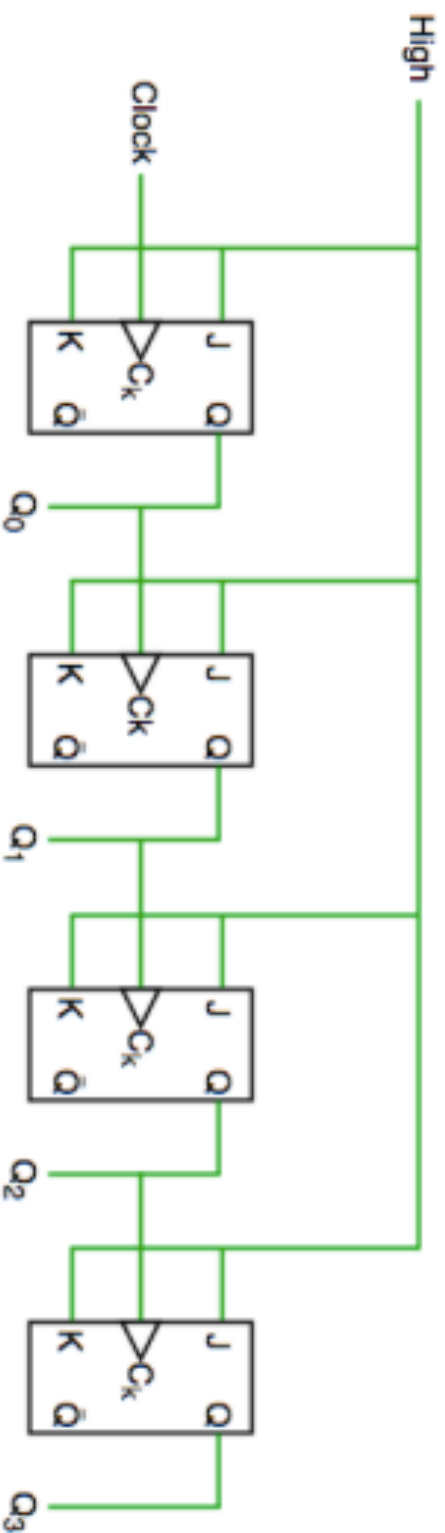SWINBURNE UNIVERSITY OF TECHNOLOGY

COS10004 Computer Systems

Lecture 3.3: More ripple counters

RIPPLE COUNTER

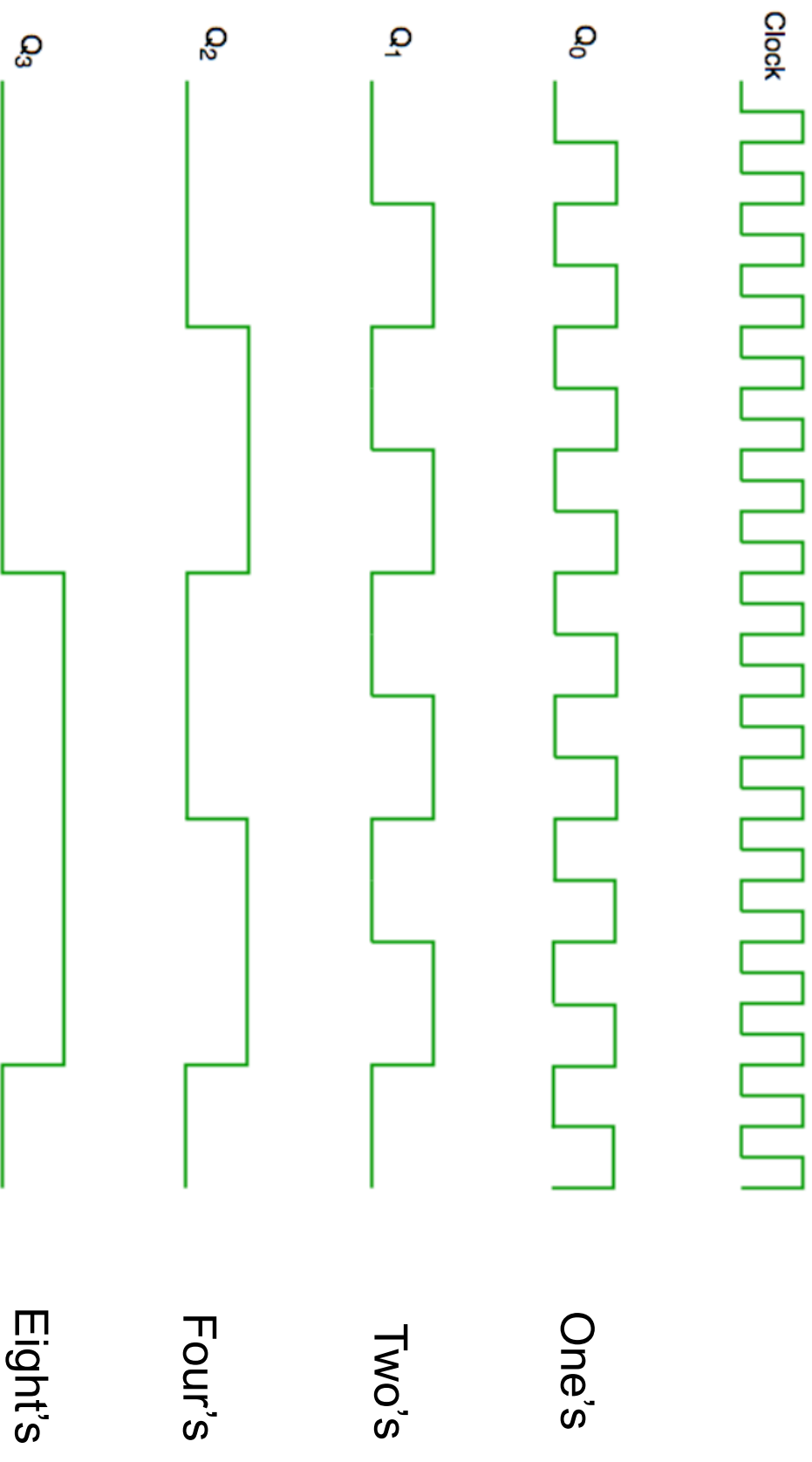> Ripple counters utilise the toggle setting of J-K Flip Flops:

RIPPLE COUNTER

Clock

Q0 — One's

Q1 — Two's

Q2 — Four's

Q3 — Eight's

MORE COUNTERS

∨ Suppose we want to count up to a power of two? For example 6

∨ Why 6 you ask ?

MORE COUNTERS

> Suppose we want to count in a modulo that is not a neat power of two? For example 6

> Why 6 you ask ?

MOD 6 COUNTER

∨ What do we need to do?

   – An incrementing counter

   – A forced reset of all Flip Flops to zero when the counter reaches 6

> What do we need to do ?

– An incrementing counter:

falling edge trigger – easy!

– A forced reset of all Flip Flops to zero when the counter reaches 6:

some extra logic gates to monitor things, and trigger a FF reset - not too tricky
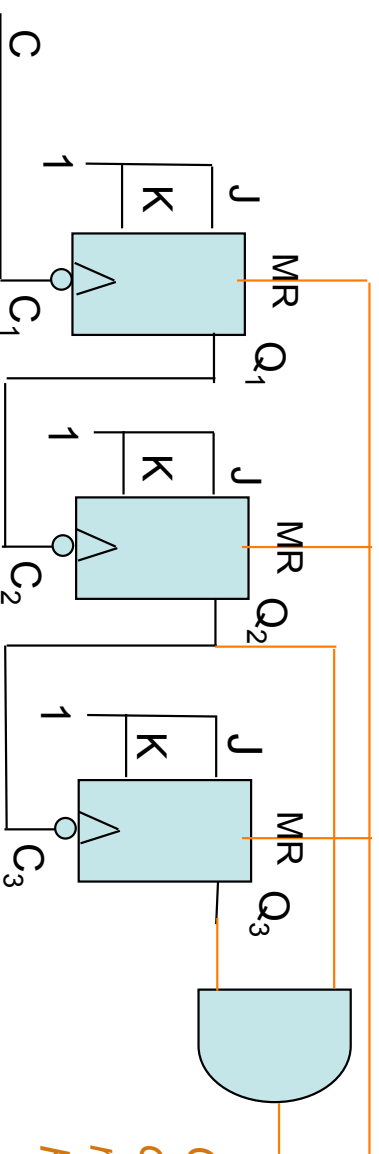
Modulo 6 counter

> Have a go !

– Detect the illegal state (6)

– Reset the FFs to wrap around to zero

∨ Detecting the first illegal state (6 in this case) and immediately resetting to 0 (don't wait for the clock) by using the asynchronous master reset (MR) or CLR'

– This circuit uses a *cascading clock*

Goes 1 if counter on 6 or 7 forcing the master resets to clear each F/ F to zero

SUMMARY

∨ Counters don't have to wrap around at powers of 2

∨ Can use outputs of FFs and approrpaite logic gates to detect "illegal state"

∨ Slight problem though:

   – Master reset is asynchronous

   – The illegal state momentarily still happens !

   – We can do better ! ….in fact .. We NEED to do better

   ….next lecture