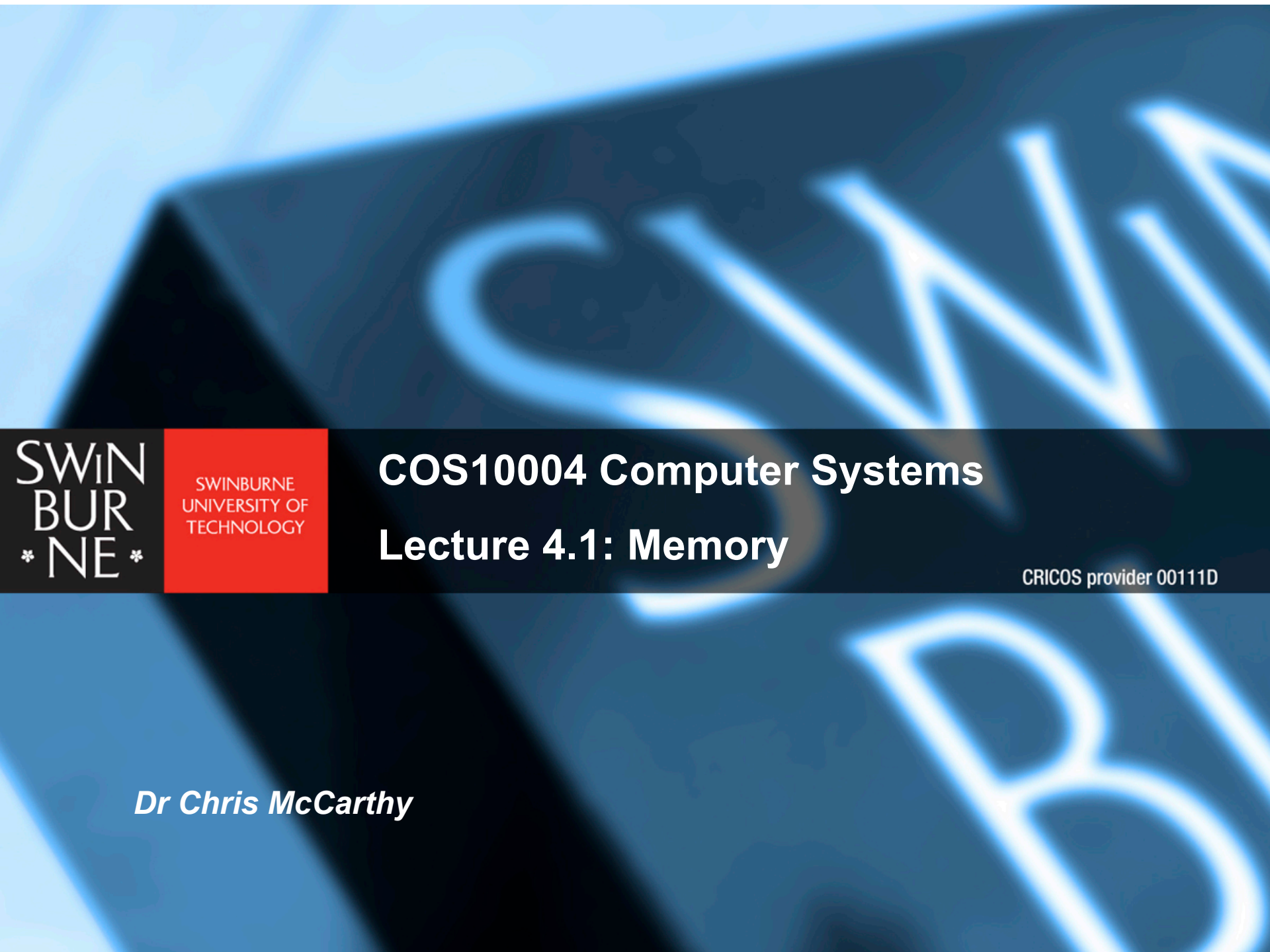


COS10004 Computer Systems

Lecture 4.1: Memory

CRICOS provider 00111D

Dr Chris McCarthy

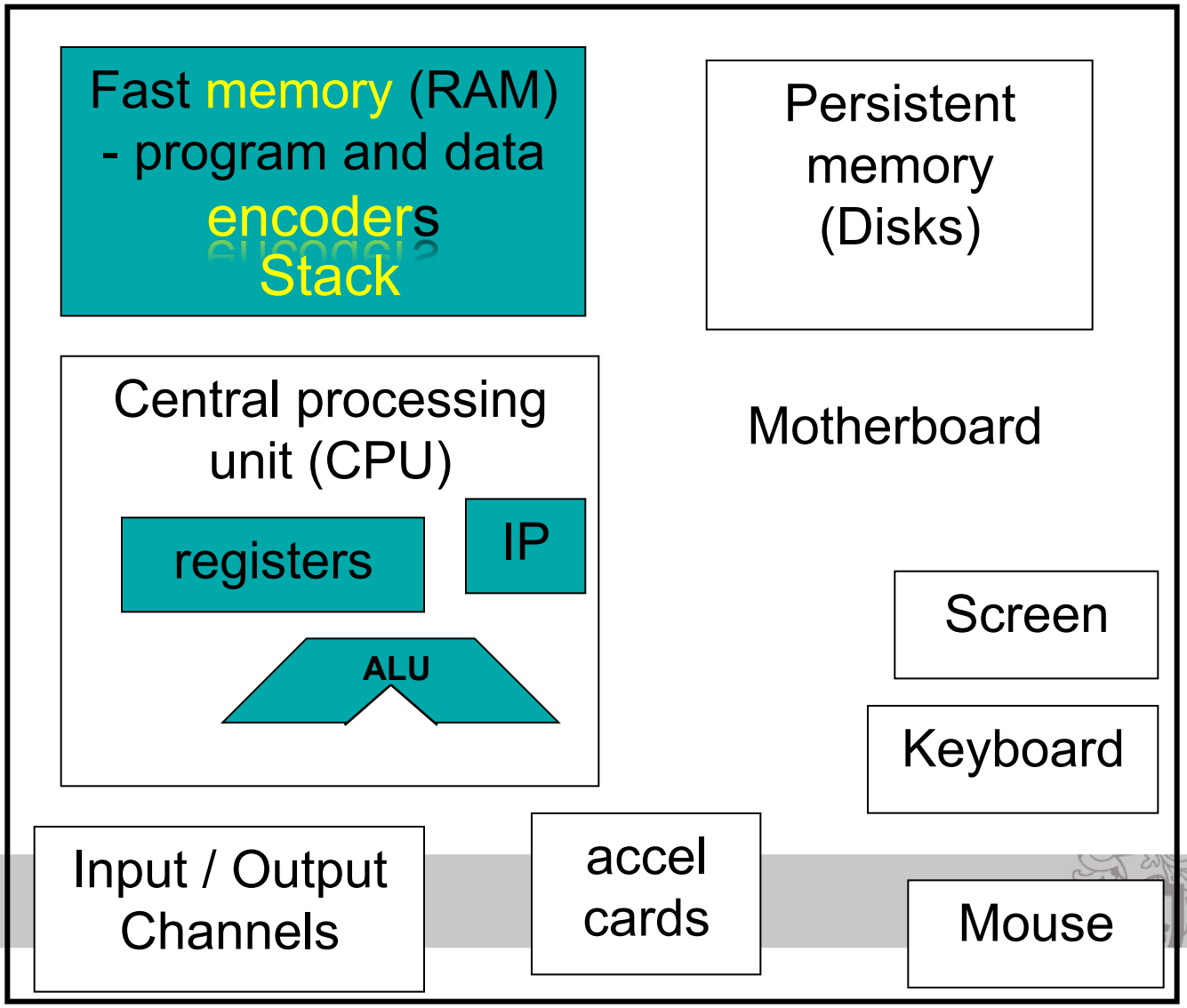
_start:

THIS WEEK:

Memory, encoders and stacks

- Memory - different types
- Need encoders/decoders for interrupt handling -
  - 4 to 2 priority encoder used to detect hardware interrupts
  - 2 to 4 used for multiplexing and memory addressing.
- Stacks look like n-dimensional shift registers

Building a computer? Things we need:



TYPES OF MEMORY - 1

ROM (read only memory): All reading at full speed. Just get the address and go there.
– contents built-in at time of manufacture.

- PROM – Programmable read only memory. Programmed by a once-only irreversible operation, e.g. in factory.
- EPROM – Erasable Programmable read only memory. Can be removed from the computer and erased and programmed (slowly) by using special apparatus (e.g. UV light).
  - Sometimes called “field-programmable”, i.e. “in the field”
  - Bulk erased: every byte erased at the same time
  - Byte programmable: write bytes one by one.
- EEPROM – Electrically erasable read only memory. Can be erased and reprogrammed byte by byte in situ, but writing is slower than normal reading.

TYPES OF MEMORY - 2

RAM random access memory.

- A misnomer it should be RWM (read write memory) – both ROM and RAM allow random access.

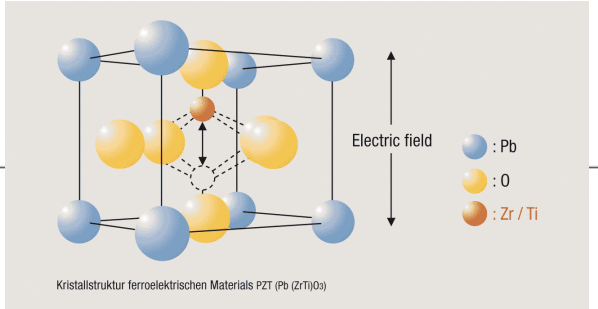
> **Static RAM** – retains information until power removed. Fast, larger area of silicon per byte, modest power requirement.

> **Dynamic RAM** - retains information as long as the contents are refreshed frequently enough. Smaller area of silicon per byte, low power requirement.
  - Does not use flip-flops.
  - Uses tiny capacitors to store electric charge.
  - Because the charge leaks away have to rewrite (“refresh”) every few milliseconds.

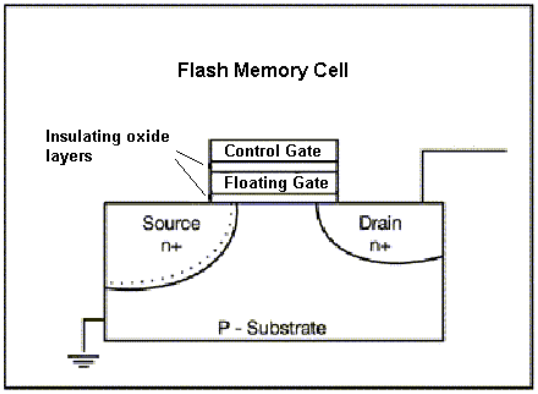
TYPES OF MEMORY - 3

- SDRAM (Synchronous DRAM)
  - Hybrid of dynamic and static technology
  - “clocked” by the main CPU clock
- DDR (double data rate) SDRAM
  - Chips produce data on rising and falling edges of the clock
  - Higher data rates, eg 64 bits / nsec

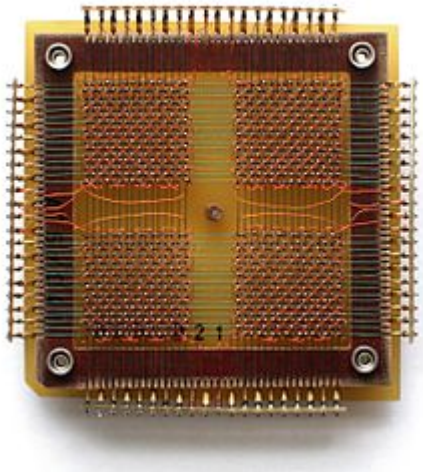
TYPES OF MEMORY - 3



- FRAM - Ferroelectric RAM
  - Uses atom position in unit cell (in theory). Actual density about the same as DRAM. Non-volatile (no power / refresh to keep state).
  - Used in specialist devices (where you never want to "turn it off and on again" to fix it). Random access



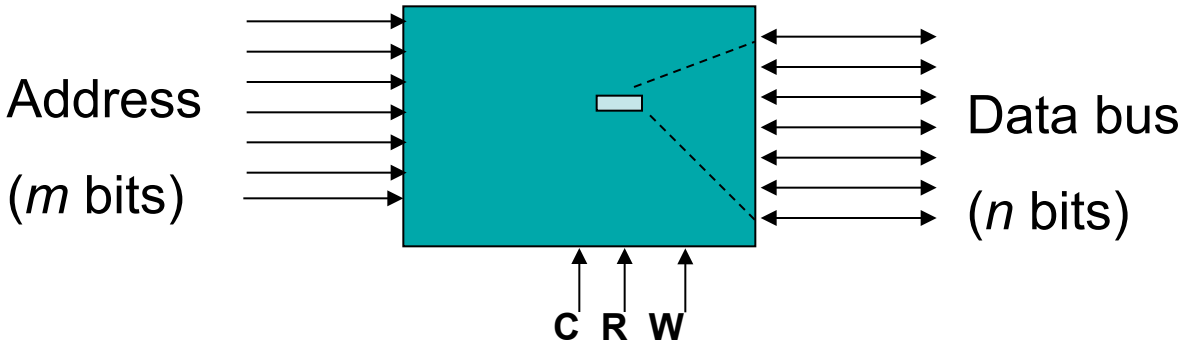
- Flash memory - (EEPROM)
  - Charge stored between insulators. Write bit by injecting electrons through a barrier layer (physically damaging it). Used in USB drives. Good for about 30,000 writes. Random access
- Core memory
  - Magnetic "core" memory: each bit is stored as the direction of magnetisation of tiny rings (like doughnuts). 1955-1975. 1000 x slower than DRAM.



Memory Addressing

- RAM consists of one or many chips
- RAM is organised into **words** (of e.g. 32 bits)
- Words are grouped into **pages**.
- Words are selected by an **address**
  - A number of *m* bits
- Control bits specify whether to read or write
  - Bits stored in the selected word go *to* or *from* the data bus

A a byte is typically the **smallest addressable chunk** of memory. We can address the 4 bytes in a 32-bit word, but we can't address individual **bits** in each byte. Exceptions include Micron 3D-XPoint



EXAMPLE

- Consider a Computer with 1024 Mbyte (1GB) RAM
  - How many bits needed to address all bytes ?

  Hint: $1024 = 2^{10}$ and $1{,}000{,}000 \sim= 2^{20}$

- Alternative to normal RAM addressing:
  - Hardware stack

LECTURE 4.1 SUMMARY

- Many different types of memory:
  - ROMS variants
  - RAM variants
  - Trade offs of speed, space, expense, longevity
- All slower to access than registers
- Memory addressing:
  - bits need to address each individual byte (via chip, page, word).