



SWINBURNE
UNIVERSITY OF
TECHNOLOGY

COS10004 Computer Systems

Lecture 4.4: CPU architectures and memory management (stacks and caching)

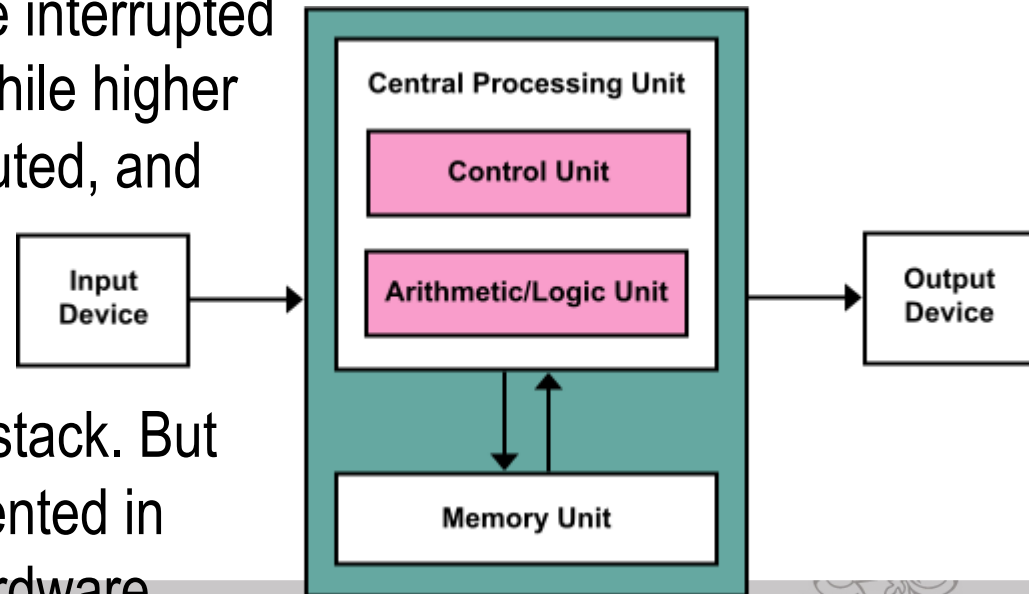
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STACKS AND VON NEUMANN



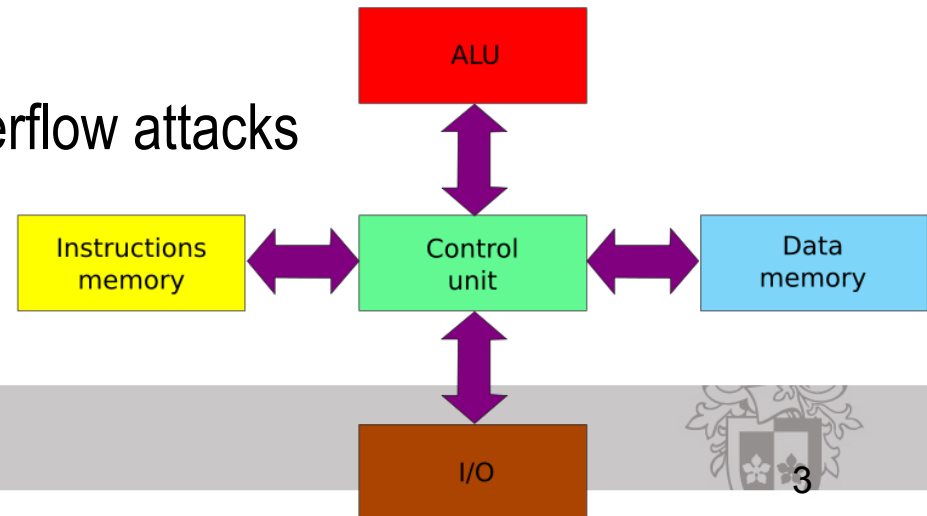
- > The most common CPU architecture.
- > Von Neumann architecture: Control bits and data bits share a common memory space / hardware (c.f. Harvard architecture).
- > Allows processes to be interrupted (and stored as data) while higher priority tasks are executed, and then restored and resumed.
- > Requires the use of a stack. But stacks can be implemented in software as well as hardware.



HARVARD ARCHITECTURE



- > A computer architecture where instructions and data are kept separate.
- > Runs faster (generally), and more secure (generally) than Von Neumann, but more expensive and less extensible.
- > Data bus and control buses can be different widths, types.
- > Used in PIC controllers, digital signal processors where memory is scarce and speed is important.
- > Reasonably immune to buffer overflow attacks (where code is input as data and then executed for malicious purposes).



MODIFIED HARVARD

- > Von Neumann with separate instruction and data caches in the CPU.
- > Has the speed advantage of Harvard but the flexibility of Von Neumann.
- > Used in ARM, most Intel CPUs.
- > Has the same security vulnerabilities as Von Neumann, so manufacturers add hardware protection which sets memory pages to be Read/Write XOR Read/Execute.
- > Supports stacks and interrupts.

CPU CACHES

- > Store frequently accessed instructions/data in high-speed memory.
- > What's in cache depends on caching algorithms
- > Can have separate Instruction and Data caches:
 - Instructions smaller, more predictable format so have dedicated hardware (read access) to data caches (RW access).
 - Increases processing speed – Instructions and Data can be loaded at the same time.
 - May save power (can power-down cache if not in use)
- > Can have separate layers (L1, L2, L3) depending on speed/frequency requirement. (

<http://www.extremetech.com/extreme/188776-how-l1-and-l2-cpu-caches-work-and-why-theyre-an-essential-part-of-modern-chips>)

SUMMARY

- > CPU architectures underpin how data and instructions are stored and processed
- > Von Neumann:
 - Data and Instructions stored in same location
 - Stack central to handling multiple tasks/interrupts
- > Harvard:
 - Separates data and instructions
 - Increased efficiency and security
 - Reduced generality and versatility
- > Caching – optimises memory access