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Roll No.: 210163

LAB REPORT – 1

Experiment 1:

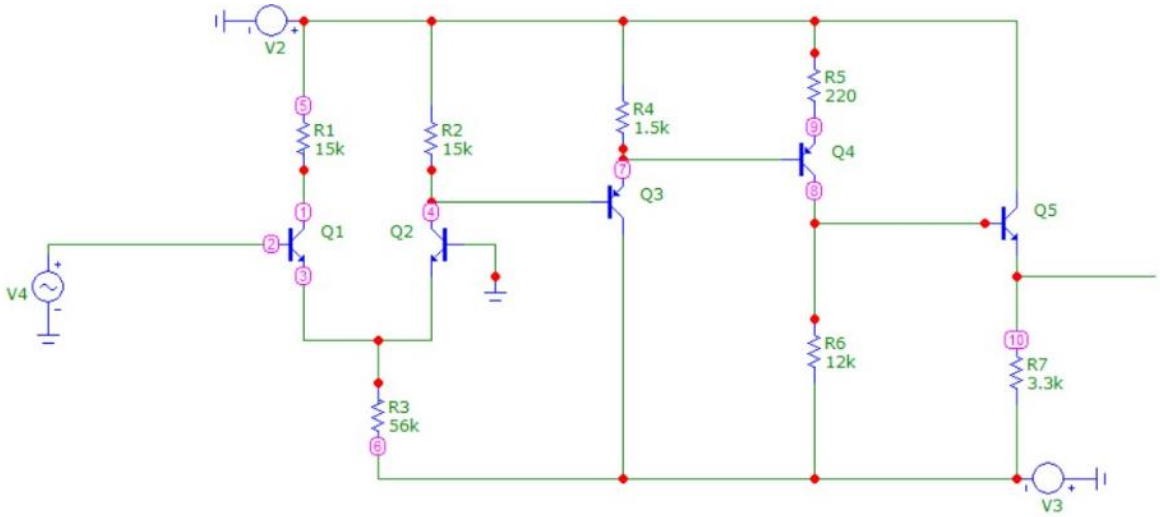
Objective: Design and Implementation of a BJT Operational Amplifier.

The implementation of Op-Amp requires the use of NPN: BC547 and PNP: BC557 transistors.
Following were the desired specifications for our Op-Amp
(a) Gain $A_v > 10^3$

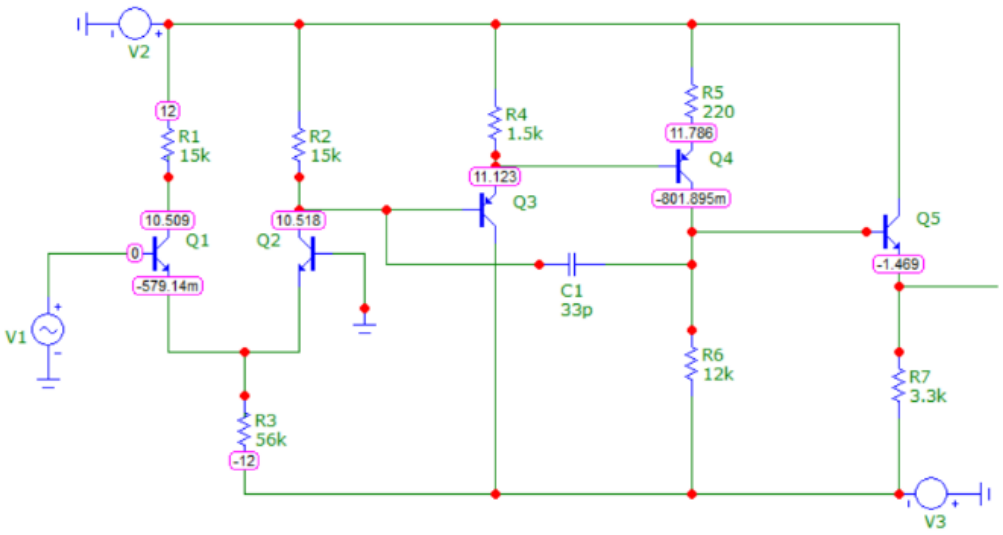
(b) Input Resistance $R_{in} > 10^5$

(c) Output Resistance $R_{out} < 10^2$

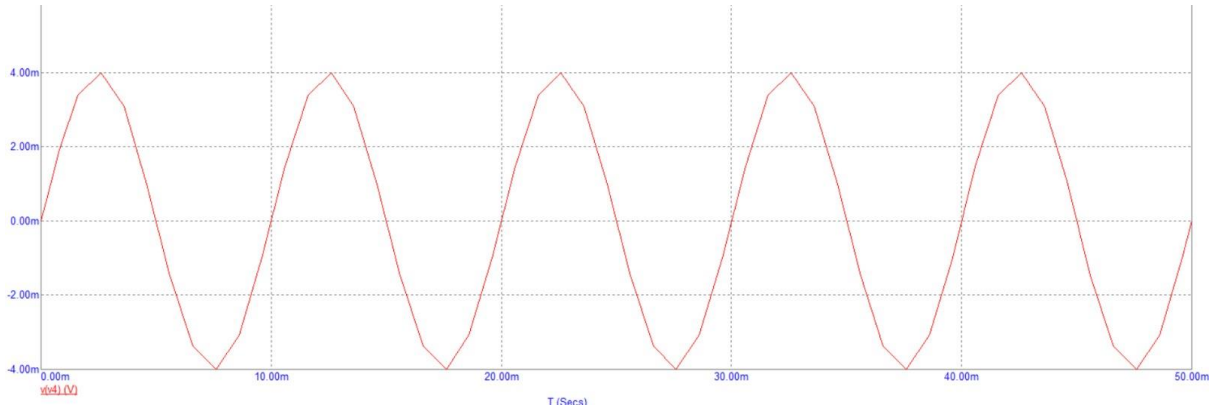
Design:



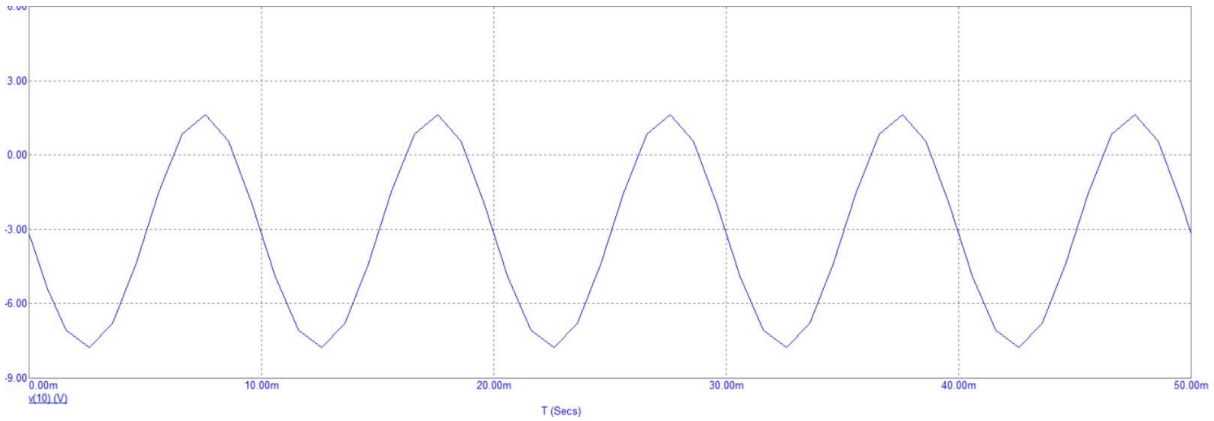
Simulation:



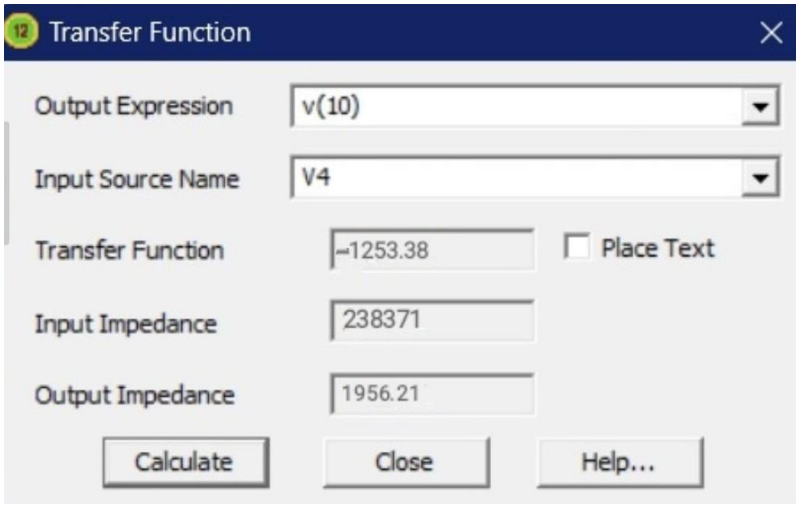
Node Voltages



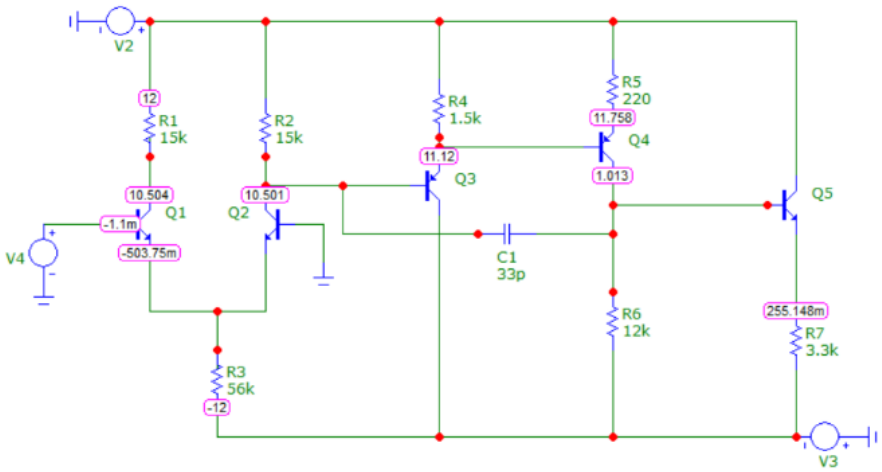
Input Waveform



Output Waveform



Transfer Function

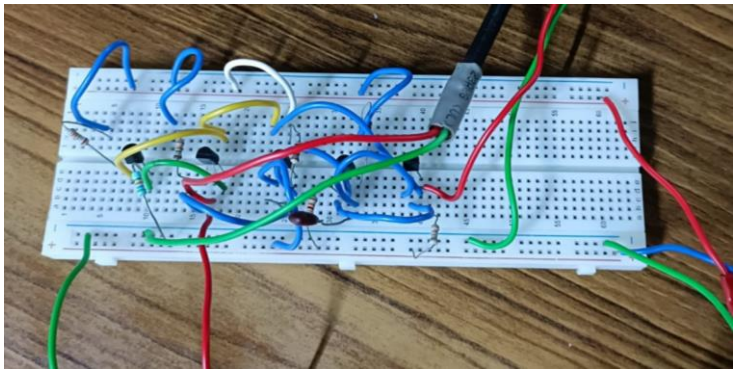


Measuring the bias voltage

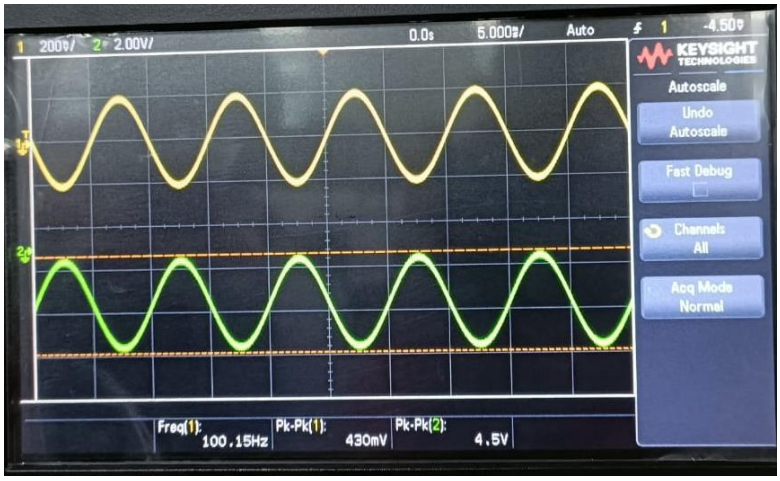
We get V_{out} almost equal to zero with 1.1mV of bias voltage magnitude at the input terminal.

- Overall Gain = v_{out}/v_{in} = - 1253.38
- Input Resistance = 238 kΩ
- Output Resistance = 1956.21Ω
- Bias voltage at output = 1.1mV

Experimental Results:



Op-Amp Circuit on Breadboard



- v_{in} = 4.3mV (pk to pk ac voltage) [through the voltage divider]
- v_{out} = 4.5V (pk to pk ac voltage)
- V_{OUT} = -16mV (Offset voltage at output)
- Overall Gain = v_{out}/v_{in} = 4.5/4.3m = 1046
- Input Resistance = 240k Ω
- Output Resistance = 1900 Ω
- Node Voltage Measurements:

Node Number	Voltage(V)
1	10.3
2	-600µ
3	-590m
4	10.38
5	-12
6	11.149
7	1.77
8	11.77
9	12
10	-2.37

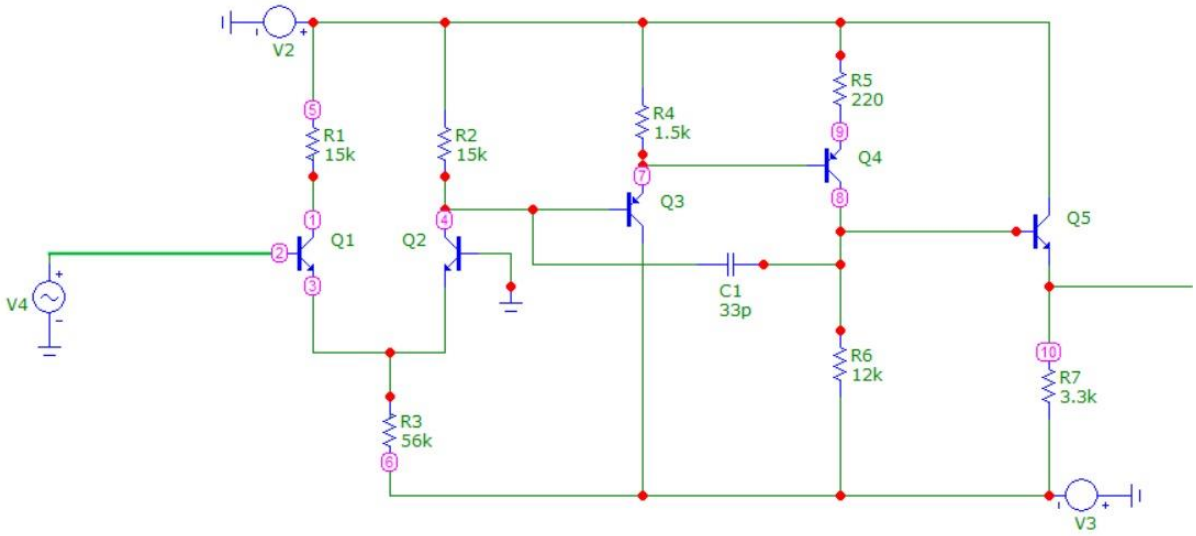
Conclusions:

- The Op-amp was designed using the Differential amplifier stage (DA), buffer, gain stage, and output stage. The values of resistors were chosen such that we get an overall gain above 1000. The use of the buffer stage was to increase the input resistance seen from the output of the DA, so that the gain of the DA doesn't change with the attachment of the gain stage. The resistor at the output stage was chosen such that the offset voltage at the output is close to zero.
- The values of resistors used in the lab were different from those in the simulation to get a good amount of gain (>1000) while keeping the Op-Amp out of saturation in a zero-bias state.

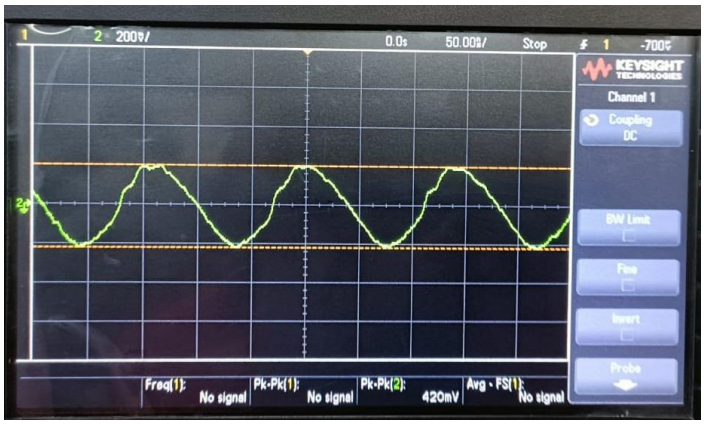
Experiment 2:

Objective: Adding compensation to remove the oscillation

Design:



Experimental Results:



Without Capacitor

With capacitor

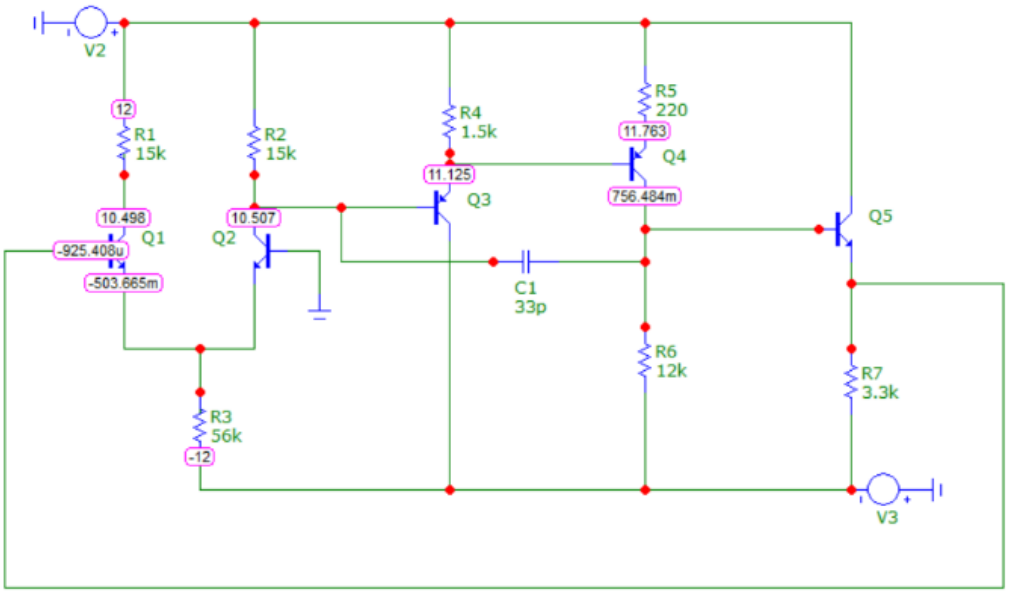
Conclusions:

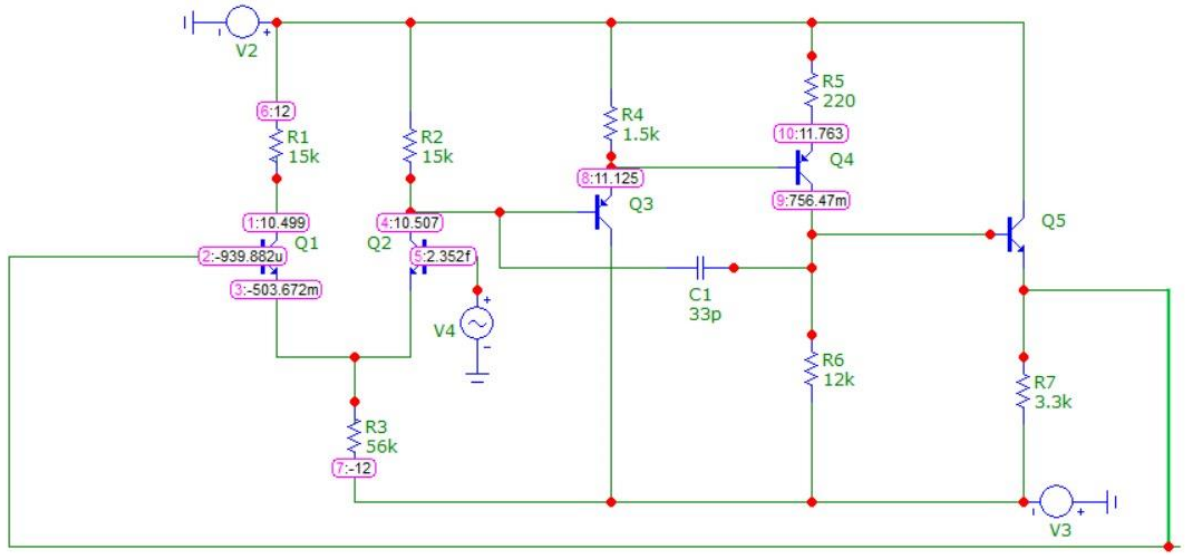
Without a capacitor, the unity gain frequency of the op-amp is very large resulting in the unstable condition in the negative feedback. Hence it oscillates. By using a capacitor, we create a pole and reduce the unity gain frequency of the op-amp thus creating a positive phase margin, and hence it doesn't go unstable and hence no oscillation.

Experiment 3

Objective: Buffer response with capacitor, Voltage Follower with input sine waveform

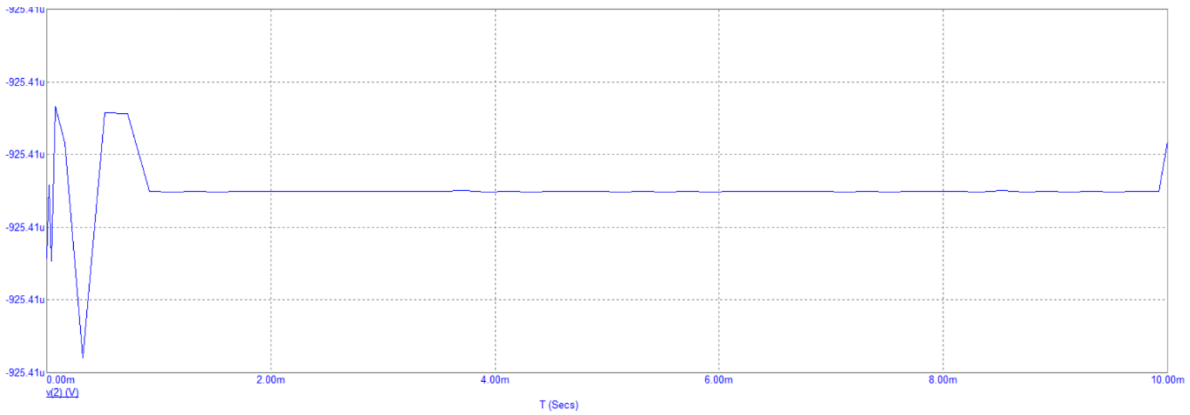
Design:

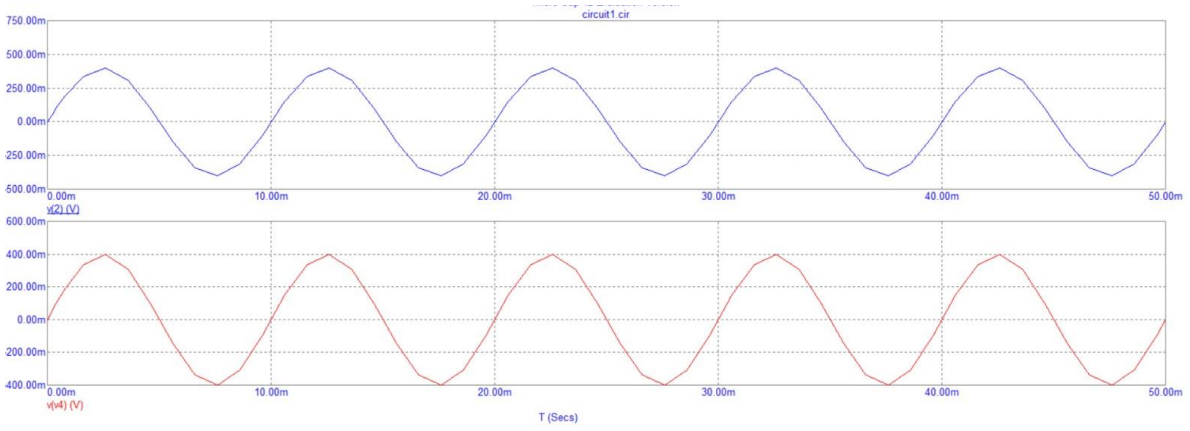




With an input sine wave

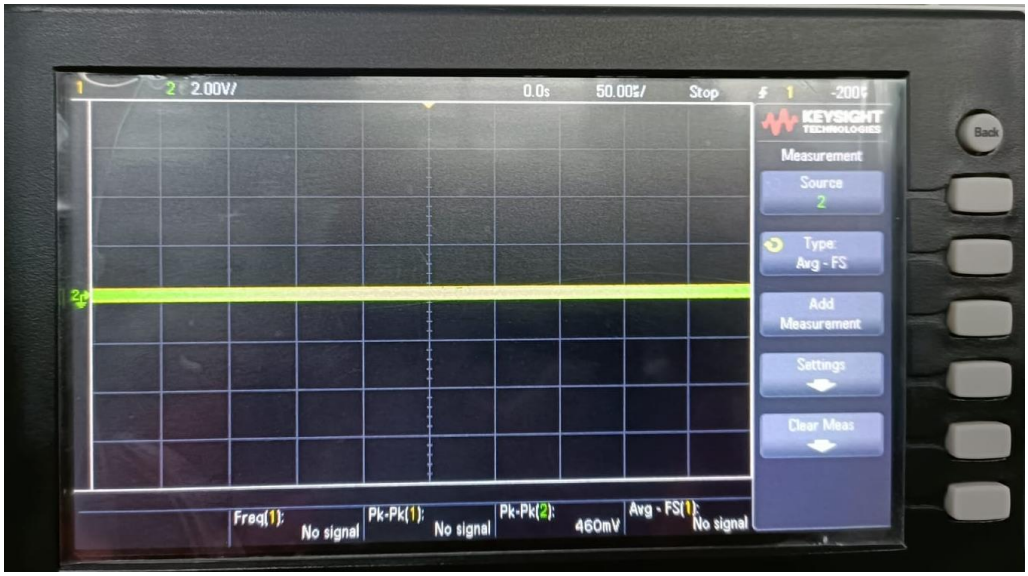
Simulations:

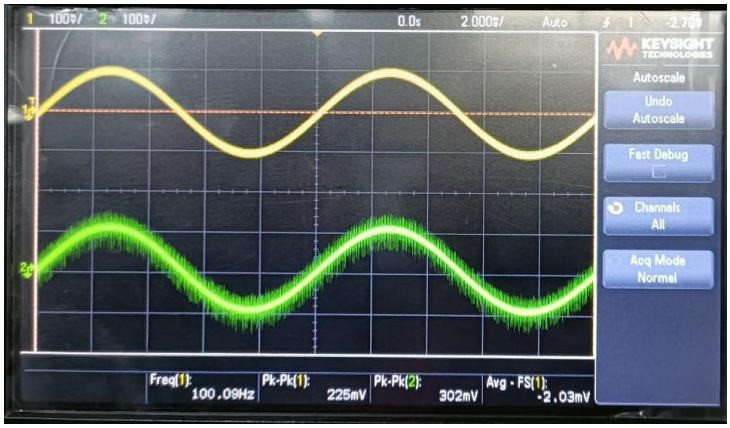




With an input sine wave

Experimental Results:





With an input sine wave

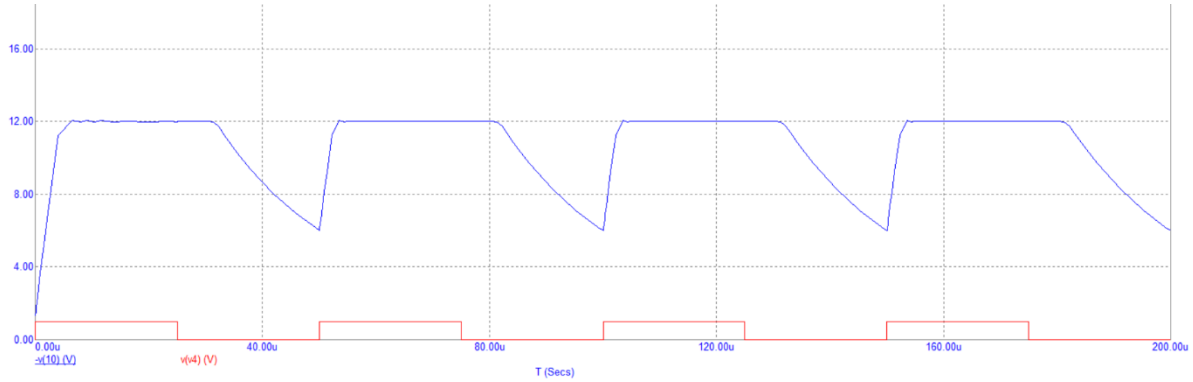
Conclusions:

- Huge oscillations were observed in the output of the circuit without a capacitor because of the negativephase margin and unstable response in feedback.
- The oscillations were almost eliminated with the use of a 33pF capacitor giving a much betterand positive phase margin.
- The output and inverting terminals were connected and a sine wave of amplitude 400mV (pk to pk) and frequency 100Hz was applied to the non-inverting terminal of the Op-Amp.
- We obtained the same waveform at the output as we applied as input, suggesting a very good buffer, in both simulation as well as experiment.

Experiment 4

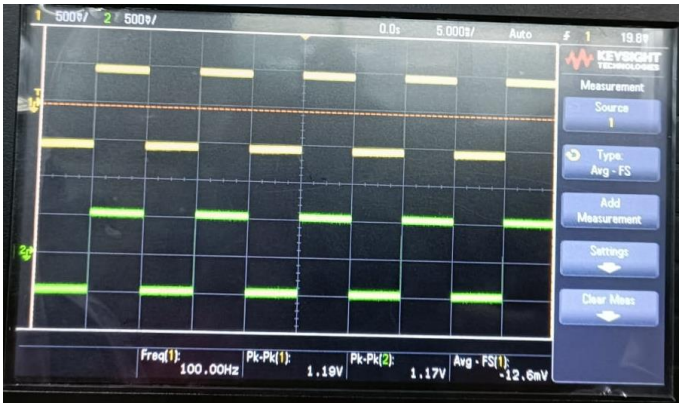
Objective: Slew rate measurement using square wave

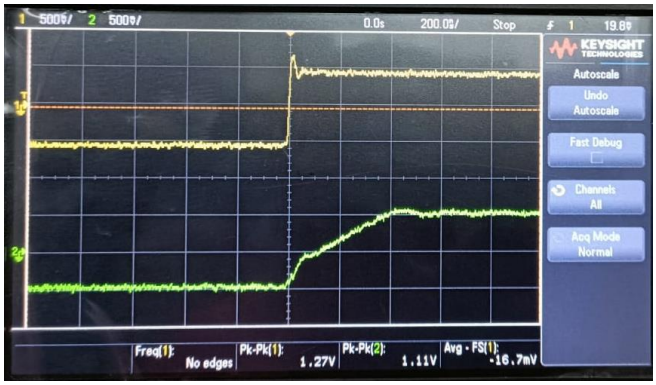
Simulations:



We can measure the slew rate by observing the buffer response to a square wave as above. The slew rate value is $2V(\mu s)^{-1}$.

Experimental Results:





- Slew rate = $\Delta V/\Delta t$ = 1.05V/444ns = 2.36V/µs

Conclusions:

- Due to the presence of a capacitor, the voltage change rate across it is limited by I/C, and I is the current flowing through the capacitor. So a sudden change in the input will not be reflected in the output and the voltage will increase with the slope of I(max)/C, and hence it increases linearly.

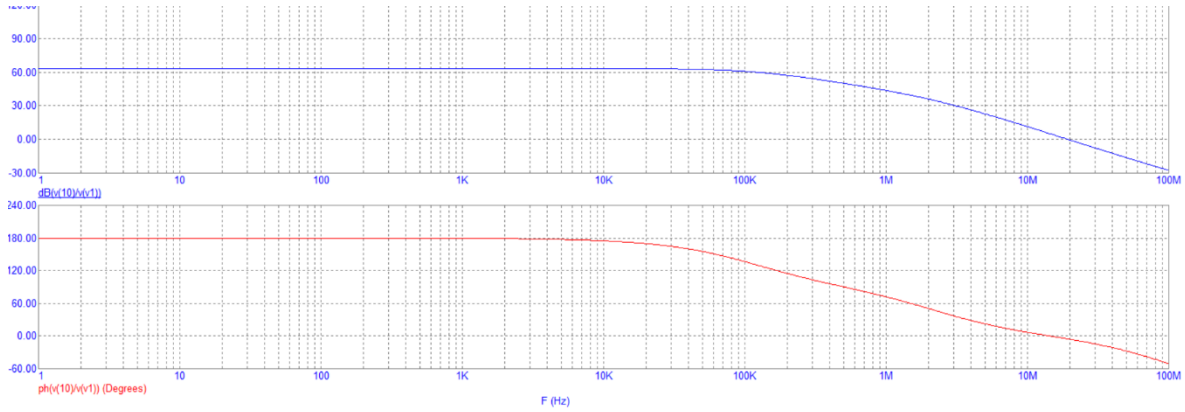
- The output and inverting terminals were connected and a square wave of amplitude 1V andfrequency 100Hz was applied to the non-inverting terminal of the Op-Amp.
- We measured the slew rate using the greater of the delays in the rise and fall times of the outputsquare waveform that we had obtained.
- We got a better slew rate in the simulation than in the actual experiment due to abnormalities in the real-world components.

Experiment 5

Objective: Frequency Response of the Op-amp with and without capacitor.

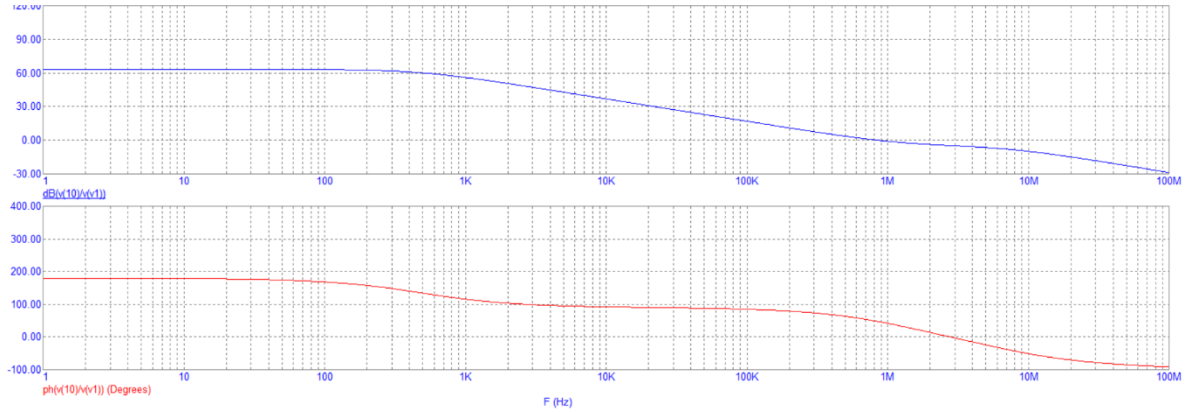
Simulations:

Transfer function



Frequency response without capacitor

From the freq. response without a capacitor, we see that the unity gain frequency is around 20.209MHz and the phase margin is −6.635°, which is negative.



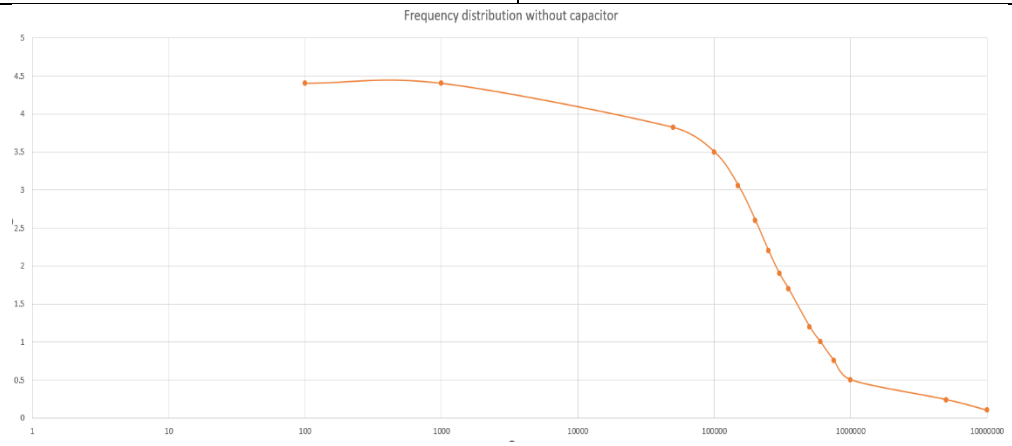
Frequency response with capacitor

We can see from the freq. response with the capacitor that the unity gain frequency is around 1MHz and the corresponding phase margin is 58°.

Experimental Results:

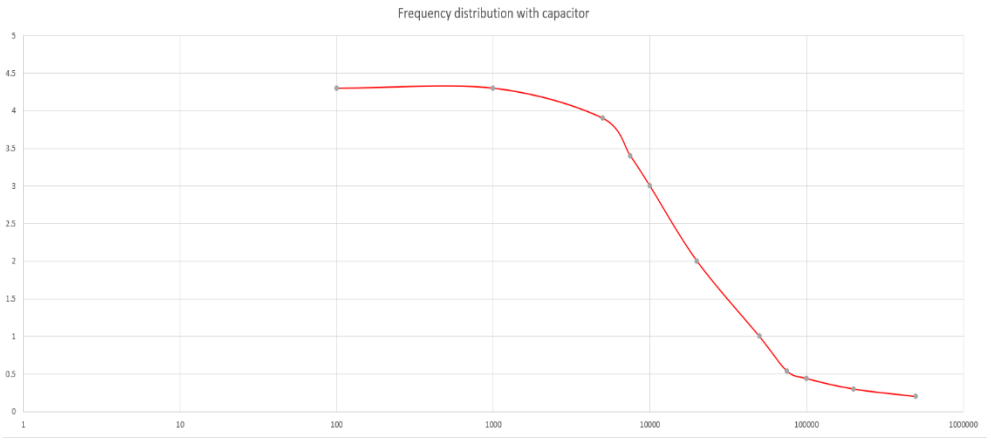
- Open-loop Frequency Response without capacitor:

Frequency (Hz)	Voltage (V)
100	4.4
1k	4.4
50k	3.82
100k	3.5
150k	3.06
200k	2.6
250k	2.2
300k	1.9
350k	1.7
500k	1.2
600k	1
750k	760m
1M	500m
5M	240m
10M	100m

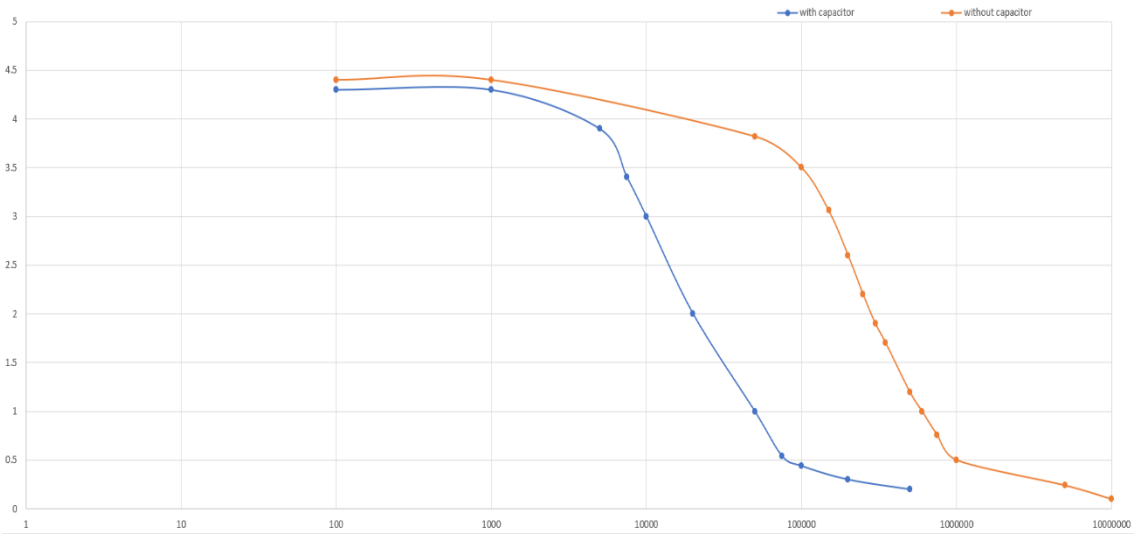


- Open-loop Frequency Response with capacitor:

Frequency (Hz)	Voltage (V)
100	4.3
1k	4.3
5k	3.9
7.5k	3.4
10k	3
20k	2
50k	1
75k	540m
100k	440m
200k	300m
500k	200m



➢ Comparison of Frequency Responses with and without capacitor:



- 3dB frequency with capacitor = 7.5kHz
- 3dB frequency for without capacitor = 60kHz

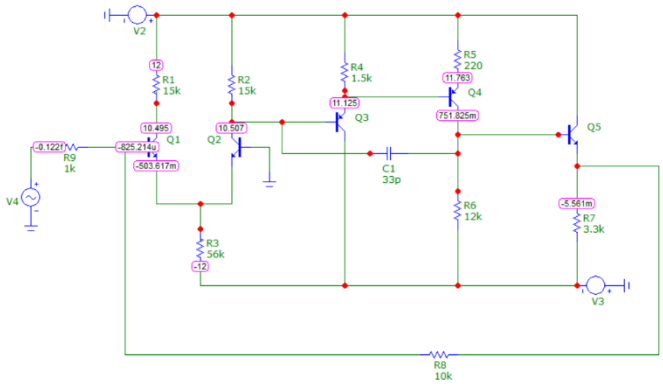
Conclusions:

- By adding a capacitor, we create a pole. Depending on the value of the capacitor, here we created a pole much before the system pole. This led to a decrease in the gain at the smaller frequency when compared to without a capacitor. Hence this decreased the high gain bandwidth but has made the op-amp stable during the unity negative feedback. Hence stability and high gain bandwidth have a trade-off.
- We observed gain and phase differences between the input and output signals for different frequencies ranging from 100Hz to 10MHz and plotted the frequency response.

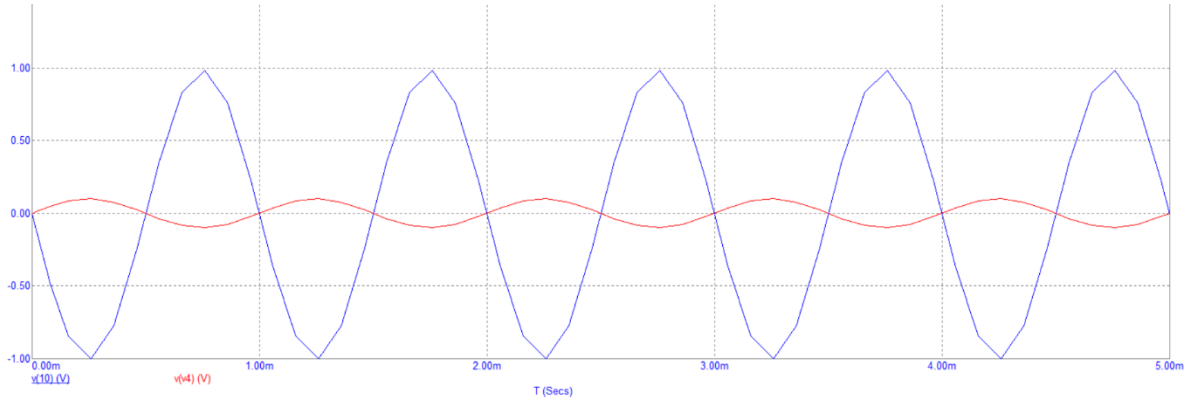
Experiment 6

Objective: Make an inverting amplifier using the designed Op-amp.

Design:



Simulations:



We see a gain of approximately 10 and a phase difference of 180° with the inverting amplifier made using the Op-Amp we designed.

Experimental Results:

- V_{in} = 217mV (pk-pk)
- V_{out} = 2.05V (pk-pk)
- R_2 = 10kΩ
- R_1= 1kΩ

- Expected gain = $\frac{V_{out}}{V_{in}} = \frac{-R_2}{R_1}$ = -10
- Obtained gain = $\frac{V_{out}}{V_{in}} = \frac{-2.05}{217m}$ = -9.447

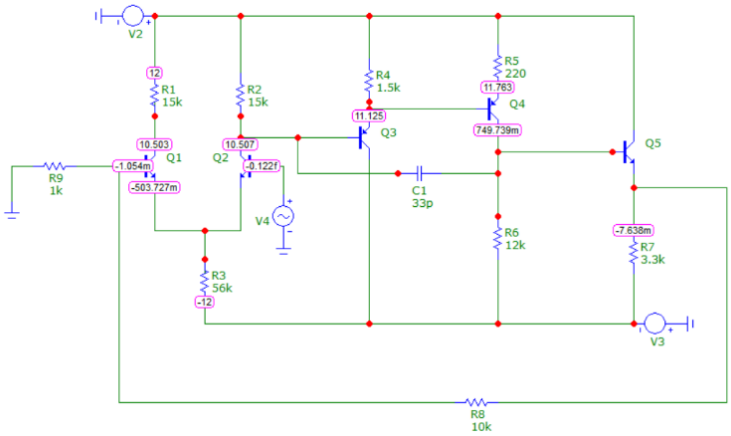
Conclusions:

- The circuit is an inverting amplifier. The gain according to the design must be -10. We can see in the output that there is a gain of -9.447.
- The difference is due to some variations in the component parameters but still close to it.
- The phase difference was 180° (output is inverted with respect to input).

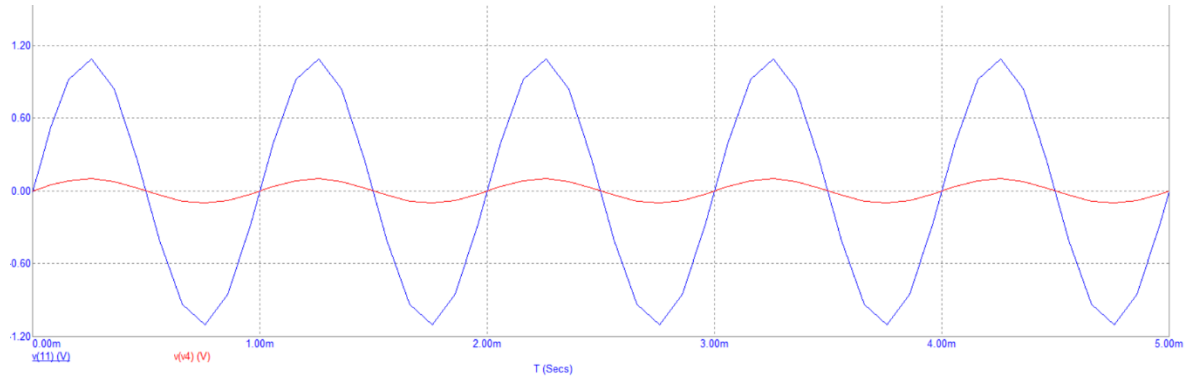
Experiment 7

Objective: Make non - inverting amplifier using the designed Op-amp.

Design:



Simulations:



Output gain of non-inverting amplifier

We see a gain of approximately 11 and no phase difference with the non-inverting amplifier made using the Op-Amp we designed.

Experimental Results:

- V_{in} = 233mV (pk-pk)
- V_{out} = 2.37V (pk-pk)
- R_2 = 10kΩ
- R_1= 1kΩ
- Expected gain = $\frac{V_{out}}{V_{in}} = 1 + \frac{R_2}{R_1}$ = 11
- Obtained gain = $\frac{V_{out}}{V_{in}} = \frac{2.37}{233m}$ = 10.17

Conclusions:

- The circuit is a non-inverting amplifier. The gain according to the design must be 11. We can see in the output that there is a gain of 10.
- The difference is due to some variation in the component parameters but still very close to it.
- The was no phase difference between the input and output signals.