Total No. of Questions :5] *[Total No. of Printed Pages :2*

Roll No .....

EC - 403

B.E. IV Semester Examination, June 2014

Digital Electronics

Time : Three Hours

Maximum Marks : 70

Note: i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.

ii) All parts of each question are to be attempted at one place.

iii) All questions carry equal marks, out of which part A and B (Max. 50 words) carry 2 marks, part C (Max. 100 words) carry 3 marks, part D (Max. 400 words) carry 7 marks.

iv) Except numericals, Derivation, Design and Drawing etc.

Unit - I

1. a) Convert the following as directed. 2

   i) $[10110]_2$ to $[\quad]_{gray}$

   ii) $[11010101.10011]_2$ to $[\quad]_8$

   b) Subtract $(1010)_2$ from $(1000)_2$ using 2's complement method. Subtract by direct method also and compare the result. 2

   c) Express the function $Y = A + \bar{B}C$ in (i) canonical SOP and (ii) canonical POS form. 3

   d) Simplify the expression $Y = \Sigma_m (3, 4, 5, 7, 9, 13, 14, 15)$ using K-map method. 7

   OR

   Find the minimal sum of product, for the Boolean expression $\Sigma (1, 2, 3, 7, 8, 9, 10, 11, 14, 15)$ using the Quine-McCluskey method. 7

Unit - II

2. a) Realise $Y = (A + C)(A + \bar{D})(A + B + \bar{C})$ using NOR gates. 2

   b) Design a half adder. 2

   c) Design a full subtractor using logic gates. 3

   d) Design BCD adder using full adders. 7

   OR

   Implement the function F(A, B, C, D) = Σ (0, 1, 3, 4, 8, 9, 15) using multiplexer. 7

Unit - III

3. a) Explain briefly the working of R-S flip flop. 2

   b) Give the applications of 555 timer chip. 2

   c) Discuss the working of J-K flip flop with the help of circuit diagram, state and excitation table. Also explain the race around condition. 3

   d) With the help of circuit diagram and timing diagram explain the working of Monostable multivibrator designed using transistors. 7

OR

Design a Modulo-7 counter using J-K flip flop. 7

Unit - IV

4. a) Give a broad classification of semiconductor memories. 2
   b) Give the construction of RAM. 2
   c) On the basis of organisation and construction compare SRAM and DRAM. 3
   d) Discuss the working and construction of RAMBUS ROM and PAL. 7

OR

Discuss the working and construction of PROM and PLA's. 7

Unit - V

5. a) Give the characteristics of RTL family. 2
   b) Give two advantages and disadvantages of totem pole output arrangements. 2
   c) Explain briefly about ECL logic family. 3
   d) Explain briefly the characteristics of MOS logics and write a note on CMOS logics. 7

OR

Compare the characteristics of different logic families. 7

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