Total No. of Questions : 10] [Total No. of Printed Pages : 4

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EC–802

B. E. (Eighth Semester) EXAMINATION, June, 2012

(Electronics & Communication Engg. Branch)

CMOS CIRCUIT DESIGN

(EC–802)

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : Attempt *one* question from each Unit. All questions carry equal marks.

Unit–I

1. (a) Discuss the small signal equivalent model for source follower. Derive equation for voltage gain of the source follower circuit. 10

   (b) Calculate the V_{out} of source follower circuit as shown in the following figure with :
   $(W/L)_{M_1} = 20/0{\cdot}5$, $I_1 = 200\,\mu$ A, $V_{TH_O} = 0{\cdot}6$ V, $2\phi F = 0{\cdot}7\,v$, $\mu_n \cos = 50\,\mu$ A/v^2 and $\gamma = 0{\cdot}4\,v^2$ and $V_{in} = 1{\cdot}2\,v$. 10

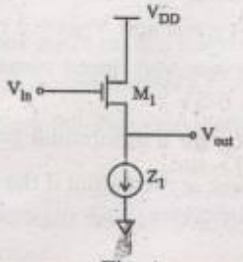

Fig. 1

P. T. O.

Or

2. (a) Discuss the high frequency model of a cascode stage. 10

   (b) Explain the effect of high frequency supply noise in differential pair. 10

Unit–II

3. The circuit shown in the following figure uses a resistor rather than a current source to define a tail current of 1 mA.

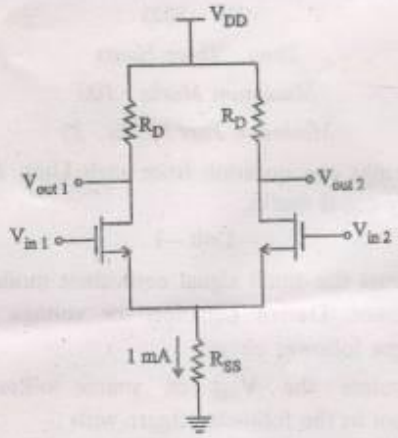

Fig. 2

Assume $(W/L)_{M_1 M_2} = 25/0{\cdot}5$, $\mu_n \cos = 50\,\mu\ A/v^2$, $V_{TH} = 0{\cdot}6\,v$, $\lambda = \gamma = 0$ and $V_{DD} = 3\,v$: 20

   (a) What is the required input common mode for which R_{SS} sustain $0{\cdot}5\,v$?

   (b) Calculate R_D for a differential gain of 5.

   (c) What happens at the output if the input common mode level is 50 mV higher than the part (a) of this problem ?

Or

4. (a) Explain in brief the different properties of feedback circuit. 10

   (b) Explain the voltage to voltage type of feedback topologies. 10

Unit – III

5. Explain why a single common source stage does not oscillate if it is placed in a unity gain loop. How can oscillation be generated ? Explain three-stage ring oscillator. 20

Or

6. (a) Discuss the mathematical model of voltage controlled oscillator. 10

   (b) Explain the block diagram of simple phase lock loop. 10

Unit – IV

7. (a) Design and explain positive edge triggered D flip-flop. 10

   (b) Explain the architecture of programmable logic array (PLA) with a neat diagram. 10

Or

8. Write short notes on the following : 20

   (a) Serial Access Memory

   (b) Content Addressable Memory

Unit – V

9. (a) Design a 4-bit adder/subtractor using data path operator. 10

(b) Design the following circuits : 10

(i) 8-bit one/zero detector

(ii) 4-bit comparator

Or

10. (a) Design a 4 × 4 array multiplier. 10

(b) Design and explain 3-bit increamentor circuit. 10