Roll No .....

EC - 605

B.E. VI Semester

Examination, June 2015

VLSI Circuits and Systems

Time : Three Hours

Maximum Marks : 70

Note: i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.

ii) All parts of each questions are to be attempted at one place.

iii) All questions carry equal marks, out of which part A and B (Max.50 words) carry 2 marks, part C (Max.100 words) carry 3 marks, part D (Max.400 words) carry 7 marks.

iv) Except numericals, Derivation, Design and Drawing etc.

Unit - I

1. a) Write short note on Y -chart.
   b) What are the main characteristics of VLSI design?
   c) Prove that p -FET pass strong logic '1' and n -FET pass strong logic '0'
   d) Explain CAD tools. Give the various steps in the CAD tools design process.

   OR

   Describe the following with the help of CMOS logic.
   i) Inverter
   ii) Compound gates
   iii) Multiplexers

Unit - II

2. a) Define the synchronous and asynchronous systems.
   b) Write short note on state equivalence.
   c) Differentiate between Mealy and Moore Model.
   d) Draw state diagram for a circuit which produces output '1' whenever it receives '110' overlapping sequence is