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Total No. of Questions : 10] [Total No. of Printed Pages : 5

Roll No. .....

CS/EC/IT–401(NGS)

B. E. (Fourth Semester) EXAMINATION, June, 2012

(Non-Grading System)

(Common For CS, EC & IT Engg. Branch)

COMPUTER SYSTEM ORGANIZATION

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : The question paper is divided into five Units. Each Unit carries an internal choice. Attempt *one* question from each Unit. Thus attempt *five* questions in all. All questions carry equal marks. Assume suitable data whenever necessary.

Unit – I

1. (i) A two-word instruction is stored in memory at an address designated by symbol w. The address field of the instruction (stored at w + 1) is designated by symbol y. The operand used during the execution of instruction is stored at an address symbolized by z. An index register contains the value x. State how z is calculated from other address if the addressing mode of instruction is : 10

(a) Direct

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(b) Indirect

(c) Relative

(d) Indexed

(ii) Write a program to evaluate the arithmetic statement : 10

$$X = \frac{A - B + C * (D * E - F)}{G + H * K}$$

(a) Using a general register computer with three address instructions.

(b) Using a general register computer with two address instructions.

(c) Using a accumulator type computer with one address instructions.

(d) Using a stack organized computer with zero address operation instructions.

Or

2. (i) Draw the functional and structural views of a computer system and explain in detail. 6

(ii) What are the major steps a processor has to perform to execute an instruction ? Explain briefly. 4

(iii) Explain the internal architecture of 8085 with a neat block diagram. 10

Unit–II

3. (i) With the help of a neat diagram and example, explain the working of a typical microprogrammed control unit. 10

(ii) What is meant by Normalization ? Explain the IEEE standards to represent floating point number. 5

(iii) Draw and explain the block diagram of general purpose register architecture of CPU. 5

Or

4. (i) A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers : 6

(a) How many selection inputs are there in each multiplexer ?

(b) How many multiplexers are there in the bus ?

(ii) Explain Booth's multiplication algorithm through an example. Give an example of multiplication and multiplier for which this algorithm takes the maximum time. 10

(iii) Compare horizontal microcode with vertical microcode. State the advantage of microprogrammed control unit. 4

Unit – III

5. (i) Explain the interrupt process in 8085 and the difference between a non-maskable and a maskable interrupt. 10

(ii) Describe the function of DMA controller in data transfer between I/O and memory. State different modes of DMA operation. 6

(iii) State the difference between I/O mapped I/O and memory mapped I/O. 4

Or

6. (i) Define the following : 10

(a) Asynchronous Data Transfer

(b) Asynchronous Communication Interface

P. T. O.

(ii) What is Interrupt ? Describe different types of interrupts and their use. How a processor handles a vectored interrupt ? 10

Unit – IV

7. (i) Explain a typical associative memory organization. Describe the various steps involved in accessing the content of the associative memory. 10

(ii) A memory system contains a cache, a main memory and a virtual memory. The access time of cache memory is 5 nsec and it has 80% hit rate. The access time of main memory is 100 nsec and it has 99·5% hit rate. The access time of virtual memory is 10 msec. What is the average access time of the hierarchy ? 5

(iii) Give a block diagram for 512 K * 32 memory using 64 K * 8 memory chips and explain. 5

Or

8. (i) Discuss the different mapping techniques used for cache memory. What is the need of mapping techniques ? 10

(ii) For a set associative cache organization, the parameters are as follows : 10

T_c → Cache access time

T_m → Memory access time

L → Number of sets

B → Block size

K * B → Set size

Calculate hit ratio for loop executed 100 times where the size of loop is N * B and N = K * M is a non-negative integer and $1 < M \leq L$.

Unit – V

9. (i) What are Pipeline Hazards ? What are the causes of pipeline hazards ? Describe briefly the hazard detection and resolution of hazards in pipelines 10

(ii) A program repeatedly executes a loop that has 120 iterations. Each iteration takes 10000 cycles. On multiprocessor systems, 50000 cycles are required to synchronize the processor once all iteration of loop have completed : 10

(a) What is the execution time of each loop on a uniprocessor system ?

(b) What is the execution time of each loop on a 2-processor system, and what is the speedup over the uniprocessor system ?

(c) What is the execution time of each loop on a 4-processor system and what is the speedup over the uniprocessor system ?

Or

10. Write short notes on the following : 20

(i) Multiprocessor systems

(ii) Message passing system

(iii) Shared memory system

(iv) Interprocess communication