Roll No .....

CS/IT - 402

EC - 401 (NGS)

B.E. IV Semester

Examination, December 2012

Computer System Organization

Time : 3 Hours

Maximum Marks : 70/100

Note : 1. Attempt any *one* question from each unit.
2. All question carry equal marks.

UNIT - I

1. a) Explain the different types of register used in a basic computer. Explain how these registers are connect to common bus. 07

   b) Draw and explain the functional block diagram of 8085 microprocessor. Also draw its flag structure. 07

OR

2. a) A digital computer has a common bus system for 16 registers of 32 bit each. The bus is constructed with multiplexers. 07

   (i) How many selection inputs are there in each multiplexer?

   (ii) What size of multiplexers are needed?

   (iii) How many multiplexers are there in the bus?

   b) Show the hardware that implement the following statement include the logic gates for the control function

and a block diagram for the binary counter with a count enable input. 7

$$xyT_0+T_1+y'T_2: AR \leftarrow AR+1$$

UNIT-II

3. a) Draw and explain Functional microprogram control unit block diagram. 7

   b) Write short notes on the following: (Any Two) 7

   (i) Control Memory

   (ii) Nono programed control unit

   (iii) Hard Wired control Unit

OR

4. a) Explain phases of instruction cycle. Also draw and explain instruction cycle flowchart. 7

   b) Draw block diagram of a BCD adder. Explain How decimal subtraction can be performed. 7

UNIT - III

5. a) Differentiate between Isolated I/O and memory mapped I/O and give advantage and disadvantage of each. 7

   b) What are different modes of data transfer? Explain the DMA controller with block diagram. What is meant by block transfer? 7

OR

6. a) What do you mean by interrupt? When a device intterrupt occurs, how does the processor determine which device issued the interrupt? 7

   b) Enlist the data transfer instruction of 8085 microprocessor. Write an assembly language program to add two 8 bit number H6H and 52H and store the result at 4008H. 7

UNIT - IV

7. a) What is cache memory? Explain different mapping techniques in cache memory system. 7

   b) A set associative cache consist of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses and tag bit in cache address. 7

OR

8. a) What do you mean by associative memory? Explain math logic of associative memory with block diagram. 7

   b) A digital computer has a memory unit of 64Kx16 and a cache memory of 1k words. The cache uses direct mapping with a block size of four words.

   (i) How many bits are there in the tag, index, block and word field of the address formate

   (ii) How many blocks can the cache accomodate

   (iii) How many bits are there in each word of cache. 7

UNIT - V

9. a) What are different conflicts that will arise in pipeline? How do you remove the conflicts. 7

   b) What is pipeline speedup? Draw a space time diagram for a six-segment pipeline showing the time it takes to process eight tasks. 7

OR

10. Write notes on following: 14

    a) Inter-processor communication.

    b) Vector processing

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