i) Inter processor arbitration

ii) Inter processor communication 2

c) Explain any one vector processing method with illustration. 3

d) What is pipe lining? 7

OR

In certain computation, following calculation is required :

$(A_i + B_i)(C_i + D_i)$ using stream of numbers. Suggest a pipeline architecture for the above computation. List the content of registers in pipeline for $i = 1$ through 6. 7

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Roll No .....

EC - 302

B.E. III Semester

Examination, June 2014

Computer System Organization

Time : Three Hours

 Maximum Marks : 70

Note: i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.

ii) All parts of each question are to be attempted at one place.

iii) All questions carry equal marks, out of which part A and B (Max. 50 words) carry 2 marks, part C (Max. 100 words) carry 3 marks, part D (Max. 400 words) carry 7 marks.

iv) Except numericals, Derivation, Design and Drawing etc.

1. a) Define: 2

i) Micro operation

ii) Control function

b) What is register transfer language? 2

c) Differentiate between Von Neumann and Harvard architecture. 3

d) Explain Von Neumann architecture. What is Von Neumann bottleneck? 7

OR

statement.

$$P = \frac{(x - y + 2) * (m * n - 0)}{Q + R * S}$$

Using i) Two-address instructions

ii) Zero-address instructions 7

2. a) Define: 2

i) Micro program sequencing

ii) Address sequencing

b) What is CMBR? 2

c) Explain various branching techniques used micro programmed control unit. 3

d) Explain multiplication algorithm for floating point numbers with their respective flow charts. 7

OR

Discuss Nano programmed control unit. 7

3. a) Compare I/O versus memory bus. 2

b) How many characters per second can be transmitted over a 1200-baud line in following modes.

i) Synchronous serial transmission.

ii) Asynchronous serial transmission with two stop bits.

iii) Asynchronous serial transmission with 1 stop bit. 2

c) How is interrupt driven I/O better than programmed I/O? 3

d) Explain i) Daisy. Chaining priority

ii) Parallel priority interrupt 7

OR

Explain DMA with block diagram. 7

4. a) What do you mean by hit ratio? 2

b) Given the cache access time as 10ns memory access time as 100 ns and cache hit ratio as 90%, calculate the effective memory access time. 2

c) A CPU has 32 bit memory address and 256kB cache memory. The cache is organized as 4 way set associative cache with cache block size of 16 bytes

i) What is number of sets in cache?

ii) What is the size of the tag field per cache block?

iii) How many address bits are required to find the byte offset within a cache block? 3

d) Explain the requirement of cache memory and its organization. 7

OR

Explain the memory Hierarchy of a typical computer system. 7

5. a) Differentiate between tightly coupled microprocessor and loosely coupled microprocessor system. 2