d) Prove that K-stage pipeline can be at most K times faster than that of non-pipelined serial processor.

OR

Explain interconnection structure and inter processor communication.

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Roll No .....

EC-302

B.E. III Semester

Examination, December 2016

Computer System Organization

Time : Three Hours

Maximum Marks : 70

Note: i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.

ii) All parts of each question are to be attempted at one place.

iii) All questions carry equal marks, out of which part A and B (Max. 50 words) carry 2 marks, part C (Max. 100 words) carry 3 marks, part D (Max. 400 words) carry 7 marks.

iv) Except numericals, Derivation, Design and Drawing etc.

Unit - I

1. a) Draw a block diagram of digital computer.

b) List different memory registers.

c) Explain Von Newman model of computer system.

d) Explain various addressing modes with example.

OR

What are the steps in the execution of C program stored in memory? What are the possible ways to increase the program execution speed?

Unit - II

2. a) Define and explain Micro-instructions.

   b) What is Micro program? How it is different from Micro-Operation?

   c) Write the procedure to find 1's and 2's complement of a binary number.

   d) Discuss multiplication algorithm with the help of flow chart.

OR

What is the advantage of biased exponent representation in floating point numbers. Draw the flow chart for addition and substraction of two floating point numbers when mantissa are in Sign-magnitude form and exponents are biased exponents.

Unit - III

3. a) What is Direct memory access?

   b) What is interrupt? List various types of interrupts.

   c) Explain Handshaking.

   d) What do you mean by Data Transfer modes? Explain various data transfer modes in detail.

OR

What disadvantages are with strobe control method in asynchronous data transfer? How it resolved by Handshaking method.

Unit - IV

4. a) Define memory hierarchy. Draw block diagram.

   b) What is the significance of Cache memory?

   c) Explain the concept of associative memory.

   d) i) How many 128×8 RAM chips are needed to provide a memory capacity of 2048 bytes?

   ii) How many lines of address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips?

OR

A two level memory is consisting of Cache memory and main memory. The Cache is having hit ratio of 80% and it is 5 time faster than main memory if average access time is increased by 20% from 50ns. What is the change in hit ratio (approx).

Unit - V

5. a) Explain Pipeline.

   b) Write a note on Array processor.

   c) Explain the following:

   i) Throughput

   ii) Efficiency in reference of pipelining