d) Explain the principle of Latch up. Discuss about its physical origin, its triggering and its prevention methods.

OR

Write short notes (any two)

i) Algotronix

ii) NMOS Process

iii) BJT Noise Model

******

Roll No .....

EC-705

B.E. VII Semester

Examination, December 2016

VLSI Design

Time : Three Hours

Maximum Marks : 70

Note: i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.

ii) All parts of each question are to be attempted at one place.

iii) All questions carry equal marks, out of which part A and B (Max. 50 words) carry 2 marks, part C (Max. 100 words) carry 3 marks, part D (Max. 400 words) carry 7 marks.

iv) Except numericals, Derivation, Design and Drawing etc.

v) Assume suitable data if required.

1. a) Give a brief history of VLSI design explaining the effects of transistors in the discussion.

b) Give a classification of integrated circuits by device count.

c) Assume an OP-AMP requires an area 100 mil × 100 mil and a microprocessor requires an area 1cm × 1cm. How many of each type of chip can be fabricated on a 5 inch wafer?

d) If 1000 devices on a chip must have specific parameter within the specified design process window, determine the soft yield if the process has been characterized by a complexity index of :

i) Cp = 0.5

ii) Cp = 1.0

iii) Cp = 1.5

iv) Cp = 2.0

OR

Discuss about the recent trends in VLSI Design. How VLSI design will be economical? Give the major costs associated with wafer processing and fabrication.

2. a) What do you mean by Modeling? Explain dc Models in VLSI.

b) Explain the use of device models in circuit analysis.

c) Explain the quiescent output voltage and small signal steady state output voltage.

d) Obtain an expression in terms of quiescent excess gate bias, Vgs - Vt, that shows where the spectral density of the 1/f noise crosses over that of the thermal noise. Assume operation in the saturation region.

OR

Derive expressions for simple MOSFET models fc digital applications. Explain derivations for the Simpl digital inverter.

3. a) Explain the flowchart of SPICE subroutines.

b) Derive a relation of Noise Model of the MOSFET.

c) Explain the collector current and base current equatior of large signal BJT model.

d) Write and explain the various parameters which show temperature dependency of the BJT. Derive expressions to justify your answer.

OR

Compare the dc transfer characteristics (I_D Vs V_{DS} as a function of V_{GS}) for a MOSFET using Level 1 and Level 2 SPICE Models. Use the SPICE process model parameters.

4. a) Explain the Weinberger Arrays.

b) Use the Weinberger NOR array structure to implement the Exclusive - OR function.

c) Write some points on Random Logic Versus Structured logic forms.

d) Determine the voltage change on a DRAM data line caused by connection to a memory cell in terms of data line capacitance and memory cell capacitance.

OR

If a manufacturer's layout rate is eight transistors/day and a chip regularization factor of 20 is achieved, how many man years are required to lay out a 300,000 transistor chip.

ı) Draw and explain the various steps for the basic n-well CMOS process.

›) Discuss about the Twin tub process and its disadvantages in fabrication technique.

:) What do you mean by Interconnects? Discuss about its circuit elements.