**Roll No** .....

# EC - 304

## B.E. III Semester

Examination, June 2014

## Electronics Devices

***Time : Three Hours***

***Maximum Marks : 70***

***Note:*** i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.

ii) All parts of each question are to be attempted at one place.

iii) All questions carry equal marks, out of which part A and B (Max. 50 words) carry 2 marks, part C (Max. 100 words) carry 3 marks, part D (Max. 400 words) carry 7 marks.

iv) Except numericals, Derivation, Design and Drawing etc.

1. a) What condition must exist for diffusion to occur? 2

   b) Define an eV? 2

   c) A semiconductor has donor and acceptor concentration of $N_D$ and $N_A$ respectively. What relationship must be used to determine the electron n and hole P concentration. 3

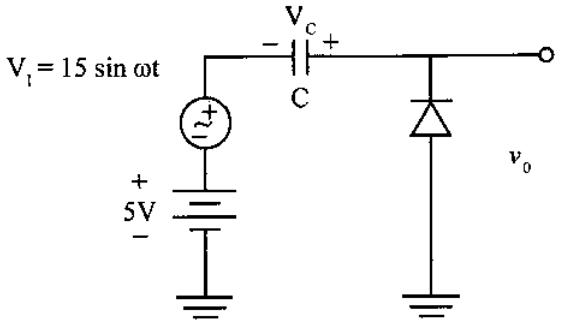
   d) Draw and explain VI characteristic of p-n junction. 7

   OR

   Explain Hall effect? 7

2. a) Explain a clipper circuit? 2

b) Find the steady state output of the diode clamper circuit shown in the fig. 2




c) Consider a full wave rectifier circuit with a 60 Hz i/p signal and a peak output voltage of $V_M = 10V$. Assume the output load resistance R = 10 KΩ and ripple voltage is to be limited to $V_r = 0.3$ V Determine capacitance required to yield a particular ripple. 3

d) Explain a sampling gate circuit. 7

OR

Explain working of a full wave bridge rectifier. 7

3. a) Describe the physical mechanism for avalanche breakdown. 2

b) What is a light emitting diode? 2

c) What are the two important difference between schottky diode and PN junction diode? 3

d) Sketch the Volt Ampere characteristic of a tunnel diode. Indicate the negative resistance portion. 7

OR





Draw the Volt Ampere characteristic of photodiode and write the equation for the volt ampere characteristic. 7

4. a) State true or false giving reasons. 2

i) Emitter area is smaller than the collector area

ii) Emitter is heavily doped than collector.

b) Define common emitter short circuit gain in words and by an equation. 2

c) What are the values of $V_{CE}$ at the edge of saturation $V_{BE}$ at cut in and $V_{BE}$ in active region? 3

d) Define four modes of BJT operation and indicate the principle behavior in each mode. 7

OR

Draw a circuit of a transistor in CE configuration sketch the output characteristics. 7

5. a) Define pinch off voltage $V_P$. 2

b) State three properties of an ideal voltage controlled current source. 2

c) Why are NMOS devices preferred over PMOS. 3

d) Explain what is meant by channel length modulation. 7

OR

Explain an NMOS enhancement device connected as a resistance. 7