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CS - 605

B.E. VI Semester

Examination, June 2014

Advance Computer Architecture

Time: Three Hours

Maximum Marks: 70

Note: Attempt one question from each unit. All questions carry equal marks. Assume data/value if required.

/ Unit - I

- Compare control-flow, data flow, and reduction computers in terms of the program flow mechanism used.
 - b) Explain the following:

- Computational granularity
- ii) Communication latency

OR

- Comment on the advantages and disadvantages in control complexity, potential for parallelism and cost effectiveness of the above computer models.
 - b) Write short note on multistage and combining networks.

Unit - II

- Distinguish between scalar RISC and super scalar RISC in terms of instruction issue, pipeline architecture and processor performance.
 - b) Explain the temporal locality, spatial locality, and sequential locality associated with program/data access in a memory hierarchy.

- Explain about addressing and timing protocol.
 - What do you understand by coherence? Explain briefly.

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PTO

Unit-III

5. Consider the five-stage pipelined processor specified by the following reservation table.

	1	2	3	4	5	6
S1	×	3.50				×
S2		×		2	×	
S3			×			
S4 S5			-	×		
S5		×				×

- List the set of forbidden latencies and the collision vector.
- What is the Minimum Average Latency (MAL) of this pipeline.
- Draw a state transition diagram.

- 6. a) Explain possible data hazards with its resolving techniques.
 - b) Discuss the difference between tomasulo's approach and using scoreboard techniques of dynamic scheduling. 7

Unit-IV

- Describe about vector super computer architecture.
 - Explain about distributed memory model.

- What is the use of snoopy protocol? Explain.
 - Write principles of multithreading. Also writes multi threading Issues.

Unit - V

- Discuss about parallel languages. Also writes its features.
 - Explain object oriented model.

- Write short note on message passing programming model.
 - b) Write features of parallel programming environment. 7

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