

**Team DOOS**  
**University of Jaffna**  
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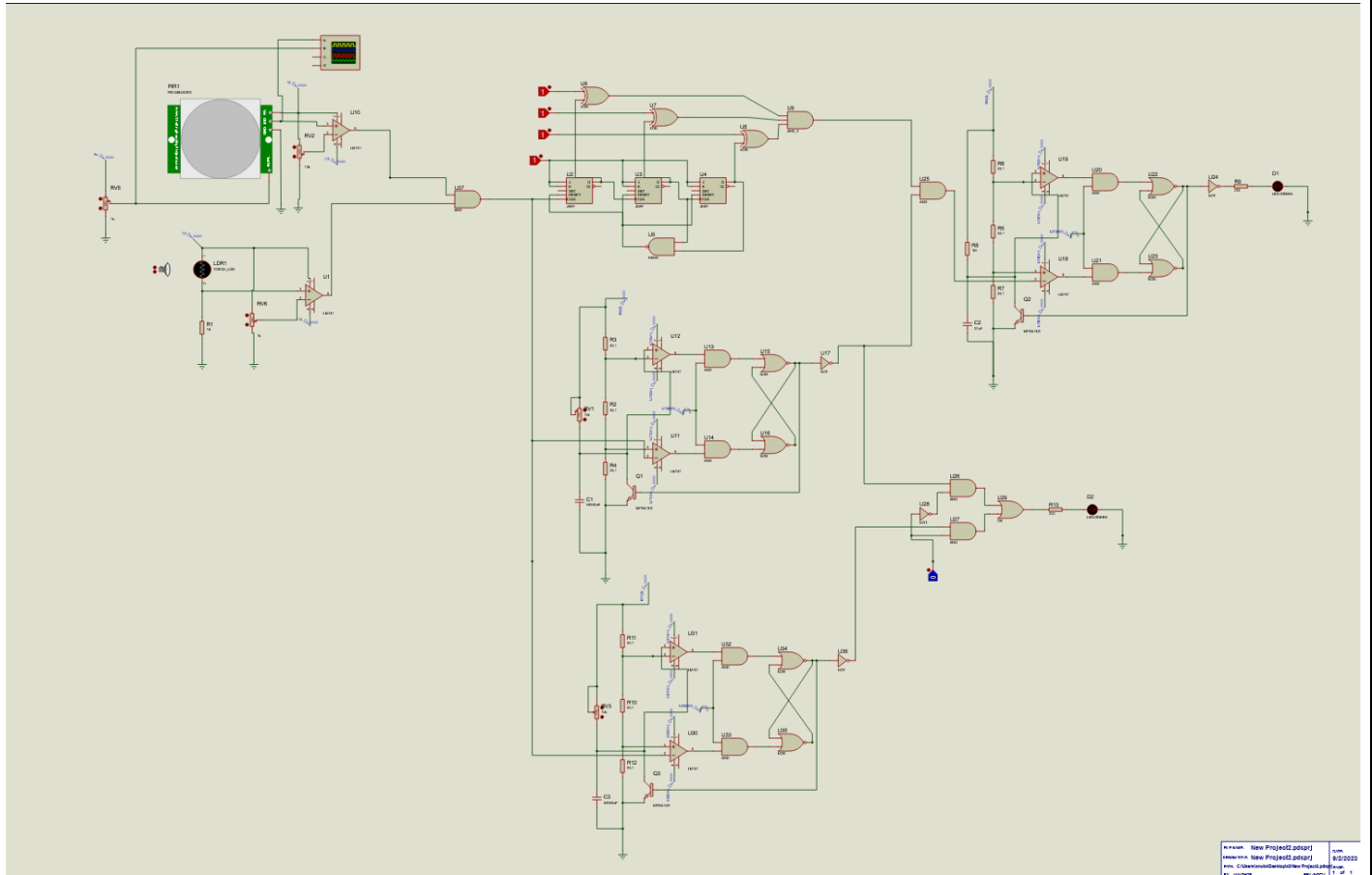
YESINDAN R

WIJAYARATHNA SKNH

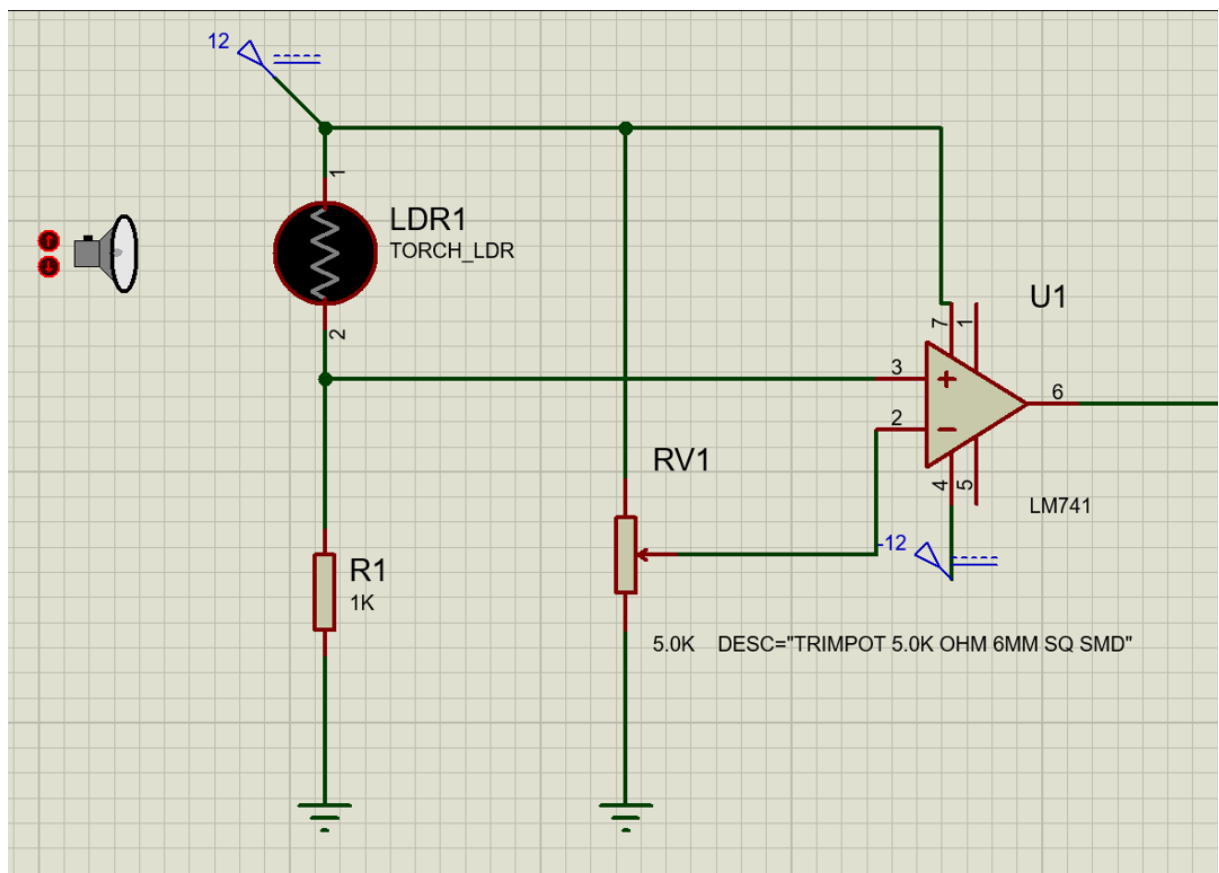
BENJAMIN R

KARUNANAYAKE DWAM

**PROTEUS VERSION – 8.13 SP0**



## DAYLIGHT ADJUSTMENT

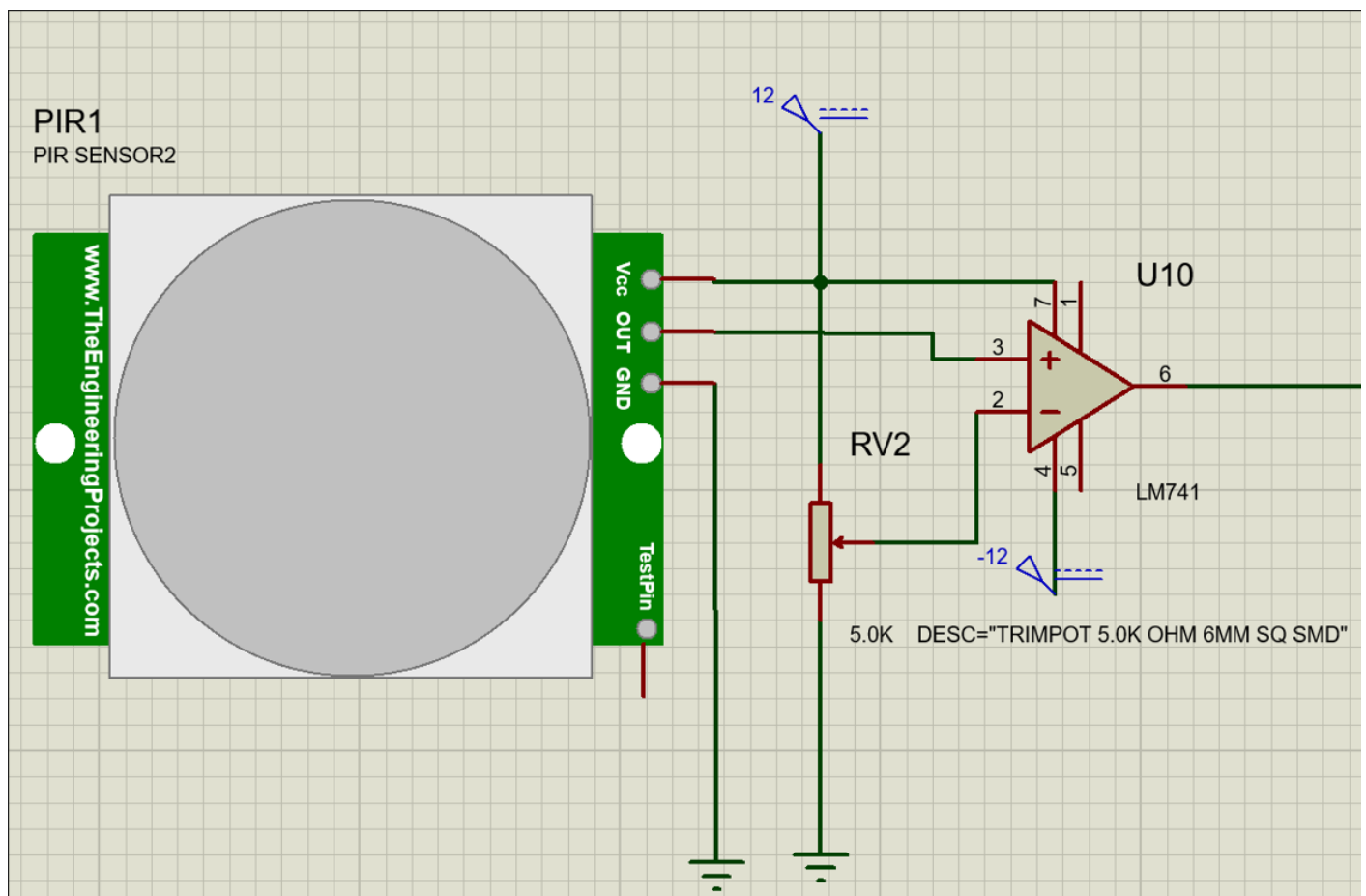


We have incorporated a sensitivity adjustment mechanism using a Light Dependent Resistor (LDR) and a comparator circuit. The LDR is connected to one input of the comparator, while the other input is connected to a potentiometer. This setup allows us to vary the threshold level for light detection by adjusting the potentiometer.

During daylight, the LDR's resistance is low, causing the comparator to maintain a high output. As the light level decreases, the resistance of the LDR increases, and when it surpasses the threshold set by the potentiometer, the comparator's output changes to low.

This configuration ensures the device to activate only when ambient light levels are below the predetermined threshold.

## Pyroelectric Motion Sensor with Adjustable Sensitivity



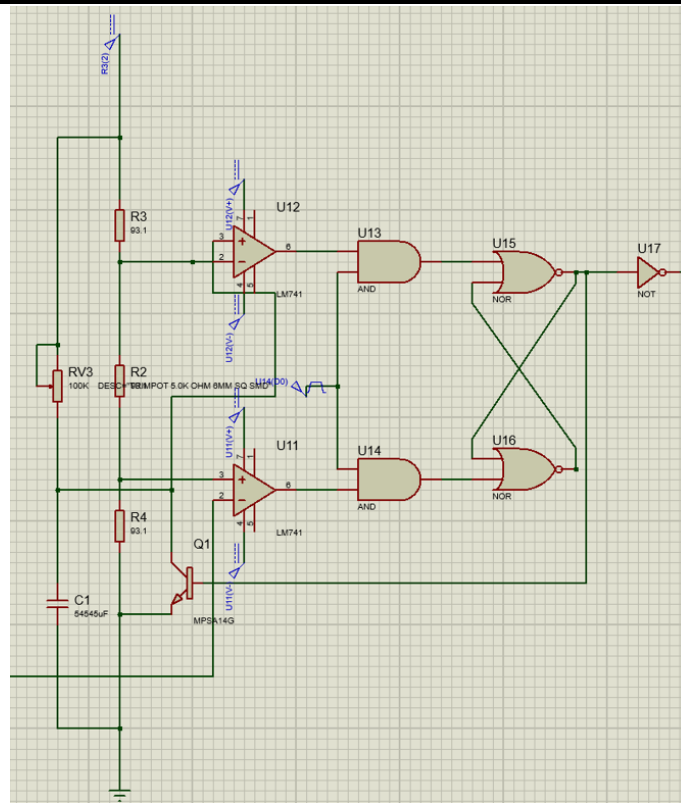
A Pyroelectric sensor, integrated with a comparator operational amplifier and potentiometer forms a sensitive motion detection system.

This potentiometer allows for precise adjustment of the sensitivity threshold. The Pyroelectric sensor detects changes in infrared radiation, it generates an electrical signal. When this electrical signal surpasses the set threshold determined by the potentiometer, the comparator's output set to produce a output signal.

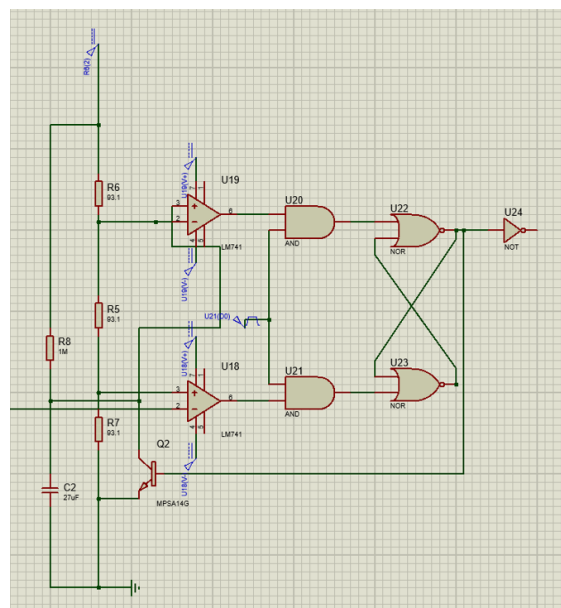
This configuration ensures that the system only responds to the specific predefined threshold

## **DAY LIGHT ADJUSTMENT 'AND' PYROELECTRIC CONFIGURATION**



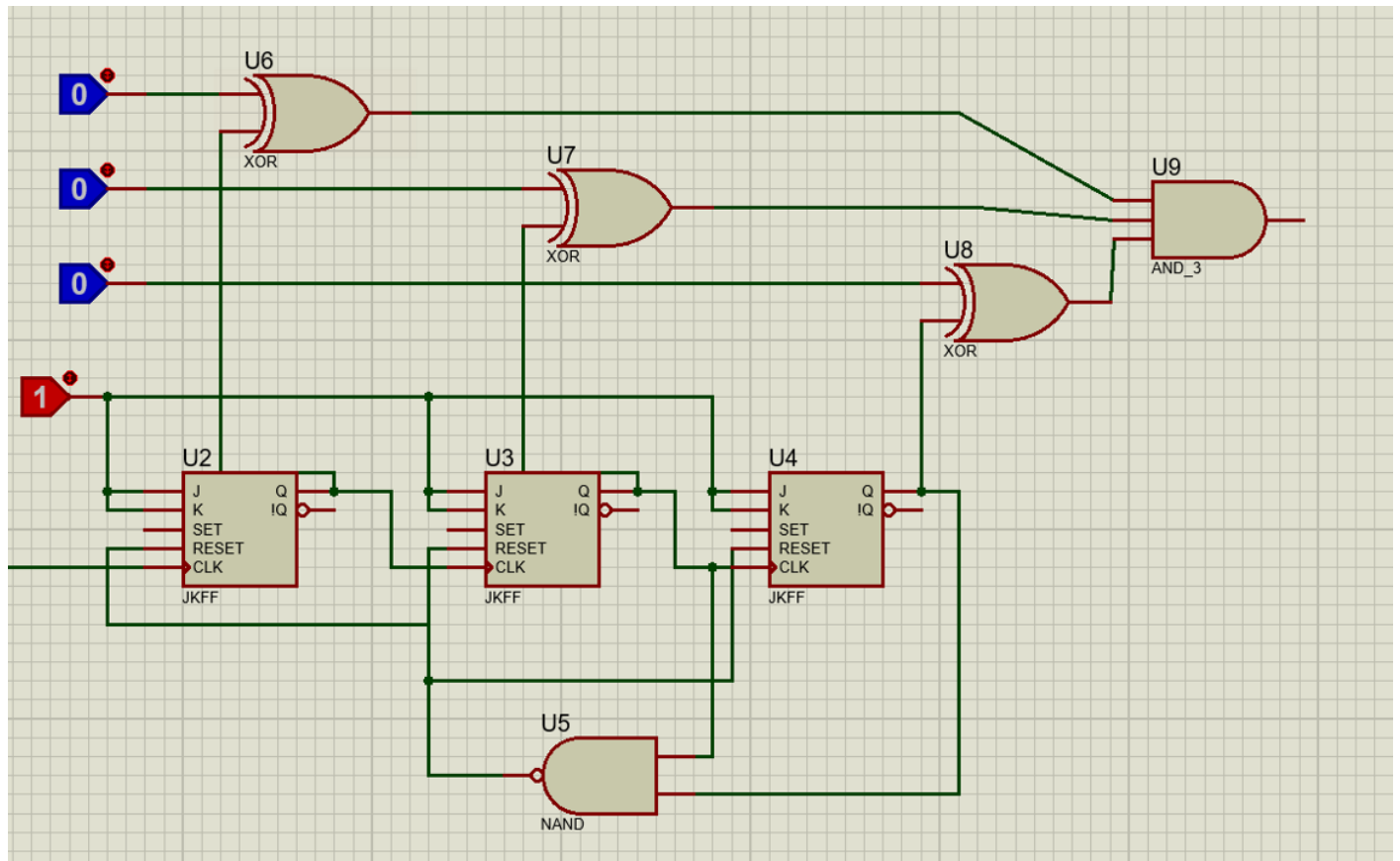


- R and C values for 30s fixed delay (Warning output)  
R-1Mohm  
C-27UF



The 555 timer IC starts in a stable LOW state. When the Trigger (PIN 2) is briefly connected to the Ground, it goes into a quasi-stable HIGH state due to the Lower Comparator, and the timing capacitor starts charging. When the capacitor voltage exceeds  $\frac{2}{3} V_{cc}$ , the Upper Comparator triggers and the output goes LOW. Simultaneously, a discharge path is activated, allowing the capacitor to discharge. This process repeats, creating a timing cycle with a duration determined by the RC network.

# UP COUNTER



The Logic toggles( input to the x-or) are used to set the threshold value for the triggers.

By configuring the switches(logic toggles) we can change the threshold level of the triggers.

up counter is a digital circuit that counts upwards, incrementing its output value with each pulse

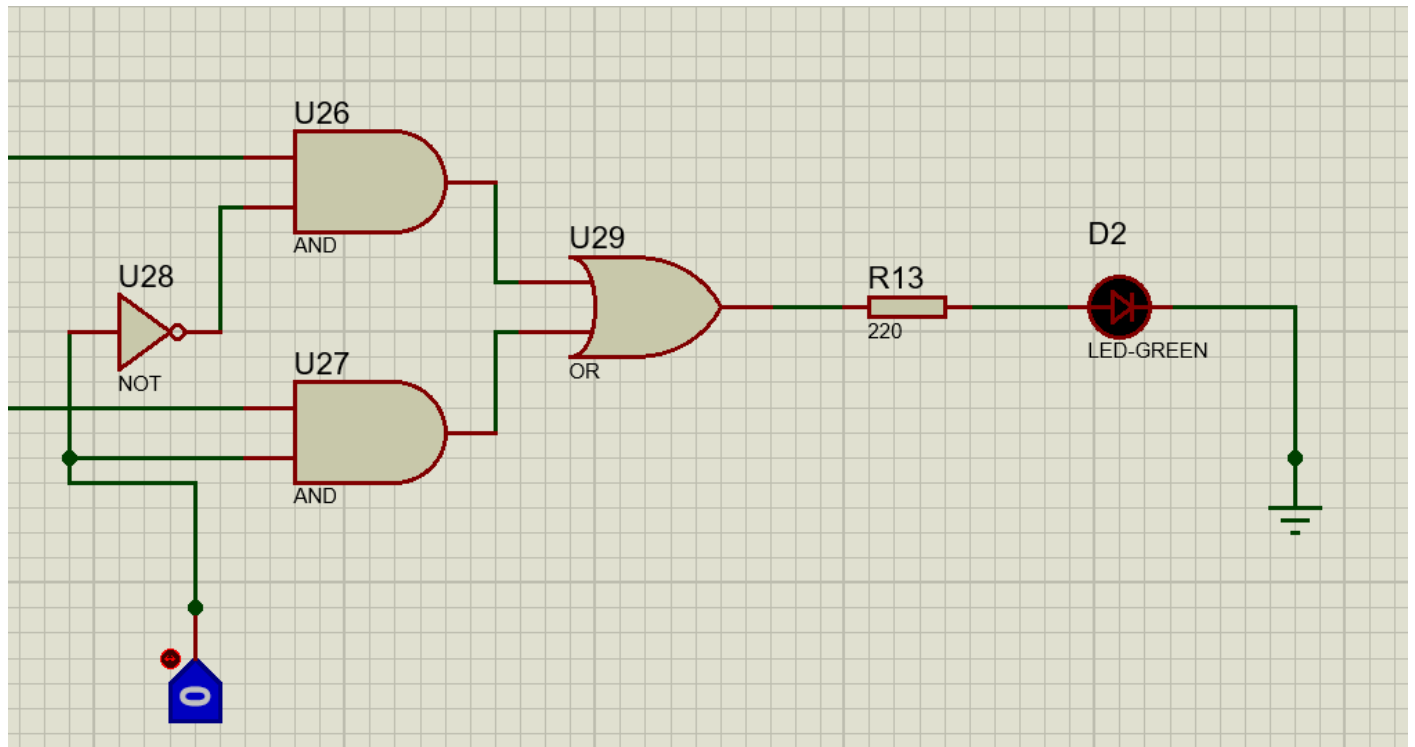
Counter Logic: The outputs of the flip-flops represent the binary count value.

- FF3 output is the least significant bit (LSB).
- FF2 output is the middle bit.
- FF1 output is the most significant bit (MSB).

To reset the counter to its initial state, set nand to '1' momentarily and then return it to '0'



## MULTIPLEXER Configuration



we have incorporated a switchable trigger mode feature using a multiplexer.

The module operates in two distinct modes: "Retrigger Mode" and "Normal Mode." In the Retrigger Mode, when the module's output is in a HIGH state and a new detection event occurs, the delay counting process restarts. This means that any subsequent detection while the output is HIGH will extend the delay period.

In Normal Mode, the module Not consider any new detections while the output is HIGH, effectively ignoring additional trigger events until the output goes LOW again.

By using Multiplexer we can toggle between these two modes.

## Normal mode and Retriggered mode combined using the multiplexer circuit

