

UNIT

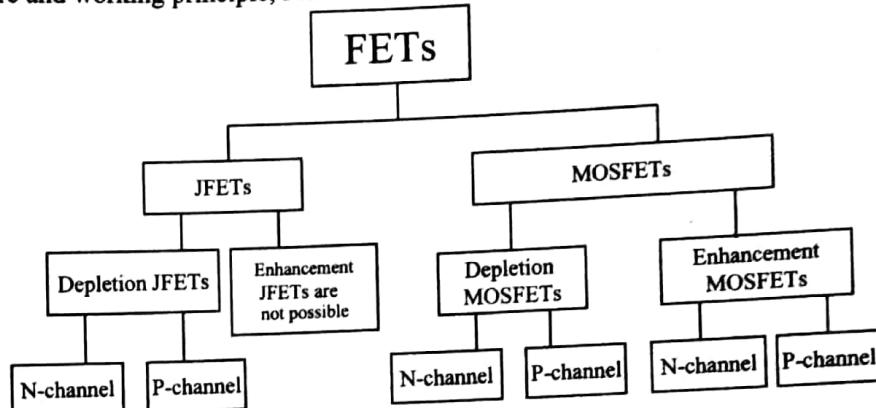
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PART-A SHORT QUESTIONS WITH SOLUTIONS

Q1. Classify different types of FETs.

Ans: Based on the structure and working principle, FETs are broadly classified as shown in figure.



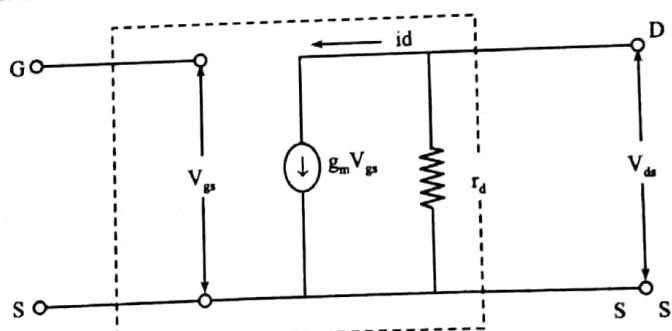
Figure

Q2. Draw the small signal equivalent model of JFET.

(Model Paper-I, Q9 | Dec.-15, Q6 | Dec.-13, Q14(b))

Ans:

The small signal equivalent model of JFET is shown in the figure.



Figure

Q3. State the advantages of Field Effect Transistor (FET) over bipolar junction transistor.

(Model Paper-II, Q9 | July-16, Q9)

(or)

List the advantages of JFET over BJT.

Ans:

The advantages of JFET over BJT are,

1. The operation of FET depends on only one type of charge carrier, either free electrons or holes, hence it is known as unipolar device.

5.2

2. It has very high input impedance.
3. JFET is less noisy than BJT.
4. JFETs are more temperature stable than BJT.
5. Fabrication is simple.
6. Occupies less space on the IC compared to BJT.

Q4. List any six applications of JFET.

Ans:

JFETs can be used for numerous applications as,

1. High Input Impedance Amplifier
2. Low-Noise Amplifier
3. Differential Amplifier
4. Constant Current Source
5. Analog Switch or Gate
6. Voltage Controlled Resistor.

Q5. List the advantages of MOSFET over JFET.

Ans:

July-10, Q5

JFET's and MOSFET's are field effect transistors which are configured and operated in, common source, common drain and common gate. But still MOSFETs are more suitable than JFETs in integrated circuits. The reasons are,

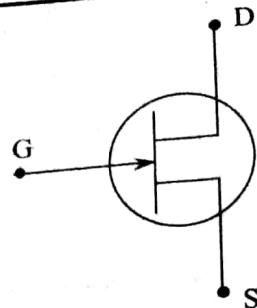
1. JFET uses p-n junction and has a direct electrical connection between the gate terminal and the channel. On the other hand, MOSFET gate is directly insulated by a semiconductor from the channel. Due to this, input resistance of MOSFET is very very high.
2. JFETs are operated only in depletion mode whereas MOSFETs are operated in both depletion and enhancement mode.
3. MOSFET's are characterized by negligible small leakage currents because of higher input impedance than compared to JFETs.
4. The characteristic curve of JFET is more flatter than that of MOSFETs, that means JFETs provide higher drain resistance.

Besides that, MOSFETs can be fabricated in small size to occupy less space in the large circuits. It can be used as resistors and diodes. Hence, due to these reasons, they are widely suitable than JFETs.

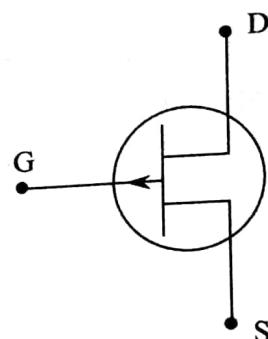
Q6. Draw the circuit symbol of P-channel and N-channel JFETs.

Ans:

The circuit symbols of P-channel and N-channel FETs are shown in figure.



(a): N-channel JFET



(b): P-channel JFET

Figure

Q7. Explain why E-MOSFET is called sometimes normally off-MOSFET.

Dec.12, Q5

(or)

Why E-MOSFET is called normally off-MOSFET?

Ans::

June/July-11, Q5

E-MOSFET has enhancement mode only it is operated with the large value of V_{GS} , i.e., gate source voltage. If V_{GS} is equal to 0 V then, the transistor goes to off condition. That is why E-MOSFET is also known as 'Off-MOSFET'.

Q8. Give the expression for drain current of a field effect transistor.

Ans:

The expression for drain current of a field effect transistor is given by,

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

Where,

I_{DSS} - Saturation drain current when $V_{GS} = 0$

V_{GS} - Gate to source voltage

V_P - Pinch-off voltage.

PART-B

ESSAY QUESTIONS WITH SOLUTIONS

5.1 JFET FORMATION – OPERATION AND CURRENT FLOW – PINCH-OFF VOLTAGE – V-I CHARACTERISTICS OF JFET

Q16. Compare BJT versus JFET.

Ans:

Dec.15, Q15(b)

The differences between BJT, JFET are mentioned below:

BJT	JFET
1. BJT is a current controlled device.	1. JFET is a voltage controlled device.
2. Two types of BJT are NPN and PNP.	2. Two types of JFET are n-channel and p-channel JFET.
3. Difficult to fabricate.	3. Fabrication process is easy.
4. Low input impedance.	4. High input impedance.
5. It is a bipolar device.	5. It is a unipolar device.
6. Switching speed is very less.	6. High switching speed.
7. Conduction is due to both majority and minority charge carriers.	7. Conduction is due to majority charge carriers.
8. It produces less signal distortion.	8. It produces more signal distortion.

Q17. Describe the construction and principle of operation of n-channel JFET.

Ans:

Construction of n-channel JFET

An n-channel JFET is fabricated (or constructed) on n-type semiconductor bar that is as shown in figure (1). The left end of the n-type semiconductor bar is known as source and the right end is known as drain. To produce a JFET the n-type bar is heavily doped with two p-type regions at its middle part as shown in figure (2). The p-type regions are doped into n-type bar using diffusion process. Both the p-type regions are connected internally and a single wire is taken out in the form of a terminal called a gate. Diffusion of p-type regions into n-type region creates two pn-junctions (shaded region) as shown in figure (2).

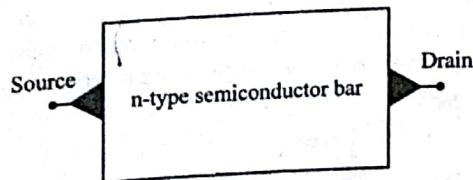


Figure (1): N-type Semiconductor Bar

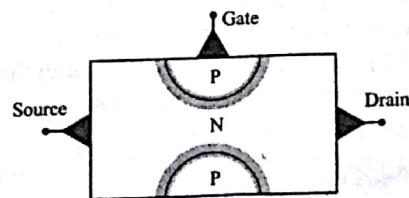


Figure (2): Field Effect Transistor

Operation

The operation of JFET is as follows,

- Initially, with $V_{GS} = 0$ V and application of a voltage V_{DD} across the drain and source terminals as shown in figure (3), causes a current I_D to flow from drain to source.

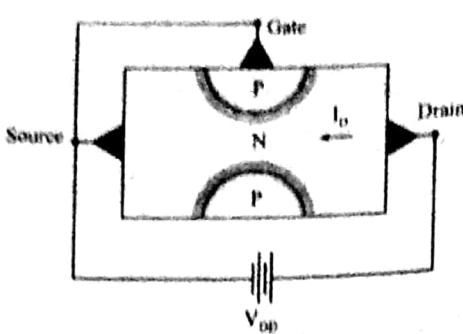


Figure (3): Application of V_{GS}

2. The current I_D flowing through the n-channel can be controlled by applying a negative voltage to the gate and source terminals as shown in figure (4). The negative V_{GS} reverse biases the two p-n junctions and widens the depletion regions. The depletion region extends (or spreads) more into the n-channel because it is doped lightly compared to p-regions. In other words, to make the depletion region extend more into the n-channel, the two p-regions are doped very heavily. The extension of depletion region decreases the width of the channel as shown in figure (4). This in turn decreases the current I_D flowing through the channel.

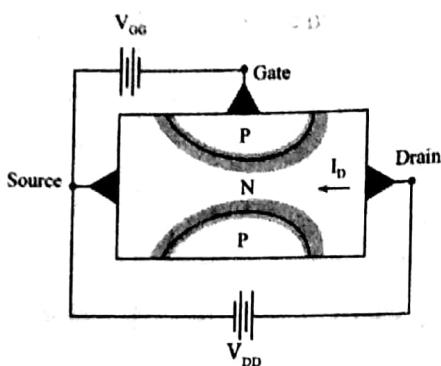


Figure (4): Application of V_{GS}

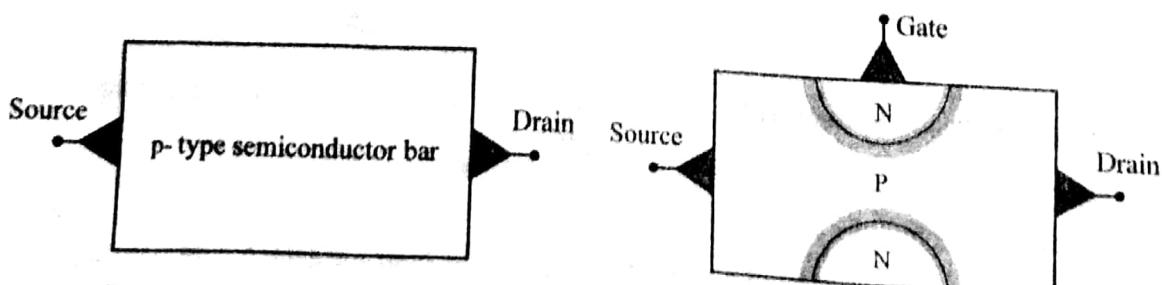
Since the current I_D flowing through the channel is controlled by the voltage V_{GS} , JFET is known as voltage controlled device.

3. Continuous increase in the negative voltage V_{GS} can cause the depletion region to extend more and more into the channel. Finally, the entire channel gets occupied by the depletion region and *depleted* of charge carriers (electrons) as shown in figure. The value of V_{GS} at which the entire channel gets occupied by the depletion-region is known as '*threshold voltage*' of the device ' V_t '. For JFETs the threshold voltage is called the "*pinch-off voltage*" and is denoted by ' V_p '.

Q3. Describe the construction and principle of operation of p-channel JFET.

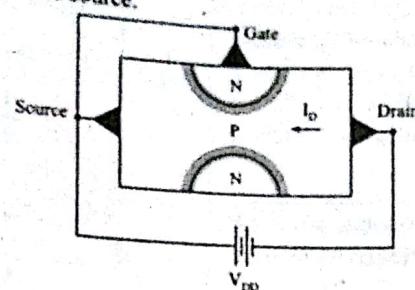
Ans:

Construction of p-channel JFET: An p-channel JFET is fabricated (or constructed) on p-type semiconductor bar that is as shown in figure (1). One end of the p-type semiconductor bar is known as source and the other end is known as drain. To produce a, JFET the p-type bar is heavily doped with two n-type regions at its middle part as shown in figure (2). The n-type regions are sandwiched into p-type bar using diffusion process. Both the n-type regions are connected internally and a single wire is taken out in the form of a terminal called a gate. Diffusion of n-type regions into p-type region creates two pn-junctions (shaded region) as show in figure (2).

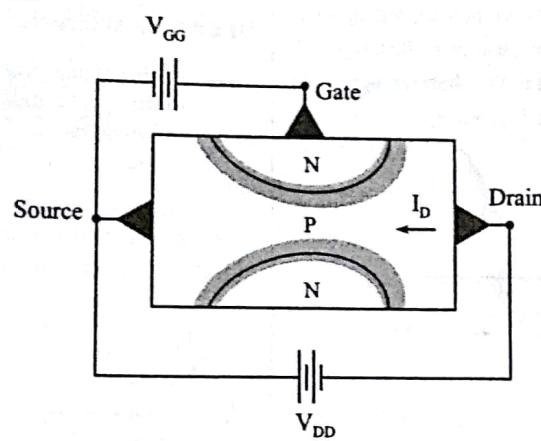


Operation

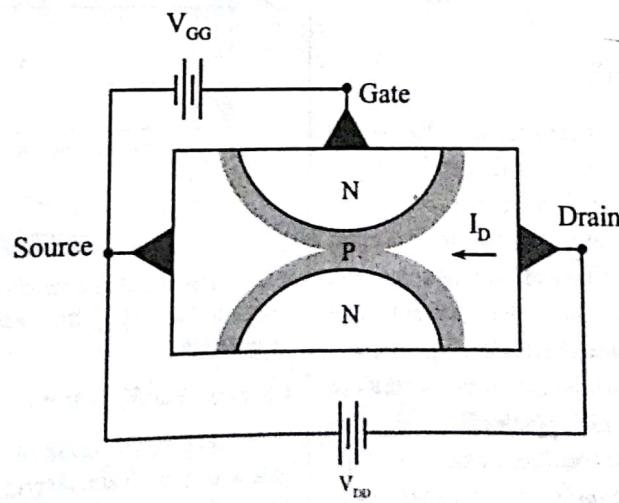
- The operation of JFET is as follows.
- Initially, with $V_{GS} = 0V$ and application of a voltage V_{DS} across the drain and source terminals as shown in figure (3), causes a current I_D to flow from drain to source.

Figure (3): Application of V_{DS}

- The current I_D flowing through the p-channel can be controlled by applying a positive voltage to the gate and source terminals as shown in figure (4). The positive V_{GS} reverse biases the two p-n junctions and widens the depletion regions. The depletion region extends (or spreads) more into the p-channel because it is doped lightly compared to n-regions. In other words, to make the depletion region extend more into the p-channel, the two n-regions are doped very heavily. The extension of depletion region decreases the width of the channel as shown in figure (4). This in turn decreases the current I_D flowing through the channel.

Figure (4): Application of V_{GS}

Since the current I_D flowing through the channel is controlled by the voltage V_{GS} , JFET is known as voltage controlled device.

Figure (5): Channel at V_{GS} Threshold

3. Continuous increase in the positive voltage V_{DS} can cause the depletion region to extend more and more into the channel. Finally, the entire channel gets occupied by the depletion region and *depleted* of charge carriers (holes) as shown in figure (3). The value of V_{DS} at which the entire channel gets occupied by the depletion region is known as '*threshold voltage*' of the device ' V_p '. For JFETs the threshold voltage is called the "*pinch-off voltage*" and is denoted by ' V_p '.

Q19. What is meant by pinch-off voltage, pinch-off locus of JFET? Mark pinch-off locus from drain characteristics.

Ans:

When a positive voltage is applied to the drain terminal of the JFET, it starts conducting the current. The drain current I_D raises to reach a saturation value I_{DSS} . The magnitude of drain current depends entirely on the channel resistance. The channel resistance increases as the depletion region from both sides penetrates into the channel. Figure (1) below shows the characteristics of V_{DS} , V_p , I_D .

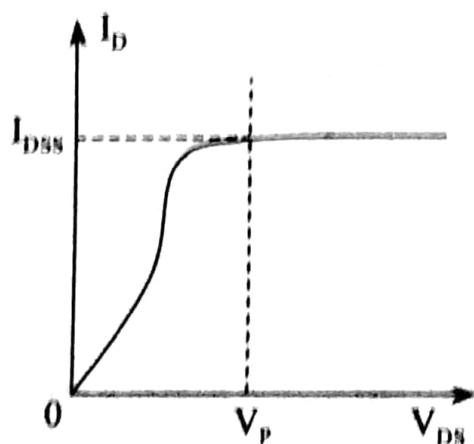


Figure (1)

As it is relevant from the characteristic, that as V_{DS} increases from 0, the drain current increases and at $V_{DS} = V_p$ the drain current is saturated, further increase in V_{DS} does not effects I_D . The voltage at which the drain current becomes constant is known as pinch-off voltage, here the two depletion regions touch each other reducing the channel width to zero and hence the channel offers large resistance. Locus of something is the point at which it occurs. Therefore pinch-off locus is the point at which pinch-off occurs. The drain characteristics are shown below. The pinch-off voltage and pinch-off locus are marked on the graph as shown in figure (2).

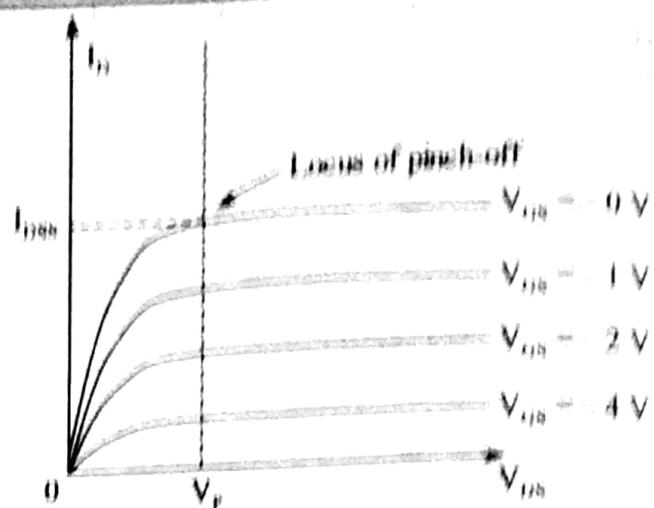


Figure (2): JFET Drain Characteristics

Q20. Explain the drain and transfer characteristics of N-channel JFET.

Ans:

(Model Paper-I, Q17(a) | July-16, Q19(a))

Drain Characteristics of JFET

A plot of the drain current I_D as a function of drain source voltage V_{DS} , keeping V_{GS} constant is known as drain curve or drain characteristics. Further, these are also known as V - I characteristics or output characteristics of the JFET.

Figure (a) illustrates the V - I characteristics, that is, the characteristics between drain current I_D and the drain to source voltage V_{DS} for various values of gate to source voltage V_{GS} .

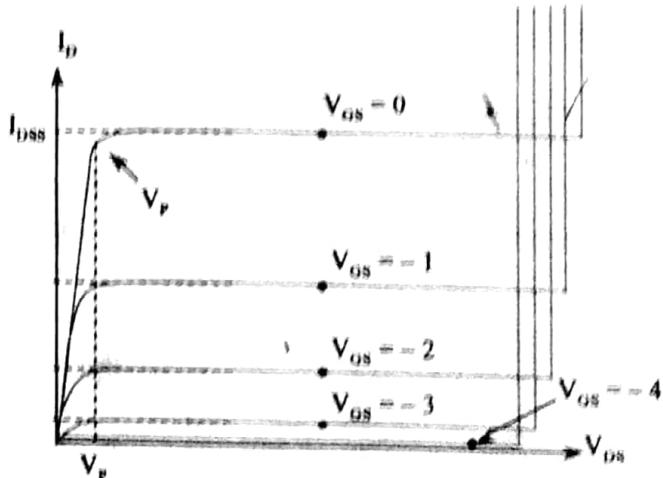


Figure (a): Drain Curves

The V - I characteristics are for various values of gate to source voltage (V_{GS}) from zero to negative, because V_{GS} cannot be positive.

Case (i) : For $V_{GS} = 0$ V

Fixing the value of V_{GS} to zero volts (short circuiting gate and source) and increasing the drain to source voltage V_{DS} from 0 V in steps, causes a drain current I_D to flow through the channel.

Initially, the current I_D increases linearly with V_{DS} and becomes constant for $V_{DS} > V_p$. The minimum drain-source voltage at which the drain current becomes constant is known as "pinch off voltage" denoted as ' V_p '. When $V_{DS} = V_p$, the depletion layers almost touch each other. This pinches off or prevents a further increase in current.

An important thing to be observed in the characteristics is that when $V_{GS} = 0V$ the current which is flowing between drain and source due to presence of small positive voltage V_{DS} saturating value of that current is known as I_{DSS} . I_{DSS} is maximum current flowing in the device when $V_{GS} = 0V$. In other words, this is the maximum drain current a JFET can produce.

Case (ii) : for V_{GS} = Negative Value

Figure (a) illustrates the plots of I_D versus V_{DS} making V_{GS} more and more negative. It is observed that as V_{GS} becomes more and more negative, the drain current becomes very less. This is because the cross-sectional area of the channel decreases. At some value of gate to source voltage V_{GS} , the depletion layers extend completely across the channel and the channel is cut-off. As a consequence, the drain current I_D becomes zero. The value of V_{GS} at which the channel is cut-off is called gate-source cut-off voltage $V_{GS(off)}$.

It is interesting to observe that the value of $V_{GS(off)}$ is equal and opposite to V_p , that is, if $V_p = 6V$ then $V_{GS(off)} = -6V$.

Regions in the Characteristics

The $V-I$ characteristics or drain characteristics of the junction field effect transistor shown in figure (a) can be divided into three regions as shown in figure (b). They are,

1. Ohmic region
2. Active region
3. Cut-off region.

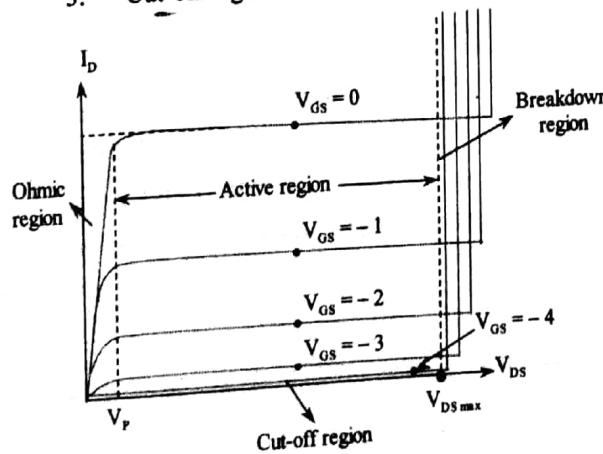


Figure (b): Drain Curves

- ❖ The region between $0 < V_{DS} < V_p$ is known as ohmic region. In this region V_{DS} is small and below pinch off.
- ❖ The region between $V_p < V_{DS} < V_{DS(\max)}$ is known as active region. $V_{DS(\max)}$ is the maximum voltage that can be applied to JFET. If V_{DS} exceeds $V_{DS(\max)}$ then JFET would or will breakdown.

The active region is also known as "constant current region". In this region I_D is independent of V_{DS} .

The region below $V_{GS(off)}$ is known as cut-off region.

Transfer Characteristics of JFET

For JFET, the current in the active region is independent of V_{DS} and varies with changes in the gate-to-source voltage V_{GS} . A plot of the drain current " I_D " as a function of gate source voltage V_{GS} is known as "Mutual Characteristics" or "transfer characteristics" of JFET.

The characteristics are plotted by reading different values of I_D for different values of V_{GS} in the $V-I$ characteristics drain characteristics of the JFET. Figure (c) illustrates the plot of mutual characteristics from the drain characteristics.

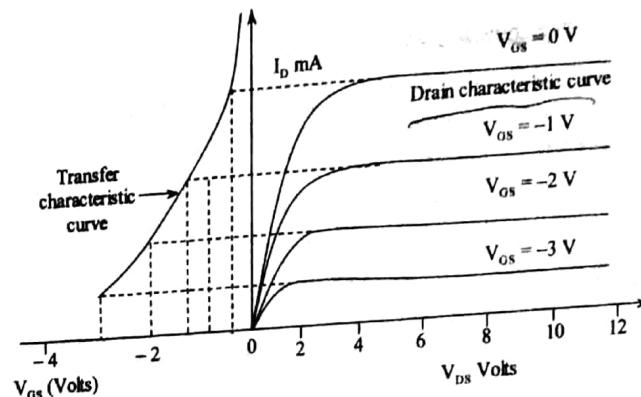


Figure (c): Characteristics of JFET

From figure (c), it is observed that the drain current ' I_D ' is related to V_{GS} in a parabolic manner. The end points on the curve are $V_{GS(off)}$ and I_{DSS} . Equation for the parabolic curve in figure (a) is,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2$$

This is an important equation that gives the relation between drain current ' I_D ' in terms of gate source voltage V_{GS} .

The curve in figure is also known as transconductance curve.

Q21. Define parameters of JFET and obtain the relation among them.

Ans:

To evaluate the performance of JFET in a circuit, the certain parameters defined are,

- (a) Dynamic drain resistance, r_d
- (b) Transconductance, g_m .
- (c) Amplification factor, μ .

5.10

(a) Dynamic Drain Resistance, r_d

Dynamic resistance also known as A.C. resistance is measured around the operating point. It is defined as the ratio of small change in drain source voltage to small change in drain current at constant gate to source voltage V_{GS} , that is,

$$r_d = \left. \frac{\Delta V_{DS}}{\Delta I_D} \right|_{V_{GS} \text{ constant}} \quad \dots (1)$$

(b) Transconductance (g_m)

Transconductance is also known as mutual conductance. It is defined as the ratio of small change in drain current to small change in gate to source voltage at a constant drain source voltage V_{GS} , that is,

$$g_m = \left. \frac{\Delta I_D}{\Delta V_{GS}} \right|_{V_{DS} \text{ constant}} \quad \dots (2)$$

(c) Amplification Factor (μ)

It is defined as the ratio of small change in drain source voltage to small change in gate source voltage at a constant drain current I_D , that is,

$$\mu = \left. \frac{\Delta V_{DS}}{\Delta V_{GS}} \right|_{I_D \text{ constant}} \quad \dots (3)$$

Relation between μ , g_m and r_d

The expression for amplification factor μ is,

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

Multiplying and dividing by ΔI_D , the above equation can be written as,

$$\begin{aligned} \mu &= \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D} \\ &= \mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}} \quad \dots (4) \end{aligned}$$

Since, $r_d = \frac{\Delta V_{DS}}{\Delta I_D}$ and $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ equation (4) can be written as,

$$\mu = r_d g_m$$

$$\therefore \mu = g_m r_d$$

Q22. Prove that the trans-conductance gm of a JFET is given by $gm = \frac{2}{|V_p|} \sqrt{I_D I_{DSS}}$,

where, V_p = Pinch-off voltage, I_{DSS} = Drain Current, I_{DSS} = Max. I_D corresponding to $V_{GS} = 0$ volt.

Ans:

(Jan-12, Q13(b); Dec-10, Q13(a))

From the transfer characteristics of JFET, the relationship between I_D and V_{GS} is defied (From shockley's equation) is,

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_p} \right]^2 \quad \dots (1)$$

Where,

I_D = Saturation drain current

I_{DSS} = I_D when $V_{GS} = 0$

V_p = Pinch-off voltage.

By taking differentiation on both sides of equation (1) it becomes,

$$\frac{\partial I_D}{\partial V_{GS}} = I_{DSS} \times 2 \left(1 - \frac{V_{GS}}{V_p} \right) \left(-\frac{1}{V_p} \right) \quad \dots (2)$$

From the definition of trans-conductance (g_m), g_m can be defined as,

$$g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{V_{DS} \text{ constant}} = \text{Constant}$$

Equation (1) may write as,

$$\sqrt{\frac{I_D}{I_{DSS}}} = \left[1 - \frac{V_{GS}}{V_p} \right] \quad \dots (3)$$

From equations (2) and (3), g_m can be expressed as,

$$g_m = \frac{+2 I_{DSS}}{-V_p} \sqrt{\frac{I_D}{I_{DSS}}}$$

$$g_m = \frac{2}{|V_p| \sqrt{I_D I_{DSS}}} \quad \{ \because V_p > 0 \}$$

Hence, proved.

Q23. A FET has a driven current of 4 mA. If $I_{DSS} = 8$ mA and $V_{GS(\text{off})} = -6$ V find the values of V_{GS} and V_p

Ans:

Given that,

$$\begin{aligned} \text{Drain current } (I_D) &= 4 \text{ mA} \\ &= 4 \times 10^{-3} \text{ A} \end{aligned}$$

$$\begin{aligned} \text{Saturation drain current } (I_{DSS}) &= 8 \text{ mA} \\ &= 8 \times 10^{-3} \text{ A} \end{aligned}$$

$$V_{GS(\text{off})} = -6 \text{ V}$$

The expression for drain current in JFET is given as,

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right]^2 \quad \dots (1)$$

Substitute the given values in above equation, we get

$$\Rightarrow 4 \times 10^{-3} = 8 \times 10^{-3} \left[1 - \frac{V_{GS}}{(-6)} \right]^2$$

$$\Rightarrow 2 \left(1 + \frac{V_{GS}}{6} \right)^2 = 1$$

$$\Rightarrow \left(1 + \frac{V_{GS}}{6} \right)^2 = \frac{1}{2}$$

$$\Rightarrow 1 + \frac{V_{GS}}{6} = \frac{1}{\sqrt{2}}$$

$$\Rightarrow \frac{V_{GS}}{6} = -1 + 0.707$$

$$\Rightarrow V_{GS} = -6 \times 0.293 \\ = -1.758$$

$$\therefore V_{GS} = -1.758$$

And we know that

$$V_P = |V_{GS}(\text{off})|$$

$$\Rightarrow V_P = |-6| \\ = 6 \text{ V}$$

$$\therefore V_P = 6 \text{ V}$$

5.2 JFET BIASING - LOW FREQUENCY SMALL SIGNAL MODEL OF FETs

Q24. Explain low frequency analysis in a small signal model of JFET.

Ans:

Low frequency equivalent circuit of JFET is shown in figure.

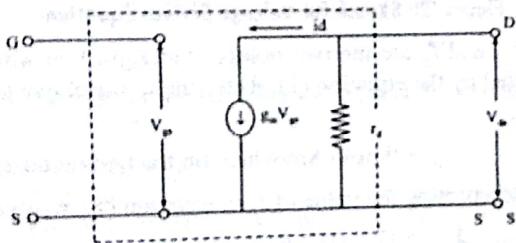


Figure: Equivalent Circuit of JFET

The value of drain current is obtained and depends on the gate to source voltage (V_{gs}) and transconductance (g_m). The product ' g_m ' and ' V_g ' represented by using current source. The drain current also depends on channel internal resistance ' r_d '. It is referred as output impedance. It is obtained from drain to source voltage. Source gate junction is always reverse biased, which means that it is open circuit in figure (1). This model satisfies the following relation,

$$I_D = V_{gs} \cdot g_m + \frac{V_{ds}}{r_d}$$

Where

V_{gs} – Gate to source voltage

V_{ds} – Drain to source voltage

g_m – trans conductance.

Q25. What are the biasing schemes available to achieve the required bias in a junction field effect transistor? Explain any one of the biasing schemes.

Ans:

The biasing schemes available to achieve the required bias in JFET are as follows,

1. Fixed bias
2. Collector to base bias
3. Self bias (or) voltage divider bias.

Fixed Bias

The commonly used fixed bias circuits are shown in figure (1).

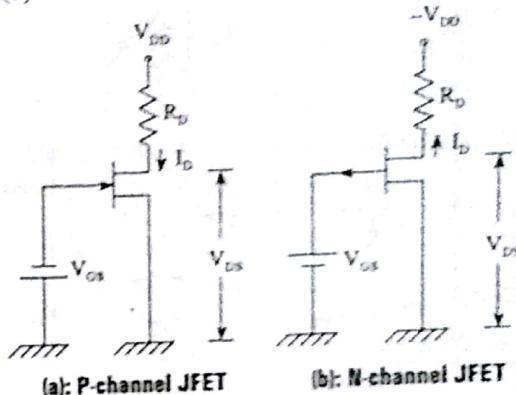


Figure (1)

The D.C voltages are used in this type of circuits, one is for providing V_{DD} and another is used for providing the gate to source voltage (V_{GS}). Here, the gate to source voltage is fixed, hence the name fixed bias.

For N-channel JFET, we have,

$$V_{DS} = V_{DD} - I_D R_D \quad \dots (1)$$

For P-channel JFET, we have,

$$V_{DS} = -[V_{DD} - I_D R_D] \quad \dots (2)$$

V_{DD} must be always positive.

Hence, V_{DS} is negative for P-channel and positive for N-channel operation.

The transfer characteristics of fixed bias JFET is shown in figure (2).

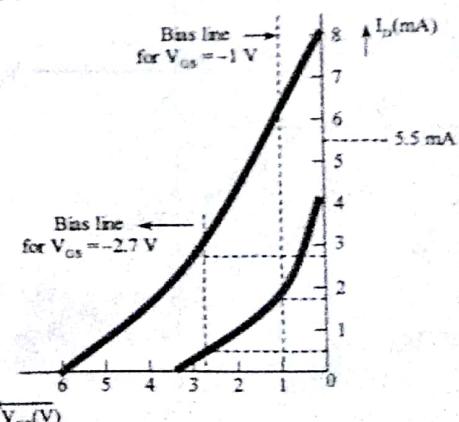


Figure (2): Transfer Characteristics of a Fixed Bias JFET

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Q.12

Q26. Draw a voltage divider bias JFET circuit and explain how the Q-point is set in it.

Ans:

Figure (1) shows the voltage divider bias JFET circuit and its Thevenin's equivalent circuit is shown in figure (2).

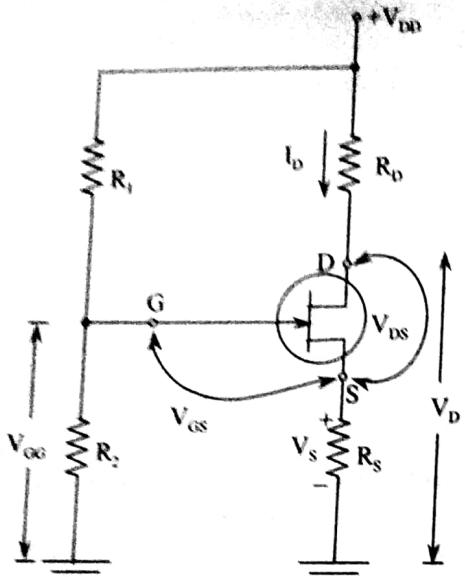


Figure 1: Voltage Divider Bias Circuit

Voltage divider is formed by connecting R_1 and R_2 on the gate side. Hence, we have,

$$\text{Gate voltage, } V_{GS} = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD} \text{ and}$$

$$\text{Gate resistance, } R_G = \frac{R_1 R_2}{R_1 + R_2}$$

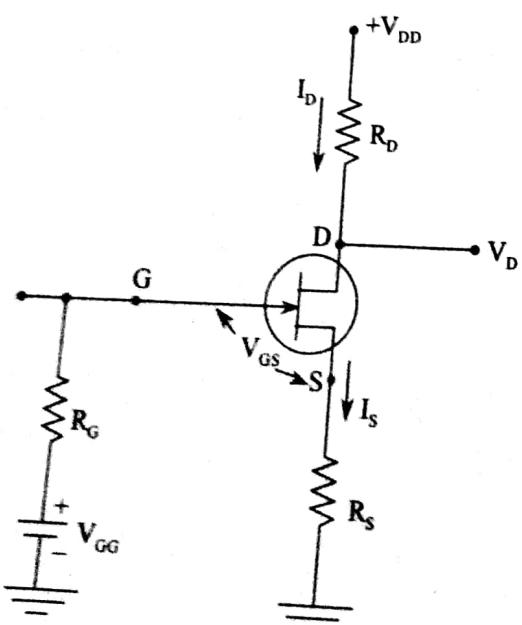


Figure 2: Representing Thevenin's Equivalent Circuit

After applying Kirchhoff's voltage law to the above circuit, we get,

$$V_{DS} = V_{DD} - I_D R_S \quad (\because I_S = I_D) \quad \dots (1)$$

The drain to ground voltage is $V_D = V_{DD} - I_D R_D$. Due to network construction, V_D and R_S are fixed. The next step is to plot the equation (1).

Equation (1) represents an equation for the straight line. Figure (3) represents the sketch for the voltage divider configuration.

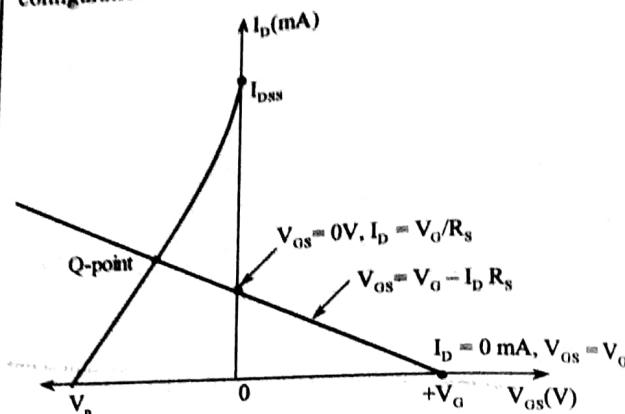


Figure 3: Sketch for Voltage Divider Equation

V_{GS} and I_D are the two points of straight line which is represented by the equation (1). Referring to the above graph, we have,

$$I_D = 0 \text{ mA (Anywhere on the horizontal axis)}$$

Substituting the value of I_D in equation (1), we get,

$$V_{GS} = V_{GG} - 0 \times R_S$$

$$V_{GS} = V_{GG}|_{I_D=0}$$

$$\text{i.e., } V_{GS} = V_{GG} \text{ when } I_D = 0$$

This is shown in the graph.

To find out second point I_D , we have,

$$V_{GS} = 0 \text{ (The value of } V_{GS} = 0 \text{ on the vertical axis)}$$

Substituting this value in equation (1), we get,

$$V_{GS} = V_{GG} - I_D R_S$$

$$0 = V_{GG} - I_D R_S$$

$$V_{GG} = I_D R_S$$

$$I_D = \frac{V_{GG}}{R_S} \Big|_{V_{GS}=0}$$

i.e., $I_D = \frac{V_{GG}}{R_S}$ when $V_{GS} = 0$. This is also shown in the graph.

These two points are needed to draw the straight line represented by equation (1). When this line intersects with the transfer curve shown in the second quadrant, the intersection point gives the operating point and corresponding levels of I_D and V_{GS} .

LAW OF VARIATION OF Q WITH V_{DS}

When $I_D = \frac{V_{DD}}{R_s}$, the straight line is intersected by the vertical axis. Since, V_{DD} is fixed, increasing or decreasing the value of R_s will decrease or increase the levels of I_D . This is shown in the figure (4).

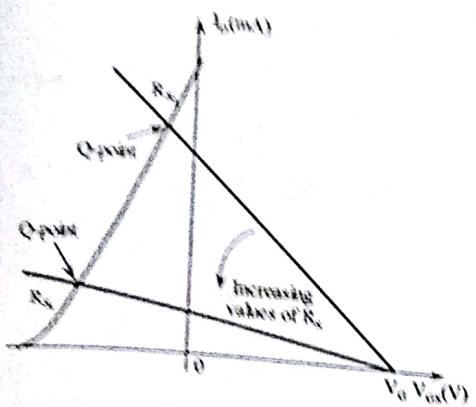


Figure (4)

Increasing the values of R_s results in lower quiescent values of I_D and more negative values of V_{GS} .

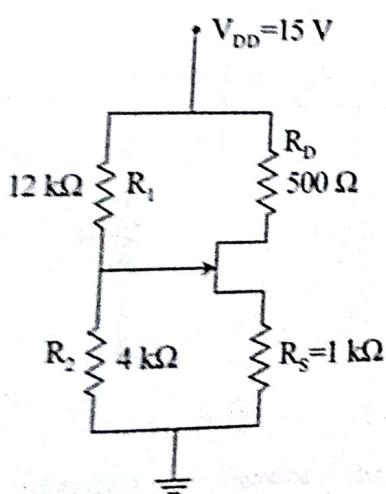
$$V_{GS} = V_{DD} - I_D (R_D + R_s)$$

$$V_D = V_{DD} - I_D R_s \quad [\because V_S = I_D R_s]$$

The current through resistors R_1 and R_2 is same i.e.,

$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$

Q27. For the JFET circuit with voltage divider bias as shown below, calculate V_G , V_S , V_D and V_{GS} if $V_{GS} = -2$ V.



Figure

Ans:

Given that,

For a JFET circuit with voltage divider bias,

$$V_{GS} = -2 \text{ V}$$

$$V_{DD} = 15 \text{ V}$$

$$R_1 = 12 \text{ k}\Omega$$

$$R_2 = 4 \text{ k}\Omega$$

$$R_D = 500 \text{ }\Omega$$

$$R_S = 1 \text{ k}\Omega$$

Find,

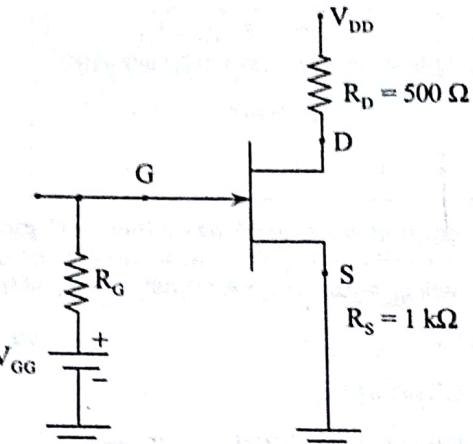
$$V_G = ?$$

$$V_D = ?$$

$$V_S = ?$$

$$V_{DS} = ?$$

The given JFET circuit with voltage divider bias can be rearranged as shown in figure below:



Figure

Where,

$$\begin{aligned} V_{GG} &= \frac{R_2 V_{DD}}{R_1 + R_2} \\ &= \frac{4 \times 10^3 \times 15}{12 \times 10^3 + 4 \times 10^3} \\ &= 3.75 \text{ V} \end{aligned}$$

$$\therefore V_G = V_{GG} = 3.75 \text{ V}$$

$$\begin{aligned} R_G &= \frac{R_1 R_2}{R_1 + R_2} \\ &= \frac{4 \times 10^3 \times 12 \times 10^3}{12 \times 10^3 + 4 \times 10^3} \\ &= 3 \text{ k}\Omega \end{aligned}$$

$$\begin{aligned} V_{GS} &= V_{GG} - I_D R_S \\ -2 &= 3.75 - I_D \times 10^3 \end{aligned}$$

$$\begin{aligned} I_D \times 10^3 &= 3.75 + 2 \\ &= 5.75 \end{aligned}$$

$$\Rightarrow I_D = 5.75 \text{ mA}$$

5.14

Then,

$$\begin{aligned} V_D &= V_{DD} - I_D R_D \\ &= 15 - 5.75 \times 10^{-3} \times 500 \\ &= 12.125 \text{ V} \end{aligned}$$

$$\therefore V_D = 12.125 \text{ V}$$

$$\begin{aligned} V_S &= I_D R_S \\ &= 5.75 \times 10^{-3} \times 10^3 \\ &= 5.75 \text{ V} \end{aligned}$$

$$\therefore V_S = 5.75 \text{ V}$$

$$\begin{aligned} V_{DS} &= V_{DD} - I_D (R_D + R_S) \\ &= 15 - 5.75 \times 10^{-3} (500 + 10^3) \\ &= 15 - 8.625 \end{aligned}$$

$$\therefore V_{DS} = 6.375 \text{ V}$$

Q28. An N-channel JFET has a Pinch-off voltage of -4.5 V and $I_{DSS} = 9 \text{ mA}$. At what value of V as will I_{DS} equal to 3 mA ? What is its g_m at this I_{DS} ?

Ans:

July-12, Q13(b)

Given that,

For an N-channel JFET,

$$V_p = -4.5 \text{ V}$$

$$I_{DSS} = 9 \text{ mA}$$

$$I_{DS} = 3 \text{ mA}$$

$$V = V_{GS} = ?$$

$$\text{Since, } I_{DS} = I_{DSS} \left[1 - \frac{V_{GS}}{V_p} \right]^2$$

$$3 \times 10^{-3} = 9 \times 10^{-3} \left[1 - \frac{V_{GS}}{(-4.5)} \right]^2$$

$$\frac{3}{9} = \left[1 + \frac{V_{GS}}{4.5} \right]^2$$

$$\therefore V_{GS} = -1.9 \text{ V}$$

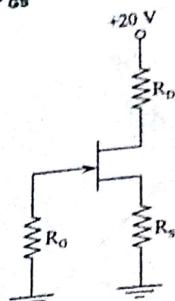
$$\text{Since, } g_m = \frac{2\sqrt{I_{DS} I_{DSS}}}{V_p}$$

$$= \frac{\left| 2\sqrt{3 \times 10^{-3} \times 9 \times 10^{-3}} \right|}{-4.5}$$

$$\therefore g_m = 2.3 \text{ S}$$

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Q29. For the FET self biased circuit shown (figure), calculate the values of R_D and R_S to obtain the bias condition. The maximum drain current is 10 mA and $V_{GS} = -2.2 \text{ V}$ at $I_D = 5 \text{ mA}$.



Figure

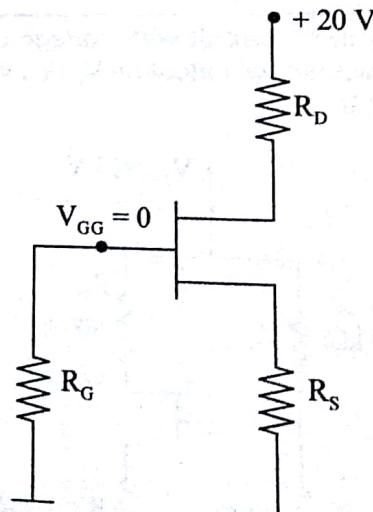
Ans:

Given that,

For a FET self biased circuit,

Maximum drain current, $I_{DSS} = 10 \text{ mA}$ Gate to source voltage, $V_{GS} = -2.2 \text{ V}$ Drain current, $I_D = 5 \text{ mA}$ Drain resistance, $R_D = ?$ Source resistance, $R_S = ?$

The given FET self biased circuit is shown in figure below:



Figure

The gate to source voltage is given by,

$$\begin{aligned} V_{GS} &= V_{GG} - I_D R_S \quad [\because V_{GG} = 0 \text{ V}] \\ \Rightarrow V_{GS} &= -I_D R_S \\ \Rightarrow R_S &= \frac{-V_{GS}}{I_D} = \frac{2.2}{5 \times 10^{-3}} = 440 \Omega \end{aligned}$$

$$\therefore R_S = 440 \Omega$$

The drain to source voltage is given by,

$$V_{DS} = V_{DD} - I_D (R_D + R_s)$$

Since,

$$V_{DD} = 20 \text{ V} \quad (\text{From figure})$$

$$V_{DS} = \frac{V_{DD}}{2} = \frac{20}{2} = 10 \text{ V}$$

Then,

$$\begin{aligned} 10 &= 20 - 5 \times 10^{-3} (R_D + R_s) \\ \Rightarrow 5 \times 10^{-3} (R_D + R_s) &= 10 \\ \Rightarrow R_D + R_s &= 2000 \\ \Rightarrow R_D &= 2000 - 440 = 1560 \Omega = 1.56 \text{ k}\Omega \\ \therefore R_D &= 1.56 \text{ k}\Omega \end{aligned}$$

5.3 ANALYSIS OF CS, CD AND CG AMPLIFIERS AND THEIR COMPARISON

Q30. With a neat schematic, explain how amplification takes place in a common drain amplifier.

Ans:

Common Drain Amplifier

The common drain amplifier is also known as source follower. The circuit diagram of this amplifier and its small signal equivalent model are as shown in figures (1) and (2) respectively.

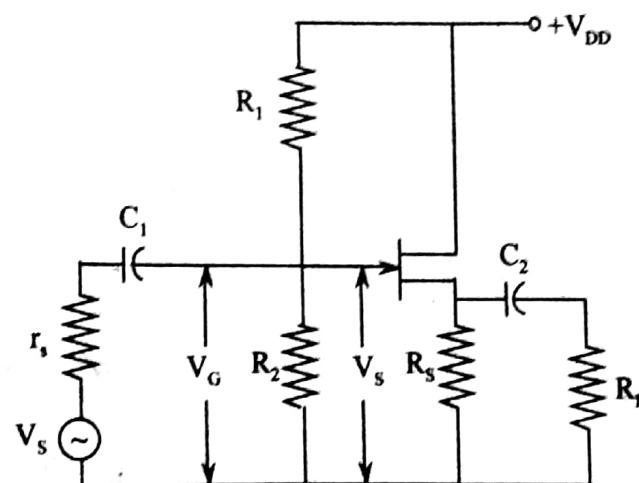


Figure (1): Circuit Diagram of Common Drain Amplifier

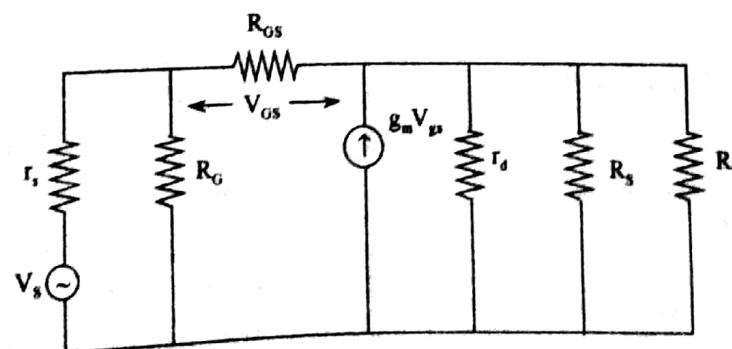


Figure (2): Small Signal Equivalent Model of Common Drain Amplifier

Here the resistors R_1 and R_2 behave as potential divider, R_L is the load resistor coupled to source terminal through the capacitor C_2 and the input is applied at the gate terminal via capacitor ' C_1 '.

5.16

Functioning

For the common drain circuit output voltage is developed across source resistance. The source voltage ' V_s ' is,

$$V_s = V_o - V_{os}$$

The gate bias voltage ' V_g ' derived from V_{DD} through potential divider R_1 and R_2 is a constant quantity. We assume that V_{os} is also constant to a large extent. When input signal is applied to the gate terminal via C_1 , the gate voltage ' V_g ' increases and decreases in accordance with increase and decrease in the input signal.

Since, $V_s = V_o - V_{os}$ the output voltage ' V_o ' also increases and decreases in accordance with input voltage ' V_i '. The gain of common drain circuit is unity.

Q31. With the help of a neat schematic, explain the functioning of a common source amplifier.

Ans:

Model Paper-II, Q17(a)

Common source amplifier is the most frequently encountered configuration of JFET. As the name indicates common source, the source of this amplifier is made common to both the input and output. The input is applied between the terminals of gate and source and the output is collected at drain and gate of JFET amplifier.

Figure (1) depicts the schematic of common source JFET amplifier. The resistor R_s and the capacitor C_s protects the JFET by providing temperature stabilization and the capacitor C_2 is a bypass capacitor, which avoids A.C degeneration by bypassing all A.C signals.

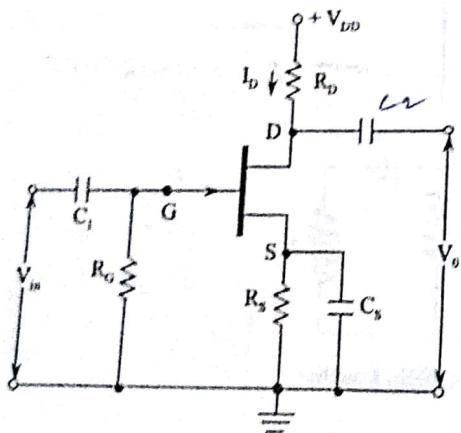


Figure (1): Common Source Amplifier

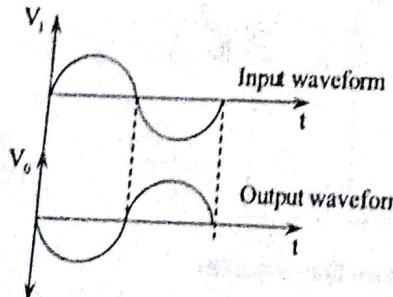


Figure (2)

Functioning

Figure (2) shows the input and output waveform of common source amplifier.

When the input is applied between the gate and source terminals of FET, it makes the gate to source voltage V_{gs} swing about its operating point and this makes the drain current to swing. As the drain current varies, it reflects on R_D i.e., when drain current increases, R_D also increases and vice versa.

Q32. With the help of a neat schematic, explain the functioning of a common gate amplifier.

Ans:

Common gate amplifier is the often used configuration of JFET. As the name indicates common gate, the gate of this amplifier is made common to both the input and output. The input is applied between the terminals of gate and source and the output is collected at drain and gate of JFET amplifier.

The figure (1) depicts the schematic of common gate JFET amplifier. The resistor R_s protects the JFET by providing temperature stabilization and the capacitor C_2 is a bypass capacitor, which avoids A.C degeneration by bypassing all A.C signals.

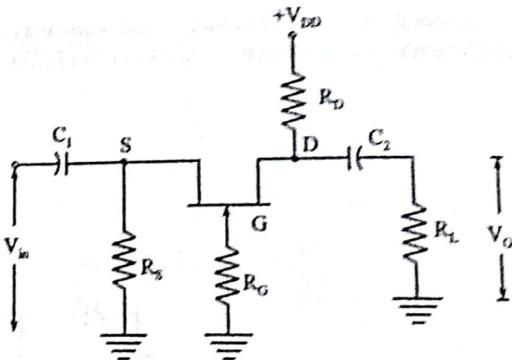


Figure (1): Common Gate Amplifier

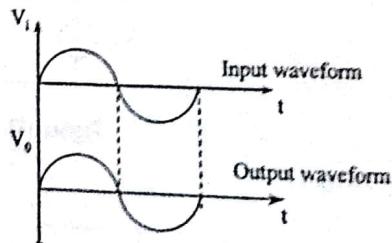


Figure (2)

Functioning

Figure (2) shows the input and output waveform of common gate amplifier.

When the input is applied between the gate and source terminals of FET, it makes the gate to source voltage V_{gs} swing about its operating point and this makes the drain current to swing. As the drain current varies, it reflects on R_D i.e., when drain current increases, R_D also increases and vice versa.

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Ans:

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UNIT-5

Q33. Compare CS, CD and CG JFET amplifiers.

Ans:

The comparison between CS, CD and CG JFET amplifiers is mentioned below:

Parameter	CS Amplifier	CD Amplifier	CG Amplifier
Definition	Source terminal is common to both drain and gate.	Drain terminal is common to both source and gate.	Gate terminal is common to both source and drain.
Circuit diagram			
Phase shift	180°	0°	0°
Voltage gain	$A_v = \frac{g_m r_D R_L}{r_s + R_L}$	$A_v = \frac{g_m R_D R_L}{(r_D + R_L) + g_m R_D R_L}$	$A_v = \frac{g_m r_D R_L}{r_D + R_L}$
Distortion	Occurs for large input	Is less due to bypass capacitor	Occurs for large input.
Input	(a) At low frequency $Z_i = \frac{R_G R_{GS}}{R_G + R_{GS}}$ (b) At high frequency	$Z_i = \frac{R_D R_{GS}}{R_D + R_{GS}}$	$Z_i = \frac{1}{g_m}$
Impedance (Z_i)	$\approx P_G$ (a) At low frequency, $Z_i = \frac{r_D R_L}{r_D + R_L}$ $\approx R_D$	$\approx P_G$ $Z_o = \frac{R_D}{1 + g_m R_L}$ $\approx \frac{1}{g_m R_L}$	$\approx \frac{1}{P_{GS}}$ $Z_o = \frac{r_D R_L}{r_D + R_L}$ $\approx R_D$
Output			
Impedance (Z_o)			

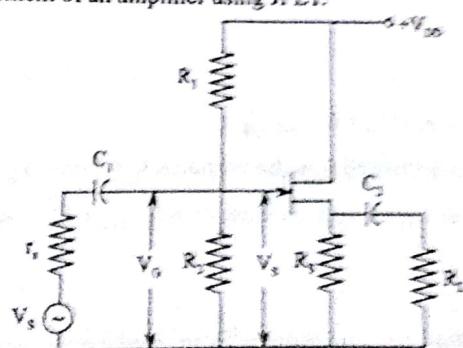
5.4 FET AS AN AMPLIFIER AND AS A SWITCH

Q34. Explain how JFET acts as an amplifier.

Ans:

JFET as an Amplifier

Figure shows the circuit arrangement of an amplifier using JFET.



Figure

Here the resistors R_s and R_L behave as potential divider, R_s is the load resistor coupled to source terminal through the capacitor C_1 and the input is applied at the gate terminal via capacitor ' C_1 '.

Functioning

For the JFET amplifiers circuit output voltage is developed across source resistance. The source voltage ' V_s ' is,

$$V_s = V_G - V_{GS}$$

The gate bias voltage V_g derived from V_{in} through potential divider R_1 and R_2 , is a constant quantity. We assume that V_g is also constant to a large extent. When input signal is applied to the gate terminal via C_1 , the gate voltage ' V_g ' increases and decreases in accordance with increase and decrease in the input signal.

Since, $V_g = V_o - V_{os}$, the output voltage ' V_o ' also increases and decreases in accordance with input voltage ' V_i '. From the above analysis, we can say that JFET acts as an amplifier.

Q35. Explain how a FET can be made to act as a switch.

Ans:

Model Paper-II, Q17(b)

Introduction

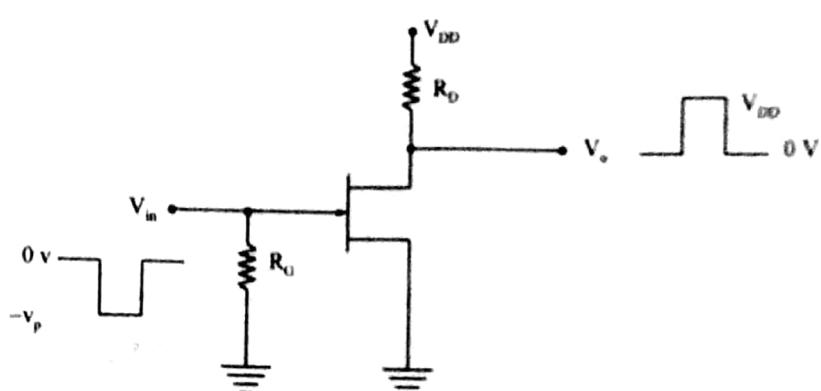
When JFET is reverse biased, the depletion region exists between the p and n regions. As we increase the reverse voltage further and further a stage comes where the depletion region equals the actual channel without leaving space to the conduction region. Hence, no current flow takes place from drain to source. Here, the gate to source voltage produces some cut-off voltage denoted by $V_{GS(OFF)}$.

JFET as a Switch

The characteristics of JFET switch that makes it distinct from BJT switch are,

1. High input impedance
2. Generates a positive output pulse for a negative input rectangular pulse.

Figure shows the circuit arrangement of a switch using JFET.



Figure

When $V_{in} = 0$, the current flowing through JFET reaches its peak value and the output is obtained by using following expression as,

$$V_o = V_{DD} - I_{DSS} R_D$$

Where,

I_{DSS} – Saturation drain current when $V_{GS} = 0$.

In the above expression, the proper selection of R_D value produces $V_o = 0$ with $V_{in} = 0$.

Now, let us consider that ' $-V_p$ ' is much higher negative value than $V_{GS(OFF)}$ (JFET rating). When $V_{in} = -V_p$, the drain current reduces to zero. Thus,

$$V_{out} = V_{DD}$$

From the above analysis, it is clear that the input pulse in figure produces the output pulse. In this way, JFET functions as a switch.

JFET	MOSFET
1. High input impedance.	1. Very high input impedance.
2. It can be operated only in depletion mode.	2. It can be operated in both depletion mode and enhancement mode.
3. A small gate current exists (due to reverse bias).	3. Gate current is zero.
4. High drain resistance.	4. Low drain resistance.
5. Conductivity is controlled by the reverse biasing of the gate.	5. Conductivity is controlled by the carriers induced in the channel.
6. Channel already exists. So, called normally ON device.	6. Initially, channel doesn't exist. So, called normally OFF device.

Table

Q37. What is MOSFET? What are the different types of MOSFETs? Give their symbols.

Ans:

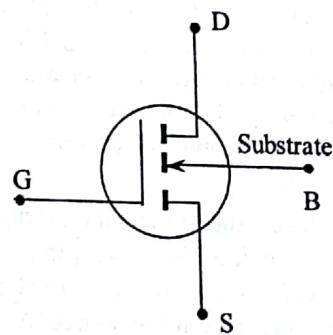
MOSFET

MOSFET is abbreviated as Metal Oxide Semiconductor Field Effect Transistor. It is a three terminal device wherein the applied gate voltage controls the drain current.

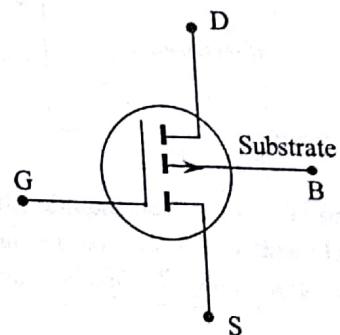
There are two types of MOSFETs,

- (a) Enhancement MOSFETs
- (b) Depletion MOSFETs.

The circuit symbols of P-channel and N-channel enhancement type MOSFETs are shown in figure (1).



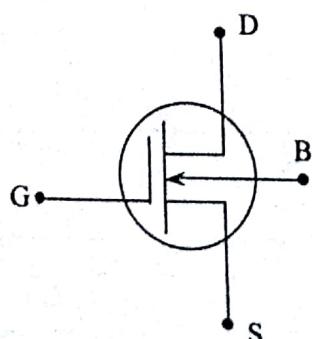
(a): N-channel Enhancement MOSFET



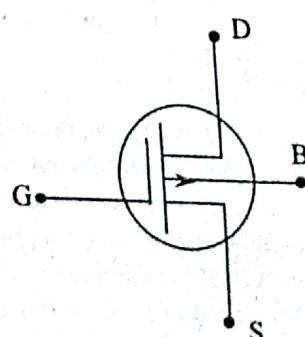
(b): P-channel Enhancement MOSFET

Figure (1)

The circuit symbols of P-channel and N-channel depletion type MOSFETs are shown in figure (2).



(a): N-channel Depletion MOSFET



(b): P-channel (Depletion MOSFET)

Figure (2)