

4.2

7.1 INTRODUCTION TO OP-AMP

Operational amplifier is a two input voltage controlled by voltage source whose output voltage is proportional to the difference between the two input voltage. Operational amplifier is most commonly referred as "Op-Amp". It is basically a direct coupled high gain amplifier usually consisting of one or more differential amplifiers followed by a level translator and an output stage.

Operational amplifiers were originally used in analog computers to perform mathematical operations such as addition, subtraction, integration, differentiation etc. That is why it is termed as operational amplifier. Op-Amp can also be used in a variety of other applications such as active filters, oscillators, comparators, regulators etc. A negative voltage shunt feedback is normally employed to the amplifier to control the overall characteristics of the op-amp.

The first IC Op amp commercially available was μ A 702 produced by Fair child semiconductor in the year 1963. Then it led to the development of μ A 709 by the same manufacturer in the year 1965. But the first internally compensated Op amp was introduced by Fair child in 1968 with μ A 741.

7.2 OP-AMP BASICS

7.2.1 Circuit Symbol

The circuit symbol for an operational amplifier is shown in Fig. 7.2.1,

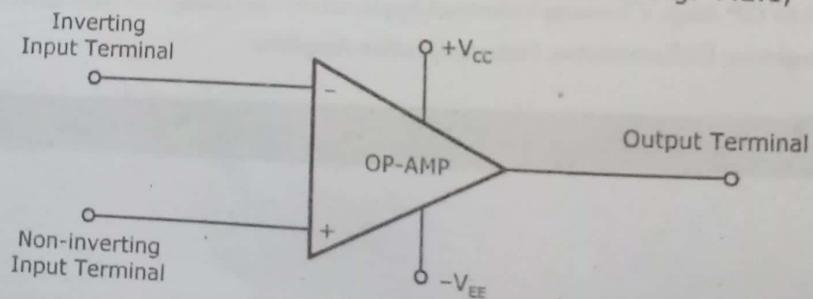


Fig. 7.2.1 Circuit Symbol of Operational Amplifier

The Op-Amp symbol shown in Fig. 7.2.1 has the following terminals,

- (1) **Two Supply Terminals** : A positive supply voltage $+V_{CC}$ and a negative supply voltage $-V_{EE}$. Typical supply voltage for Op-Amp usually ranges from ± 5 V to ± 22 V.
- (2) **Two Input Terminals** : An inverting input terminal indicated by -ve sign and non-inverting input terminal indicated by +ve sign. Any input signal fed to the inverting input terminal produces an inverted output and any input signal fed to the non-inverting input terminal produces a non-inverted output.
- (3) **One Output Terminal**

7.2.2 Equivalent Circuit of a Practical Op-Amp

Fig. 7.2.2 depicts the equivalent circuit of an Op-Amp,

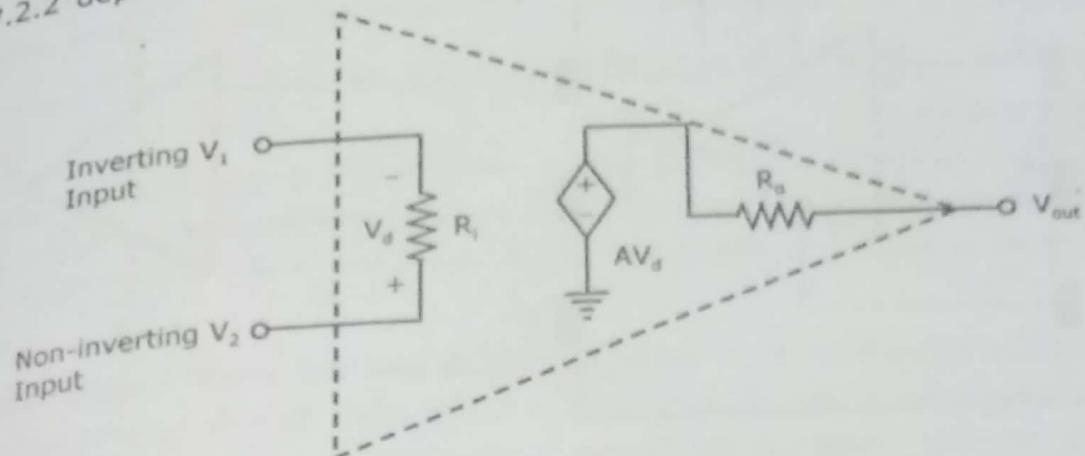


Fig. 7.2.2 Equivalent Circuit of Op-Amp

The output section consists of a voltage controlled source in series with the output resistance R_o .

It is evident from Fig. 7.2.2, that the input resistance R_i is the Thevenin equivalent resistance seen at the input terminal. The differential input voltage V_d is given by,

$$V_d = V_2 - V_1$$

Where,

V_1 = Voltage between the inverting terminal and ground.

V_2 = Voltage between the non-inverting terminal and ground.

The output voltage is,

$$V_{out} = AV_d$$

$$V_{out} = A(V_2 - V_1)$$

Where A is called the open-loop voltage gain (It is also represented as A_{OL}) because it is the gain of the Op-Amp without any feedback from output to input.

7.2.3 Pin Configuration of an Op-Amp

The pin configuration and schematic symbol for Op-Amp IC 741 is given in 7.2.3(a) and Fig. 7.2.3(b),

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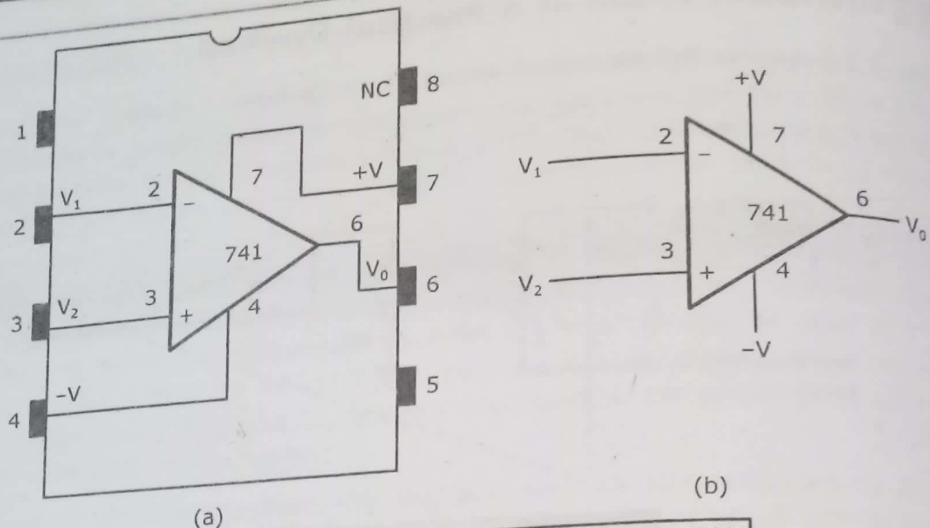


Fig. 7.2.3 Pin Configuration of Op-Amp 741

First, the pins labeled +V (pin 7) and -V (pin 4) represent the power supply connections. The voltages applied to these pins will usually be +15V and -15V, or +12V and -12V. The inverting input is marked with -ve sign (pin 2). The non-inverting input is marked with a +ve sign (pin 3). The output is labeled as V_0 (pin 6). Pin 8 is not used and marked NC, which means 'no-connection'. The remaining two pins (pins 1 and 5) are called 'Off-set Null' terminals. All input and output voltages are measured with respect to the ground (common).

7.2.4 Block Diagram of Op-Amp

Operational amplifier is basically a directed coupled high gain amplifier usually consisting of one or more differential amplifiers followed by a level translator (shifted) and an output stage. Block diagram of an Op-amp is shown in Fig. 7.2.4,

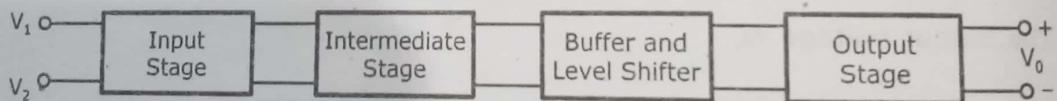


Fig. 7.2.4 Functional Block Diagram of OP-AMP IC

Each block is explained as follows,

- (1) **Input Stage :** Design of input stage is very crucial in determining overall OP-AMP characteristics. Some of the essential requirements are,
 - (i) **It must Provide very High Input Impedance :** To prevent loading of the input ideally it must be infinite.
 - (ii) **It must have Differential (Two) Inputs :** Any common mode signal such as noise signals are eliminated by using differential inputs.

- (iii) **It must have High CMRR(ρ)** : High CMRR eliminates all the noise voltage.
- (iv) **D.C (Direct Coupled) Input Terminals** : It will increase bandwidth so that OP-AMP can be used for very low frequency (D.C) and high frequency signals.
- (v) **Low Input Impedance** : This will prevent loading of intermediate stage used for further amplifications.

All above requirements are satisfied by the Difference Amplifier (D.A). Difference Amp also gives low input offset voltages and bias currents which causes output offset voltage. Usually DIFF - AMP with dual-input and balanced output is used as a input stage.

- (2) **Intermediate Stage** : This is also known as Gain stage. This will provide additional voltage gain to achieve large overall gain. Since it is difficult to get a large gain using single stage amplifiers, so cascaded (multistage) amplifiers are used. Usually there will be one or two intermediate stages. For intermediate stage, DIFF-AMP with unbalanced output is used.
- (3) **Buffers and Level Shifter** : Buffer is usually emitter follower with high input impedance, low output impedance and unity gain that will prevent loading when it is connected between intermediate stage and output stage. As intermediate stage is an unbalanced output DIFF-AMP, there is D.C voltage in addition to the A.C voltage at its output. As final (output) stage is push-pull amplifier this D.C. voltage can drive maximum output voltage swing without distortions. Hence level shifting (level shifter) are used to bring the D.C output voltage to zero (ground) voltage when no signal (quiescent condition) at the input is applied. Level shifter network are basically clamps (D.C restorer) circuits.

- (4) **Output Stage** : Requirements of an output stage are,

- (i) Output impedance must be low.
- (ii) Output D.C voltage swing must be large.
- (iii) High current sourcing and sinking capability.
- (iv) Low stand by (quiescent) power dissipation.

Push-pull amplifier will meet all the above requirements. These amplifiers are usually operated in class AB mode to prevent cross-over distortions.

7.2.5 Ideal Op-Amp

Fig. 7.2.5(a) shows an ideal Op-Amp symbol. It is having two input terminals V_1 and V_2 two supply voltages $+V_{cc}$ (or) V^+ and $-V_{ee}$ (or) V^- and one output V_o .

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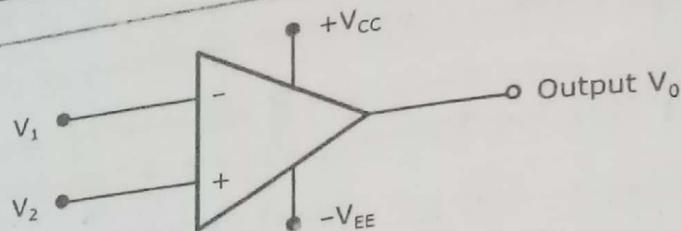


Fig. 7.2.5(a) Ideal Op-Amp

An amplifier with infinite open loop gain, infinite input resistance and zero output resistance is called an ideal op-amp. If an op-amp is ideal, it is having the following characteristics,

- (1) Infinite voltage gain.
- (2) Infinite input impedance.
- (3) Zero output impedance.
- (4) Infinite open loop bandwidth.
- (5) Zero input offset voltage and current.

Fig. 7.2.5(b) shows an equivalent circuit of Ideal op-amp,

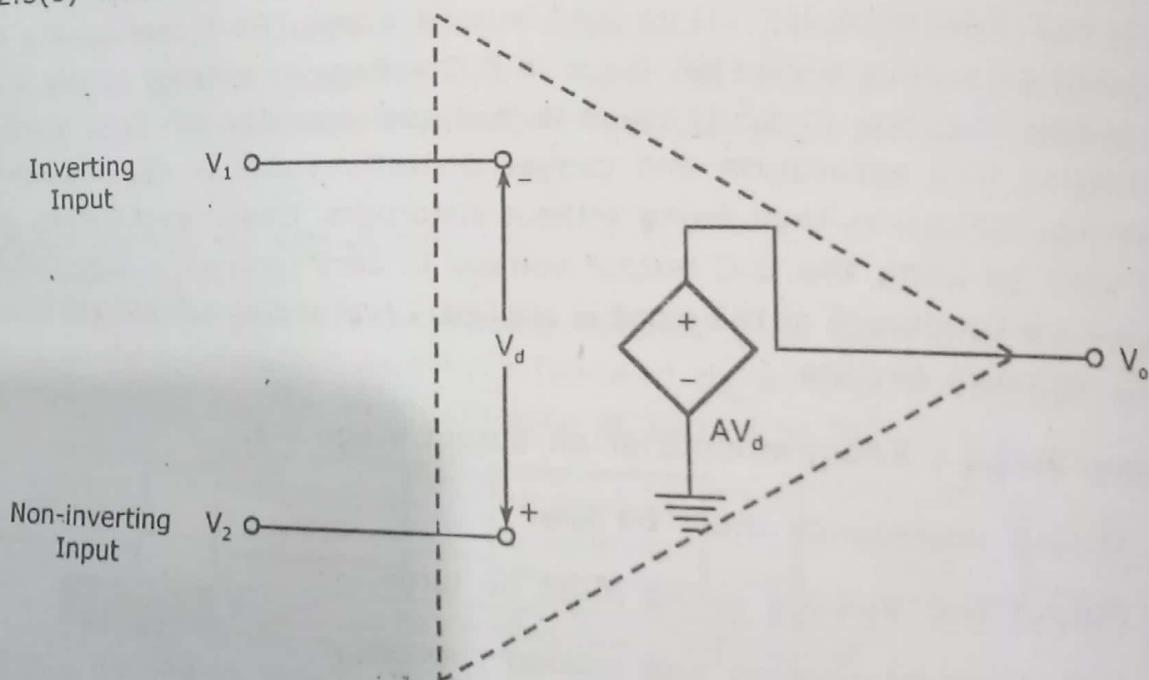


Fig. 7.2.5(b) Equivalent Circuit of Ideal Op-amp

CONCEPT OF VIRTUAL GROUND

Consider an ideal op-amp with infinite gain. Let the input voltage be V_i and the output voltage V_o , as shown in Fig. 7.2.5(b). We know that the gain of an op-amp is given by,

$$A = \frac{V_o}{V_i}$$

Since $A = \infty$ for the ideal op-amp, we find that,

$$V_i = \frac{V_o}{\infty} = 0$$

This result indicates that the input voltage is zero. A voltage can be zero only under a short-circuit condition. However, in the case of op-amps, there exists no real short circuit across input terminals. Therefore, we conclude that the input terminals of the op-amp are virtually shorted together. In turn, we state that there exists a virtual short circuit across the input terminals of an op-amp. If one of the input terminals is grounded, the virtual short becomes a virtual ground.

Fig. 7.2.6 shows virtual short circuit across input terminals.

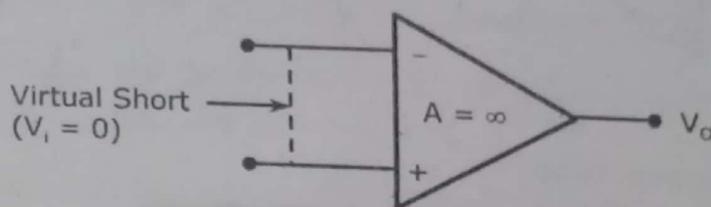


Fig. 7.2.6 Virtual Short-Circuit Across Input Terminals

7.3 CHARACTERISTICS OF OP-AMPS

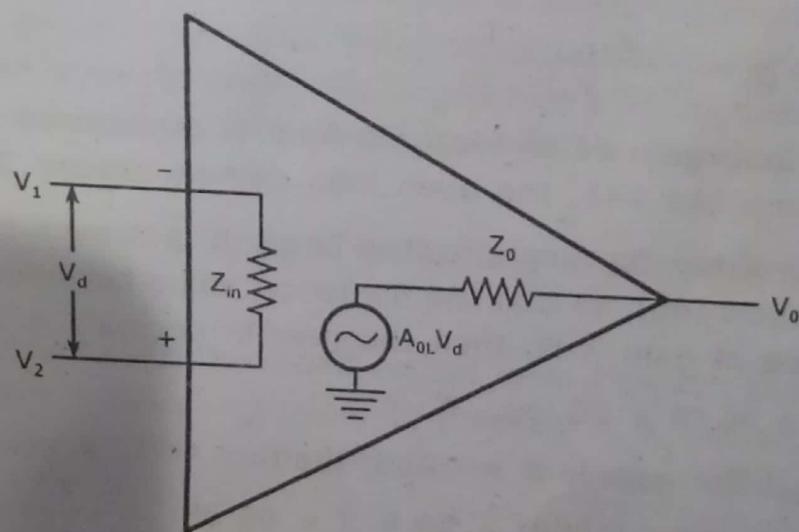


Fig. 7.3.1 Equivalent Circuit of Practical Op-Amp

Considering the equivalent circuit of an Op-Amp shown in Fig. 7.3.1. We can discuss the following important characteristics of an Op-Amp,

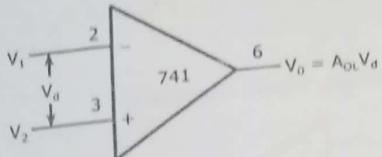
- (1) **Open Loop Gain - A_{OL}** : Let V_1 be the input voltage applied to the inverting terminal and V_2 be the input voltage applied to the non-inverting terminal.

The difference between these two voltages is called as differential voltage, V_d . i.e.,

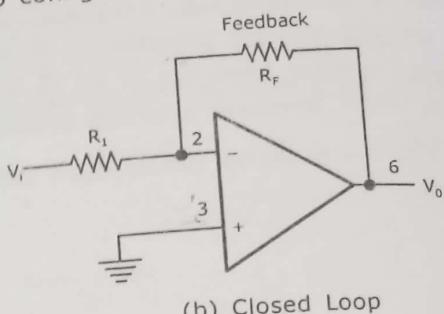
$$(V_1 - V_2) = V_d$$

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When there is no feedback connection between the output to one of the input terminals, the Op-Amp is said to be in open loop condition. Usually most of the Op-Amp circuits employ a negative feedback from the output to the inverting input. Then the Op-Amp is said to be in closed loop condition. The open loop and a sample circuit for closed loop arrangement is shown in Fig. 7.3.2(a) and Fig. 7.3.2(b). (Most of the circuits used with Op-Amp are of closed loop configuration).



(a) Open Loop



(b) Closed Loop

Fig. 7.3.2

The open loop voltage gain of the Op-Amp is represented as A_{OL} and is defined as the ratio of the output voltage to the differential input voltage.

$$\text{i.e., } A_{OL} = \frac{V_o}{(V_1 - V_2)} = \frac{V_o}{V_d}$$

The open loop gain of an ideal Op-Amp is considered as infinity. However, for practical Op-Amp like 741, the open loop gain is around 200,000.

When gain of the Op-Amp circuit is large, it is convenient to represent the gain in units of decibels (dB), so that the numerical value becomes smaller. If the absolute numerical value of gain is N , then the gain in decibels is given by,

$$A \text{ in dB} = 20 \log_{10} N$$

For example, if the gain is $N = 1000$, then

$$\text{Gain in dB} = 20 \log_{10} (1000) = 20 \times 3 = 60 \text{ dB.}$$

$$\text{If } N = 2000, \text{ then the gain is } 20 \log_{10} (2000) = 20 (3.3010) = 66.02 \text{ dB}$$

$$\text{If the gain is unity, then the gain in dB is } 20 \log_{10} 1 = 0 \text{ dB.}$$

- (2) **Input Impedance - Z_{in}** : The input impedance of the Op-Amp is the equivalent resistance that is measured at the inverting input or non inverting input with respect to ground.

The input impedance can also be defined as the ratio of the change in input voltage to the change in input current measured at either of the input terminals with respect to ground. The input impedance of an ideal Op-Amp is considered as infinity. However, for practical Op-Amp like LM741, the typical value of input impedance is 2,000,000 ohms ($2M\Omega$).

(3) **Output Impedance - Z_o** : The output impedance of the Op-Amp is the equivalent resistance that is measured at the output terminal with respect to ground.

The output impedance can also be defined as the ratio of the change in output voltage to the change in output current. The output impedance of an ideal Op-Amp is considered to be zero. However, for practical Op-Amp like LM741, the output impedance is 75 ohms.

(4) **Unit-gain Bandwidth (GB)** : Bandwidth of an Op-Amp is the range of frequencies where the gain does not fall below 0.707 times the maximum constant value. For an ideal operational amplifier bandwidth is predicted as infinity. Under open loop condition, the Op-Amp has a poor frequency response, having a bandwidth of only 10 Hz. Therefore, the frequency response of an Op-Amp is measured under closed loop condition where the gain of the amplifier is somewhat low.

Unit gain bandwidth is the bandwidth of the amplifier when the gain is unity (0 dB). For Op-Amp LM741 this value is 1 MHz.

The product of gain and bandwidth is usually referred as Gain Bandwidth (GB) product. When it is calculated for unit gain, then the quantity is called as Unit Gain Bandwidth (UGB).

(5) **Input Offset Voltage - V_{io}** : For an ideal Op-Amp when the inverting input and non inverting input are grounded or supplied with equal voltages, we may expect the output voltage to be equal to zero. But in practice a small difference in voltage is required to make the output zero. This voltage which is required to make the output zero is called input offset voltage.

For an ideal Op-Amp the input offset voltage is zero. For LM741 this value is $\pm 15\text{mV}$.

When the two inputs are grounded for an ideal Op-Amp the output voltage is zero. This is a perfect balance condition. In practice, it is not achieved and a small offset voltage is present. This voltage is called as output offset voltage.

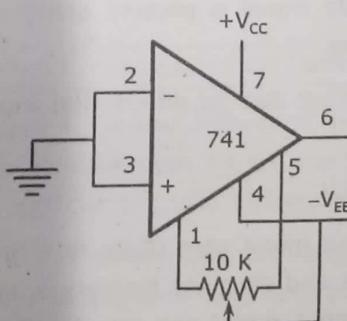


Fig. 7.3.3 Arrangement of Offset Null

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For Op-Amp 741 pins 1 and 5 can be used to make the output offset voltage zero. Therefore, these two terminals are called as offset null terminals. The arrangement for offset null is shown in Fig. 7.3.3. The two ends of 10K potentiometer are connected to pins 1 and 5 and the centre-tap is connected to $-V_{EE}$ (-15V or -12V). The 10 K pot is adjusted to make the output voltage zero when the input terminals are grounded.

- (6) **Slew Rate :** Slew rate (S_R) of an Op-Amp is defined as the maximum rate of change of its output voltage with respect to time. In mathematical form,

$$\text{Slew rate } (S_R) = \left[\frac{dV_o}{dt} \right]_{\max}$$

Slew rate is expressed in V/ μ s. For an ideal Op-Amp, the slew rate is infinity. For practical Op-Amp like LM741, the slew rate is 0.5 V/ μ s.

- (7) **Common Mode Rejection Ratio (CMRR) :** We have seen that when a differential input V_d is present, the open loop gain is given by,

$$A_{OL} = \frac{V_o}{(V_1 - V_2)} = \frac{V_o}{V_d}$$

This quantity is also called as differential gain, A_d under open loop condition.

In practice, besides the input signals V_1 and V_2 , additional noise signals present in the atmosphere also affect the potential present at the input terminals. These noise signals affect both inverting and non-inverting signals equally and unwanted error voltage is produced at the output. A good Op-Amp must reject these unwanted common signals as much as possible. To calculate the output due to common mode signals, the value of common mode input is required. The common mode input V_c is defined as,

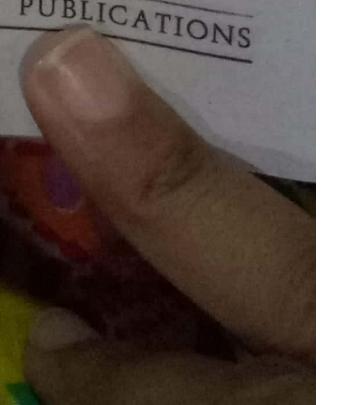
$$V_c = \frac{(V_1 + V_2)}{2}$$

When the common mode signal is present along with the differential input, the resultant output is given as,

Resultant output = Output due to differential input + Output due to common mode signal

$$V_o = A_d V_d + A_c V_c$$

Where A_c is the common mode gain (Gain due to common mode signals only). Naturally, A_d must be large and A_c must be very small. The ability of the Op-Amp to amplify the differential input signal and reject common mode signal is measured by a quantity called Common Mode Rejection Ratio, CMRR.



CMRR is defined as the ratio of the differential gain to the common mode gain.

$$\text{CMRR} = \left| \frac{A_d}{A_c} \right|$$

Now we can write the output equation as,

$$V_o = A_d V_d + A_c V_c$$

$$= A_d V_d \left\{ 1 + \frac{A_c V_c}{A_d V_d} \right\}$$

$$= A_d V_d \left\{ 1 + \frac{1}{\text{CMRR}} \frac{V_c}{V_d} \right\}$$

For an ideal Op-Amp, CMRR is infinity. But for practical Op-Amp like LM741, the CMRR is around 95 dB. We can go in the reverse and calculate the numerical value of the CMRR. Let the numerical value be N. Then,

$$95 \text{ dB} = 20 \log_{10} N$$

$$\log_{10} N = \frac{95}{20} = 4.75$$

$$N = \text{antilog } (4.75) = 10^{4.75} = 56230$$

- (8) **Input Offset Current :** Fig. 7.3.4 shows determination of input offset current of Op-Amp,

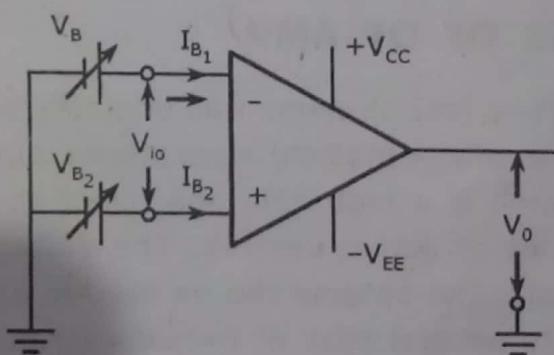


Fig. 7.3.4 Determination of Input Offset Current by Adjusting I_{B1} and I_{B2}

The input offset current I_{io} is the difference between the two input currents of 20 nA. If input offset current more than 20 nA, the false output voltage is produced. The smaller the input offset current, the better is the op-amp's performance.

- (9) **Input Bias Current :** The IC 741 op-amp has an input bias current of 80 nA. The input bias current is the average of currents that flow into two inputs i.e., non-inverting and inverting terminals. Input bias current function is it affects all op-amp applying of Op-Amp.

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Table 7.3.1 summarizes the electrical characteristics.

Table 7.3.1 Electrical Characteristics of Op-Amp

| S.No. | Parameter | Ideal Op-Amp | Characteristics of Ideal and Practical Op-Amp |
|-------|------------------------------------|--------------|---|
| (1) | Open loop gain - A_{OL} | Infinity | 200,000 |
| (2) | Input impedance - Z_{in} | Infinity | $2M\Omega$ |
| (3) | Output impedance - Z_o | Zero | 75Ω |
| (4) | Input offset voltage - V_{io} | Zero | $\pm 15 \text{ mV}$ |
| (5) | Input offset current - I_{io} | Zero | 80 nA |
| (6) | Slew rate - SR | Infinity | $0.5 \text{ V}/\mu\text{s}$ |
| (7) | Common mode Rejection ratio - CMRR | Infinity | 95 dB (or) 56,230 |
| (8) | Bandwidth - BW | Infinity | 10 Hz only in open loop 1 MHz for unit gain. |

7.4 APPLICATIONS OF OP-AMP

The operational amplifiers (or) op-amps was originally developed for analog computer designers to perform the mathematical operations such as addition, subtraction multiplication etc. An op-amp is a high gain and direct coupled amplifiers. The op-amp designed with various types of active devices. The voltage gain can be controlled by various feedback components. The op-amp can be used in amplifiers and signal processing applications involving dc to several MHz of frequency ranges. In op-amp,

IC technology is successful for providing low cost high performance, versatile and building block of modern signal processing and conditioning circuits. If op-amp's are used for op-amps which are expensive, versatile and easy to use. Some of the applications are given as,

- (1) Inverting amplifier
- (2) Non-inverting amplifier
- (3) Summing amplifier
- (4) Difference amplifier
- (5) Differentiator
- (6) Integrator
- (7) Instrumentation amplifier

7.4.1 Inverting Amplifier

The inverting amplifier of op-amp is shown in Fig. 7.4.1,

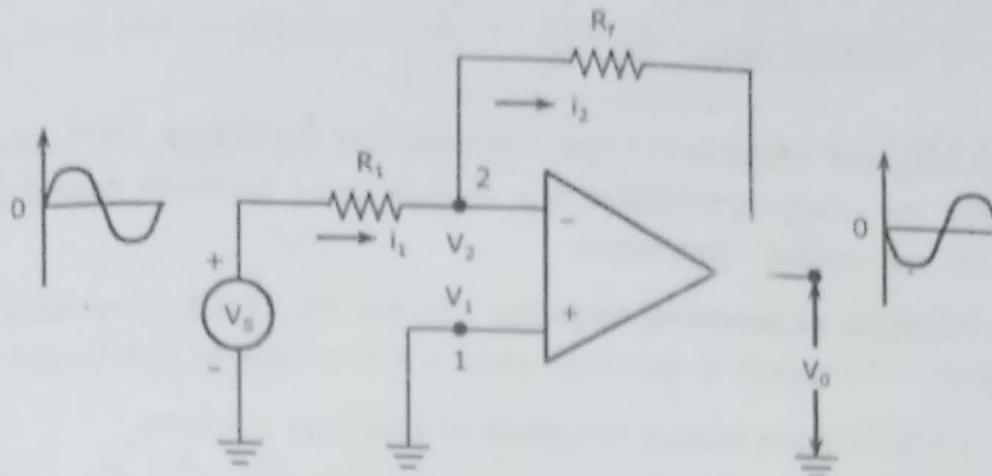


Fig. 7.4.1 Inverting Amplifier

In Fig. 7.4.1, the inverting terminal connected to voltage source 'V_s' and non-inverting terminal connected to ground. The terms R₁ and R_f are feedback elements. When a input voltage signal 'V_s' is applied to inverting-input terminal, an input current starts flowing into the op-amp. However, since the input impedance of the op-amp is infinity, so this I₁ current will not flow into the amplifier, rather it flows through the output loop (or) feedback (through R_f) to the output.

Let, the voltage gain $A_V = \frac{V_0}{V_s}$. Applying KCL at node 2,

$$\text{We get, } \frac{V_s - V_2}{R_1} = \frac{V_2 - V_0}{R_f} \quad \dots (7.4.1)$$

But voltage at node 2 (due to virtual ground) V₂ = 0. Substituting V₂ = 0 in Eq. (7.4.1),

$$\begin{aligned} \text{We obtain, } \frac{V_s - 0}{R_1} &= \frac{0 - V_0}{R_f} \\ \Rightarrow \frac{V_s}{R_1} &= \frac{-V_0}{R_f} \end{aligned} \quad \dots (7.4.2)$$

Thus, the voltage gain of inverting amplifier is given as,

$$A_V = \frac{V_0}{V_s} \quad \dots (7.4.3)$$

According to the Eq. (7.4.3), cross-multiplying the Eq. (7.4.2),

$$\text{We get, } V_s R_f = -V_0 R_1$$

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$$\frac{V_0}{V_S} = -\frac{R_f}{R_1}$$

 \Rightarrow

$$\text{Voltage gain } A_V = \frac{V_0}{V_S} = -\frac{R_f}{R_1}$$

... (7.4.4)

In Eq. (7.4.4), the negative (-) sign indicates that the output 180° out-of-phase with the input. Since the inverting amplifier is a voltage shunt feedback connection and it has very low input and output impedance.

Input-output Functions of Inverting Amplifier : In the Fig. 7.4.1, sine wave is applied to the input signal. This signal is inverted 180° out-of-phase at the output side.

Fig. 7.4.2 shows input-output functions of inverting amplifier,

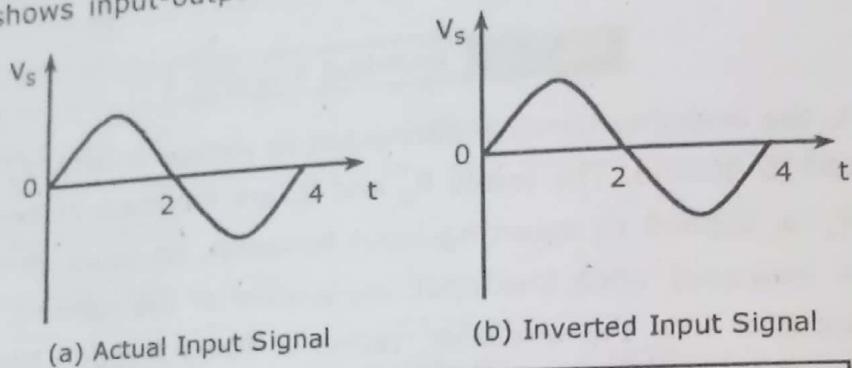


Fig. 7.4.2 Input-output functions of Inverting Amplifier

7.4.2 Non-Inverting Amplifier

Fig. 7.4.3 shows non-inverting amplifier of op-amp,

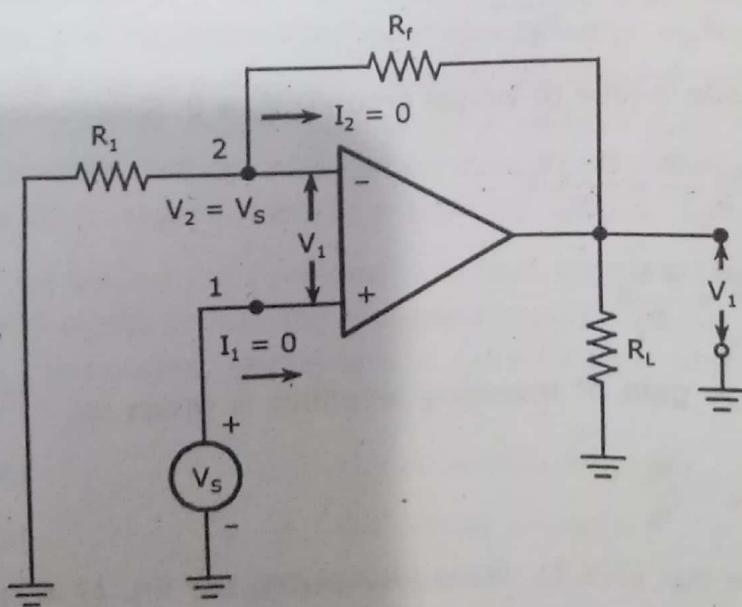


Fig. 7.4.3 Non-inverting Amplifier

In Fig. 7.4.3, the input signal ' V_s ' is applied at noninverting terminal and inverting terminal is grounded. Because of virtual ground concept, at node 2, voltage V_2 and input signal voltage V_s are equal, i.e., $V_2 = V_s$. When ' V_s ' is applied at noninverting terminal, the current I_1 flows into op-amp and current I_2 flows through feedback (or) output loop (R_f).

Applying voltage division rule at Fig. 7.4.3,

$$\text{We get, } V_2 = V_s = \frac{V_0 R_1}{R_1 + R_f}$$

$$\Rightarrow \frac{V_s}{V_0} = \frac{R_1}{R_1 + R_f}$$

$$\Rightarrow \frac{V_0}{V_s} = \frac{R_1 + R_f}{R_1}$$

$$\frac{V_0}{V_s} = 1 + \frac{R_f}{R_1}$$

$$\therefore \text{Voltage gain } A_V = \frac{V_0}{V_s} = 1 + \frac{R_f}{R_1} \quad \dots (7.4.5)$$

From Eq. (7.4.5), we observe that the output is in phase with the input. Since the non-inverted amplifier is the voltage series feedback connection, it has high input and low output impedances. It is also called as voltage follower (or) buffer because input is same as output is shown in Fig. 7.4.4,

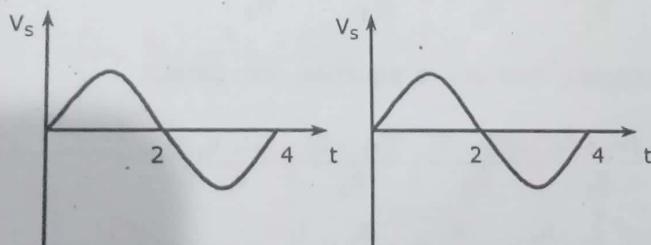


Fig. 7.4.4 | Input-output Combinations of Non-inverting Amplifier

7.4.3 Summer

Op-Amp can be used to perform the mathematical operation addition. The following sections explains how the inverting and non-inverting amplifier configurations of op-amps can be used as a summer.

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7.4.3.1 Inverting Summing Amplifier

Inverting type summing amplifier is shown in Fig. 7.4.5,

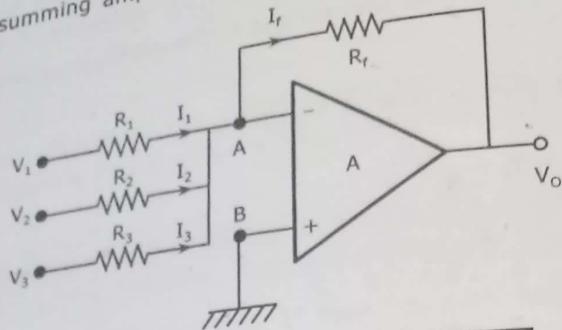


Fig. 7.4.5 Inverting Summing Amplifier

In this circuit all the input voltages to be added are applied to the inverting terminal of the op-amp.

In Fig. 7.4.5 as node B is grounded, due to virtual ground concept, the node A is also at virtual ground potential. Thus, $V_A = V_B = 0$.

Applying KCL at node A gives,

$$I_1 + I_2 + I_3 = I_f$$

$$\frac{V_1 - V_A}{R_1} + \frac{V_2 - V_A}{R_2} + \frac{V_3 - V_A}{R_3} = \frac{V_A - V_0}{R_f}$$

$V_A = 0$. Substituting this above equation, we obtain,

$$\frac{(V_1 - 0)}{R_1} + \frac{(V_2 - 0)}{R_2} + \frac{(V_3 - 0)}{R_3} = \frac{0 - V_0}{R_f}$$

$$\therefore V_0 = -\left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right] \quad \dots (7.4.6)$$

If $R_f = R_1 = R_2 = R_3$, then output will be,

$$V_0 = -[V_1 + V_2 + V_3] \quad \dots (7.4.7)$$

Since the output will be negative of the sum of the inputs so it is called inverting summer.

7.4.2 Non-Inverting Summing Amplifier

Non-inverting summing amplifier circuit is shown in Fig. 7.4.6,

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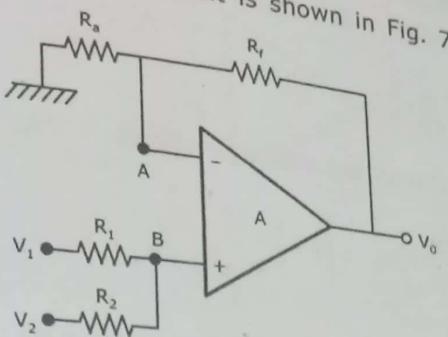


Fig. 7.4.6 Non-inverting Summer

In this circuit all the input voltages to be added are applied to the non-inverting terminals of an op-amp.

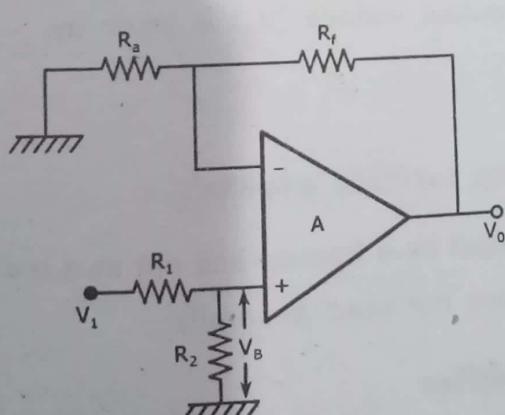
To obtain an expression for output voltage, make use of superposition theorem.

- (1) Consider V_1 only make $V_2 = 0$: The circuit will be as shown in Fig. 7.4.7(a). This is an non inverting amplifier. From Fig. 7.4.7(a), we have,

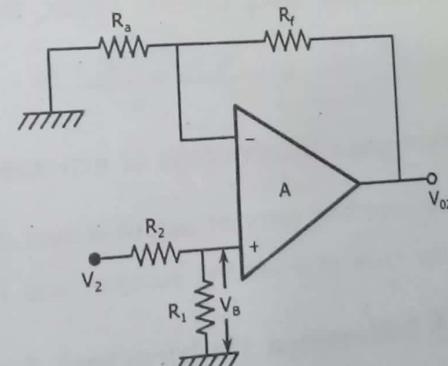
$$V_B = \frac{R_2}{R_1 + R_2} V_1$$

Output voltage for non-inverting amplifier is thus given by,

$$\begin{aligned} V_{01} &= \left(1 + \frac{R_f}{R_a}\right) V_B \\ &= \left(1 + \frac{R_f}{R_a}\right) \frac{R_2}{R_1 + R_2} \cdot V_1 \end{aligned}$$



(a) When $V_2 = 0$



(b) When $V_1 = 0$

Fig. 7.4.7 Equivalent Circuit of Fig. 7.4.6

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(2) Consider V_2 only and Make $V_1 = 0$: Circuit will be as shown in Fig. 7.4.7(b). Using voltage division rule voltage at node B is given by,

$$V_B = \left[\frac{R_1}{R_1 + R_2} \right] V_2$$

Output voltage for non-inverting amplifier shown in Fig. 7.4.7(b) is thus given by,

$$V_{02} = \left[1 + \frac{R_f}{R_a} \right] V_B = \left[1 + \frac{R_f}{R_a} \right] \left[\frac{R_1}{R_1 + R_2} \right] V_2$$

(3) By Superposition Theorem

We have,

$$\begin{aligned} V_0 &= V_{01} + V_{02} \\ V_0 &= \left(1 + \frac{R_f}{R_a} \right) \left[\frac{R_2}{R_1 + R_2} V_1 + \frac{R_1}{R_1 + R_2} V_2 \right] \end{aligned} \quad \dots (7.4.8)$$

If we make $R = R_1 = R_2$ then,

$$V_0 = \left(1 + \frac{R_f}{R_a} \right) \left(\frac{V_1 + V_2}{2} \right) \quad \dots (7.4.9)$$

This is the required output of a summing amplifier.

For $R_f = 0$ and $R = R_1 = R_2$ we have,

$$V_0 = \left(\frac{V_1 + V_2}{2} \right)$$

For the four input summer circuit, the output voltage (V_0) is given by,

$$V_0 = \frac{V_1 + V_2 + V_3 + V_4}{4} \quad \dots (7.4.10)$$

Disadvantages : Disadvantage of non-inverting summing amplifier.

Non-inverting summer output is sum of input by a fraction and not as a real summer as in the case of inverting summer and hence not used generally.

7.4.4 Difference (Subtractor) Amplifier

The difference (or) subtractor amplifier gives the output is proportional to difference between the two voltages V_1 and V_2 . Fig. 7.4.8 shows the difference amplifier of op-amp.

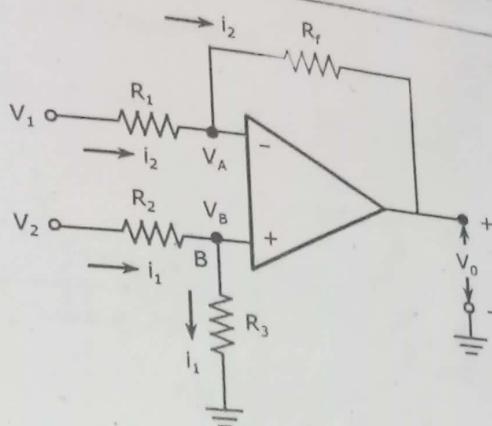


Fig. 7.4.8

The input signal V_1 is applied to inverting input through a resistance R_1 and other input signal V_2 is applied to a non-inverting terminal through a resistance R_2 . R_f is the feedback resistance and R_3 is another resistance connected between the non-inverted input terminal and ground.

According to the virtual ground condition, the node A voltage ' V_A ' and node B voltage are equal,

$$\text{i.e., } v_B = v_A$$

Applying kCL at node B,

$$\text{We get, } \frac{V_2 - v_B}{R_2} = \frac{v_B - 0}{R_3}$$

$$\frac{V_2}{R_2} - \frac{v_B}{R_2} = \frac{v_B}{R_3}$$

$$\Rightarrow \frac{V_2}{R_2} = \frac{v_B}{R_3} + \frac{v_B}{R_2}$$

$$\Rightarrow \frac{V_2}{R_2} = v_B \left(\frac{1}{R_3} + \frac{1}{R_2} \right)$$

$$\Rightarrow v_B = \frac{V_2}{R_2 \left[\frac{1}{R_3} + \frac{1}{R_2} \right]}$$

$$v_B = \frac{V_2}{\left(\frac{R_2}{R_3} + 1 \right)}$$

... (7.4.11)

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Applying kCL at node 2,

We get,

$$\frac{V_1 - V_A}{R_1}$$

$$\frac{V_1}{R_1} - \frac{V_A}{R_1} = \frac{V_A}{R_f} - \frac{V_0}{R_f}$$

$$\Rightarrow \frac{V_1}{R_1} = \frac{V_A}{R_f} + \frac{V_A}{R_1} - \frac{V_0}{R_f}$$

$$\Rightarrow \frac{V_1}{R_1} = V_A \left(\frac{1}{R_f} + \frac{1}{R_1} \right) - \frac{V_0}{R_f}$$

$$V_1 = V_A \left(1 + \frac{R_1}{R_f} \right) - V_0 \frac{R_1}{R_f} \quad \dots (7.4.12)$$

Since $V_A = V_B$, substitute Eq. (7.4.11) in Eq. (7.4.12),

$$\text{We get, } V_1 = \frac{V_2}{\left(\frac{R_2}{R_3} + 1 \right)} \left[1 + \frac{R_1}{R_f} \right] - V_0 \frac{R_1}{R_f}$$

We assume $R_1 = R_2 = R_f = R_3$, then we get,

$$V_1 = \frac{V_2}{Z} (Z') - V_0$$

$$V_1 = V_2 - V_0$$

∴

$$V_0 = V_2 - V_1 \quad \dots (7.4.13)$$

From the Eq. (7.4.13), the output voltage is directly proportional to difference between the two input voltages ' V_2 ' and ' V_i '.

7.4.5 Differentiator

The circuit which produces the differentiation of the input voltage at its output is called differentiator.



7.4.1 Ideal Op-Amp Differentiator

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The op-amp differentiator circuit is shown in Fig. 7.4.9.

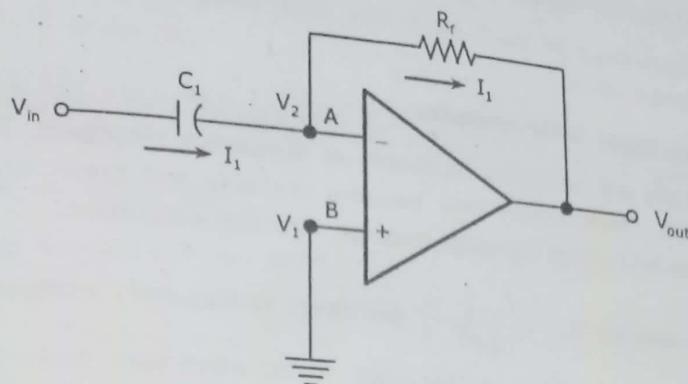


Fig. 7.4.9 Op-Amp Differentiator

An input voltage V_{in} is applied at the inverting terminal of the op-amp.

The potential of node A is same as node B due to virtual ground concept, hence $V_2 = V_1 = 0$.

Since input current inside op-amp is zero, entire current I_1 flows through the resistance R_f .

From the input side of differentiator, we have,

$$I_1 = C_1 \frac{d}{dt} (V_{in} - V_2) = C_1 \left[\frac{dV_{in}}{dt} \right] \quad \dots (7.4.14)$$

From the output side of differentiator, we have,

$$I_1 = \frac{V_2 - V_{out}}{R_f} = \frac{-V_{out}}{R_f} \quad \dots (7.4.15)$$

Equating Eqs. (7.4.14) and (7.4.15), we obtain,

$$\frac{C_1 dV_{in}}{dt} = \frac{-V_{out}}{R_f} \quad \dots (7.4.16)$$

$$V_{out} = -C_1 R_f \frac{dV_{in}}{dt}$$

Eq. (7.4.16) shows that the output of differentiator is $C_1 R_f$ times the differentiation of the input and product $C_1 R_f$ is called time constant of the differentiator.

The negative sign indicates that there is a phase shift of 180° between input and output.

The main advantage of such an active differentiator is the small time constant required for differentiation.

Limitations of an Ideal Differentiator

- (1) The gain of the differentiator increases as frequency increases. Thus at some high frequency, the differentiator may become unstable and break into the oscillations. There is possibility that op-amp may go into the saturation.
 - (2) The input impedance $X_{C_1} = \left(\frac{1}{2\pi f C_1} \right)$ decreases as frequency increases. This makes the circuit very much sensitive to the noise. Thus, when such noise gets amplified due to high gain at high frequency, noise may completely override the differentiated output.
- These limitations can be corrected by using some additional parameters in the basic differentiator circuit. Such a differentiator circuit is called practical differentiator circuit.

7.4.5.2 Practical Differentiator

The noise and stability at high frequency can be corrected, in the practical differentiator circuit using the resistance R_1 in series with C_1 and the capacitor C_f in parallel with resistance R_f . The practical differentiator circuit is shown in Fig. 7.4.10. The resistance R_{comp} is used for bias compensation.

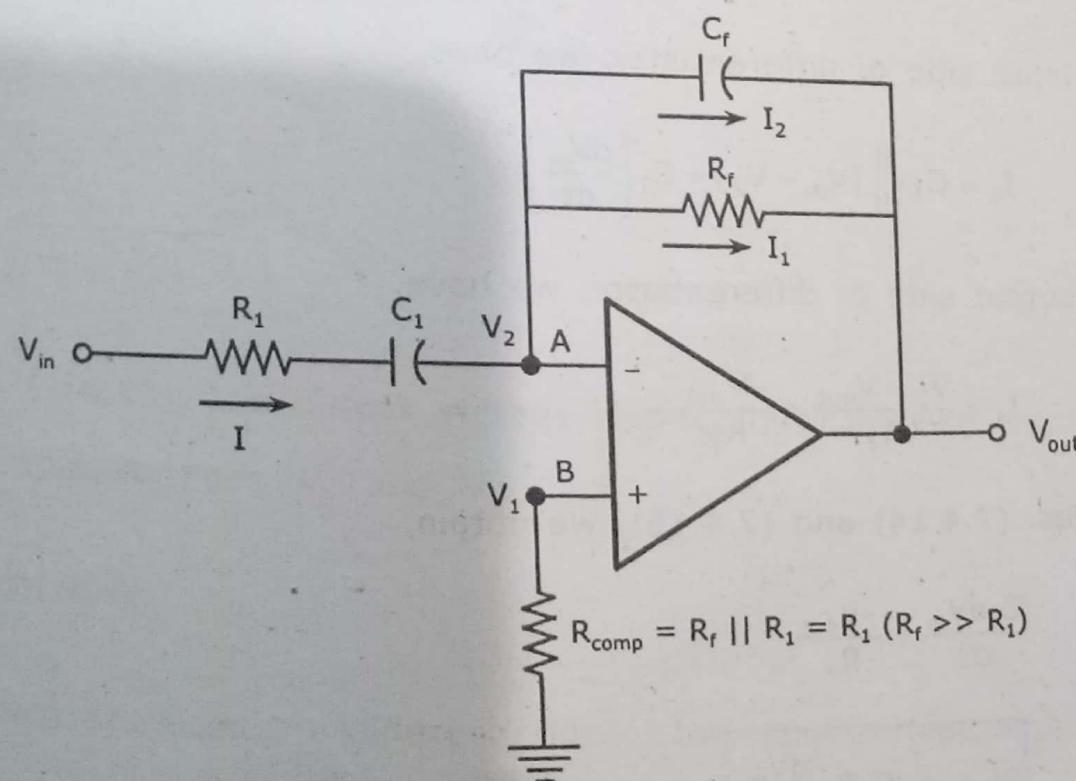


Fig. 7.4.10 Practical Differentiator Circuit

(1) **Analysis of a Practical Differentiator** : Since input current inside op-amp is zero there is no current input at node B. Hence it is at the ground potential. From the concept of the virtual ground, node A is also at the ground potential and hence $V_1 = V_2 = 0$ in Fig. 7.4.10.

The current I , is given by,

$$I = \frac{V_{in} - V_2}{Z_1} = \frac{V_{in}}{Z_1} \quad \dots (7.4.17)$$

where $Z_1 = R_1$ in series with C_1

So, in Laplace domain we can write,

$$Z_1 = R_1 + \frac{1}{sC_1} = \frac{1 + sR_1C_1}{sC_1} \quad \dots (7.4.18)$$

Substituting Eq. (7.4.18) in Eq. (7.4.17), we get,

$$I = \frac{V_{in}(s)}{\frac{1 + sR_1C_1}{sC_1}} = \frac{sC_1V_{in}(s)}{(1 + sR_1C_1)} \quad \dots (7.4.19)$$

Now the current I_1 is given by,

$$I_1 = \frac{V_2 - V_{out}}{R_f} = \frac{-V_{out}}{R_f}$$

In Laplace form, we have,

$$I_1 = \frac{-V_{out}(s)}{R_f}$$

$$\text{And } I_2 = C_f \frac{d(V_2 - V_{out})}{dt} = -C_f \frac{dV_{out}}{dt}$$

Taking Laplace transform, we obtain

$$I_2 = -sC_f V_{out}(s)$$

Applying KCL at node A, we obtain,

$$I = I_1 + I_2$$

$$\frac{sC_1V_{in}(s)}{(1 + sR_1C_1)} = \frac{-V_{out}(s)}{R_f} - sC_f V_{out}(s)$$

$$\frac{sC_1V_{in}(s)}{(1 + sR_1C_1)} = -V_{out}(s) \left[\frac{1 + sR_fC_f}{R_f} \right]$$

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A quality product marketed by



$$\Rightarrow V_{\text{out}}(s) = \frac{sR_f C_1 V_{\text{in}}(s)}{(1 + sR_f C_f)(1 + sR_1 C_1)} \quad \dots (7.4.20)$$

If $R_1 C_1 = R_f C_f$ then we have,

$$V_{\text{out}}(s) = \frac{-sR_f C_1 V_{\text{in}}(s)}{(1 + sR_f C_f)^2} \quad \dots (7.4.21)$$

The time constant $R_f C_1$ is much greater than $R_1 C_1$ or $R_f C_f$ and hence the Eq. (7.4.21) reduces to,

$$V_{\text{out}}(s) = -sR_f C_1 V_{\text{in}}(s)$$

On applying inverse Laplace transform, we get,

$$V_{\text{out}} = -R_f C_1 \left[\frac{d}{dt} V_{\text{in}}(t) \right]$$

Thus the output voltage is the $R_f C_1$ times the differentiator of the input.

It may be noted that though $R_f C_1$ is much larger than $R_f C_f$ or $R_1 C_1$, yet it is less than or equal to the time period T of the input, for the true differentiation. Hence, we have,

$$R_f C_1 \leq T$$

7.4.5.3 Guidelines to Design Practical Differentiator

By using following steps, a good practical differentiator can be designed,

- (1) Choose f_c as the highest frequency of the input signal.
- (2) Choose C_1 to be less than $1 \mu\text{F}$ and calculate the value of R_f .
- (3) Choose f_b as 10 times f_a which ensures that $f_a < f_b$.
- (4) Finally, calculate the values of R_1 and C_f from the expression $R_1 C_1 = R_f C_f$.
- (5) The R_{comp} can be selected as $R_1 \parallel R_f$ but practically it is almost equal to R_L .

7.4.6 Integrator

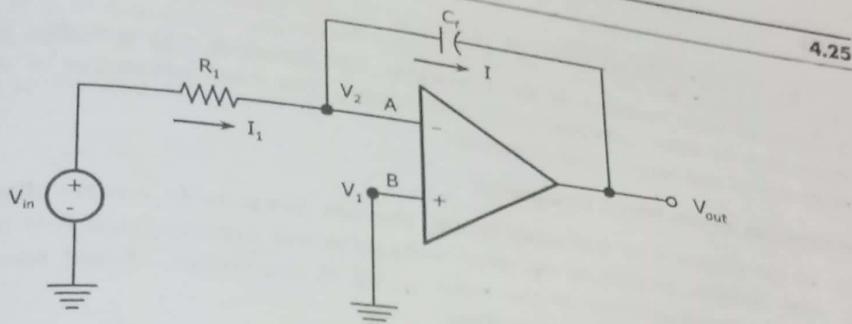
The circuit which produces the integration of the input voltage at its output is called integrator.

7.4.6.1 Ideal Op-Amp Integrator

The integrator circuit can be obtained by exchanging the position of R and C in the basic differentiator circuit. The op-amp integrator circuit is shown in the Fig. 7.4.11,

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Fig. 7.4.11 Integrator

Replacing the feedback resistor R_f of the ideal amplifier in the inverting mode by a capacitor as shown in Fig. 7.4.11. We obtain an integrator.

The input voltage V_{in} is applied to the negative input terminal through resistor R_1 . Current through capacitor, C_f is given by,

$$I = C_f \frac{d}{dt} (V_2 - V_{out})$$

Applying KCL at node A,

$$\frac{V_{in} - V_2}{R_1} = C_f \frac{d}{dt} (V_2 - V_{out}) \quad \dots (7.4.22)$$

As node B is ground, node A is also at grounded potential, from the concept of virtual ground, so $V_2 = 0$.

∴ Equation (7.4.22) becomes,

$$\begin{aligned} \frac{V_{in}}{R_1} &= -C_f \frac{d}{dt} [V_{out}] \\ \Rightarrow dV_{out} &= \frac{-V_{in} dt}{R_1 C_f} \end{aligned} \quad \dots (7.4.23)$$

Taking integration on both sides of Eq. (7.4.23), we have,

$$\begin{aligned} \int dV_{out} &= \frac{-1}{R_1 C_f} \int_0^t V_{in}(t) dt \\ \therefore V_{out} &= -\frac{1}{R_1 C_f} \int_0^t V_{in}(t) dt + V_{out}(0) \end{aligned} \quad \dots (7.4.24)$$

where, $V_{out}(0)$ is the constant for integration which indicates initial output voltage.

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Eq. (7.4.24) shows that the output is $-\frac{1}{R_1 C_f}$ times the integral of input and $R_1 C_f$ is called as time constant of the integrator. The negative sign indicates that there is a phase shift of 180° between input and output. The main advantage of such an active integrator is the large time constant.

Limitations of an Ideal Integrator

- (1) In the presence of the input signal, the two components namely offset voltage and bias current, contribute an error voltage at the output. Thus, it is not possible to get a true integration of the input signal at the output. Output waveform may be distorted due to an error voltage.
- (2) Another limitation of an ideal integrator is its bandwidth, which is very small. Hence an ideal integrator can be used for a very small frequency range of the input only.

Because of these limitations, an ideal integrator is not used in practice. Some additional components are used along with the basic integrator circuit to reduce the effect of an error voltage, in practice such as integrator is called as practical integrator circuit.

7.4.6.2 Practical Integrator

The limitations of an ideal integrator can be minimized in the practical integrator circuit, which use a resistance R_f in parallel with the capacitor C_f . The practical integrator circuit has been shown in Fig. 7.4.12,

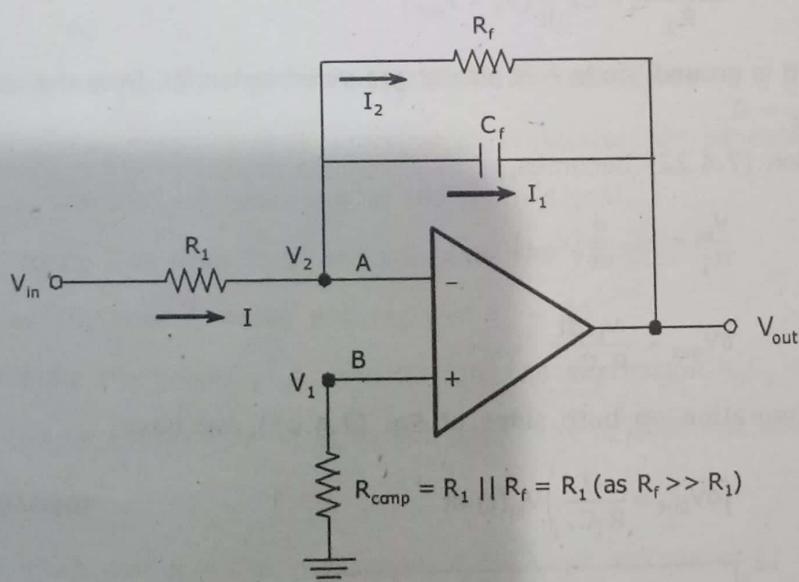


Fig. 7.4.12 Practical Integrator Circuit

The resistance R_{comp} is also used to overcome the error due to bias current. The resistance R_f reduces the low frequency gain of the op-amp.

(1) **The Analysis of Practical Integrator :** Since the input current inside op-amp is zero the node B is at ground potential. Hence, the node A is also at the ground potential from the concept of virtual ground. So, $V_1 = V_2 = 0$.

Referring to Fig. 7.4.12, we have,

$$I = \frac{V_{in} - V_2}{R_1} = \frac{V_{in}}{R_1} \quad \dots (7.4.25)$$

Similarly, $I_1 = \frac{C_f d(V_2 - V_{out})}{dt} = \frac{-C_f dV_{out}}{dt}$ $\dots (7.4.26)$

And $I_2 = \frac{V_2 - V_{out}}{R_f} = \frac{-V_{out}}{R_f}$ $\dots (7.4.27)$

Applying KCL at node A we have,

$$I = I_1 + I_2 \quad \dots (7.4.28)$$

Substituting Eqs. (7.4.26), (7.4.26) and (7.4.27), in Eq. (7.4.28), we get,

$$\frac{V_{in}}{R_1} = \frac{-C_f dV_{out}}{dt} - \frac{V_{out}}{R_f} \quad \dots (7.4.29)$$

Taking Laplace transform of Eq. (7.4.29), we get,

$$\frac{V_{in}(s)}{R_1} = -sC_f V_{out}(s) - \frac{V_{out}(s)}{R_f}$$

$$\Rightarrow \frac{V_{in}(s)}{R_1} = -V_{out}(s) \left[sC_f + \frac{1}{R_f} \right]$$

$$\Rightarrow \frac{V_{in}(s)}{R_1} = -V_{out}(s) \left[sC_f + \frac{1}{R_f} \right]$$

$$\Rightarrow \frac{V_{in}(s)}{R_1} = \frac{-V_{out}(s)[1 + sC_f R_f]}{R_f}$$

$$\Rightarrow V_{out}(s) = \frac{R_f}{R_1(1 + sC_f R_f)} V_{in}(s)$$

$$\therefore V_{out}(s) = -\frac{1}{\left(sR_1 C_f + \frac{R_1}{R_f} \right)} V_{in}(s)$$

When R_f is large then $\frac{R_1}{R_f}$ can be neglected.

$$V_{\text{out}}(s) = -\frac{1}{sR_1C_f} V_{\text{in}}(s)$$

On applying inverse Laplace to above equation, we get,

$$V_{\text{out}}(t) = -\frac{1}{R_1C_f} \int V_{\text{in}}(t) dt$$

... (7.4.30)

7.4.7 Instrumentation Amplifier

Measurement control of physical quantities is required in large number of industrial and consumer applications. Some of the typical examples are measurement and control of temperature, humidity, water flow etc. These physical quantities are in general measured with the help of transducers. The output of transducer has to be amplified in order to drive the indicator or display system. This function is preferred by an instrumentation amplifier.

The main features of an instrumentation amplifier are as follows,

- (1) High gain accuracy.
- (2) High CMRR.
- (3) Low output impedance.
- (4) Low D.C offset.
- (5) High gain stability with low temperature coefficient.

The instrumentation amplifier is also called as data amplifier and is basically a differential amplifier.

The Fig. 7.4.13 shows the circuit diagram of a differential amplifier.

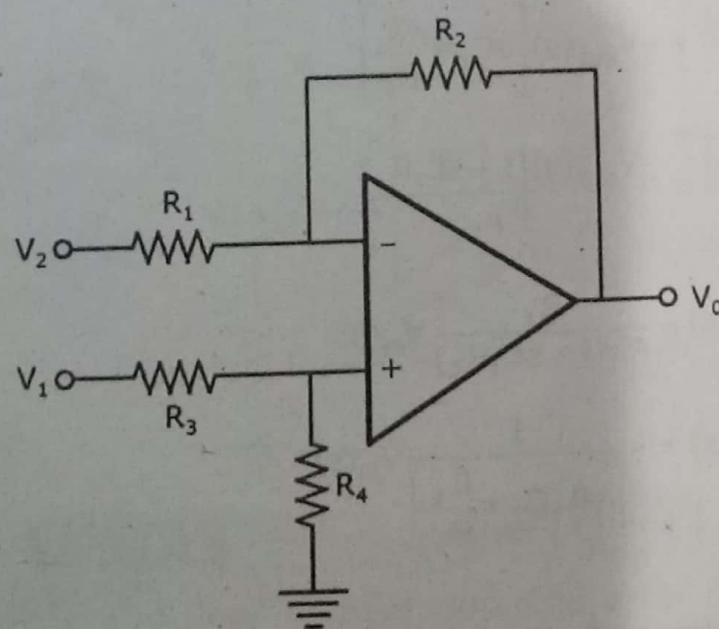


Fig. 7.4.13 Differential Amplifier

From the Fig. 7.4.13 we can be easily seen that output voltage V_0 is given by,

$$V_0 = \frac{R_2}{R_1} [V_1 - V_2]$$

One of the commonly used instrumentation amplifier circuit is the three op-amp instrumentation amplifier. A non-inverting amplifier is added to each of the basic differential amplifier inputs in the circuit. This circuit provides high input resistance for accurate measurement of signals from transducers.

The following Fig. 7.4.14 is the circuit diagram of 3 op-amp instrumentation amplifier.

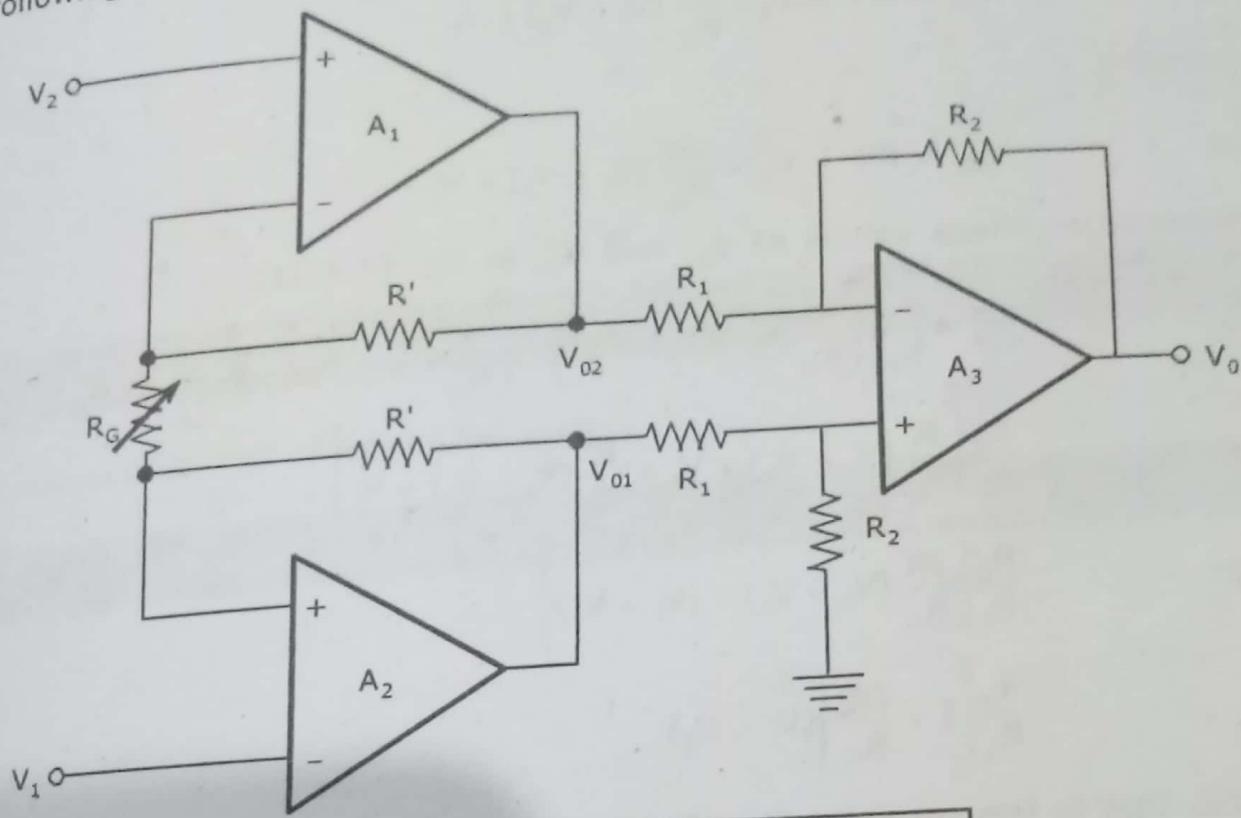


Fig. 7.4.14 Instrumentation Amplifier

The op-amps A_1 and A_2 have differential input voltage as zero. When $V_1 = V_2$ i.e., under common mode condition, the voltage across R_G is zero. Hence no current flows through R_G and R' . Thus the non inverting amplifier A_1 acts as a voltage follower, so its output $V_{02} = V_2$. Similarly, the op-amp A_2 acts as a voltage follower and has the output $V_{01} = V_1$.

When $V_1 \neq V_2$, current flows through the resistors R_G , R' and $(V_{02} - V_{01}) > (V_2 - V_1)$. Thus, the circuit has differential gain and CMRR more when compared to signal op-amp circuit.

8.1 INTRODUCTION

Digital systems have a vast application in every area. Digital systems are used in communication, traffic control, entertainment, weather monitoring etc. We have some commonly used digital devices such as digital television, digital camera, digital computer etc.

The term digital system refers to the systems which manipulate discrete quantities of information that are represented in binary form.

Every digital system has some common features,

- (1) Discrete elements of information are represented by physical quantities called signals. The signals use discrete values ON and OFF, hence said to be binary.
- (2) The instructions are represented by a BINARY DIGIT called a BIT, has two values 0 and 1. So, the discrete values of information are represented by a group of bits called "Binary Codes".
- (3) A digital system is an interconnection of digital modules. (Digital circuits and their logic functions).
- (4) Digital circuits are also referred as logic circuits, process data using binary logic elements (logic gates by giving binary signals).
- (5) All digital systems have binary storage elements (flip-flops to store the binary quantities).
- (6) The best known example of digital system is the general purpose "digital computer".

The peculiar property of the digital computer is its generality.

8.2 BASIC LOGIC GATES

- (1) Logic gates are the functional building blocks of digital systems. Logic gate is an electronic circuit that operates on one or more input signals to produce an output signal.
- (2) The inputs and outputs of logic gates can occur only in two levels. These two levels are termed as HIGH and LOW or TRUE and FALSE or ON and OFF or simply 1 and 0. The output level (logic HIGH or logic LOW) depends upon the combinations of input levels. Any logic gate operation can be understood with the help of Truth Table.
- (3) Digital electronics deals with different types of logic gates. They are,
 - (i) OR, AND, NOT gates (also known as basic gates) which are mostly used in combinational logic design.
 - (ii) NAND, NOR gates (also known as universal gates) because all the other gates can be realized using either, only by NAND gates or only by NOR gates.

8.2.1 NOT Gate

The NOT gate performs a basic logic function called inversion (or) complementation. It is having only one input and one output. The purpose of NOT gate is to change one logic level into opposite logic level i.e., '0' to '1' and '1' to '0'.

Fig. 8.2.1 shows the symbols of NOT gate,

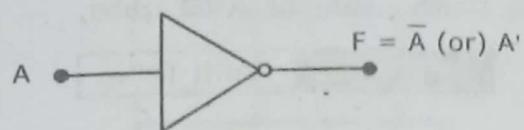


Fig. 8.2.1 Symbol of NOT Gate

If A is applied to the NOT gate input, output is the complement form of A, i.e., $F = \bar{A}$ (or) A' .

The NOT operation can be expressed as "F equals to NOT A (or) F equals to inverse A (or) F equals to the complement of A".

The NOT gate is also known as inverter.

The Table 8.2.1 represents the truth table of NOT gate.

Table 8.2.1 Truth Table

| Inputs A | Output F |
|-------------|-------------|
| 0 | 1 |
| 1 | 0 |

8.2.2 AND Gate

The AND gate performs logical multiplication.

Fig. 8.2.2 shows logical symbol of AND gate,

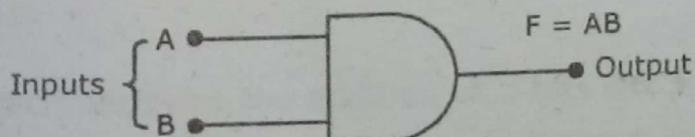


Fig. 8.2.2 Symbol of AND Gate

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The AND gate having two (or) more inputs and single output. In Fig. 8.2.2, the two inputs A and B are combined using AND operation, the result F can be represented as,

$$F = AB$$

The operation of AND gate is such that "The output is logic high when all inputs are high otherwise output is logic low".

Table 8.2.2 represent the truth table of AND gate,

Table 8.2.2 Truth Table

| Inputs | | Output |
|--------|---|-----------------|
| A | B | $F = A \cdot B$ |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

8.2.3 OR Gate

The OR gate performs logical addition, commonly known as OR function. It is having two (or) more inputs and only one output.

Fig. 8.2.3 shows symbol of OR gate,

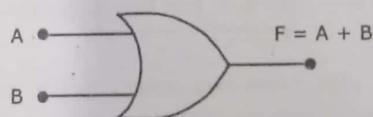


Fig. 8.2.3 Symbol of OR Gate

The two inputs A and B are combined to the OR operation, the output result F can be represented as,

$$F = A + B$$

The operation of OR gate is such that "the output is logic high when any one of the input is high otherwise the output is low".

Table 8.2.3 shows the Truth Table of OR gate,

Table 8.2.3 Truth Table

| Input | | Output A + B |
|-------|---|-----------------|
| A | B | |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

8.2.4 Timing Diagrams of Basic Logic Gates

Fig. 8.2.4 shows the timing diagrams for the corresponding output signal for each type of gate. The horizontal axis of a timing diagram represents time and the vertical axis shows a signal as it changes between the two possible voltage levels.

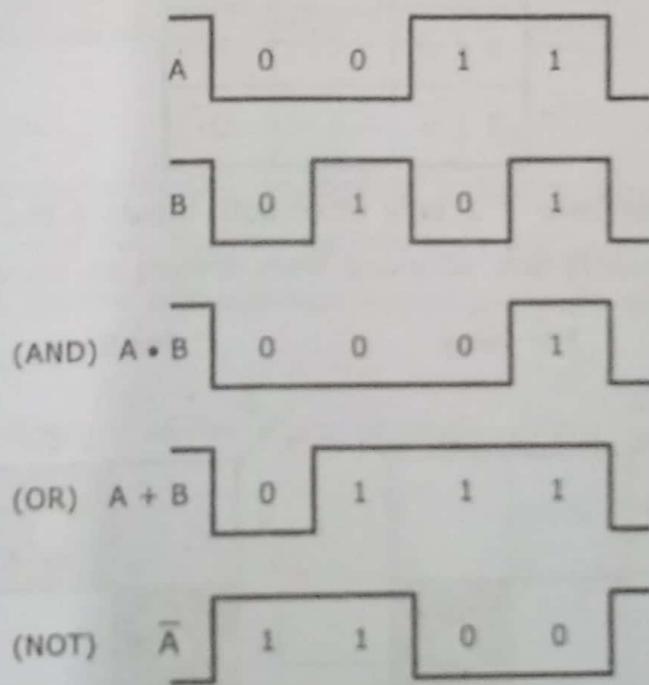


Fig. 8.2.4 Timing Diagram

8.3 HALF ADDER

The adder circuit which performs the addition of 2-bits is called as half adder. It needs two binary inputs which are designated as the 'augend' and 'addend' bits and two binary outputs which are designated as the sum and carry.

Let, the inputs be represented by A and B, the outputs be given by S (sum) and C (carry).

The schematic block diagram of half-Adder is shown in Fig. 8.3.1.

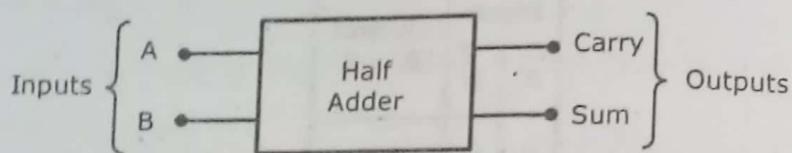


Fig. 8.3.1 Schematic Block Diagram of Half Adder

The truth table is shown in Table 8.3.1,

Table 8.3.1 Truth Table of Half Adder

| Inputs | | Outputs | |
|--------|---|-----------|---------|
| A | B | Carry (C) | Sum (S) |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

It can be seen that the carry = 1, only when both inputs A and B are 1. The simplified expressions for sum and carry are obtained from K-map as shown in Fig. 8.3.2,

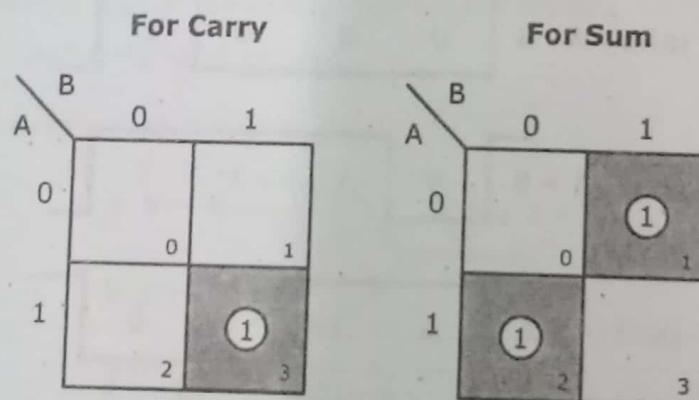


Fig. 8.3.2 K-map Simplifications for Half Adder Outputs

From the K-map simplifications, we have the output expressions as,

$$(\text{Sum}) \quad S = \bar{A}\bar{B} + A\bar{B} = A \oplus B$$

$$(\text{Carry}) \quad C = AB$$

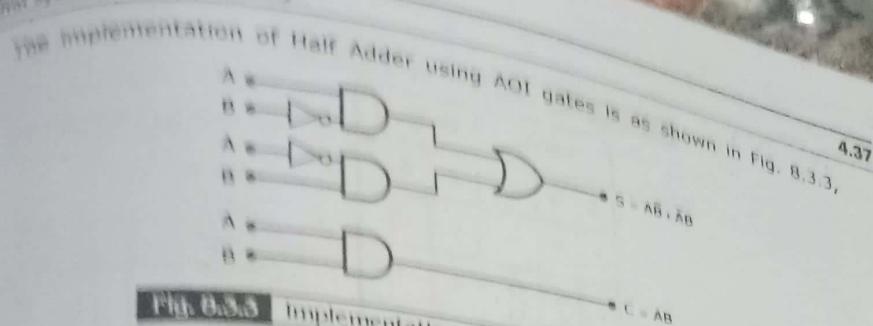


Fig. 8.3.3 Implementation of Half-Adder using AOT Gates

Logic circuit of Half-Adder drawn using an Ex-OR gate and AND gate is shown in Fig.

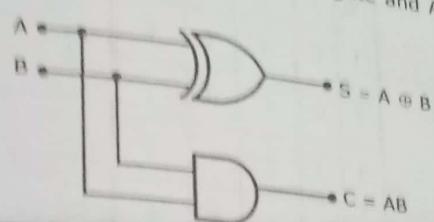


Fig. 8.3.4 Logic Diagram of a Half-adder

8.4 FULL ADDER

The adder circuit that performs the addition of 3 bits is called as Full-adder. It has three inputs (A , B and C_{in}) and two outputs namely sum (S) and carry (C_{out}). In general, out of 3 binary inputs, 2 inputs are used as external inputs and third input is used as a carry in previous stage.

The schematic block diagram of full adder is shown in Fig. 8.4.1 and Truth Table is shown in Table 8.4.1.

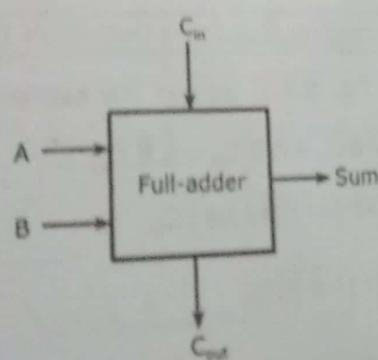


Fig. 8.4.1 Block Diagram of Full Adder

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Table 8.4.1 Truth Table of Full Adder

| Inputs | | | Outputs | |
|--------|---|-----------------|---------|------------------|
| A | B | C _{in} | S | C _{out} |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

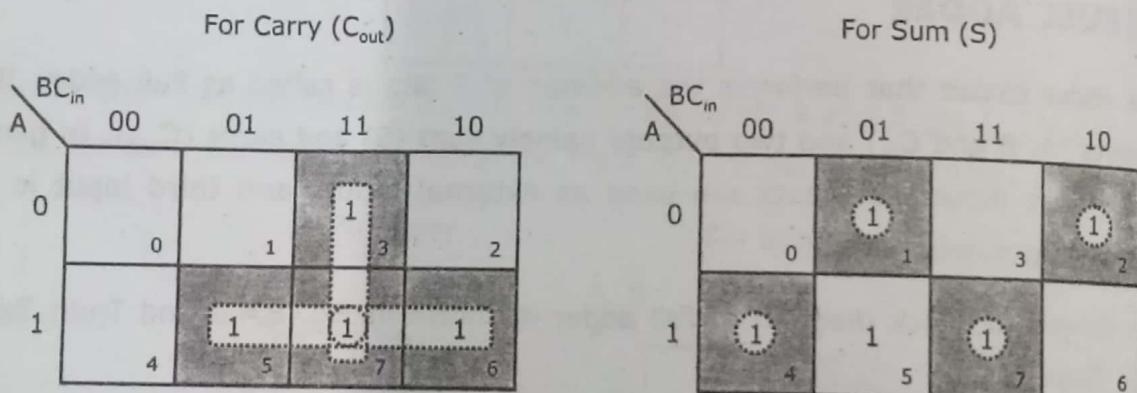
K-map Simplification

Fig. 8.4.2 K-map for Sum Carry Outputs of Full-adder

From the K-map shown in Fig. 8.4.2, we get the expressions for sum and carry as,

$$\begin{aligned}
 S &= \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}C_{in} + A\bar{B}\bar{C}_{in} \\
 &= \bar{C}_{in}(\bar{A}B + A\bar{B}) + (\bar{A}\bar{B} + AB)C_{in} \\
 &= \bar{C}_{in}(A \oplus B) + (\overline{A \oplus B})C_{in} \\
 &= A \oplus B \oplus C_{in}.
 \end{aligned}$$

$$C_{out} = AB + BC_{in} + AC_{in}$$

Since, the sum and carry expressions have XOR, OR, and AND operations only. Therefore full adder can be easily realized by using two XOR gates, one OR gate and two AND gates i.e., two half adders and one OR gate is as shown in Fig. 8.4.3.

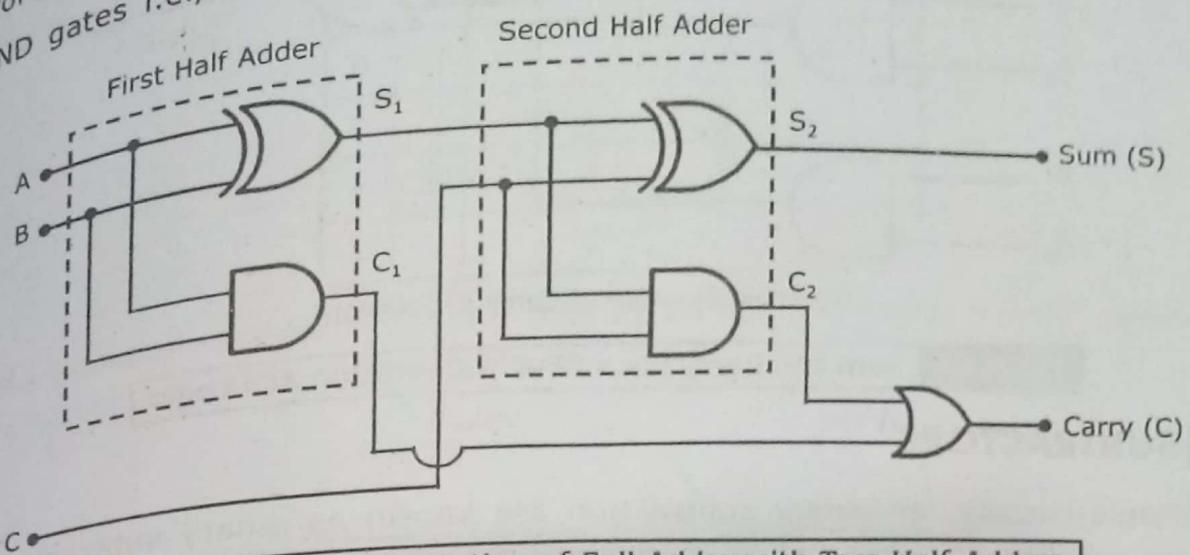
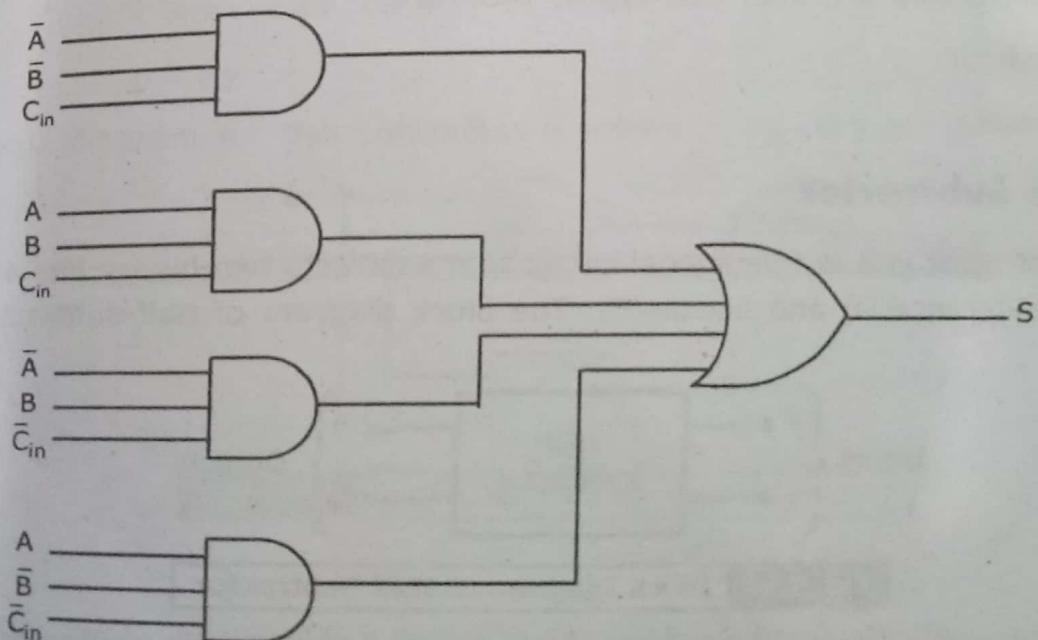
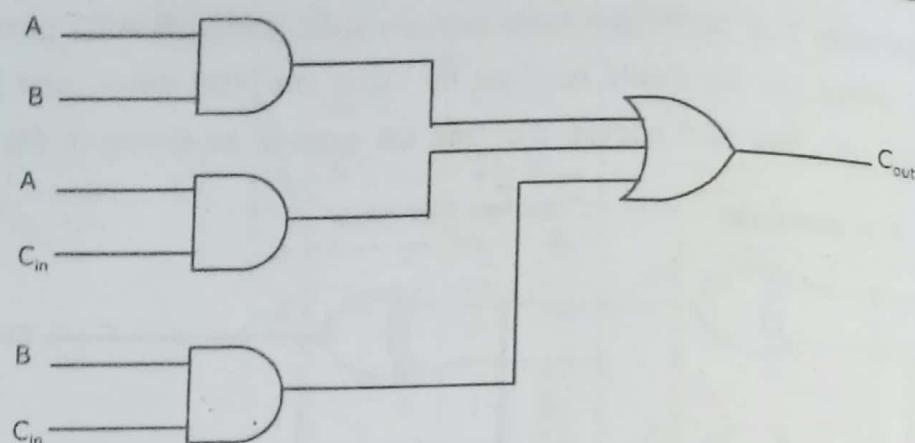


Fig. 8.4.3 Implementation of Full Adder with Two Half Adders

The construction of a full adder using two half adders and OR gate is simple, but this arrangement needs more propagation delay, because the bits must propagate through several gates in succession. The construction of full adder using AOI logic is shown in Fig. 8.4.4. AOI logic requires less propagation delay as compared to construction of full adder using two half adders and OR gate.



(a) Logic Diagram of Sum Expression



(b) Logic Diagram of Carry Expression

Fig. 8.4.4 Sum and Carry Bits of Full Adder using AOI Logic

8.5 SUBTRACTORS

The logic circuits for binary subtraction are known as binary subtractors. The subtraction consists of four possible elementary operations, namely,

$$0 - 0 = 0$$

$$0 - 1 = 1 \text{ with } 1 \text{ borrow}$$

$$1 - 0 = 1$$

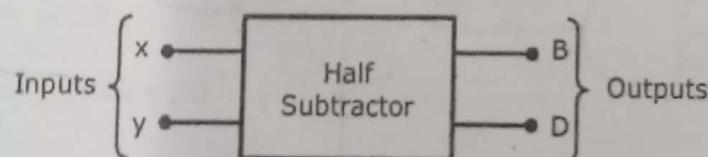
$$1 - 1 = 0$$

In all operations, each subtrahend bit is subtracted from the minued bit. In case of second operation the minued bit is smaller the subtrahend bit, hence 1 is borrowed. As adders, subtractors are also two types, they are,

- (1) Half subtractor.
- (2) Full subtractor.

8.5.1 Half Subtractor

A half subtractor is a combinational circuit that subtracts two binary bits and produces two outputs, difference(D) and borrow(B). The block diagram of half-subtractor is shown in Fig. 8.5.1.

**Fig. 8.5.1** Block Diagram of Half Subtractor

If x is the minuend and y is the subtrahend, then the result of operation of $x - y$ for all possible values of x and y are tabulated in Table 8.5.1.

Table 8.5.1 Truth-Table for Half-Subtractor

| Inputs | | Outputs | |
|--------|---|----------------|------------|
| x | y | Difference (D) | Borrow (B) |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

The Boolean expression for the outputs of half subtractor can be determined as follows by using K-maps shown in Fig. 8.5.2,

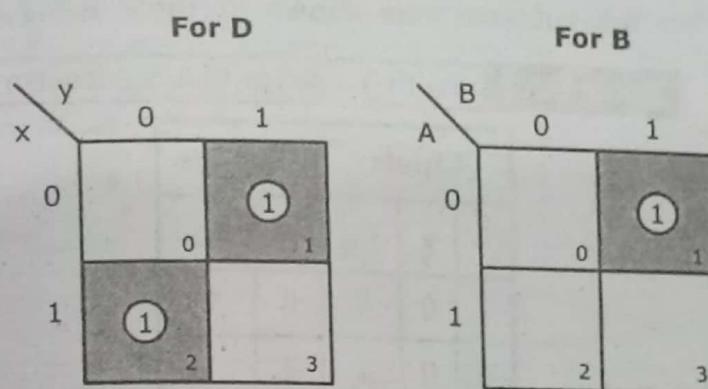


Fig. 8.5.2 K-maps for Difference and Borrow

The Boolean functions for two outputs of the half-subtractor are,

$$D = \bar{x}y + x\bar{y} = x \oplus y$$

$$B = \bar{x}y$$

The logic diagram for half-subtractor is shown in Fig. 8.5.3,

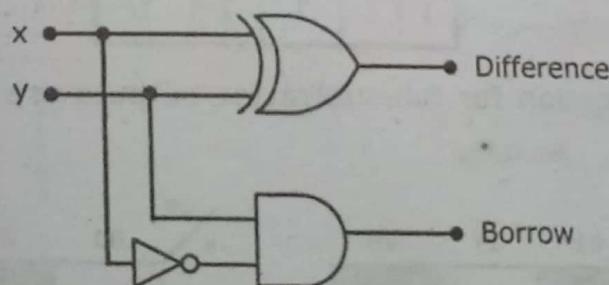


Fig. 8.5.3 Logic Diagram for Half Subtractor

COMMENTS

- (1) Half adder can be converted to a half Subtractor with one inverter at the input of AND gate.
- (2) The logic expression difference D is same as sum(S) expression of the half-adder.

8.5.2 Full Subtractor

A full subtractor is a combinational circuit that performs a subtraction of two bits, taking into consideration borrow of the lower significant bit. This circuit has three inputs and two outputs as shown in Fig. 8.5.4. The three inputs are x , y and B_{in} denoting minuend, subtrahend and previous borrow, respectively.

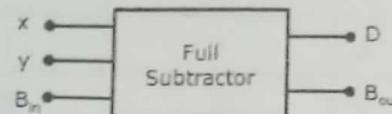


Fig. 8.5.4 Symbol for Full-Subtractor

The two outputs are, D and B_{out} , which represent the difference and output borrow respectively.

The truth table for full-subtractor is shown in Table 8.5.2,

Table 8.5.2 Truth-Table for Full-Subtractor

| Inputs | | | Outputs | |
|--------|-----|----------|---------|-----------|
| x | y | B_{in} | D | B_{out} |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

The K-map simplification for full-subtractor outputs are shown in Fig. 8.5.5,

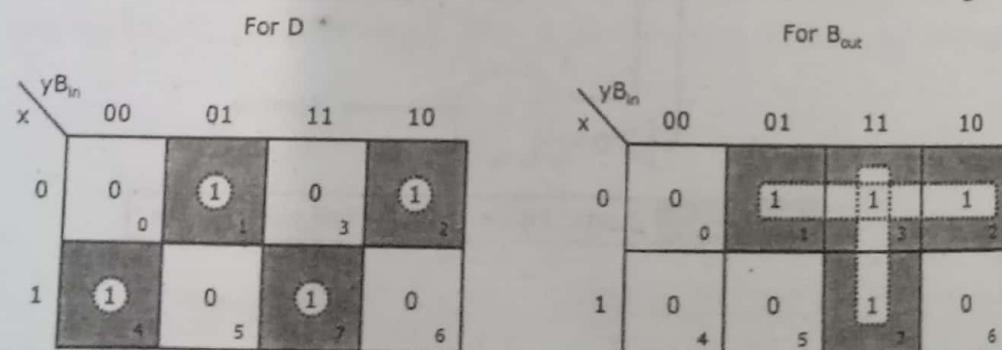


Fig. 8.5.5 K-map Simplifications for D and B_{out}

From the K-map shown in Fig. 8.5.5, we get the expressions for difference and borrow

$$\begin{aligned}
 D &= \bar{x}\bar{y}B_{in} + \bar{x}y\bar{B}_{in} + x\bar{y}\bar{B}_{in} + xyB_{in} \\
 &= B_{in}(\bar{x}\bar{y} + xy) + \bar{B}_{in}(\bar{x}y + x\bar{y}) \\
 &= B_{in}(x \oplus y) + \bar{B}_{in}(\bar{x} \oplus y) = B_{in}(\overline{x \oplus y}) + \bar{B}_{in}(x \oplus y) \\
 D &= X \oplus Y \oplus B_{in}
 \end{aligned}$$

$$\therefore B_{out} = \bar{X}B_{in} + \bar{X}Y + YB_{in}$$

And

Since the difference and borrow expression have XOR, OR and AND expressions only, hence full subtractor can be realized by using two XOR gates, one OR gate, two AND gates and two invertors as shown in Fig. 8.5.6,

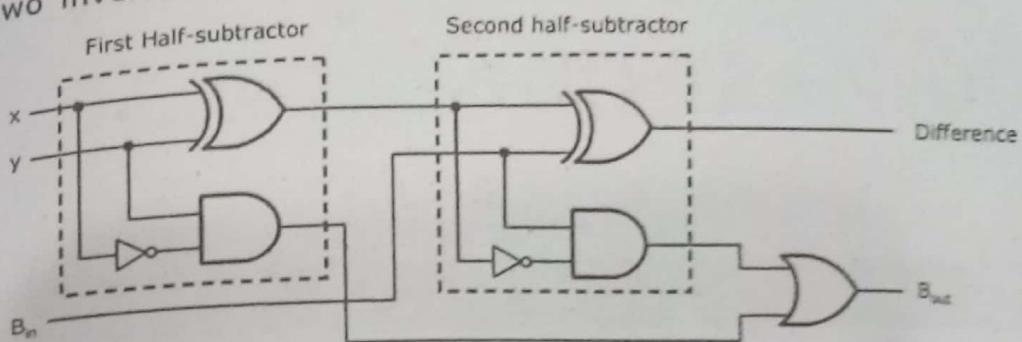


Fig. 8.5.6 Implementation of a Full-subtractor with Two Half-subtractors and an OR Gate

The logic diagram using AOI logic gates for implementing difference and borrow outputs of a Full-subtractor is as shown in Fig. 8.5.7,

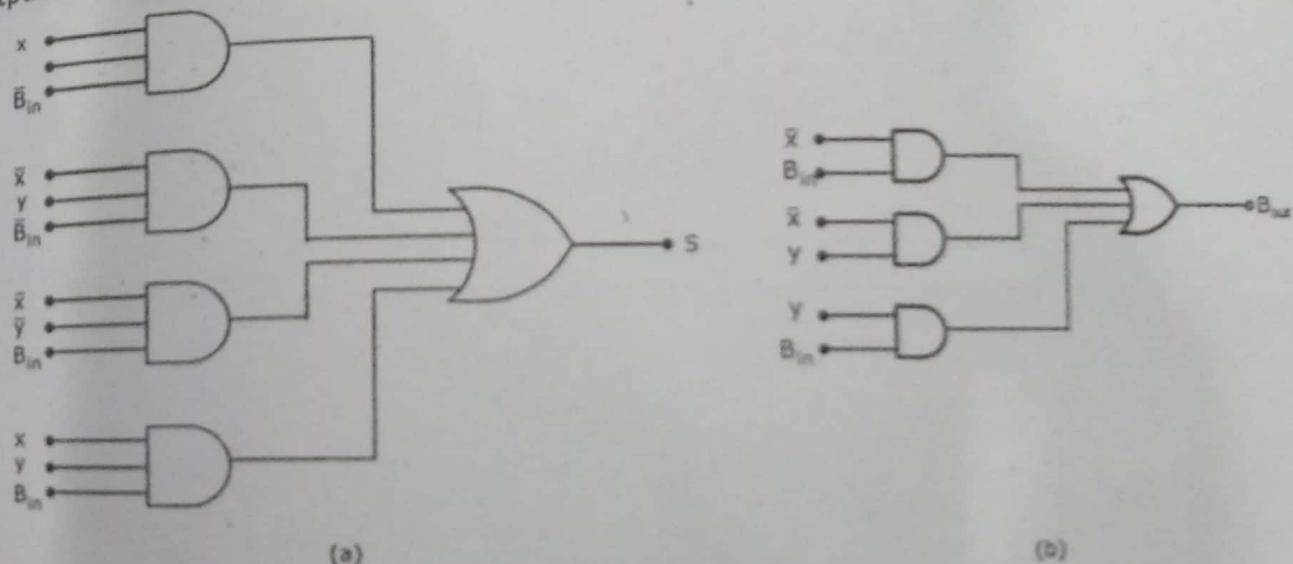


Fig. 8.5.7 Logic Diagrams for Difference and Borrow of Full Subtractor

