

4.1 FIELD EFFECT TRANSISTOR (FET)

The Field Effect Transistor (FET) was developed in the early 1960s. The name field effect is derived from the fact that the current flow in the device is controlled by an electric field, setup by an externally applied voltage. BJT, FET is also a three terminal devices, however the principle of operation of FET is completely different from that of BJT. The three terminals of FET are named as Drain (D), Source (S) and Gate (G), out of these three terminals gate terminal acts as a controlling terminal. FET is a voltage-controlled device.

Fig. 4.1.1 shows the symbol of FET,

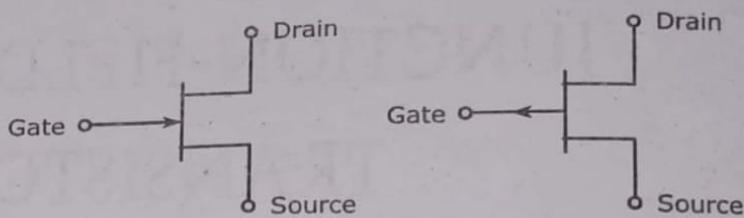


Fig. 4.1.1 Symbol of FET

Depending upon the constructional features and operating principles, FETs are classified into two types, they are,

- (1) Junction-Field Effect Transistor (JFET).
 - (2) Metal Oxide Semiconductor Field Effect Transistor (MOSFET).
- (or)

Insulated Gate Field Effect Transistor (IGFET).

Both of these two FETs are again divided into N-channel and P-channel.

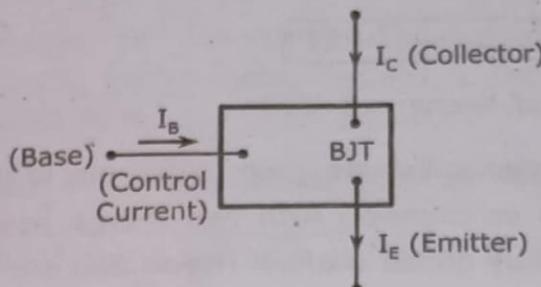
In this chapter, we will discuss only JFET.

4.1.1 Advantages of FETs Over BJT

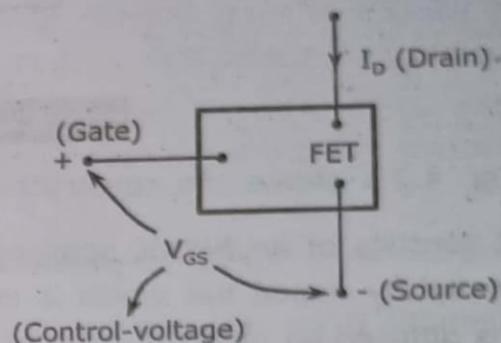
Following are the advantages of FETs over BJT,

- (1) The FET is a Unipolar device (i.e., the conduction of the device depends only on the single charge carriers i.e., either of electrons or holes in N-type and P-type respectively), whereas BJT is a bipolar device i.e., the conduction of the device depends on both the charge carriers.
- (2) FET has high input resistance in the order $10 \text{ M}\Omega$ for JFET and 10^{10} to $10^{15} \Omega$ for MOSFET. On the other hand, under normal operation of BJT input side is forward biased, giving low input resistance ($\approx 1 \text{ k}\Omega$).
- (3) FET is less noisy than BJT.

- (4) FET is less affected by radiation.
- (5) FETs are more thermally stable than BJTs.
- (6) FETs are simpler to fabricate and occupies less place in integrated form than BJTs.
- (7) FET has smaller size, high efficiency and longer life.
- (8) FET has very high power gain.
- (9) FET is a voltage - controlled device as shown in Fig. 4.1.2(a) whereas, BJT is a current controlled as shown in Fig. 4.1.2(b) device. Since most of the signals to be processed are voltage-signals, hence FETs are better than BJTs.



(a) BJT (Current Controlled Device)



(b) FET (Voltage Controlled Device)

Fig. 4.1.2 Working Operation Analogy of BJT and FET

4.1.2 Disadvantages of FETs over BJTs

The FET has the following disadvantages over the BJTs,

- (1) FETs has a very low transconductance and hence the voltage gain is low. Whereas in case of BJTs, transconductance is high, hence the voltage gain is high.
- (2) FETs are more expensive than BJTs.
- (3) FET has relatively small gain bandwidth product, when compared to BJTs.
- (4) FETs are susceptible to damage by ESD (Electro Static Discharge) such as lightening. Hence they are to be wrapped in Velostat paper during storage.

4.2 CONSTRUCTION AND WORKING OF JFET

4.2.1 Constructional Details of JFET

JFET can be abbreviated as Junction Field Effect Transistor. Based on the structure, JFET can be classified into two types, they are,

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(1) **N-channel JFET** : The basic construction of an N-channel JFET is as shown in Fig. 4.2.1,

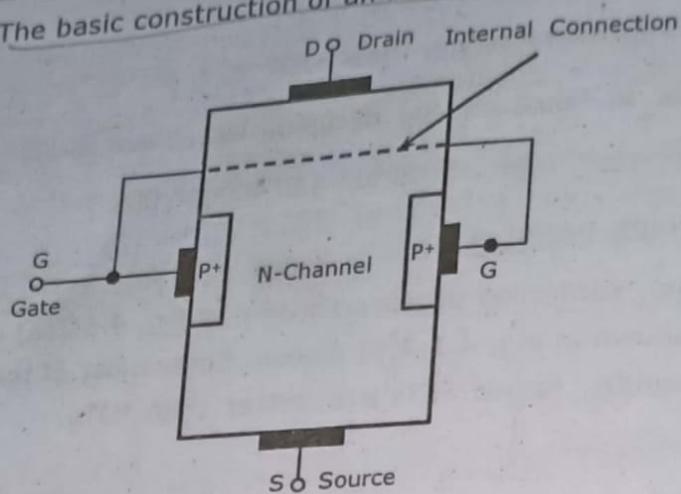


Fig. 4.2.1 N-channel J-FET

Fig. 4.2.1 shows the construction of N-channel JFET.

It consists of an N-type semiconductor substrate (here substrate is nothing but a very lightly doped bar which is used as channel) with two P-type heavily doped regions diffused on opposite sides of lightly doped channel region and are designated as P+. Thus two P-type regions form two PN-junctions. The space between the junctions (i.e., N-type region) is called a Channel. Both the P-type regions are connected internally and a single wire is taken out in the form of terminal called the Gate (G). The ohmic contacts are made to both ends of the N-type semiconductor and are taken out in the form of two terminals called Drain (D) and Source (S). The current carriers in N-channel JFET are electrons.

(2) **P-channel JFET**. The basic construction of P-channel JFET is shown in Fig. 4.2.2,

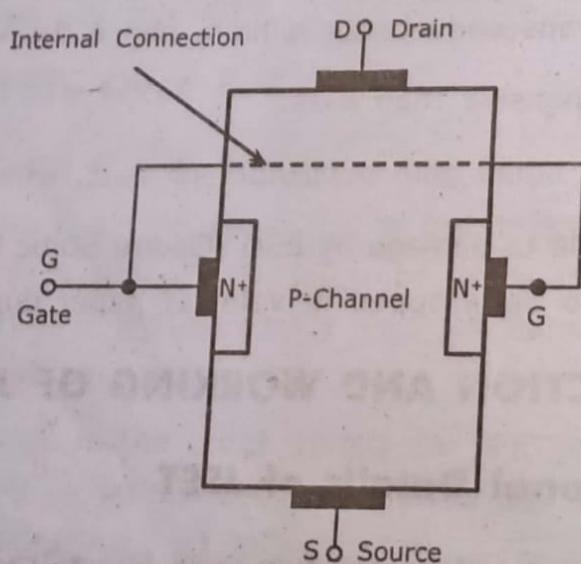


Fig. 4.2.2 P-channel J-FET

Fig. 4.2.2 shows the construction of P-channel JFET.

It consists of a lightly doped P-type substrate (i.e., channel region) with two heavily doped N-type regions diffused on opposite sides of it. The current carriers in P-channel JFET are holes. A typical structure of a junction field-effect transistor (N or P-channel) consists of four basic terminals. They are,

- (i) **Source** : It is the terminal through which the majority carriers enter the bar. It is analogous to the emitter terminal in BJT.
- (ii) **Drain** : It is the terminal through which the majority carriers leave the bar. It is similar to the collector terminal of a conventional BJT.
- (iii) **Gate** : The two heavily doped regions usually connected (internally) to a common terminal called as gate. Here gate terminal is analogous to the base terminal of BJT. It is used to control the flow of current from source to drain. The conventional current entering the bar at G is designated by I_G .
- (iv) **Channel (or Substrate)** : The region of N-type or P-type material between two heavily doped (gate) regions is the channel through which the majority carriers move from source to drain.

4.2.2 Working on Principle of Operation of JFET

To illustrate the working operation of JFET let us consider an N-channel JFET.

(i) How the Depletion Regions are Formed

Let us assume that the heavily doped P^+ regions (gate terminals) are biased by connecting to the negative gate supply (V_{GG}) and with no drain voltage ($V_{DD} = 0$) is applied between the drain and source terminals as shown in Fig. 4.2.3. It can be seen that the two heavily doped P^+ regions and N-channel region forms two P-N junction.

Since gate terminals are heavily doped than N-channel hence depletion region is penetrated more into the N-channel region as shown in Fig. 4.2.3,

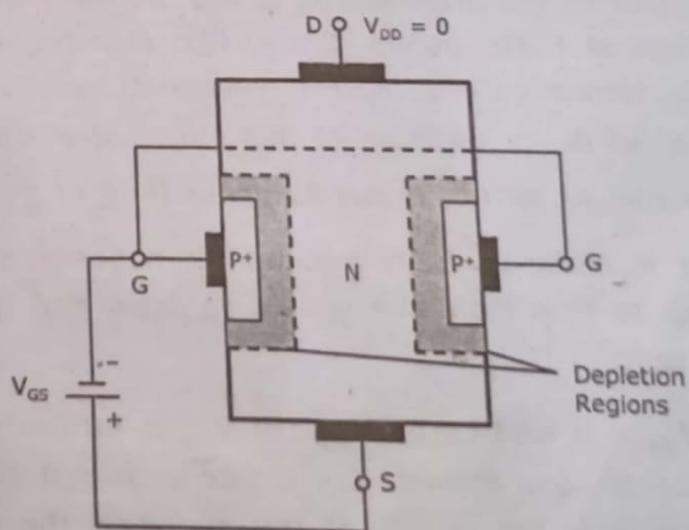


Fig. 4.2.3 Depletion Regions in N-Channel JFET when $V_{DD} = 0$

With this knowledge of depletion region created in JFET, let us consider following three cases to clearly understand the working operation of JFET.

CASE 1 (When $V_{GS} = 0$ and Small V_{DS}): Let us now consider a case, where a small positive voltage is applied between the drain and source terminals and no bias potential is applied between the gate and source terminals (i.e., $V_{GS} = 0$).

- (i) As drain is at positive potential with respect to source, hence electrons (carriers in N-channel FET) start flowing from source to drain which results a conventional current (I_D) to flow from drain to source as shown in Fig. 4.2.4(a),

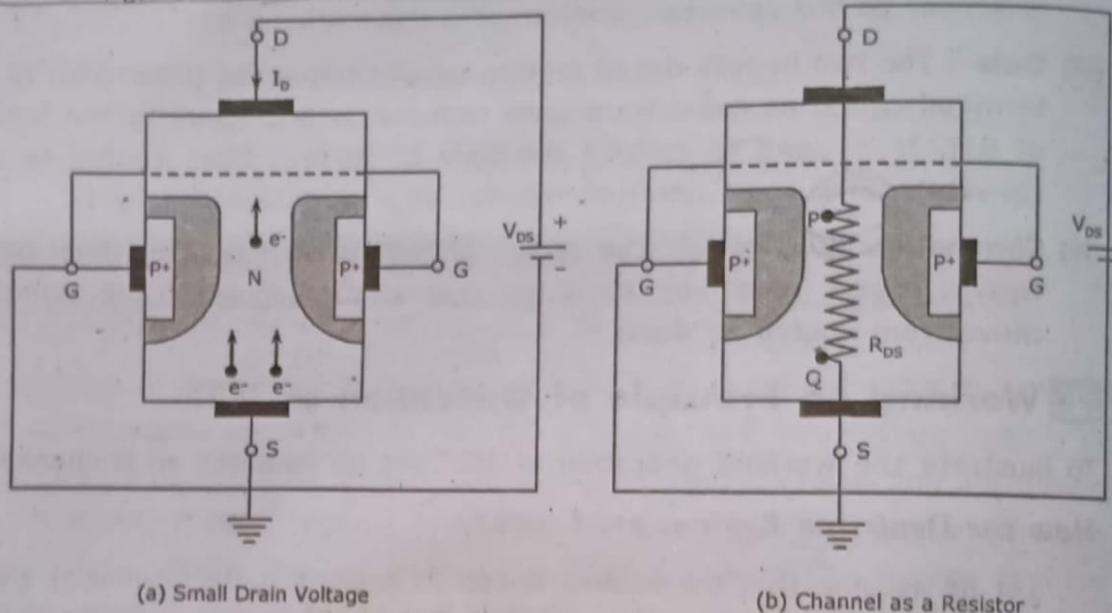


Fig. 4.2.4 JFET Operation when $V_{GS} = 0$ and V_{DS} is Applied

Due to the flow of current, there will be a voltage drop along the channel. As channel opposes the flow of drain current I_D , hence it acts as a resistor denoted by R_{DS} as shown in Fig. 4.2.4(b). Consider two points P and Q within the channel such that P is near to the drain and Q is near to the source end. Let V_p and V_Q be the voltage drops at these points. Since, P is at a higher potential than point Q, that is $V_p > V_Q$. Hence gate is more negative at various points along the channel which are nearer to drain. Because of this reason *depletion regions penetrate more deeply into channel at points closer to drain than at points closer to source*.

- (ii) With further increase in drain voltage, the negative plate of battery V_{DS} repels the electrons to flow from the source to drain and hence results the increase in drain current.

CASE 2 (When $V_{GS} = 0$ and Large V_{DS}): If V_{DS} is furtherly increased then at some situation depletion regions comes very closer such that the drain current becomes pinched off as shown in Fig. 4.2.5. At this condition the drain current maintains a constant value (saturation value) called as drain saturation current, denoted by I_{DSS} .

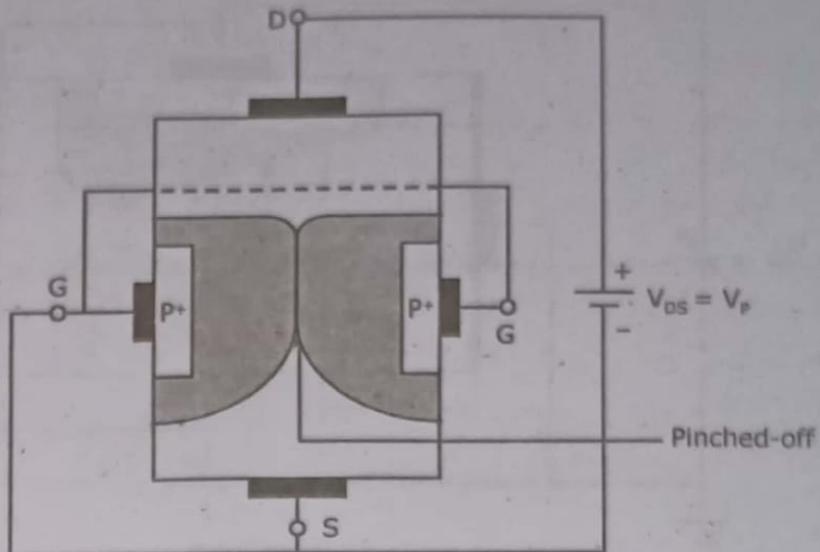


Fig. 4.2.5 JFET at Pinch-off Condition

CASE 3 (When $V_{GS} < 0V$ and V_{DS} Applied) : Let us now consider a case with gate regions are reverse biased by applying a various negative potentials V_{GS} between gate and source terminals.

When V_{GS} applied, the pinch-off condition will occur for smaller values of $|V_{DS}|$ and the maximum drain current will be smaller than at $V_{GS} = 0V$. The minimum value of V_{GS} at which drain-current reaches cut-off is called as *cut-off voltage* ($V_{GS,OFF}$). Since the negative gate voltage controls the flow of drain current, hence the FET is called as *voltage controlled device*.

(2) Why channel does not completely come closer at drain region.

Let us assume that channel becomes closed at pinch-off condition. If it so then there will be no drain current from drain to source and hence there will be no voltage drops along the length of channel since there is no voltage drops, the wedge-shape depletion region will now become rectangular shaped. Hence the channel will be opened and the drain current will flow, which is contradiction to our assumptions. Hence at pinch-off condition, channel will almost come closer such that is allows a constant value of drain current.

4.2.3 Pinch-off Voltage

The minimum gate reverse voltage (V_{GS}) required to remove all the free charge carriers from the channel is known as the *pinch-off voltage* and is denoted by V_p .

Expression For Pinch-off Voltage : We now derive an expression for pinch-off voltage that removes all the charge carriers using J-FET physical structure as shown in Fig. 4.2.6,

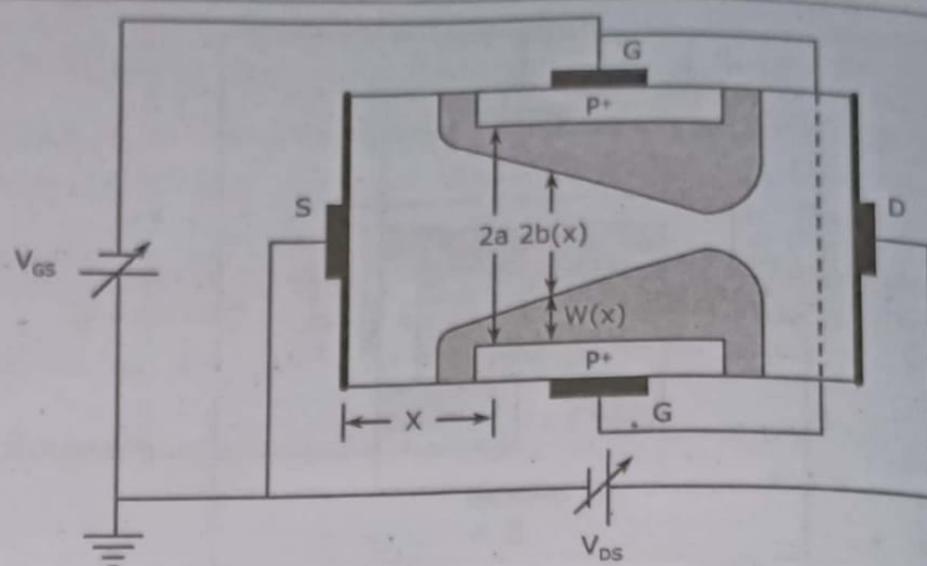


Fig. 4.2.6 Non-Uniform Construction of the Channel

Assume that P-type material doped with acceptors (N_A) is much greater than n-type material doped with donor atoms (N_D) i.e., $N_A \gg N_D$. If $N_A \gg N_D$ then $W_p \ll W_n$ and space - charge width $W_n(x) = W(x)$ at a distance 'X' along the channel.

Mathematically, space charge width is expressed as,

$$W(x) = a - b(x)$$

$$= \left[\frac{2 \epsilon}{qN_D} (V_0 - V(x)) \right]^{1/2} \quad \dots (4.2.1)$$

Where,

ϵ = Dielectric constant of channel material.

q = magnitude of electric charge.

V_0 = Junction contact potential at x.

$V(x)$ = Applied potential across space charge region at x and is a negative number for an applied reverse bias,

$a - b(x)$ = Penetration $w(x)$ of depletion region into channel at a point x along channel.

For drain current, $I_D = 0$, both $b(x)$ and $V(x)$ are independent of distance, x, so $b(x) = b$. Assume that $|V_0| \ll |V|$ and for pinch-off condition, substitute $b(x) = b = 0$. Substituting $b=0$, and ignoring contact potential V_0 , we get an expression for pinch-off voltage, V_p which removes all the free charge carriers from the channel as,

$$|V_p| = \frac{qN_D}{2\epsilon} a^2 \quad \dots (4.2.2)$$

Gate-to-source voltage is given as, $V_{GS} = V_0 - V(x)$

On substituting $b(x) = b$, $V_0 - V(x) = V_{GS}$ in Eq. (4.2.1),

$$\text{We have, } a - b = \left[\frac{2 \epsilon}{qN_D} (V_{GS}) \right]^{1/2}$$

$$\Rightarrow \frac{2 \epsilon}{qN_D} (V_{GS}) = (a - b)^2$$

$$\Rightarrow \frac{a^2}{|V_p|} (V_{GS}) = (a - b)^2 \quad \left(\because \text{From Eq. (4.2.2), } \frac{2 \epsilon}{qN_D} = \frac{a^2}{|V_p|} \right)$$

$$\Rightarrow V_{GS} = |V_p| \left(\frac{a - b}{a} \right)^2$$

$$V_{GS} = |V_p| \left[1 - \frac{b}{a} \right]^2$$

... (4.2.3)

It is to be noted here that V_{GS} represents the reverse bias across gate junction and is independent of distance along the channel if $I_D = 0$.

Note,

$$\begin{aligned} \epsilon &= 12 \epsilon_0 \text{ for Si} \\ \epsilon &= 16 \epsilon_0 \text{ for Ge} \end{aligned}$$

EXAMPLE PROBLEM 1

An n-channel silicon (dielectric constant = 12) FET with a channel width $a = 3 \times 10^{-6} \text{ m}$ is doped with 10^{21} electrons / m^3 . Determine the pinch-off voltage.

SOLUTION

Given Data : Dielectric constant (ϵ_r) = 12

Channel width (a) = $3 \times 10^{-6} \text{ m}$

Doping concentration (N_D) = 10^{21} electrons/ m^3 .

Given n-channel silicon, so

$$\epsilon = 12 \epsilon_0$$

$$= 12 \times 8.85 \times 10^{-12} \text{ F/m}$$

$$= 106.2 \times 10^{-12} \text{ F/m}$$

From Eq. (4.2.2), we have Pinch-off voltage as,

$$\begin{aligned} V_p &= \frac{qa^2N_D}{2\epsilon} \\ \Rightarrow V_p &= \frac{1.6 \times 10^{-19} \times (3 \times 10^{-6})^2 \times 10^{21}}{2 \times 106.2 \times 10^{-12}} \\ \Rightarrow V_p &= \frac{1.6 \times 9 \times 10^2}{212.4} \\ &= \frac{1440}{212.4} \\ &= 6.8 \text{ V} \end{aligned}$$

EXAMPLE PROBLEM 2

For an n-channel silicon FET with $a = 3 \times 10^{-4} \text{ cm}$ and $N_D = 10^{15} \text{ electrons/cm}^3$, find

(a) The pinch-off voltage and

(b) The channel half-width for $V_{GS} = \frac{1}{2} V_p$ and $I_D = 0$

SOLUTION

Given Data : $a = 3 \times 10^{-4} \text{ cm}$

$$N_D = 10^{15} \text{ electrons/cm}^3$$

$$V_{GS} = \frac{1}{2} V_p$$

$$I_D = 0$$

(a) Given N-channel silicon JFET, So,

$$\begin{aligned} \epsilon &= \epsilon_0 \epsilon_r \\ &= 12\epsilon_0 = 12 \times 8.85 \times 10^{-12} \\ &= 106.2 \times 10^{-12} \text{ F/m} \end{aligned}$$

Also given doping concentration,

$$\begin{aligned} N_D &= 10^{15} \text{ electrons/cm}^3 \\ &= 10^{21} \text{ electrons}/(10^{-2}\text{m})^3 = 10^{21} \text{ electrons m}^3. \end{aligned}$$

From the Eq. (4.2.2), we have pinch voltage given by,

$$\begin{aligned} |V_p| &= \frac{qN_D}{2\epsilon} a^2 \\ \Rightarrow |V_p| &= \frac{1.60 \times 10^{-19} \times 10^{21} \times (3 \times 10^{-6})^2}{2 \times 106.2 \times 10^{-12}} = \frac{14.4 \times 10^2}{212.4} = 6.8 \text{ V} \end{aligned}$$

Junction-Field Effect Transistor (JFET) [Unit - II, Ch. - 4]

(b) From Eq. (4.2.3), we have, gate-source voltage V_{GS} given by,

$$V_{GS} = \left(1 - \frac{b}{a}\right)^2 |V_p|$$

Solving for b , we get,

$$b = a \left[1 - \left(\frac{V_{GS}}{V_p} \right)^{\frac{1}{2}} \right]$$

Substituting the approximate given values,

$$\text{We get, } b = (3 \times 10^4) \left[1 - \left(\frac{1}{2} \right)^{\frac{1}{2}} \right]$$

$$= 0.87 \times 10^{-4} \text{ cm}$$

4.3 JFET PARAMETERS (OR) CHARACTERISTIC PARAMETERS OF JFET

In order to determine the performance of the JFET, there are certain characteristics described below which are known as JFET parameters.

4.3.1 A.C Drain Resistance

A.C. drain resistance of a FET (r_d) is defined as, the ratio of the change in drain-source voltage (ΔV_{DS}) to the change in drain current (ΔI_D) at constant gate-source voltage (V_{GS}).

That is,

$$r_d = \left. \frac{\Delta V_{DS}}{\Delta I_D} \right|_{V_{GS} = \text{Constant}}$$

... (4.3.1)

4.3.2 Transconductance

FET has transconductance which determines the control that the gate-source voltage (V_{GS}) has over the drain current (I_D). The prefix "trans" reveals that it establishes a relationship between an output and input quality. The root word "conductance" was chosen because g_m is determined by a voltage-to-current ratio similar to the ratio that

defines the conductance of a resistor $G = \frac{1}{R} = \frac{I}{V}$. It may be defined as,

The ratio of change in drain current (ΔI_D) to the change in gate-source voltage (ΔV_{GS}) at constant drain source voltage (V_{DS}) i.e.

$$g_m = \left. \frac{\Delta I_D}{\Delta V_{GS}} \right|_{V_{DS} = \text{Constant}}$$

... (4.3.2)

We have Schokley's equation as,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \quad \dots (4.3.3)$$

Differentiating Eq. (4.3.3) with respect to V_{GS} , we get,

$$\frac{\partial I_D}{\partial V_{GS}} = I_{DSS} \times 2 \left[1 - \frac{V_{GS}}{V_P} \right] \left[-\frac{1}{V_P} \right]$$

We know that,

$$g_m = \left[\frac{\partial I_D}{\partial V_{GS}} \right]_{V_{DS} = \text{constant}} \Rightarrow g_m = -\frac{2I_{DSS}}{V_P} \left(1 - \frac{V_{GS}}{V_P} \right) \quad \dots (4.3.4)$$

Now from Eq. (4.3.3), we have,

$$\left[1 - \frac{V_{GS}}{V_P} \right] = \sqrt{\frac{I_D}{I_{DSS}}} \quad \dots (4.3.5)$$

Using Eq. (4.3.5) in Eq. (4.3.4), we have,

$$g_m = \frac{-2\sqrt{I_D I_{DSS}}}{V_P} \quad \dots (4.3.6)$$

Suppose $g_m = g_{m0}$ when $V_{GS} = 0$, then from Eq. (4.3.3), $I_D = I_{DSS}$. Thus,

$$g_{m0} = -\frac{2I_{DSS}}{V_P} \quad \dots (4.3.7)$$

Where g_{m0} indicates the transconductance when gate-to-source voltage is zero.

Using Eq. (4.3.7) in Eq. (4.3.4), we get transconductance as,

$$g_m = g_{m0} \left[1 - \frac{V_{GS}}{V_P} \right] \quad \dots (4.3.8)$$

Eq. (4.3.6) shows that g_m varies as the square root of the drain current I_D , and Eq. 4.3.8) shows that g_m decreases linearly with increases of V_{GS} .

Slope of the Transfer Characteristic at I_{DSS} : From Eq. (4.3.6), we have transconductance given by,

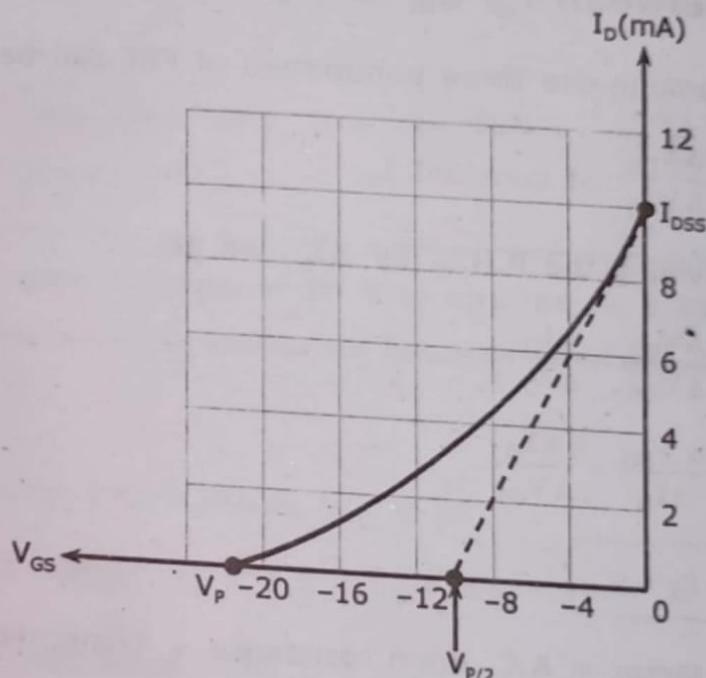
$$g_m = \frac{-2\sqrt{I_D I_{DSS}}}{V_p}$$

$$\frac{\partial I_D}{\partial V_{GS}} = \frac{-2\sqrt{I_D I_{DSS}}}{V_p}$$

Substituting $I_D = I_{DSS}$, we have,

$$\frac{\partial I_D}{\partial V_{GS}} = -\frac{2I_{DSS}}{V_p} = \frac{I_{DSS}}{-\frac{V_p}{2}}$$

This equation shows that the tangent to the curve at $I_D = I_{DSS}$ and $V_{GS} = 0$, will have an intercept at $-\frac{V_p}{2}$ on the axis of V_{GS} . Therefore, the value of V_p can be found by drawing the tangent at $I_D = I_{DSS}$ and $V_{GS} = 0$.



The gate source cut off voltage, $V_{GS(off)}$, on the transfer characteristics is equal to the pinch-off voltage, V_p , on the drain characteristics, i.e. $V_p = |V_{GS(off)}|$.

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(off)}} \right]^2$$

Transconductance is usually expressed either in mA/volt or micromhos (or) millisiemens.

4.3.3 Amplification Factor (μ)

The amplification factor (μ) of FET may be defined as the ratio of change in drain-source voltage (ΔV_{DS}) to the change in gate-source voltage (ΔV_{GS}) at constant drain current (I_D) i.e.,

$$\mu = \left. \frac{\Delta V_{DS}}{\Delta V_{GS}} \right|_{I_D = \text{Constant}} \quad \dots (4.3.9)$$

Amplification factor has no unit, it is just a number. It indicates how much more control the gate voltage have over drain current than has the drain voltage.

For instance, if the amplification factor of a FET is 90, it indicates that gate voltage is 90 times as effective as the drain voltage in controlling the drain current in the given FET.

4.3.4 Relation Between r_d , g_m and μ

The relationship among the three parameters of FET can be established as under,

We know, $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$ at constant I_D

Multiplying and dividing the R.H.S. by ΔI_D , we get,

$$\begin{aligned} \mu &= \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D} \\ &= \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}} \\ \therefore \mu &= r_d \times g_m \end{aligned} \quad \dots (4.3.10)$$

i.e., amplification factor = A.C. drain resistance \times transconductance.

4.3.5 Power Dissipation

The continuous power dissipation P_D of the FET is the product of drain current I_D and drain source voltage (V_{DS}).

\therefore Power dissipation,

$$P_D = \Delta I_D \times \Delta V_{DS} \quad \dots (4.3.11)$$

EXAMPLE PROBLEM 1

Show that if $|V_{GS}| \ll |V_p|$, then drain current can be approximated as $I_D = I_{DSS} - g_{m0} V_{GS}$

V_{GS}

SOLUTION

$$\text{Given that, } I_D = I_{DSS} - g_{m0} V_{GS}$$

Using Schokley's equation for N-channel,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

$$\Rightarrow I_D = I_{DSS} \left[1 - 2 \frac{V_{GS}}{V_p} + \left(\frac{V_{GS}}{V_p} \right)^2 \right]$$

Solving given $|V_{GS}| \ll |V_p|$, hence neglecting the square term, we get,

$$I_D = I_{DSS} - \frac{2I_{DSS} V_{GS}}{V_p}$$

$$I_D = I_{DSS} - g_{m0} V_{GS} \quad \left(\because g_{m0} = -\frac{2I_{DSS}}{V_p} \right)$$

EXAMPLE PROBLEM 2

When a reverse gate voltage of 20 V is applied to a FET, the gate current is $1.6 \times 10^{-3} \mu\text{A}$. Determine the resistance between gate and source.

SOLUTION

Given Data : Reverse gate voltage, $V_{GS} = 20 \text{ V}$

Gate current, $I_G = 1.6 \times 10^{-3} \text{ mA}$

$$\therefore \text{Gate to source resistance} = \frac{V_{GS}}{I_G} \quad [\because \text{From the def of A.C dynamic resistance}]$$

$$= \frac{20}{1.6 \times 10^{-3}} = 12.5 \times 10^9 \text{ ohms}$$

$$= 12500 \text{ M ohm}$$

It is seen from this example that a FET has high impedance (usually hundreds of megaohms) which permits high degree of isolation between the input and output.

EXAMPLE PROBLEM 3

Determine the transconductance of a FET if its amplification factor is 96 and drain resistance is 32 k Ω .

SOLUTION

Given Data : Amplification factor, (μ) = 96

Drain resistance, (r_d) = 32 k Ω = 32×10^3 Ω

From Eq. (4.3.10) Transconductance is given by,

$$\begin{aligned} g_m &= \frac{\mu}{r_d} \\ &= \frac{96}{32 \times 10^3} \\ &= 3 \times 10^{-3} \text{ mhos} \\ g_m &= 3000 \mu\text{S} \end{aligned}$$

EXAMPLE PROBLEM 4

The reading obtained experimentally from a JFET are as follows,

Table 4.3.1 JFET Parameters and Its Values

Drain-source voltage, (V_{DS}) in volts	5	12	12
Gate-source voltage, (V_{GS}) in volts	0	0	-0.25
Drain current, (I_D) in mA	8	8.2	7.5

Determine,

- (i) AC drain resistance.
- (ii) Transconductance.
- (iii) amplification factor.

SOLUTION

- (i) The drain current increases from 8.0 mA to 8.2 mA when drain-source voltage is increased from 5 V to 12 V, keeping gate-source voltage constant at 0 V.

∴ AC drain resistance,

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$$

$$\begin{aligned}
 &= \frac{(12 - 5)}{(8.2 - 8)} \\
 &= \frac{7}{0.2 \times 10^{-3}} \\
 &= 35 \text{ k}\Omega
 \end{aligned}$$

- (ii) The drain current changes from 8.2 mA to 7.5 mA when gate-source voltage is changed from 0 to -0.25 V, keeping drain-source voltage constant at 12 V.
- Transconductance,

$$\begin{aligned}
 g_m &= \frac{\Delta I_D}{\Delta V_{GS}} \\
 &= \frac{(7.5 - 8.2) \text{ mA}}{(-0.25 - 0) \text{ V}} \\
 &= 2.8 \text{ mA/V}
 \end{aligned}$$

- (iii) Amplification factor,

$$\begin{aligned}
 \mu &= r_d \times g_m \\
 &= 35 \times 1,000 \times 2.8 \times 10^{-3} \\
 &= 98
 \end{aligned}$$

4.4 THE JFET VOLT-AMPERE CHARACTERISTICS

Electrical characteristics of any device can be better understood with its V - I characteristics. There are two types of characteristics namely,

- (1) Drain (or) Output characteristics.
- (2) Transfer Characteristics.

4.4.1 Drain Characteristics

A curve drawn between drain current (I_D) and drain-source voltage (V_{DS}) of a FET at constant gate-source voltage (V_{GS}) is known as output or drain characteristic of FET.

The drain characteristics are divided into three regions,

- (1) Ohmic Region.
- (2) Pinch-off (or) Saturation Region.
- (3) Breakdown Region.

Let us now study the drain characteristics for the following two cases,

CASE I : Drain Characteristics with shorted Gate [$V_{GS} = 0$]

Fig. 4.4.2 shows the circuit arrangement to plot drain characteristics at $V_{GS} = 0$ V.

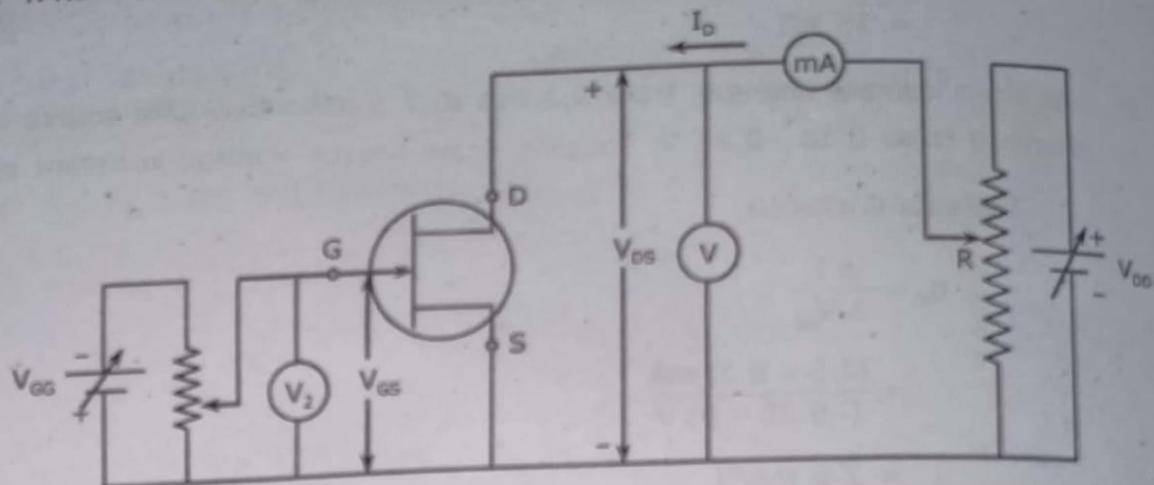


Fig. 4.4.1 Circuit Diagram for Determining Drain Characteristics with Shorted Gate for an N-Channel FET

Fig. 4.4.2 shows the drain characteristics N-channel JFET at $V_{GS} = 0$ V

(1) When $V_{GS} = 0$ and $V_{DS} = 0$

When $V_{DS} = 0$, there is no attracting potential at the drain and hence drain current $I_D = 0$, even though the channel between the gates is fully open (as $V_{GS} = 0$). This is shown by point 'O' in Fig. 4.4.2,

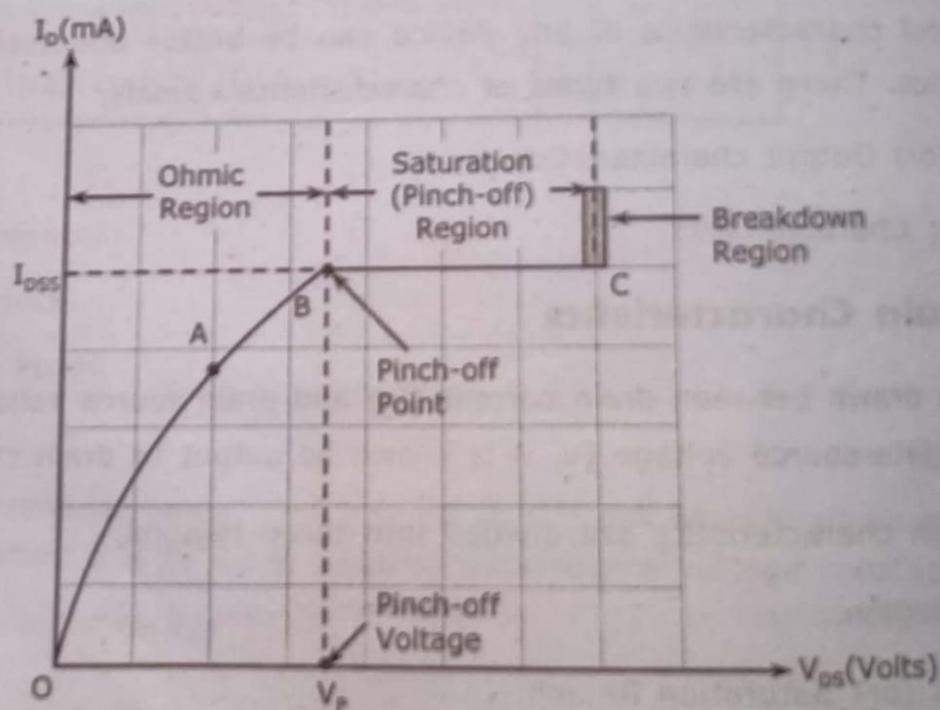


Fig. 4.4.2 Drain Characteristic on N-Channel JFET with $V_{GS} = 0$ V

(2) When $V_{GS} = 0$ and $V_{DS} > 0$

(i) **Ohmic Region :** As V_{DS} is increased, the electrons start flowing from source to drain terminals through channel between depletion layers and the drain current I_D increases linearly upto a point A (Knee point), as shown in Fig. 4.4.2. This shows that FET behaves like an ordinary resistor till point A is reached. The region from $V_{DS} = 0V$ to $V_{DS} = V_p$ is known as the *Ohmic Region*.

The FET resistance in the ohmic region is given by,

$$R_{DS} = \frac{V_p}{I_{DSS}}$$

Where,

V_p = Pinch-off voltage

I_{DSS} = Maximum drain current

The ratio $\frac{V_{DS}}{I_D}$ at the origin is called as the ON drain resistance i.e.

$$r_{ds(ON)} = \frac{1}{2aqN_d\mu} \left(\frac{L}{W} \right)$$

... (4.4.1)

Where,

$2a$ = Width of the channel

q = Charge of electron

N_d = Donar concentration

μ = Mobility of electron

L = Length of the channel.

As the voltage V_{DS} is progressively increased, the drain current I_D , from point A, increases at reverse square law rate upto point B which is called pinch - off point. The voltage corresponding to point B is known as pinch-off voltage and is denoted by V_p . At this voltage the channel is more or less blocked. Thus, pinch off voltage is defined as the minimum drain to source voltage where the drain current approaches a constant value (saturation value). Beyond pinch off voltage, the channel width cannot be reduced. Here it should be remembered that Pinch-off does not mean drain current I_D cut-off. Moreover the channel is not completely closed and hence I_D does not reduce to zero.

(2) **Pinch-off (or) Saturation Region :** As V_{DS} is further increased, the channel resistance also increases in such a way that I_D practically remains constant upto a point C. The region BC is known as saturation region or pinch-off region. In this region, a FET operates as a constant current device. In this region, drain current is related to gate-voltage by,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2 \quad \dots (4.4.2)$$

Where,

I_{DSS} = Drain saturation current when gate is shorted to source.

V_{GS} = Voltage between gate and source.

This above relation is known as Shockley's equation. The pinch off region is the normal operating region of JFET, when used as an amplifier.

(3) **Break - down Region :** With continue's increase of V_{DS} corresponding to point-C (called avalanche breakdown voltage V_A), eventually breakdown across the gate junction takes place and current I_D shoots to a high value. This happens because the reverse-biased P-N junction undergoes avalanche breakdown where a small change in V_{DS} produces a very large changes in I_D .

CASE II (Drain characteristics with external Bias (V_{GS})) : Fig. 4.4.3 shows the circuit arrangement to draw drain characteristics at various levels of negative bias voltage V_{GG} .

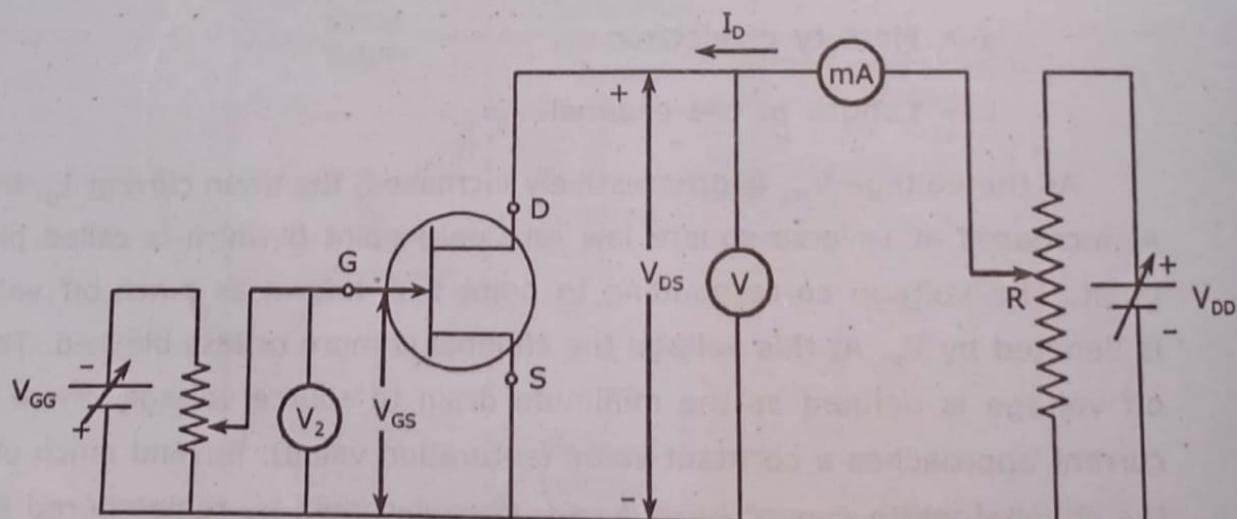


Fig. 4.4.3

Circuit Diagram for Determining Drain Characteristics with External Bias for An N-Channel JFET

Fig. 4.4.4 shows a family of I_D versus V_{DS} curves for different values of V_{GS} .

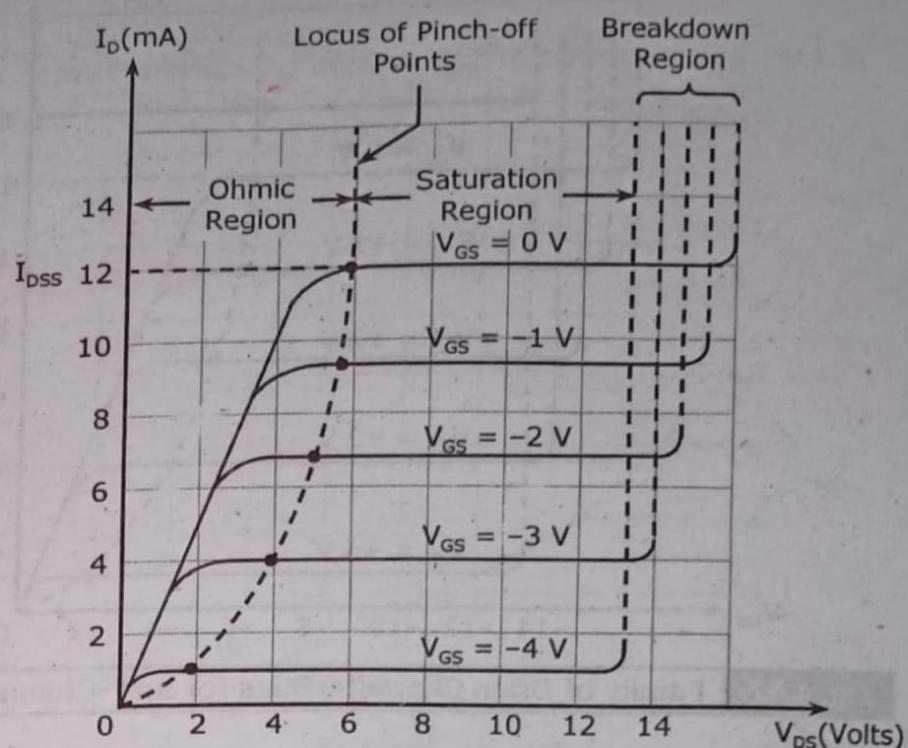


Fig. 4.4.4 I_D Vs V_{DS} Characteristics for an N-Channel JFET with Various Levels of V_{GS}

It is seen from Fig. 4.4.4 that as the negative gate bias voltage is increased, the resulting I_D vs V_{DS} curves are similar to the one for $V_{GS} = 0$ except for the following points,

- (i) The avalanche breakdown occurs at progressively lower values of V_{DS} . The reason is that the reverse bias gate voltage adds to the drain voltage thereby increasing the voltage effective across the gate junctions.
- (ii) The maximum saturation drain current reduces as the negative bias voltage increases.

(4) P-Channel JFET Characteristics : Fig. 4.4.5 shows the family of drain characteristics for P-channel JFET. Since in a P-channel FET, gate regions are heavily doped N^+ , hence to reverse bias these regions, we apply a positive gate-source voltage rather than negative gate-source voltage.

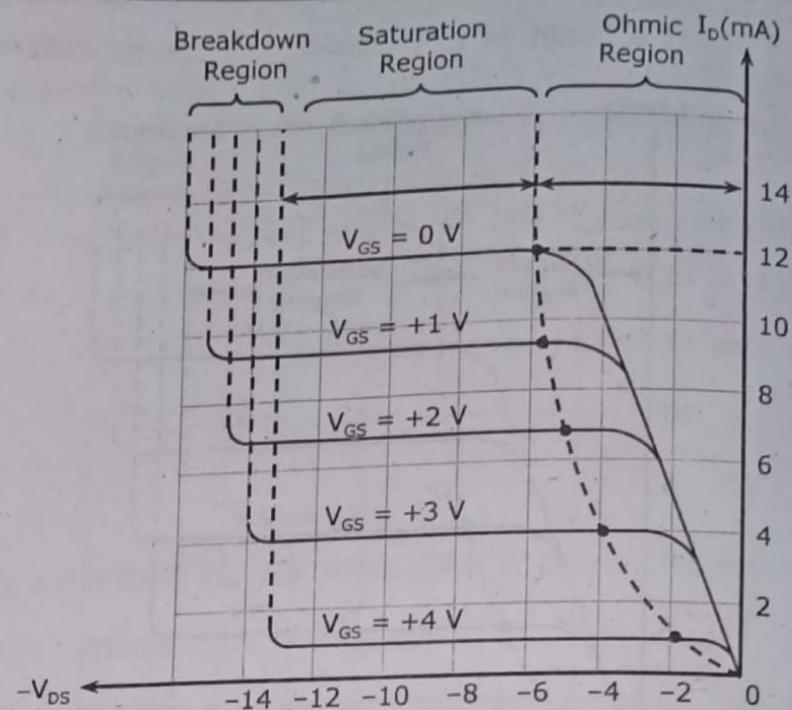


Fig. 4.4.5 Family of Drain Characteristics for an P-Channel JFET

4.4.2 Transfer Characteristics

The transfer characteristics is a plot of drain current I_{DS} , versus voltage between gate and source V_{GS} for a constant value of voltage between drain and source V_{DS} .

Fig. 4.4.6 shows the circuit arrangement to determine the transfer characteristics of N-channel JFET.

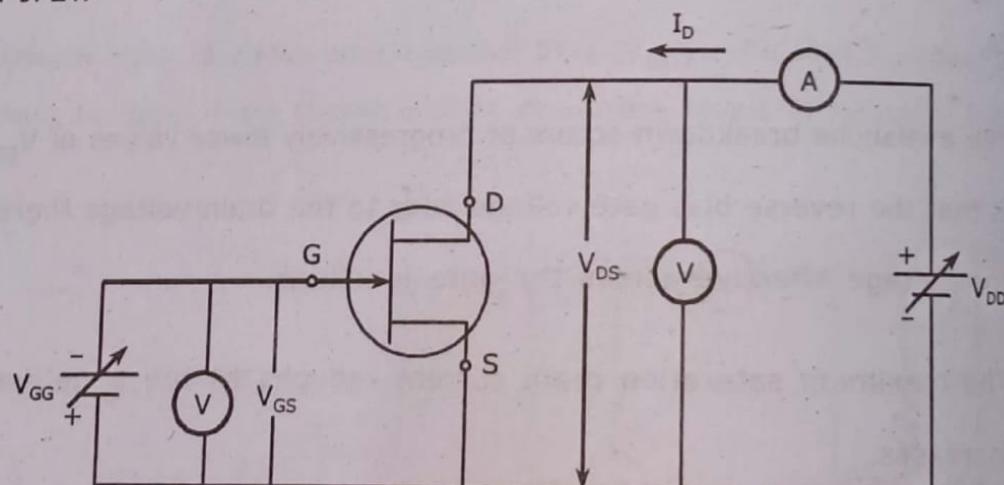


Fig. 4.4.6 Circuit Arrangement to Determine the Transfer Characteristics of N-Channel JFET

The shape of the transfer characteristic is very nearly a parabola because the relationship between drain current (I_D) and gate-to-source (V_{GS}) is non-linear as defined by Shockley's equation.

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

The transfer characteristics I_D versus V_{GS} is shown in Fig. 4.4.7.

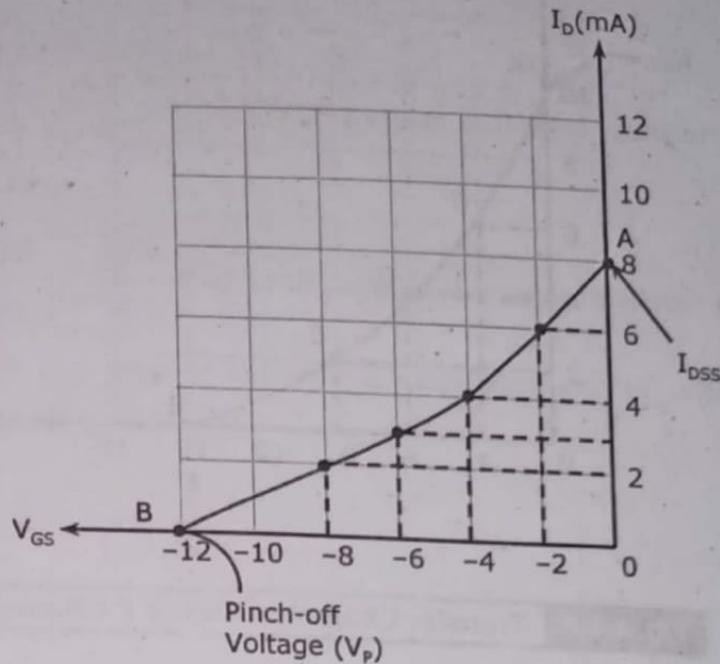


Fig. 4.4.7 Transfer characteristics of N-Channel JFET

Guidelines to Draw Transfer Characteristics : For a given values of I_{DSS} and V_P ,

STEP 1 : Mark point A and B as such,

When, $V_{GS} = 0$ then $I_D = I_{DSS}$

When, $I_D = 0$ then $V_{GS} = V_P$

STEP 2 : Using schockley's equation, obtain the values of drain current (I_D) for various values of V_{GS} and Mark all these points on the graph. Let the points obtained be C, D, E, F.

STEP 3 : Finally join the points A, B, C, D, E, F to get the transfer characteristics.

Transfer Characteristics of P-Channel JFET : It may be noticed that a P-channel JFET operates in the same way and have the similar characteristics as an N-channel JFET except that channel carriers are holes instead of electrons and the polarities of V_{GS} and V_{DS} are reversed. (i.e.),

$$I_D = I_{DSS} \left(1 + \frac{V_{GS}}{V_P} \right)^2 \quad \dots (4.4.3)$$

Fig. 4.4.8 shows the transfer characteristics of P-channel J-FET.

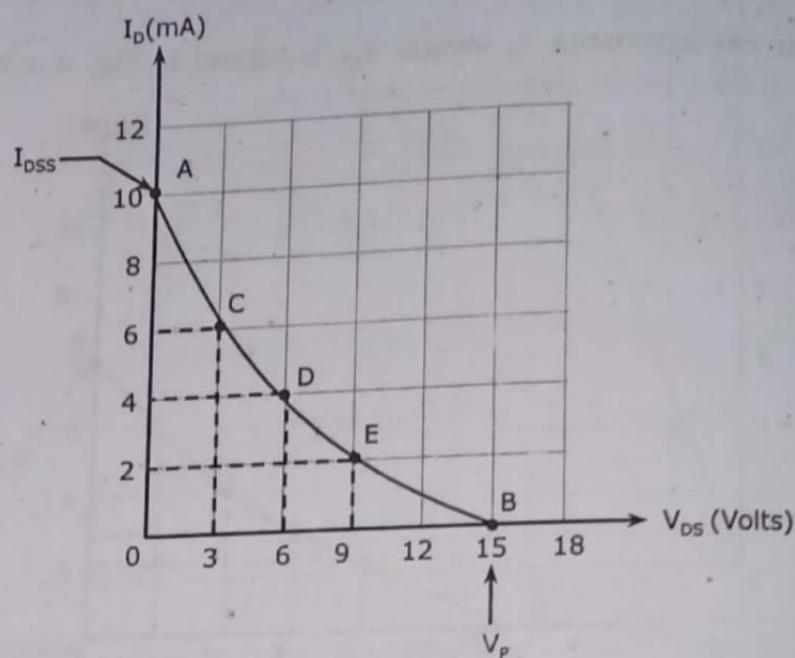


Fig. 4.4.8 Transfer Characteristics of P-Channel JFET

EXAMPLE PROBLEM 1

Sketch the transfer curve defined by $I_{DSS} = 10 \text{ mA}$ and $V_p = -4\text{V}$

SOLUTION

Given Data : $I_{DSS} = 10 \text{ mA}$

$$V_p = -4 \text{ V}$$

V_p value has - ve value hence the device is n-channel FET

STEP 1 : Mark points A and B

When $V_{GS} = 0\text{V}$ then $I_D = I_{DSS} = 10 \text{ mA}$; indicates a point A (0, 10 mA) on the Y-axis,

When $I_D = 0$ then $V_{GS} = V_p = -4 \text{ V}$; indicates a point B(-4V, 0) on X axis.

STEP 2 : Use Shockley's equation to obtain value of I_D for various values of V_{GS}

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$$

(i) When $V_{GS} = -2V$;

$$I_D = 10 \times 10^{-3} \left(1 - \frac{-2}{-4}\right)^2 = 0.25 \text{ mA which indicates another point C}(-2, 2.5)$$

(ii) When $V_{GS} = -3 V$;

$$I_D = 10 \times 10^{-3} \left(1 - \frac{-3}{-4}\right)^2 = 0.625 \text{ mA, which indicates another point D}(-3, 0.625)$$

(iii) When, $V_{GS} = -1 V$;

$$I_D = 10 \times 10^{-3} \left(1 - \frac{-1}{-4}\right)^2 = 6.625 \text{ mA, which indicates another point E}(-1, 5.625).$$

STEP 3 : Now with the help of the above calculated points, plot the characteristics graph, as shown in Fig. 4.4.9,

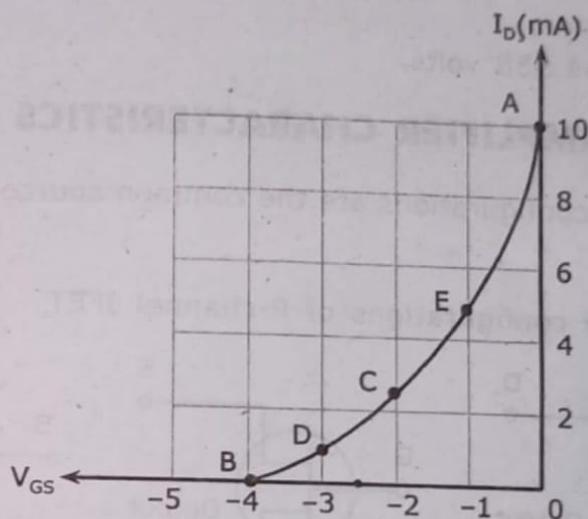


Fig. 4.4.9 Transfer Characteristics

EXAMPLE PROBLEM 2

The pinch-off voltage of a p-channel junction FET is $V_p = 5 V$ and the drain-to-source saturation current $I_{DSS} = -40 \text{ mA}$. The value of drain-source voltage V_{DS} is such that the transistor is operating in the saturated region. The drain current is given as $I_D = -15 \text{ mA}$. Find the gate-source voltage V_{GS} .

SOLUTION

Given Data : $V_p = 5 V$

$$I_{DSS} = -40 \text{ mA}$$

$$I_D = -15 \text{ mA}$$

It is found experimentally that a square-law characteristic closely approximates the drain current in saturation,

$$I_D = I_{DSS} \left(1 + \frac{V_{GS}}{V_P} \right)^2 \quad (\text{For P-channel})$$

$$\Rightarrow -15 \text{ mA} = -40 \text{ mA} \left(1 + \frac{V_{GS}}{5} \right)^2$$

$$\Rightarrow \sqrt{\frac{15}{40}} = 1 + \frac{V_{GS}}{5}$$

$$\Rightarrow 1 + \frac{V_{GS}}{5} = 0.612$$

$$\Rightarrow \frac{V_{GS}}{5} = 0.612 - 1 = -0.3876$$

$$\therefore V_{GS} = -1.938 \text{ volts.}$$

4.5 CS, CG, CD AMPLIFIER CHARACTERISTICS

The three basic JFET configurations are the common source (CS), common Drain (CD) and Common Gate (CG).

Fig. 4.5.1 shows the configurations of P-channel JFET,

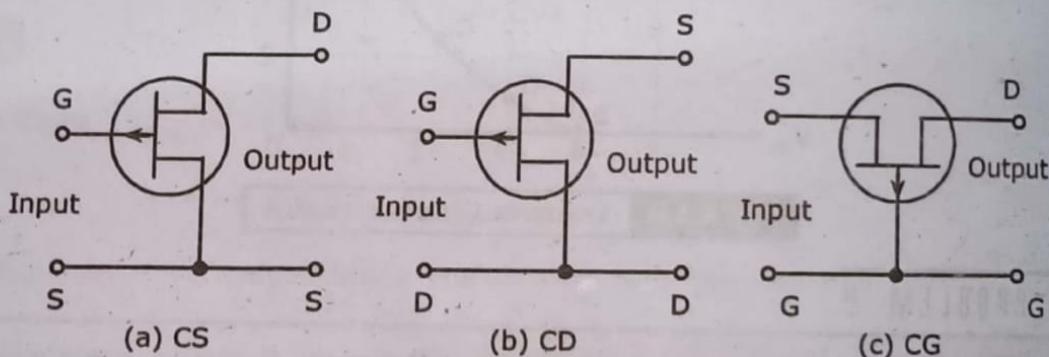


Fig. 4.5.1 | The Three FET Configurations

The CS amplifier provides good voltage amplification and this amplification is most frequently used. The CD amplifier is used as a buffer amplifier when it is having high input impedance and unity voltage gain. Finally, the CG amplifier is used as a high frequency amplifier.

4.5.1 Common Source Amplifier

Fig. 4.5.2(a) shows the basic configuration of CS amplifier and the small signal equivalent circuit of CS amplifier is shown in Fig. 4.5.2(b),

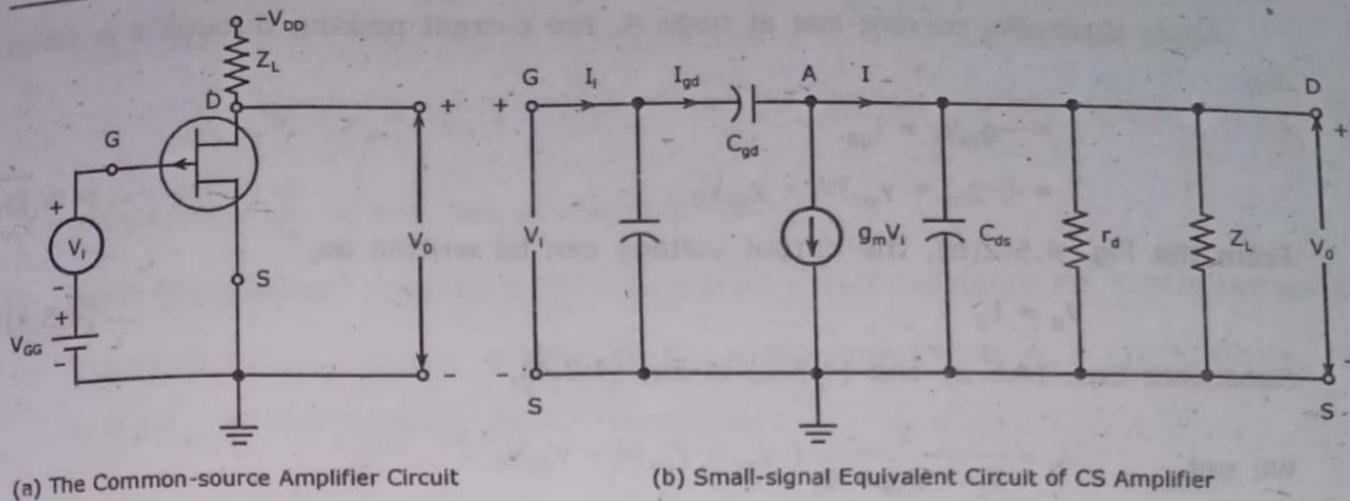


Fig. 4.5.2

By using the equivalent circuit of CS amplifier in Fig. 4.2.5(a), we can determine the voltage gain, input admittance, input capacitance and output resistance etc.

(1) **Voltage Gain (A_V)** : The gain of CS amplifier can be obtained as follows. In Fig. 4.5.2(b), the terms z_L , c_{ds} and r_d are the parallel combinations. These can be replaced by an impedance z between the terminals D and S.

Then, Z is given as,

$$Z = \frac{1}{Y_L + Y_{ds} + g_d} \quad \dots (4.5.1)$$

Where,

$$Y_L = \frac{1}{z_L} = \text{Admittance of } z_L.$$

$$Y_{ds} = j\omega C_{ds} = \text{Admittance of } C_{ds}.$$

$$g_d = \frac{1}{r_d} = \text{Conductance of } r_d.$$

In Fig. 4.5.2(a), the voltage across capacitor C_{gd} is $V_I - V_0$, since the voltages A and D terminals is same as output voltage V_0 . Thus, the current I_{gd} is passing through the gate-drain capacitor is given by,

$$I_{gd} = Y_{gd}(V_I - V_0) \quad \dots (4.5.2)$$

Where,

$$Y_{gd} = j\omega C_{gd} = \text{Admittance of } C_{gd}.$$

Apply Kirchoff's current law at node A, the current passing through z is given by,

$$\begin{aligned} I &= -g_m V_i + I_{gd} \\ &= (-g_m + y_{gd})V_i - y_{gd}V_0 \end{aligned} \quad \dots (4.5.3)$$

From the Fig. 4.5.2(b), the output voltage can be written as,

$$V_0 = I_z \quad \dots (4.5.4)$$

Substitute Eqs. (4.5.3) and (4.5.1) in Eq. (4.5.4),

$$\begin{aligned} \text{We get, } V_0 &= \frac{1}{y_L + y_{ds} + g_d} (-g_m + y_{gd})V_i - y_{gd}V_0 \\ &= \frac{(-g_m + y_{gd})V_i - y_{gd}V_0}{y_L + y_{ds} + g_d} \\ A_v &= \frac{V_0}{V_i} = \frac{-g_m + y_{gd}}{y_L + y_{ds} + y_{gd}V_0 + g_d} \end{aligned} \quad \dots (4.5.5)$$

At low frequencies, FET capacitance can be neglected, i.e., $y_{ds} = y_{gd} = 0$ and Eq. (4.5.5) can be written as,

$$\begin{aligned} A_v &= \frac{V_0}{V_i} \\ &= \frac{-g_m}{y_L + g_d} \\ &= \frac{-g_m Z_L}{1 + g_d Z_L} \\ &= -g_m Z_L \end{aligned} \quad \dots (4.5.6)$$

Where,

$$Z_L = R_d \parallel Z_L$$

- (2) **Input Admittance :** In Fig. 4.5.2(b), the current passed through C_{gs} is $I_{gs} = y_{gs}V_i$. Then, the total input current I_i can be written as,

$$\begin{aligned} I_i &= I_{gs} + I_{gd} \\ &= y_{gs}V_i + I_{gd} \\ &= y_{gs}V_i + y_{gd}(V_i - V_0) \quad (\because \text{From the Eq. (4.5.2)}) \end{aligned}$$

Where,

$$y_{gs} = j\omega C_{gs} = \text{Admittance of } C_{gs}$$

From the Fig. 4.5.2(b), the input admittance is $y_i = \frac{I}{V_i}$, we can write.

$$y_i = y_{gs} + y_{gd}(1 - A_v) \quad \dots (4.5.7)$$

Where, $A_v = \frac{V_o}{V_i}$ is the gain of the amplifier.

- (3) **Input Capacitance :** Consider a FET with a drain-circuit resistance R_d . Within the audio-frequency range, the gain is given by the simple expression $A_v = -g_m R'_d$, where, R'_d is $R_d || r_d$. In this case, Eq. (4.5.7) becomes,

$$\frac{Y_i}{j\omega} = C_i = C_{gs} + (1 + g_m R'_d) C_{gd} \quad \dots (4.5.8)$$

The input capacitance C_i increases over the capacitance from gate to source is caused by the Miller effect.

- (4) **Output Resistance :** The output resistance R_0 is given by the parallel combination of R_d and r_d ,

$$\text{i.e., } R_0 = \frac{r_d R_d}{r_d + R_d} \quad \dots (4.5.9)$$

Eq. (4.5.9) is valid at low frequencies, where the effect of capacitors in Fig. 4.5.2(b) is negligible and with a load resistance $Z_L = R_d$.

EXAMPLE PROBLEM 1

Consider the common-source amplifier circuit of Fig. 12.16(a). The FET used in the circuit has following parameter values, $g_m = 1.5 \text{ mA/V}$, $r_d = 150 \text{ k}$, $C_{gs} = 5 \text{ pF}$, $C_{gd} = 2 \text{ pF}$ and $C_{ds} = 0.8 \text{ pF}$. Assume $Z_L = 40 \text{ k}$.

- (a) Compute the voltage gain of the amplifier when V_i is a sinusoidal signal of frequency 1 kHz.
 (b) Repeat part (a) for signal frequency of 100 mHz.

SOLUTION

Given Data : $g_m = 1.5 \text{ mA/V}$

$$r_d = 150 \text{ k}$$

$$C_{gs} = 5 \text{ pF}$$

$$C_{gd} = 2 \text{ pF}$$

$$C_{ds} = 0.8 \text{ pF}$$

- (a) For the low signal frequency of 1 kHz, the effect of internal capacitances of the FET can be neglected and thus the gain of the amplifier can be obtained from Eq. (4.5.6) as,

$$\begin{aligned} A_V &= \frac{-g_m Z_L r_d}{r_d + Z_L} \\ &= -\frac{(1.5 \text{ mA/V}) \times 40 \text{ K} \times 150 \text{ K}}{150 \text{ K} + 40 \text{ K}} \\ &= -47.37 \end{aligned}$$

Note the negative sign indicates a phase shift of 180° of the output signal with respect to the input signal V_i .

- (b) For a signal frequency of 100 mHz, we obtain,

$$\begin{aligned} Y_L &= \frac{1}{40 \text{ K}} \\ &= 2.5 \times 10^{-5} \Omega^{-1} \\ &= 2.5 \times 10^{-5} \Omega^{-1} (\text{i.e., mho}) \end{aligned}$$

$$\begin{aligned} g_d &= \frac{1}{r_d} \\ &= \frac{1}{150 \text{ K}} \\ &= 6.67 \times 10^{-6} \Omega^{-1} \end{aligned}$$

$$\begin{aligned} Y_{gd} &= j2\pi f C_{gd} \\ &= j2\pi \times (100 \times 10^6 \text{ Hz}) \times 2 \times 10^{-12} \text{ F} \\ &= j0.0013 \Omega^{-1} \end{aligned}$$

$$\begin{aligned} Y_{ds} &= j2\pi f C_{ds} \\ &= j2\pi \times (100 \times 10^6 \text{ Hz}) \times 106 \text{ Hz} \times 0.8 \times 10^{-12} \text{ F} \\ &= j5.027 \times 10^{-4} \Omega^{-1} \end{aligned}$$

Using the above computed values of Y_L , g_d , Y_{gd} and Y_{ds} in Eq. (4.5.5), the voltage gain of the amplifier can be obtained as,

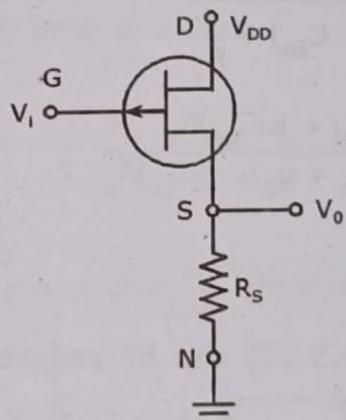
$$\begin{aligned} A_V &= \frac{-g_m + Y_{gd}}{Y_L + Y_{ds} + g_d + Y_{gd}} \\ &= \frac{-1.5 \times 10^{-3} (\text{A/V}) + j0.0013 \Omega^{-1}}{2.5 \times 10^{-5} \Omega^{-1} + j5.027 \times 10^{-4} \Omega^{-1} + 6.67 \times 10^{-6} \Omega^{-1} + j0.0013 \Omega^{-1}} \end{aligned}$$

$$\begin{aligned}
 &= \frac{-1.5 \times 10^{-3} + j0.0013}{3.16 \times 10^{-5} + j0.0018} \\
 &= 0.707 + j0.846 \\
 &= 1.103 \angle 0.874 \text{ rad}
 \end{aligned}$$

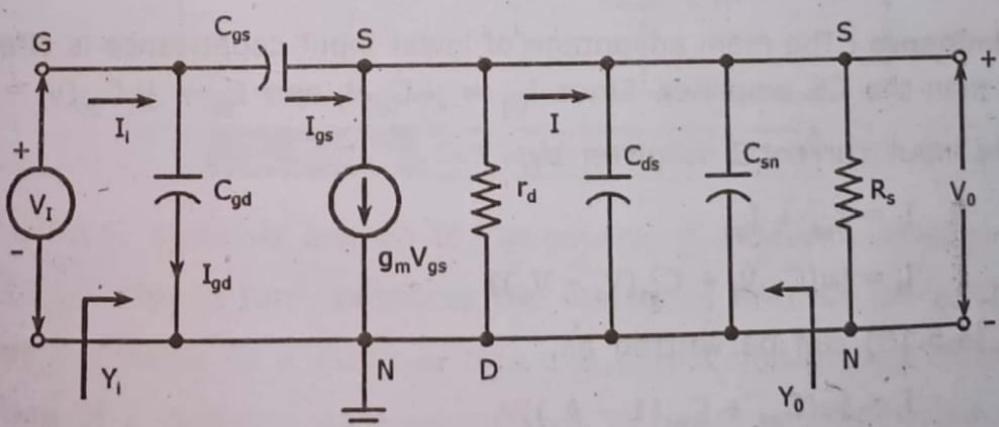
Note that gain is no longer a real quantity when the effects of interelectrode capacitances of the FET are taken into consideration. Further, the magnitude of the gain is drastically reduced at high frequencies due to the ac signal drops across the internal capacitances of FET. Moreover, the phase shift of the output signal is no longer fixed at 180° as in the case of low-frequency amplifier. Instead, the change in phase of the output signal is a function of the internal capacitances of the FET used in the amplifier circuit.

4.5.2 Common Drain Amplifier

The common drain amplifier is also known as source follower. The schematic circuit diagram of a common drain amplifier with drain resistance $R_d = 0$ is shown in Fig. 4.5.3(a) and Fig. 4.5.3(b) shows the equivalent circuit of common drain amplifier. As we observed in the Fig. 4.5.3(b), the additional capacitance C_{sn} is added in the equivalent circuit. Where, C_{sn} is the capacitance from source to ground.



(a) Schematic Diagram of a Common-drain (CD) (or) Source-follower Circuit



(b) Small-signal High-frequency Equivalent Circuit of the CD Amplifier

Fig. 4.5.3

(1) Voltage gain

$$A_v = \frac{V_o}{V_i}$$

As the A.C input voltage $V_i = V_{GS}$

The A.C. output voltage, is given by,

$$V_o = I_D \times (r_d || R_D)$$

$$= I_D \cdot \frac{r_d R_D}{r_d + R_D}$$

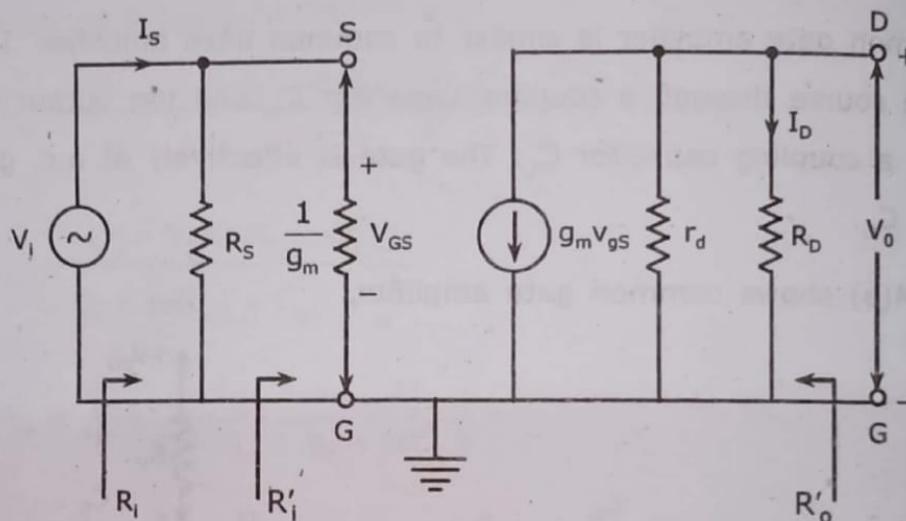


Fig. 4.5.4(b) A.C. Equivalent Circuit of Common Gate Amplifier

Substituting $I_D = g_m \cdot V_{GS} = g_m V_i$, we have,

$$A_v = \frac{V_o}{V_i} = \frac{g_m r_d R_D}{r_d + R_D}$$

$$A_v = \frac{\mu R_D}{r_d + R_D}$$

($\because \mu = g_m r_d$)

... (4.5.19)

It is same as the gain for a common source amplifier except that it is a positive quantity. It means that V_o and V_i are in phase as shown in Fig. 4.5.4(a).

(2) Input Resistance : Input resistance is defined as,

$$R_i = \frac{V_i}{I_i}$$

But, $V_i = V_{GS}$ and $I_i = I_S \approx I_D$.

Thus,

$$R_i = \frac{V_{GS}}{I_D} = \frac{V_{GS}}{g_m \cdot V_{GS}}$$

$$R_i = \frac{1}{g_m}$$

But from A.C. equivalent circuit shown in Fig. 4.5.4(b) it can be seen that R_s is parallel to R_i .

Hence the total input resistance of the amplifier is given as,

$$\frac{1}{R'_i} = \frac{1}{R_s} + g_m \quad \frac{1}{R'_i} = \frac{1 + g_m R_s}{R_s}$$

$$\therefore R'_i = \frac{R_s}{1 + g_m R_s} \quad \text{or} \quad R'_i = R_s \parallel \frac{1}{g_m}$$

If $R_s \gg \frac{1}{g_m}$, then $R'_i = R_s$... (4.5.20)

(3) **Output Resistance** : Output resistance is defined by,

$$R'_o = \frac{V_o}{I_o}$$

From Fig. 8.4.2, we have $V_o = I_D R_D$.

Thus, $R'_o = \frac{I_D \cdot R_D}{I_o}$

$$\therefore R'_o = R_D$$

... (4.5.21)

It implies that the output resistance of the CG amplifier is equal to the external drain resistance (R_D). If there is a load resistor (R_L) connected to the amplifier output, then the output resistance of the amplifier is,

$$R'_o = R_D \parallel R_L$$

EXAMPLE PROBLEM 1

The amplifier of Fig. 4.5.5 uses a FET with $I_{DSS} = 3 \text{ mA}$, $V_p = 2.4 \text{ V}$, $r_d \gg R_D$. Find the quiescent drain current, quiescent drain to source voltage, and small signal voltage gain A_v .

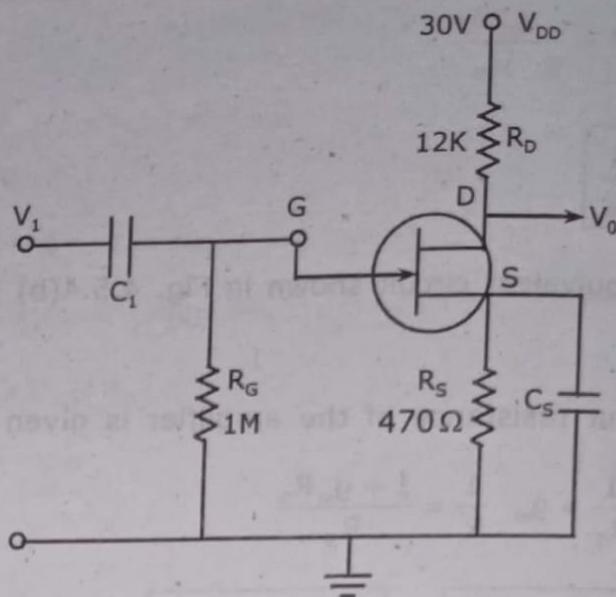


Fig. 4.5.5 FET Amplifier Circuit

SOLUTION

Given Data : $I_{DSS} = 3 \text{ mA}$

$$V_p = 2.4 \text{ V}$$

We have Schokley's equation as,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

$$\Rightarrow I_D = 3 \left(1 - \frac{-0.47 I_D}{-2.4} \right)^2$$

$$\Rightarrow \frac{1}{3} I_D = (1 - 0.1958 I_D)^2 = 1 - 0.3916 I_D + 0.3835 I_D^2$$

$$\Rightarrow 0.03835 I_D^2 - 0.7249 I_D + 1 = 0$$

$$\Rightarrow I_D = \frac{0.7249 \pm [0.5255 - 0.1534]^{1/2}}{2 \times 0.03834} = 1.496 \text{ mA} \approx 15 \text{ mA}$$

Drain voltage V_D is given by,

$$V_D = V_{DD} - I_D R_D = 30 - 1.5 \times 12 = 12 \text{ V}$$

Source voltage,

$$V_S = I_D R_S = 0.47 \times 1.5 = 0.7 \text{ V}$$

$$\Rightarrow V_{DS} = V_D - V_S = 12 - 0.7 = 11.3 \text{ V}$$

$$\therefore (I_{DQ}, V_{DSQ}) = (1.5 \text{ mA}, 11.3 \text{ V})$$

We have transconductance given by,

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_p} \right) = \frac{-2I_{DSS}}{V_p} \left(1 - \frac{V_{GS}}{V_p} \right)$$

$$\Rightarrow g_m = \frac{-2 \times 3}{-2.4} \left(1 - \frac{-0.7}{-2.4} \right) = 1.76 \text{ mA/V}$$

For a CS amplifier with bypassed resistance, we have voltage gain as,

$$\Rightarrow A_v = -g_m R_D = -1.76 \times 12 = -21.18.$$

EXAMPLE PROBLEM 2

In the common source amplifier, drain resistance $R_D = 10 \text{ k}\Omega$, amplification factor $\mu = 60$ and $r_d = 30 \text{ k}\Omega$. Find the voltage gain A_v and output resistance R_o .

SOLUTION

Given Data : Drain resistance, $R_D = 10 \text{ k}\Omega$

Amplification factor, $m = 60$

$r_d = 30 \text{ k}\Omega$

For a common source amplifier we have, voltage gain as,

$$A_v = \frac{V_o}{V_i} = \frac{-\mu R_D}{R_D + r_d}$$

$$\Rightarrow A_v = \frac{-60 \times 10 \times 10^3}{(10 + 30) \times 10^3} = -\frac{600}{40} = -15$$

Here, the negative sign indicates a 180° phase shift between V_i and V_o .

We have, output resistance as,

$$R_o = R_D \parallel r_d$$

$$\Rightarrow \frac{1}{R_o} = \frac{1}{R_D} + \frac{1}{r_d}$$

$$R_o = \frac{r_d R_D}{R_D + r_d}$$

$$= \frac{30 \times 10^3 \times 10 \times 10^3}{(10 + 30) \times 10^3}$$

$$= \frac{300 \times 10^3}{40}$$

$$= 7.5 \text{ k}\Omega$$

EXAMPLE PROBLEM 3

If the common-drain circuit uses a JFET having the following parameters, $r_d = 100 \text{ k}$, $g_m = 300 \text{ mS}$ and $R_s = 10 \text{ K}$ then calculate :

- (i) Voltage gain A_v .
- (ii) Total output resistance R_o .

SOLUTION

Given Data : $r_d = 100 \text{ k}$

$$g_m = 300 \text{ mS}$$

$$R_s = 10 \text{ k}$$

- (i) Voltage gain

$$\begin{aligned} A_v &= \frac{g_m r_d R_s}{r_d + R_s + g_m r_d R_s} \quad [\text{Using Eq. (8.3.1)}] \\ &= \frac{3600 \times 10^{-6} \times 100 \times 10^3 \times 10 \times 10^3}{(100 \times 10^3) + (10 \times 10^3) + (3000 \times 10^{-6} \times 100 \times 10^3 \times 10 \times 10^3)} \\ &= 0.965 \end{aligned}$$

- (ii) Output resistance

$$R_o = R_s \parallel \frac{r_d}{1 + g_m r_d}$$

Consider,

$$\frac{r_d}{1 + g_m r_d} = \frac{100 \times 10^3}{1 + 3000 \times 10^{-6} \times 100 \times 10^3} = 330 \Omega$$

$$\therefore R_o = 10 \text{ K} \parallel 330 \Omega$$

$$= \frac{10K \times 330}{10K + 330}$$

$$= 320 \Omega$$

EXAMPLE PROBLEM 4

The N-Channel JFET used in the source-follower circuit of Fig. 4.5.6 has $I_{DSS} = 16 \text{ mA}$, $V_p = -4 \text{ V}$ and $r_d = 40 \text{ k}\Omega$. The self-bias used gives $V_{GS} = -2.8 \text{ V}$. Calculate the voltage gain, the input resistance and the output resistance of the circuit.

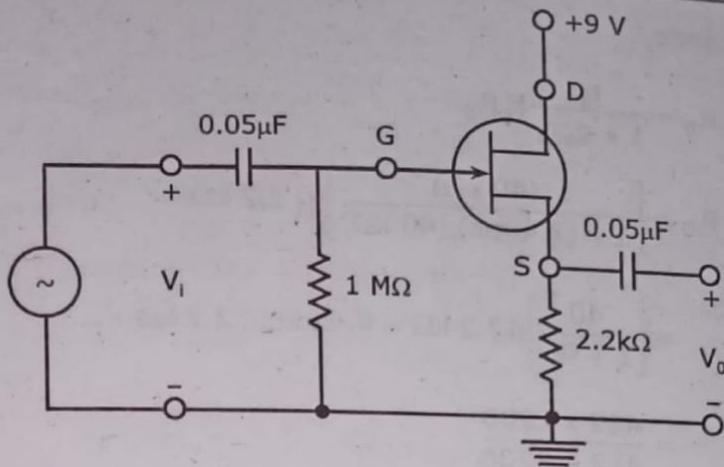


Fig. 4.5.6 Common Drain Amplifier Circuit Diagram

SOLUTIONGiven Data : $I_{DSS} = 16 \text{ mA}$

$$V_p = -4 \text{ V}$$

$$r_d = 40 \text{ k}\Omega$$

$$V_{GS} = -2.8 \text{ V}$$

Transconductance (g_{mo}),

$$g_{mo} = \frac{2I_{DSS}}{|V_p|} = \frac{2 \times (16 \text{ mA})}{|-4 \text{ V}|} = 8 \text{ mS}$$

Also we have, transconductance (g_m) related to g_{mo} by,

$$g_m = g_{mo} \left(1 - \frac{V_{GS}}{V_p}\right) = (8 \text{ mS}) \left(1 - \frac{-2.8 \text{ V}}{-4 \text{ V}}\right) = 2.4 \text{ mS}$$

$$\text{Consider, } r_d \parallel R_s = \frac{r_d \times R_s}{r_d + R_s} = \left(\frac{(2.2 \text{ k}\Omega) \times (40 \text{ k}\Omega)}{2.2 \text{ k}\Omega + 40 \text{ k}\Omega}\right) = 2.085 \text{ k}\Omega$$

Voltage gain of source follower is given by,

$$A_v = \frac{g_m(r_d \parallel R_s)}{[1 + g_m(r_d \parallel R_s)]} \quad [\text{Using (Eq. (8.3.2))}]$$

$$A_v = \frac{(2.4 \text{ ms})(2.085 \text{ k}\Omega)}{1 + (2.4 \text{ ms})(2.085 \text{ k}\Omega)} = \frac{5.004}{1 + 5.004} = 0.833$$

Input resistance,

$$R_i = R_g = 1 \text{ M}\Omega$$

Output resistance,

$$\begin{aligned}
 R_0 &= \frac{r_d}{1 + g_m r_d} \parallel R_s \\
 R_0 &= \left[\frac{(40 \text{ k}\Omega)}{1 + (2.4 \text{ ms}) (40 \text{ k}\Omega)} \right] \parallel 2.2 \text{ k}\Omega \\
 &= \left[\frac{40}{1 + 96} \right] \parallel 2.2 \text{ k}\Omega = 0.41 \text{ k}\Omega \parallel 2.2 \text{ k}\Omega \\
 &= \frac{412 \times 2200}{412 + 2200} \\
 &= 347 \text{ }\Omega
 \end{aligned}$$

EXAMPLE PROBLEM 5

In a JFET amplifier, $R_D = 12 \text{ k}\Omega$, $R_g = 1 \text{ M}\Omega$, $R_s = 1 \text{ k}\Omega$, $C_s = 25 \mu\text{F}$. No external load has been connected. The JFET has $\mu = 80$ and $r_d = 200 \text{ k}\Omega$. If the input signal voltage is 0.1 V at a frequency of 1 kHz, find the output signal voltage of the amplifier.

SOLUTION

Given Data : $R_D = 12 \text{ k}\Omega$

$R_g = 12 \text{ k}\Omega$

$R_s = 1 \text{ k}\Omega$

$C_s = 25 \mu\text{F}$

$\mu = 80$

$T_d = 200 \text{ k}\Omega$

$V_i = 0.1 \text{ V}$

The reactance of the bypass capacitor C_s is

$$\begin{aligned}
 X_{C_s} &= \frac{1}{2\pi f C_s} \\
 &= \frac{1}{2 \times 3.141 \times 1 \times 10^3 \times 25 \times 10^{-6}} \\
 &= 6.3 \text{ }\Omega
 \end{aligned}$$

This is much smaller than R_s . Thus, we can safely assume that R_s is completely bypassed. Now, the transconductance of the JFET is,

$$g_m = \frac{\mu}{r_d}$$

$$= \frac{80}{200 \times 10^3}$$

$$= 400 \mu\text{S}$$

Therefore, the magnitude of the voltage gain is,

$$A_v = g_m (r_d \parallel R_D)$$

$$= g_m \frac{r_d R_D}{r_d + R_D}$$

$$= 400 \mu\text{S} \times \frac{(200 \text{ k}\Omega) \times (12 \text{ k}\Omega)}{(200 \text{ k}\Omega + 12 \text{ k}\Omega)}$$

$$= 4.53$$

$$V_0 = A_v V_i = 4.53 \times 0.1 = 0.453 \text{ V}$$

EXAMPLE PROBLEM 6

Calculate the voltage gain of the FET amplifier circuit given in Fig. 4.5.7. The JFET has $I_{DSS} = 8 \text{ mA}$, $V_p = -4 \text{ V}$ and $r_d = 25 \text{ k}\Omega$, and is biased at $V_{GS} = -1.8 \text{ V}$.

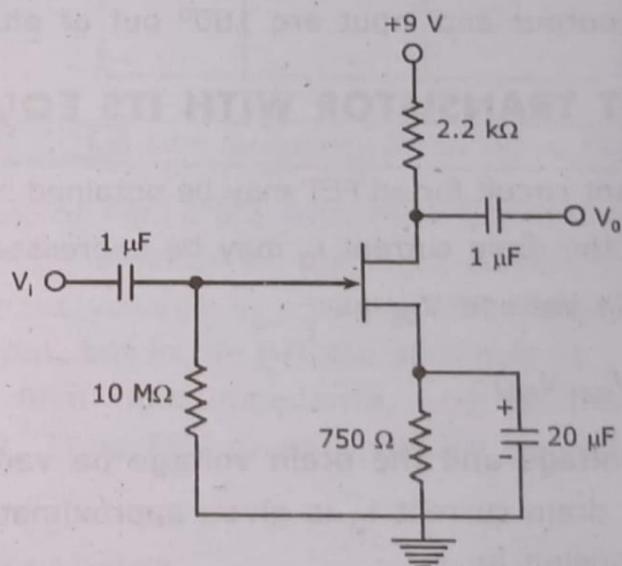


Fig. 4.5.7 FET Amplifier Circuit

SOLUTION

Given Data : $I_{DSS} = 8 \text{ mA}$

$V_p = -4 \text{ V}$

$r_d = 25 \text{ k}\Omega$

$V_{GS} = -1.8 \text{ V}$

We have g_{mo} given by,

$$\begin{aligned} g_{mo} &= \frac{2I_{DS}}{|V_p|} \\ &= \frac{2 \times 8 \times 10^{-3}}{|-4|} \\ &= 4 \text{ mS} \end{aligned}$$

We have gm related g_{mo} given by,

$$g_m = g_{mo} \left(1 - \frac{V_{GS}}{V_p}\right) = 4 \text{ mS} \left(1 - \frac{-1.8}{-4}\right) = 2.2 \text{ mS}$$

The voltage gain is $A_v = -g_m (r_d || R_D) = -2.2 \text{ mS} (2.2 \text{ k}\Omega || 25 \text{ k}\Omega)$

$$\begin{aligned} A_v &= -2.2 \text{ mS} \times \frac{(2.2 \text{ k}\Omega)(25 \text{ k}\Omega)}{(2.2 \text{ k}\Omega + 25 \text{ k}\Omega)} \\ &= -4.4 \end{aligned}$$

The minus sign indicates that the output voltage is inverted with respect to the input. That is, the output and input are 180° out of phase.

4.6 FIELD EFFECT TRANSISTOR WITH ITS EQUIVALENT CIRCUIT

Small signal equivalent circuit for an FET may be obtained in the same general manner as for a BJT. Accordingly the drain current i_D may be expressed as a function of the gate voltage V_{GS} and the drain voltage V_{DS} as

$$i_D = f(V_{GS}, V_{DS}) \quad \dots (4.6.1)$$

Let both the gate voltage and the drain voltage be variable. Then the increment Δi_D in the instantaneous drain current i_D is given approximately by the first two terms in the Taylor series expansion as,

$$\Delta i_D = \frac{\partial i_D}{\partial V_{GS}} \Bigg|_{V_{DS}} \cdot \Delta V_{GS} + \frac{\partial i_D}{\partial V_{DS}} \Bigg|_{V_{GS}} \cdot \Delta V_{DS} \quad \dots (4.6.2)$$

Using the conventional small signal notation, Δi_D , ΔV_{GS} and ΔV_{DS} may be replaced respectively by i_d , V_{gs} and V_{ds} . Hence Eq. (4.6.2) reduces as,

$$i_d = g_m V_{gs} + \frac{1}{r_d} \cdot V_{ds} \quad \dots (4.6.3)$$

Where,

$$g_m = \left. \frac{i_d}{V_{gs}} \right|_{V_{ds}} = \text{transconductance of the FET}$$

$$r_d = \left. \frac{V_{ds}}{i_d} \right|_{V_{gs}} = \text{dynamic drain resistance.}$$

Fig. 4.6.1. shows a circuit which satisfies Eq. (4.6.3) and thus, constitutes the low frequency small signal model of FET. The model given in Fig. 4.6.1 has a Norton's output voltage V_{GS} . The constant of proportionality is nothing but the transconductance g_m and the output resistance is nothing but the drain resistance r_d .

In the low frequency model shown in Fig. 4.6.1. The input resistance between the gate and source is infinite since reverse-biased gate current is assumed to be zero. Similarly the resistance between the gate and drain is infinite.

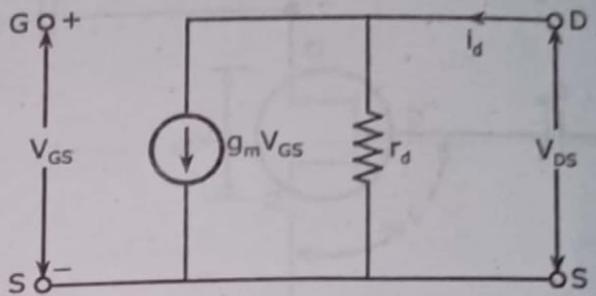


Fig. 4.6.1 Low Frequency Small Signal FET Model

Comparing the circuit of Fig. 4.6.1 with the CE hybrid model of the BJT, we see that the current source $h_{fe} i_b$ depends on the input current i_b while the current source $g_m V_{gs}$ depends on the input voltage V_{gs} . In the FET model, no feedback takes place from the output to the input, but in the BJT the parameter h_{re} provides such a feedback. Also the FET has a very high input impedance, whereas the input impedance of a CE amplifier is about $1\text{ k}\Omega$. Thus FET gives a better low frequency amplifier than a conventional BJT.

4.6.1 FET as an Amplifier

The FET amplifier circuit is shown in Fig. 4.6.2. The input signal is applied between gate - source terminals and the amplified output signal is obtained across the drain-source terminals. The gate-source circuit is always reverse biased due to which a depletion layer is formed which reduces the channel width.

When a weak input signal is applied across the gate and source, the reverse bias on the gate decreases during the positive half of the signal. This increases the channel width and hence the drain current I_D .

However, during the negative half of the signal, the reverse bias on the gate increases. This decreases the channel width and hence the drain current. Thus, a small change in gate voltage produces a large change in drain current. These large variations in drain current produce large output across the load R_L . Hence, it is seen that FET acts as an amplifier.

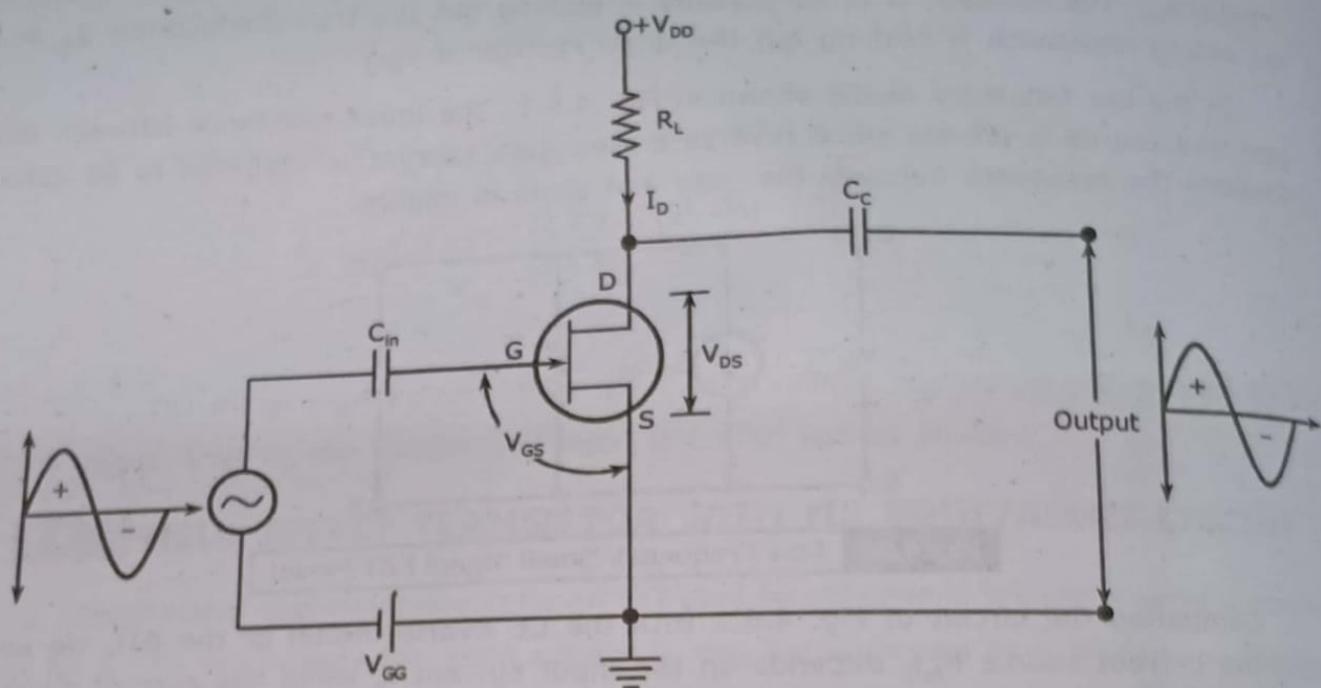


Fig. 4.6.2 FET Amplifier Circuit

Just as like BJT configurations (CE, CB and CC), FET also can be configured in three different configurations. They are,

- (1) Common source (CS) amplifier.
- (2) Common drain (CD) amplifier.
- (3) Common gate (CG) amplifier.

SMALL SIGNAL EQUIVALENT CIRCUITS FOR FETS.

Table 4.6.1 gives the small signal equivalent circuits for various FET configurations.

Table 4.6.1 Equivalent Circuits of a FET

Configuration	Circuit	Equivalent Circuit
Common source amplifier.		
Common drain amplifier.		
Common Gate Amplifier		

