VLSI Tute-1-Hax-1

① Threshold Voltage at zero-bias: when $V_{SB} = 0\ V$

$$\boxed{V_{TO} = \phi_{GC} - 2\phi_F - \frac{Q_{BO}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}}$$ unit = V

where: (i) $\phi_{GC} = \phi_F(\text{substrate}) - \phi(\text{Gate})$ unit V
↳ surface potential b/w Gate & Channel
(ii) ϕ_F = Fermi Potential unit V
(iii) Q_{BO} = Charge on body unit C/cm^2
(iv) Q_{ox} = " " oxide unit C/cm^2
(v) C_{ox} = oxide capacitance unit F/cm^2

② $$\boxed{\phi_F = \text{Fermi Potential} = \frac{KT}{q} \ln\left(\frac{n_i}{N_A}\right) = \frac{KT}{q} \ln\left(\frac{N_D}{n_i}\right)}$$

Imp. Common Bullshit	where:
(i) $\frac{KT}{q} = 0.026$ ↳ 1.6×10^{-19}	(i) $\frac{KT}{q} = 0.026$
(ii) $n_i = 1.45\times10^{10}$	(ii) K = Boltzman's const = 1.38×10^{-23}
(iii) $\epsilon_{si} = 11.7\epsilon_0 = 11.7\times8.85\times10^{-14}$	(iii) T = temp
(iv) $\epsilon_{ox} = 3.97\epsilon_0 = 3.97$ ↓ in cm	(iv) q = charge = $1.6\times10^{-19}\ C$
	(v) $n_i = 1.45\times10^{10}$ (always)
	(vi) N_D, N_A = Acceptor, Donor impurity density

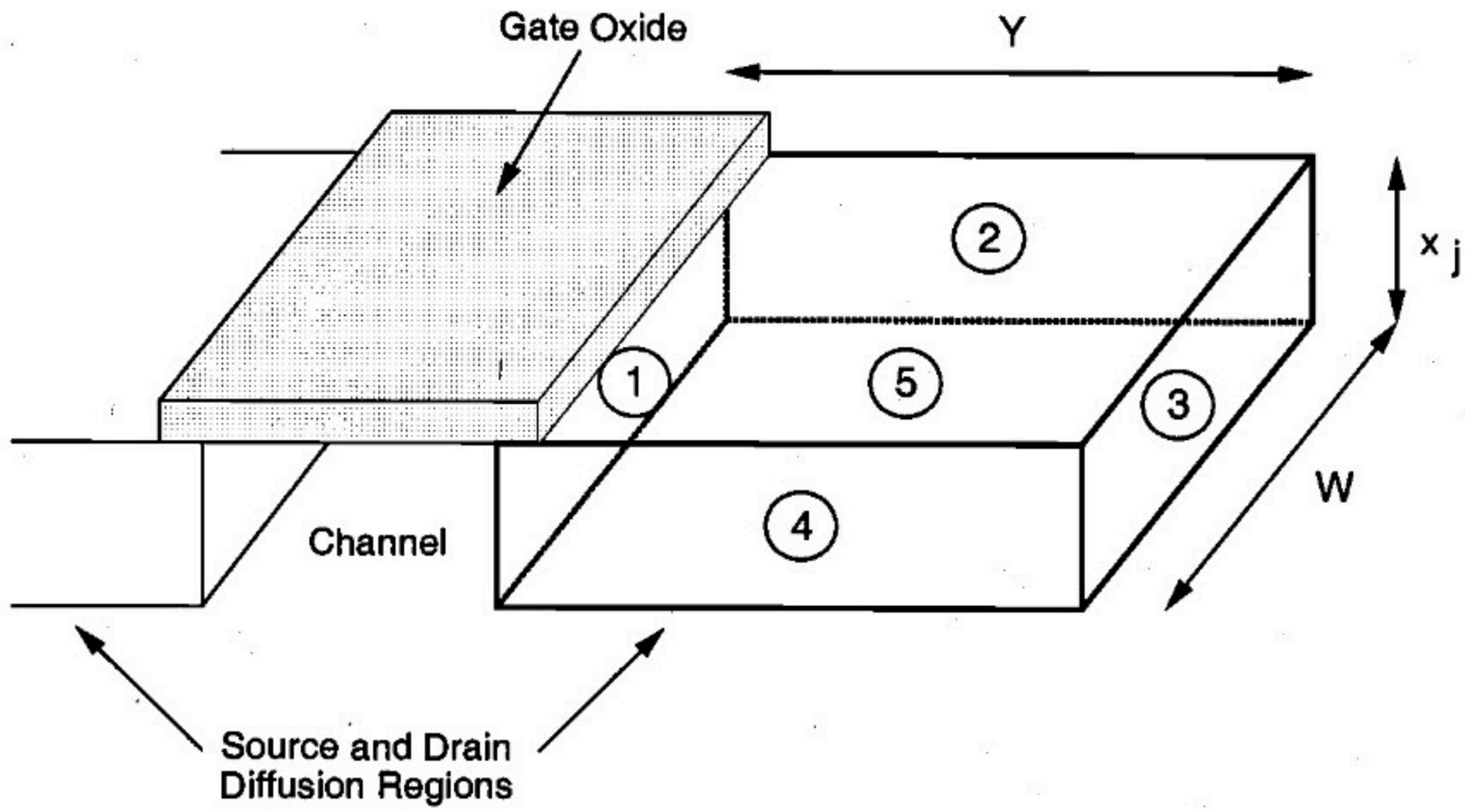
③ $$\boxed{Q_{BO} = \text{Charge on body} = -\sqrt{2qN_A\epsilon_{si}|-2\phi_F|} = -\sqrt{2qN_D\epsilon_{si}|-2\phi_F|}}$$

where: (i) $\epsilon_{si} = 11.7\epsilon_0 = 11.7\times8.85\times10^{-14}$
↳ in cm

④ $$\boxed{C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}} = \frac{3.97\epsilon_0}{t_{ox}}$$ → always same unit F/cm^2
↳ oxide thickness

⑤ $$\boxed{Q_{ox} = N_{ox}\, q}$$ unit C/cm^2

Spiral



Junction	Area	Type
1	$W \cdot x_j$	n^+/p
2	$Y \cdot x_j$	n^+/p^+
3	$W \cdot x_j$	n^+/p^+
4	$Y \cdot x_j$	n^+/p^+
5	$W \cdot Y$	n^+/p

VLSI – Tute – 2 – Max

① C_{jo} = zero bias Capacitance = $\sqrt{\frac{\epsilon_{si} q}{2} \frac{N_A N_D}{N_A + N_D}} \sqrt{\frac{1}{\phi_0}}$

② $\phi_0 = \frac{KT}{q} \ln \frac{N_A N_D}{n_i^2}$

⑦ $C_{jsw} = n_j C_{josw}$

③ $C_{josw} = \sqrt{\frac{\epsilon_{si} q}{2} \frac{N_A' N_D}{N_A + N_D}} \sqrt{\frac{1}{\phi_{osw}}}$

④ $\phi_{osw} = \frac{KT}{q} \ln \frac{N_A' N_D}{n_i^2}$

⇒ where N_A' represents "channel stop doping" OR "Side Wall doping"

⑤ $C_j(V) = \sqrt{\frac{\epsilon_{si} q}{2} \frac{N_A N_D}{N_A + N_D}} \sqrt{\frac{1}{\phi_0 - V}}$

⑥ $C_{jsw}(V) = \sqrt{\frac{\epsilon_{si} q}{2} \frac{N_A' N_D}{N_A + N_D}} \sqrt{\frac{1}{\phi_{osw} - V}}$

↳ ↳ Both same, just in terms of V

⑧ $C_{drain} = K_{eq} C_{jo} A + K_{eq}' C_{jsw} P$

where: A = Area of 1,5 = $WY + Wx_j$
P = " " 2,3,4 = $2(Yx_j) + Wx_j$ ⇒ Imp

⑨ $K_{eq} = \frac{-2\sqrt{\phi_0}}{V_2 - V_1} \left[\sqrt{\phi_0 - V_2} - \sqrt{\phi_0 - V_1} \right]$

where: if V goes higher to lower, ⇒ -ve values of V_1, V_2
" " " lower " higher ⇒ +ve " " " "

⑩ $K_{eq}' = \frac{-2\sqrt{\phi_{osw}}}{V_2 - V_1} \left[\sqrt{\phi_{osw} - V_2} - \sqrt{\phi_{osw} - V_1} \right]$

⑪ All C's unit ⇒ F/cm^2
ϕ ⇒ V
A, P ⇒ μm^2 of simply m^2

⑫ $C_g = C_{ox} W L$

VLSI - All - Formulae

$\epsilon_{Si} = 11.7 \times 8.85 \times 10^{-14}$ cm
$\epsilon_{ox} = 3.97 \times 8.85 \times 10^{-14}$
$q = 1.6 \times 10^{-19}$, $\frac{KT}{q} = 0.026$

① $V_{TO} = \phi_{GC} - 2\phi_F - \frac{Q_{BO}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \Rightarrow V$

② $\phi_{GC} = \phi_F(\text{sub}) - \phi_F(\text{gate}) \Rightarrow V$

③ $Q_{BO} = -\sqrt{2q\epsilon_{Si} N_A |-2\phi_F|}$ (NMOS) $= \sqrt{2q\epsilon_{Si} N_A |-2\phi_F|}$ (PMOS) $\Rightarrow C/cm^2$

④ $\phi_F = \frac{KT}{q} \ln\left(\frac{N_D}{n_i}\right) = \frac{KT}{q} \ln\left(\frac{n_i}{N_A}\right)$

⑤ Modes:

(i) Cutoff : $V_{GS} < V_T \Rightarrow I_D = 0$

(ii) Linear : $V_{DS} < V_{GS} - V_T$

$\Rightarrow I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \left[1 + \lambda V_{DS}\right]$

$V_T = V_{TO} + \gamma \left[\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}\right]$

(iii) Saturation : $V_{DS} \geq V_{GS} - V_T$

$\Rightarrow I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$

⑥ $C_{j0} = \sqrt{\frac{\epsilon_{Si} q}{2} \frac{N_A N_D}{n_i^2}} \sqrt{\frac{1}{\phi_0}}$

⑦ $C_{jsw} = \sqrt{\frac{\epsilon_{Si} q}{2} \frac{N_A' N_D}{n_i^2}} \sqrt{\frac{1}{\phi_{0sw}}}$

⑧ $C_{jsw} = n_j C_{j0sw}$

⑨ $K_{eq} = -\frac{2\sqrt{\phi_0}}{V_2 - V_1}\left(\sqrt{\phi_0 - V_2} - \sqrt{\phi_0 - V_1}\right)$

If V gas ↑ to ↓
⇒ take -ve value
If V gas ↓ to ↑
⇒ take +ve value

⑩ IMP

$N_I = \frac{C_{ox} \Delta V}{q}$

$A = WY + WX_j$
$P = 2(XY) + Wx_j$

$C_g = C_{ox} WL$

$\phi_0 = \frac{KT}{q} \ln \frac{N_A N_D}{n_i^2}$

$\phi_0 = \frac{KT}{q} \ln \frac{N_A' N_D}{n_i^2}$

Spiral

Tute - 4 - Max

① $$\tau_{PHL} = \frac{C_{load}}{k_n[V_{DD} - V_{T,n}]}\left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left[\frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1\right]\right]$$

② $$\tau_{PLH} = \frac{C_{load}}{k_p[V_{DD} - |V_{T,p}|]}\left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left[\frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1\right]\right]$$

③ $$\boxed{-I = C\frac{dV}{dt}}$$

if high to low V transition = Linear Region
" low " high " " = Saturation "

where: (i) $I(\text{linear}) = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n\left[2(V_{OH} - V_{Ton})V_{out} - V_{out}^2\right]$

(ii) $I(\text{sat}) = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n\left[(V_{in} - V_{T,n})^2\right]$

④ $$\boxed{\tau_{fall} = \frac{C\,\Delta V}{I_{avg}}}$$ fall time from avg curr method

$$I_{avg} = \frac{1}{2}\left[I(\text{sat}) + I(\text{lin})\right]$$

$$\Delta V = V_{out}(\text{sat}) - V_{out}(\text{lin})$$

⑥ Elmore: RC + R+RC ... + R(C+2C+3C)..
main branch:
↳ add R's mul. curr C
oth branch:
↳ first R. mult. addition of C's

⑤ Differential method:

$$\int_0^{t_{delay}} dt = \frac{-2C_{load}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n}\int_{\text{high value}}^{\text{low value}} \frac{1}{2(V_{OH} - V_{Ton})V_{out} - V_{out}^2}\,dV$$

$$t_{delay} = \frac{-2C_{load}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n(V_{OH} - V_{Ton})}\ln\left[\frac{V_{out}}{2(V_{OH} - V_{Ton})V_{out} - V_{out}^2}\right]\Bigg|_{\text{high value}}^{\text{low value}}$$

POSSESSION OF MOBILES IN EXAM IS UFM PRACTICE

Name Anurag Dwivedi Enrolment No. 9912270204 B

Jaypee Institute of Information Technology, Noida

Test-2 Examination, Even Semester-2024-25

B.Tech VI Semester

Course Title: VLSI DESIGN **Max.Time; 1 Hrs**

Course Code: 18B11EC315 **Max. Marks: 20**

CO1	Understand VLSI design flow, VLSI design styles, digital systems modeling using Verilog-HDL
CO2	Apply MOSFET models for circuits simulation and its effect on scaling.
CO3	Analyze the concepts of static and dynamic characteristic of MOS inverters, combinational and sequential circuits.
CO4	Explain and evaluate dynamic logic circuits, stick diagram, layout and different types of semiconductor memories.

Q1. Consider a resistive-load inverter circuit with VDD=5 V, $\mu_n C_{ox}$=20 $\mu A/V^2$, Vt0,n= 1V, R_L=200KΩ, and *W/L*=2. Compute V_{OL}, V_{IL} and Noise Margin (NM_L).[CO3 (Analyzing), Marks 5]

Q2.(a) Drive the expression for CMOS inverter threshold voltage (V_{TH}).

(b) Find V_{TH} of CMOS inverter if the ratio of (W/L)p/(W/L)n =1.392, and mobility are related as μ_n=2.2μ_p. Assume that Vton=0.6 V, Vtop= - 0.6 V, and power supply V_{DD} is 3 V.

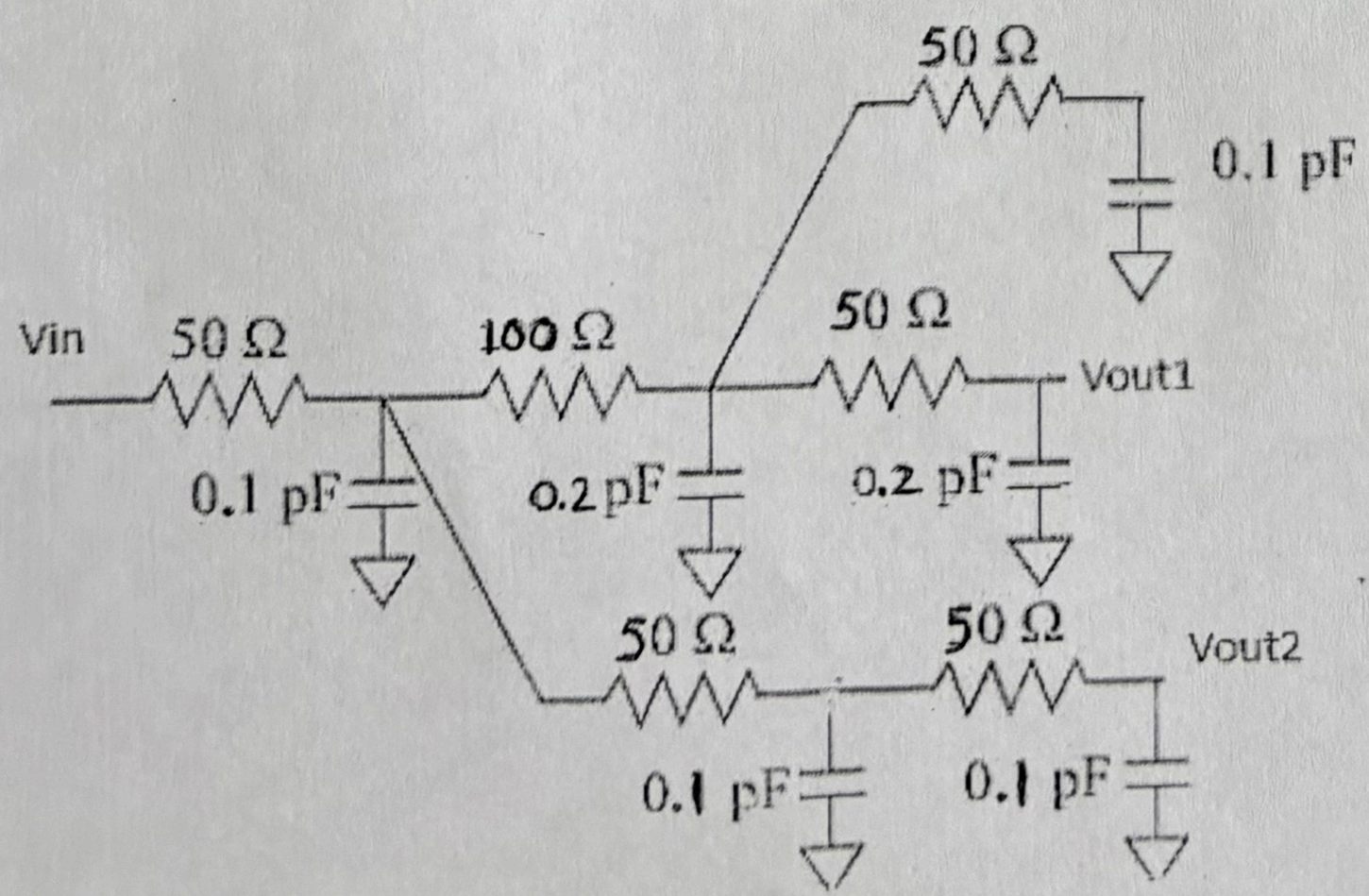
(c) If CMOS inverter discussed in part(b) is symmetrical, then find the ratio of (W/L)p and (W/L)n. [CO3 (Analyzing), Marks 2+2+1]

Q3. For a CMOS inverter assume that VDD =2.5 V, $\mu_n C_{ox}$= 115 $\mu A/V^2$, L_n=L_p=0.25 μm, $V_{t0,n}$=0.4V,$V_{t0,p}$= -0.5V, and $\mu_p C_{ox}$= 30$\mu A/V^2$. Find the ratio of W_p/W_n such that τ_{PHL}=τ_{PLH}. Assume differential equation method is used to compute the value of τ_{PHL} and τ_{PLH}.

[CO3 (Analyzing), Marks 5]

Q4.(a) Discuss Elmore delay for RC tree network.

(b) Calculate the Elmore delay from vin to vout1 and vin to vout2. [CO3 (Analyzing), Marks 2+3]



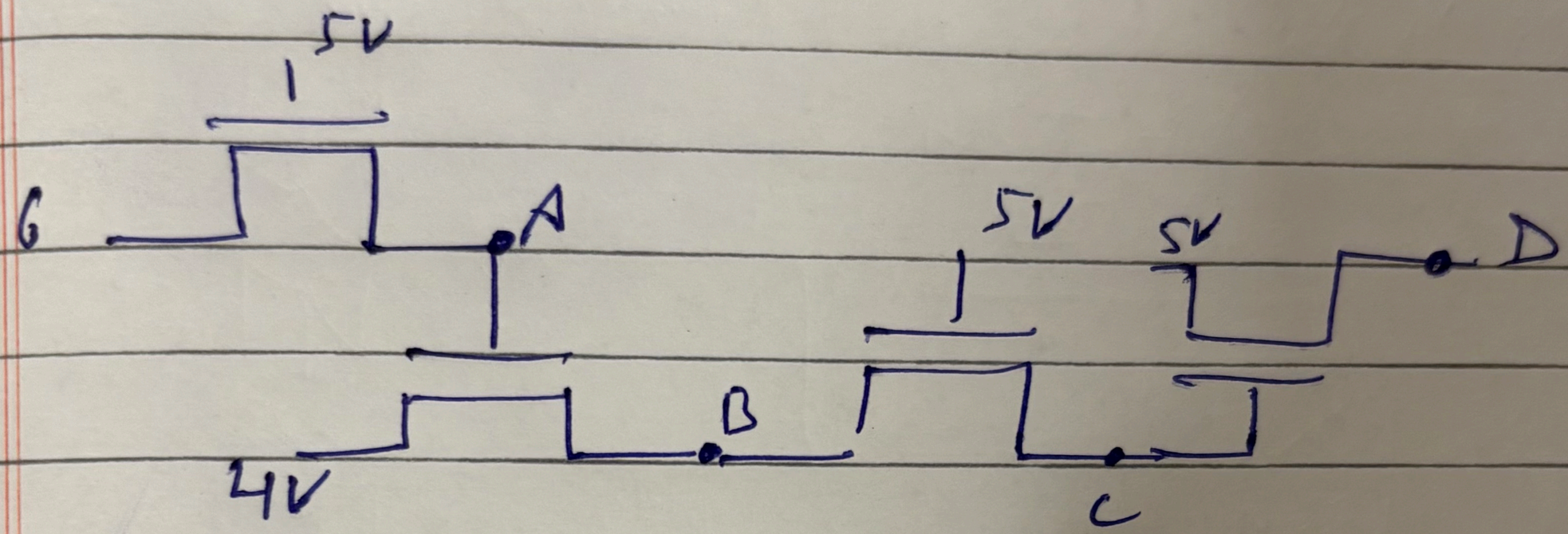
(4) Things : Voltage Ques

(i) min (Gate Volt − V_{th} , i/p Volt)

(ii)

(5)

$V_{th} = 1V$



at A : Volt = min (5 − 1 , 6) = 4 V

" B : Volt = min (4 − 1 , 4) = 3 V

" C : Volt = min (5 − 1 , 3) = 3 V

" D : Volt = min (3 − 1 , 5) = 2 V

⑥ Mode of operation:

(i) Cut-off Region:

↳ $\boxed{V_{GS} < V_T} \Rightarrow \boxed{I_D = 0}$

(ii) Linear Region:

↳ $\boxed{V_{DS} < V_{GS} - V_T}$

$$\Rightarrow \boxed{I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \left[2(V_{GS} - V_T) V_{DS} - V_{DS}^2 \right] \left[1 + \lambda V_{DS} \right]}$$

$k' = \mu_n C_{ox}$

$$= \frac{k'}{2} \frac{W}{L} \left[2(V_{GS} - V_T) V_{DS} - V_{DS}^2 \right] \left[1 + \lambda V_{DS} \right]$$

(iii) Saturation:

↳ $\boxed{V_{DS} \geq V_{GS} - V_T}$

$$\Rightarrow \boxed{I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})}$$

$$= \frac{k'}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

where: $k' = \mu_n C_{ox}$

⑦ Threshold Voltage $\Rightarrow \boxed{V_T = V_{TO} + \gamma \left[\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|} \right]}$

where: (i) λ = Channel Length Modulation unit V^{-1}

(ii) γ = Body effect coefficient unit $V^{1/2}$

(iii) $k' = \mu_n C_{ox}$, ~~$k = \mu_n C_{ox}$~~

(iv) $V_{GS} = V_G - V_S$, $V_{SB} = V_S - V_B$, $V_{DS} = V_D - V_S$

(v) γ = Body Effect coefficient $= \dfrac{V_T - V_{TO}}{\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}}$ unit $V^{1/2}$

Spiral

POSSESSION OF MOBILES IN EXAM IS UFM PRACTICE.

Name Anuncay Dwivedi **Enrollment No.** 9922102048

Jaypee Institute of Information Technology, Noida

T1 Examination, Even 2025
B. Tech, VI Semester

Course Title: VLSI Design **Maximum Time: 1 Hr**
Course Code :18B11EC315 **Maximum Marks : 20**

CO1	Understand VLSI design flow, VLSI design styles, digital systems modeling using Verilog-HDL.
CO2	Apply MOSFET models for circuit simulation and its effect on scaling.
CO3	Analyze the concepts of static and dynamic characteristics of MOS inverters, combinational and sequential circuits.
CO4	Explain and evaluate dynamic logic circuits, stick diagram, layout and different types of semiconductor memories.

Note: *Attempt all the questions. Usage of Calculator is allowed.*

Q.1 Discuss the VLSI design flow and explain various VLSI Design styles in brief.
[CO1 (Understanding), 3+1 Marks]

Q.2 Discuss any three short-channel effects in MOSFETs.
[CO2 (Applying), 3 Marks]

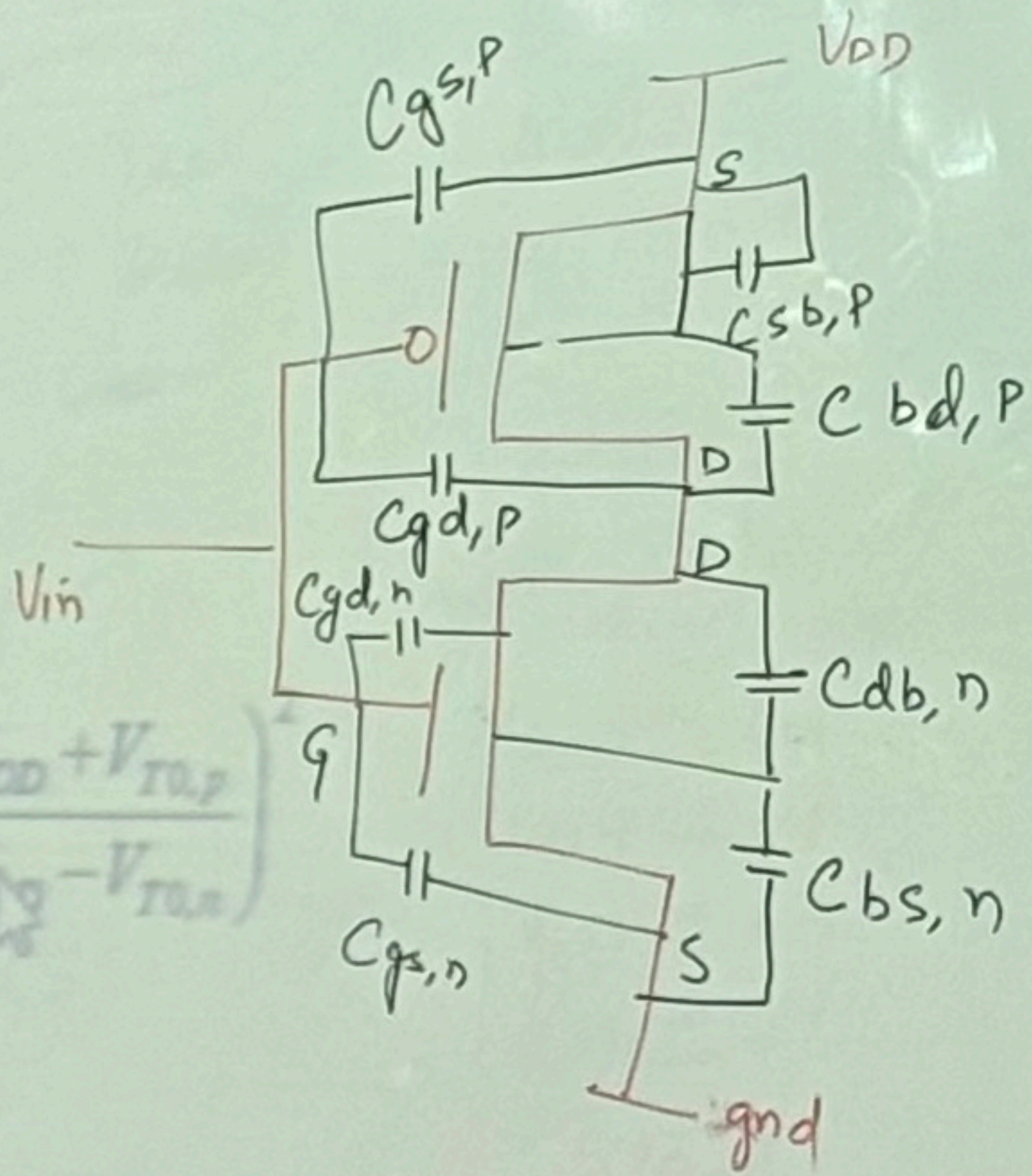
Q.3 Explain different types of scaling methods in MOSFETs and discuss their effects on device characteristics.
[CO2 (Applying), 4 Marks]

Q.4 An NMOS transistor has the following parameters: $V_{T0} = 0.8\,V$, $\gamma = 0.2\,V^{1/2}$, $\lambda = 0.05\,V^{-1}$, $|2\phi_F| = 0.6\,V$, $\mu_n C_{ox} = 20\,\mu A/V^2$.
(a) When the transistor is biased with $V_G = 2.8\,V$, $V_D = 2.8\,V$, $V_S = 1\,V$, $V_B = 0\,V$, the drain current $I_D = 0.24\,mA$. Determine W/L.
(b) Calculate I_D for $V_G = 5\,V$, $V_D = 3\,V$, $V_S = 2\,V$, and $V_B = 0\,V$.
[CO2 (Applying), 5 Marks]

Q.5 Consider an abrupt p-n junction. The doping density of the n-type region is $N_D = 10^{19} cm^{-3}$ and the doping density of the p-type region is $N_A = 10^{16} cm^{-3}$. The junction area is $10\,\mu A \times 10\,\mu A$. Assume that the reverse bias voltage changes from $V_1 = 0\,V$ to $V_2 = -5\,V$. Calculate the equivalent junction capacitance at room temperature. Given $n_i = 1.45 \times 10^{10} cm^{-3}$, $\varepsilon_{si} = 11.7\,\varepsilon_0$, $\varepsilon_0 = 8.85 \times 10^{-14}\,F/cm$.
[CO2 (Applying), 4 Marks]

END OF PAPER

verter threshold voltage Vth is one
most important parameters
haracterize the steady-state input-
t behavior of the CMOS inverter



$\cdot V_{DD} + V_{T0,p}$

$\cdot V_{DD} - V_{T0,n}$

Symmetricity: $V_{T0,n} = |V_{T0,p}|$

Tute-3-Max

① $$\boxed{k_r = \frac{k_n}{k_p} = \frac{k_n' \left(\frac{W}{L}\right)_n}{k_p' \left(\frac{W}{L}\right)_p} = \frac{\mu_n C_{ox} \left(\frac{W}{L}\right)_n}{\mu_p C_{ox} \left(\frac{W}{L}\right)_p} = \left(\frac{V_{DD} + V_{TO,P} - V_{th}}{V_{th} - V_{TO,n}}\right)^2}$$

② $$\boxed{V_{th} = \text{Threshold Voltage} = \frac{V_{TO,n} + \sqrt{\frac{1}{k_r}}\left(V_{DD} + V_{TO,P}\right)}{1 + \sqrt{\frac{1}{k_r}}}}$$

③ Resistive Load:

(i) $V_{OH} = V_{DD}$

(ii) $$V_{OL} = V_{DD} - V_{TO} + \frac{1}{k_n R_L} - \sqrt{\left(V_{DD} - V_{TO} + \frac{1}{k_n R_L}\right)^2 - \frac{2V_{DD}}{k_n R_L}}$$

(iii) $$V_{IL} = V_{TO} + \frac{1}{k_n R_L}$$

(iv) $$V_{IH} = V_{TO} + \sqrt{\frac{8}{3}\frac{V_{DD}}{k_n R_L}} - \frac{1}{k_n R_L}$$

(v) Noise Margin Low $\Rightarrow N_{ML} = V_{IL} - V_{OL}$

(vi) " " High $\Rightarrow N_{MH} = V_{OH} - V_{IH}$

VLSI - Max

① Realization Using CMOS :

(i) Find Y_N = w/o bar

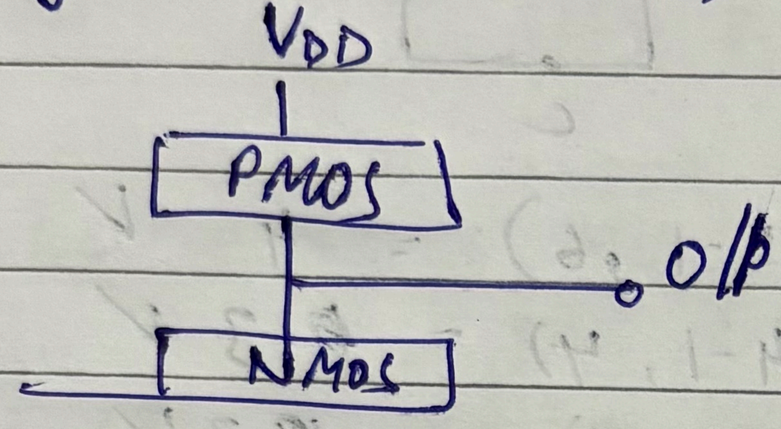
Y_P = w bar & reduced down using DeMorgan

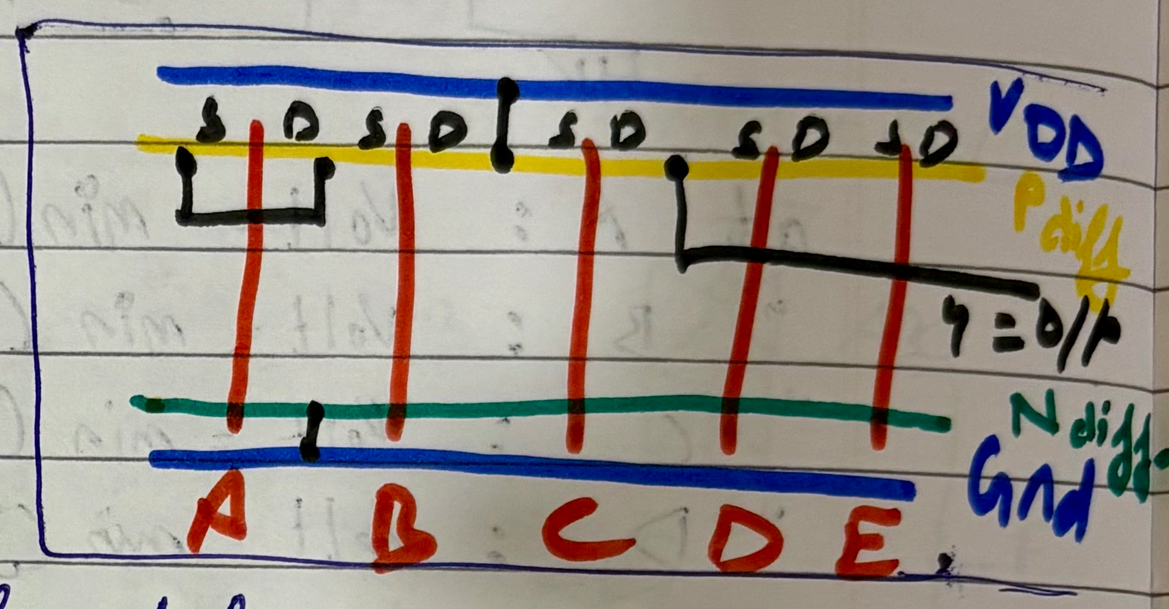
$\overline{A+B} = \bar{A}\bar{B} \leftrightarrow \overline{AB} = \bar{A}+\bar{B}$

(ii) If "AND" ⇒ Series ⇒ Downwards

If "OR" ⇒ Parallel ⇒ Sideways

(iii)





② Stick Diagram :

(i) no. of trans = no. of red lines

(ii) Order of trans ⇒ Euler's Method

(iii) " " "S" & "D" ⇒ ↓ exactly as they appear in the circuit realization diagram

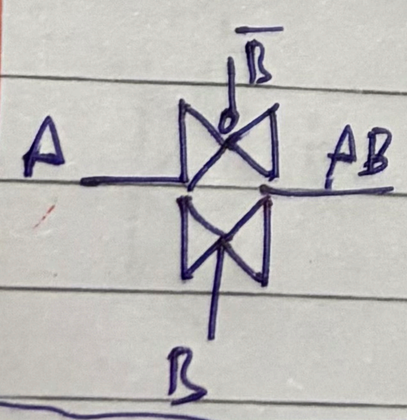
③ Euler :

(i) Draw nodes b/w trans, connect them

(ii) Try finding common path from both

↳ can't be repeated as back-traversed

④ Transmission Gate :



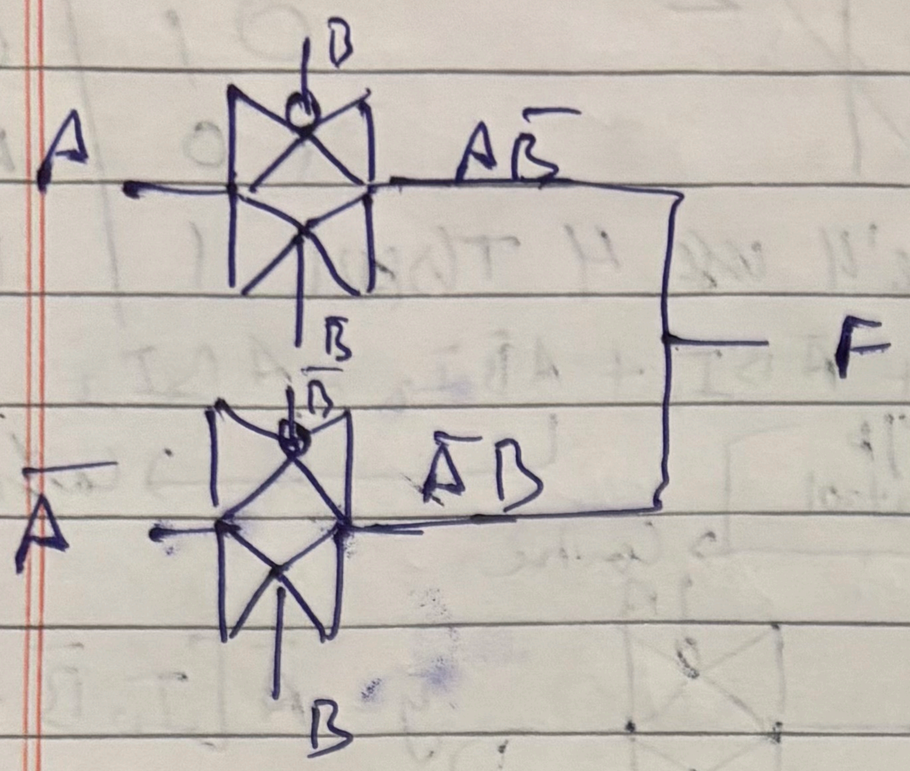
(i) No. of Gates = No. of product terms

(ii) Take two variables at a time, if more, add another gate by taking prev as i/p and (new) as control line (bottom)

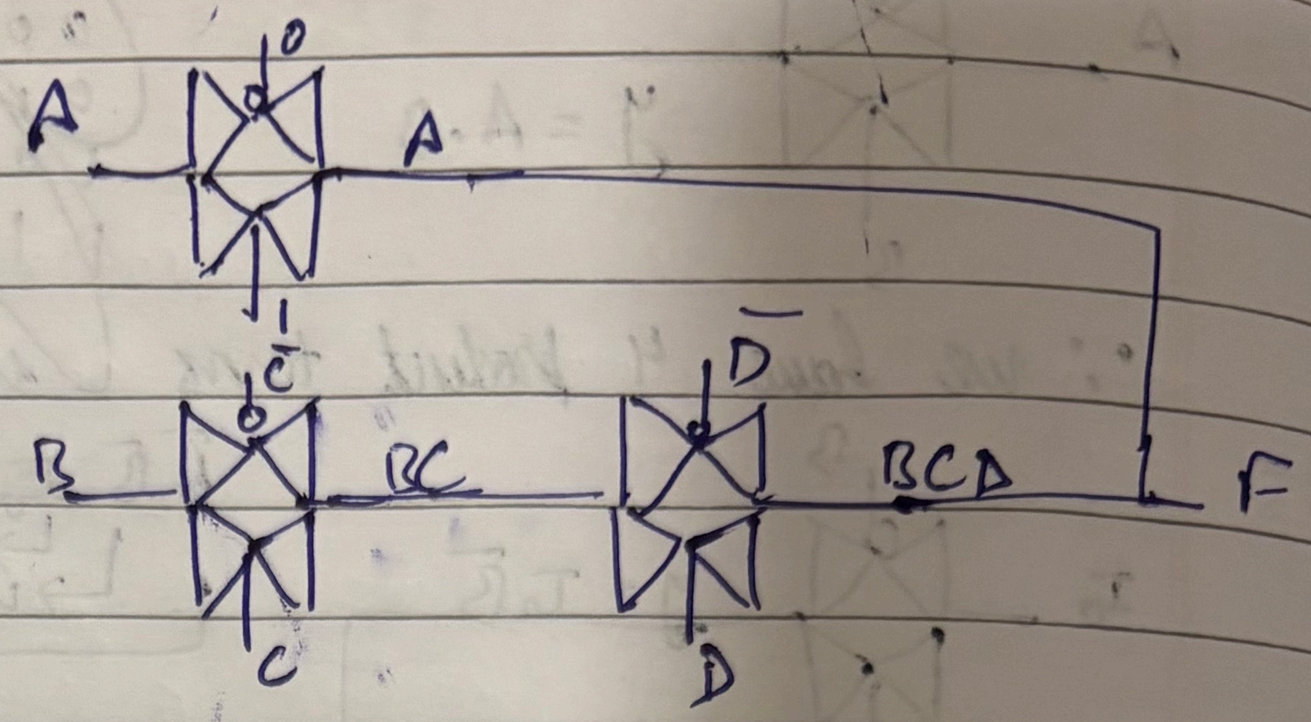
⑤ Voltage at Node = min (Gate Volt − V_{th} , i/p Volt)

↳ threshold volt

(2) $F = A\bar{B} + \bar{A}B$



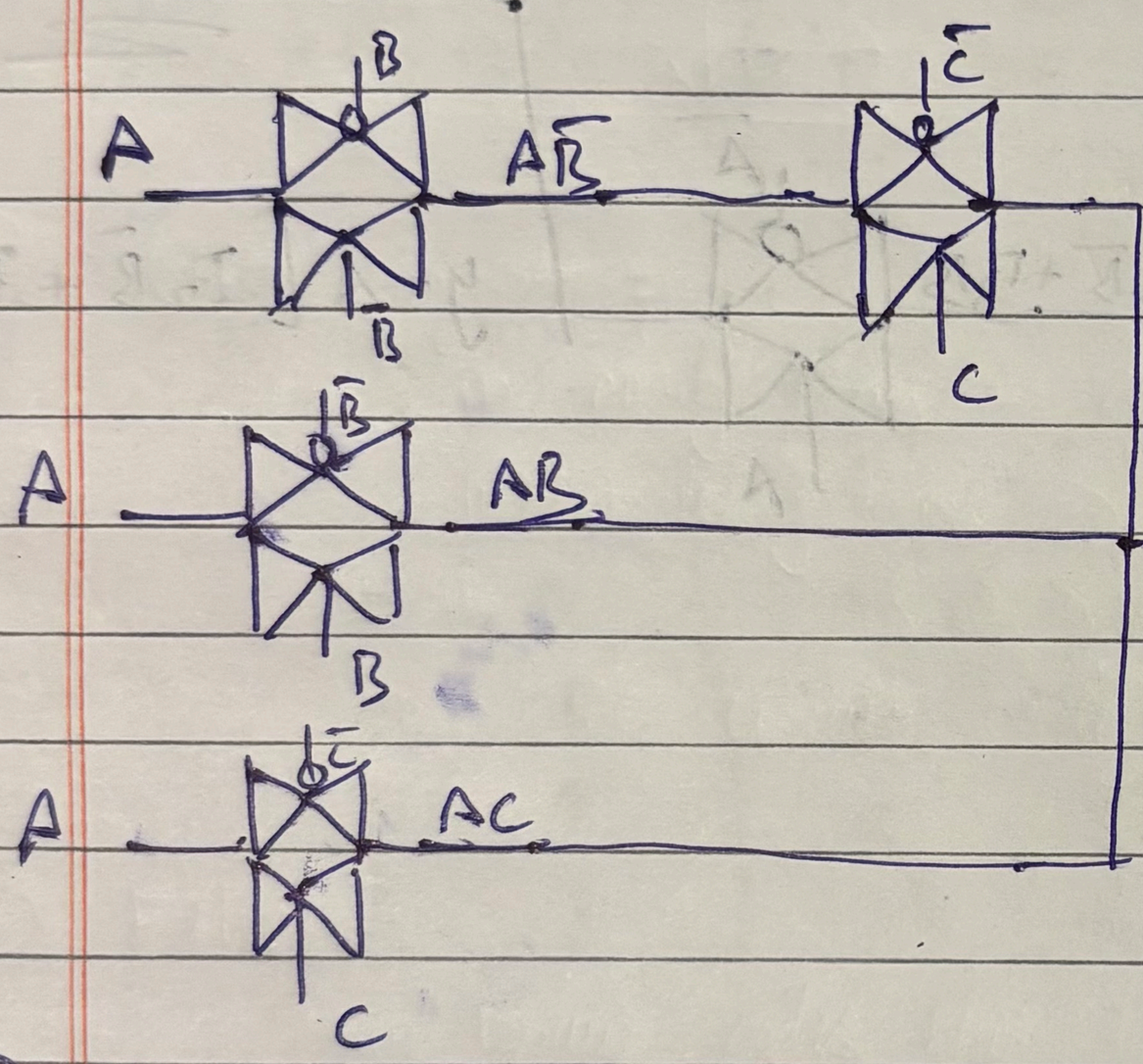
(b) $F = A + (BC)D$

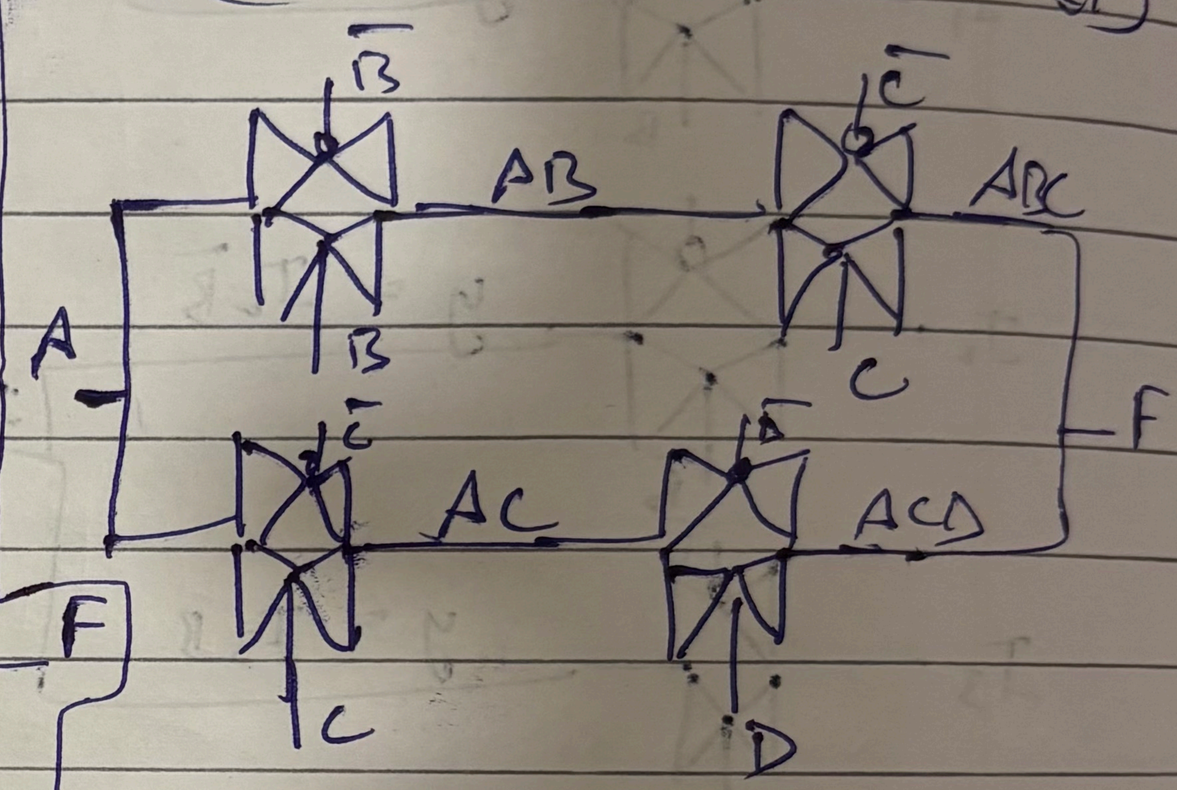


(c) $F = A(B+C)D$

$= (AB+AC)D = ABC + ACD$

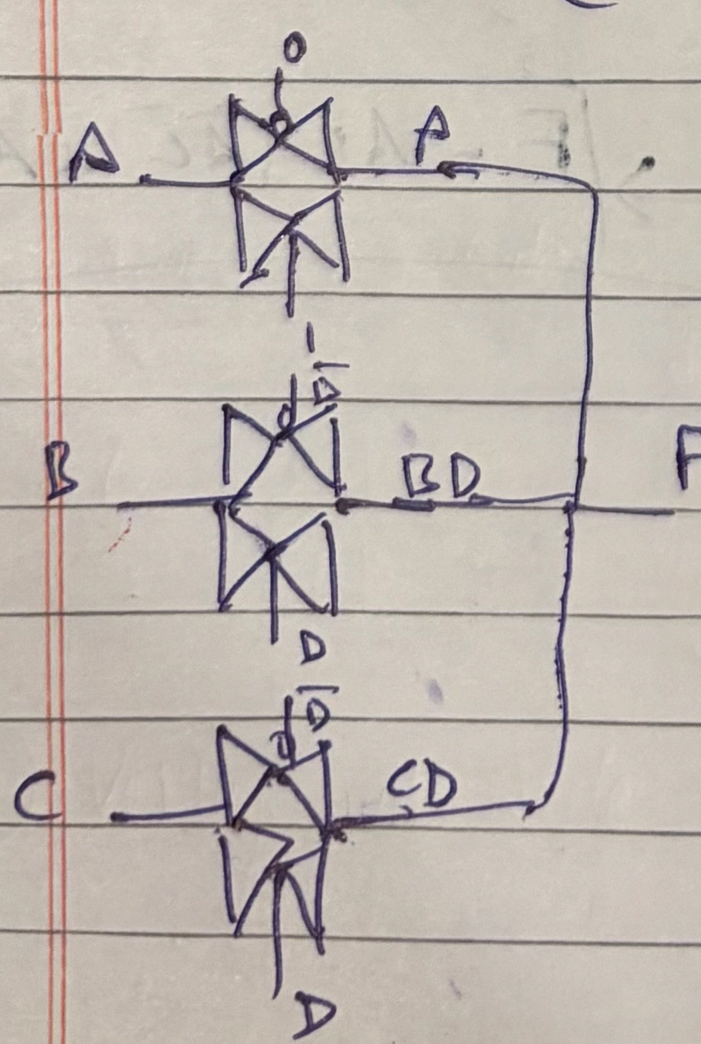
(3) $F = A\bar{B}C + AB + AC$

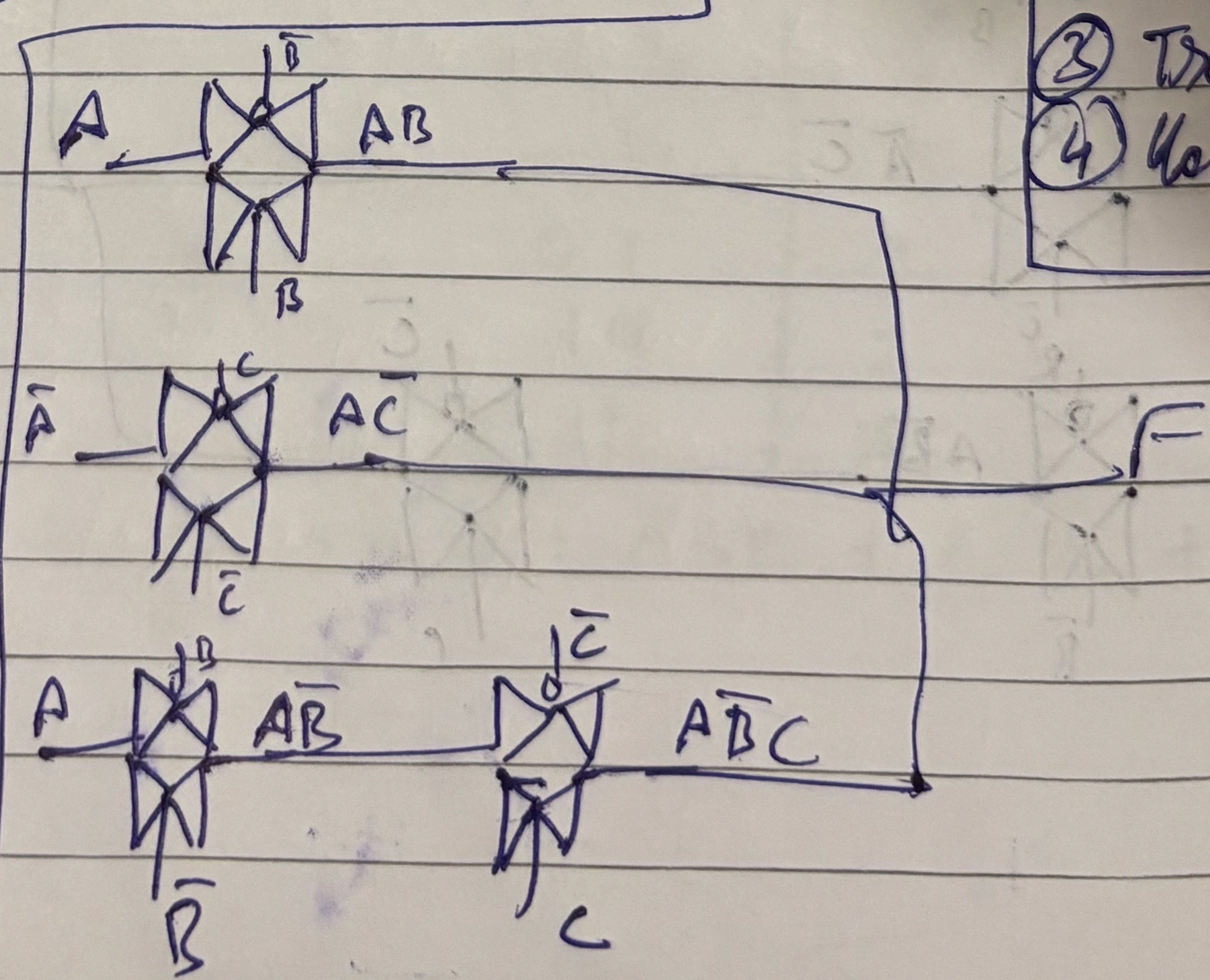




(d) $F = AB + \bar{A}\bar{C} + A\bar{B}C$

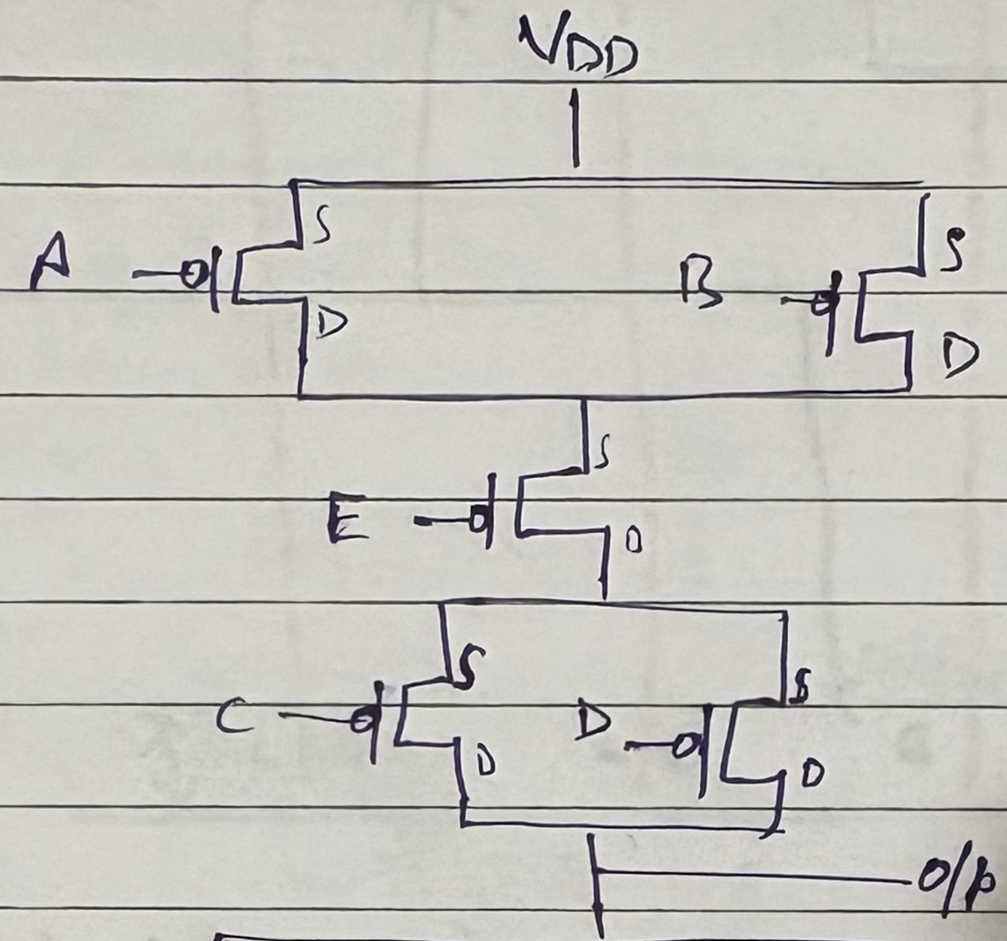
(5) (a) $F = A + (B+C)D = A + BD + CD$



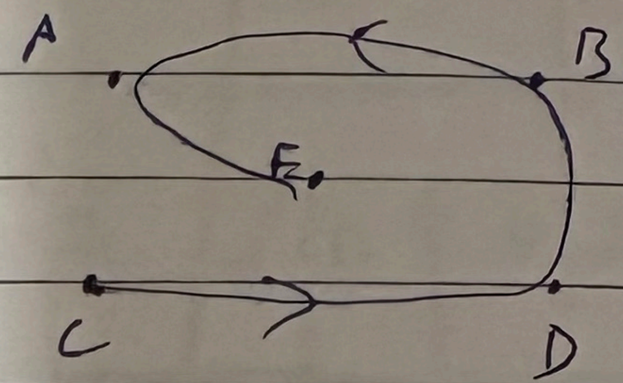


1. Stick, Realization
2. Euler
3. Transmission
4. Voltage

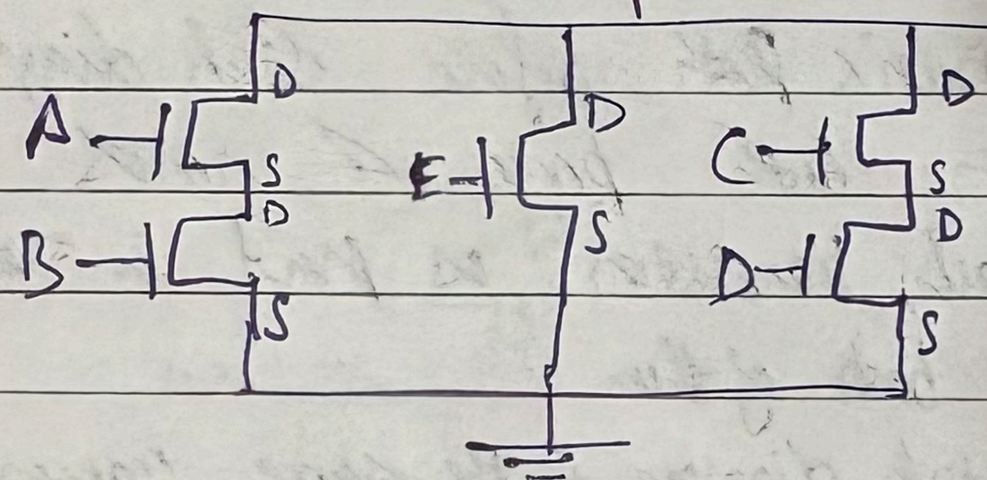
① $Y = \overline{AB + E + CD} = \overline{AB} \cdot \overline{E} \cdot \overline{CD} = (\overline{A} + \overline{B}) \cdot \overline{E} \cdot (\overline{C} + \overline{D})$

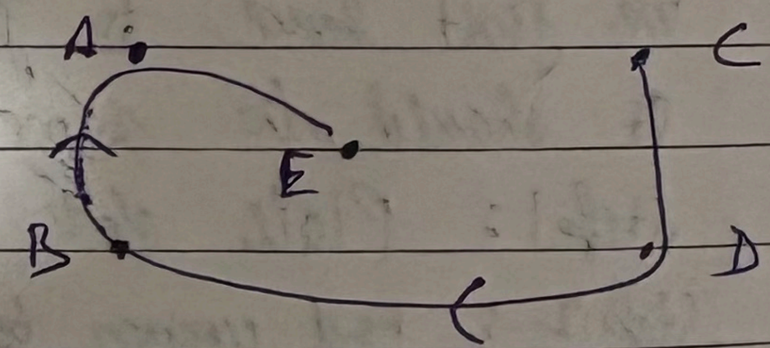


Euler's Path:

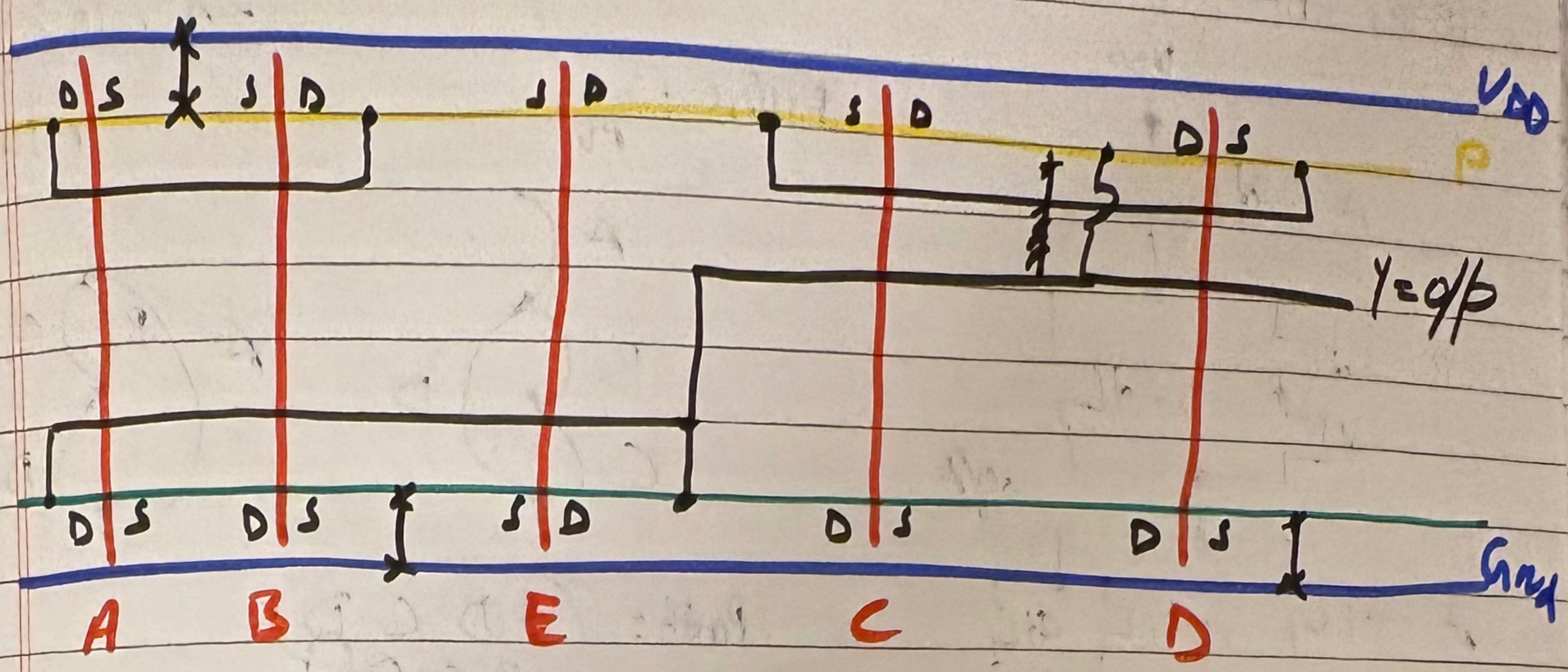


Path: CDBAE





Path : ABECD

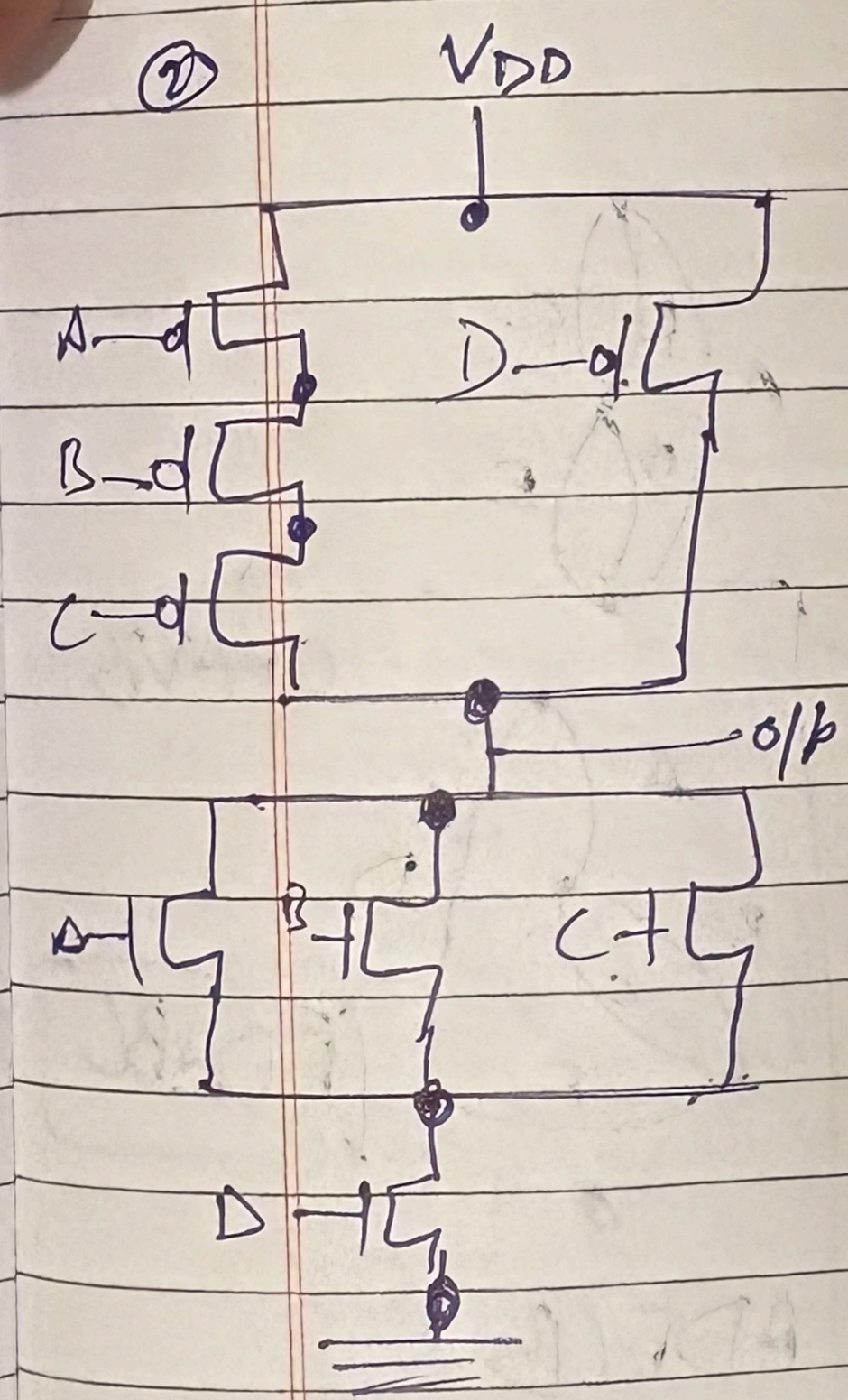


① Finding Euler's path :

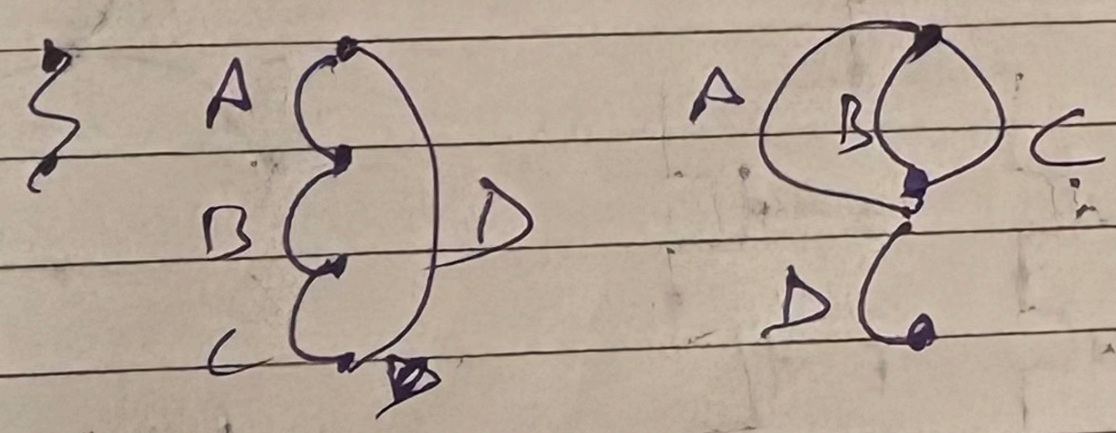
Rule : (i) Nodes can be repeated by not path

(ii) Path should be valid for both PU & PD

②



Draw nodes that connect the transistor:



Path 1: A B C D A B C D

Path 2: