

Q.1

Total banks = 64 (Samples)

 $T_s = 125 \mu s$ 

→ time duration available for Tx. of each sample =  $\frac{125 \mu s}{64}$   
 $= 1.95 \mu s$

→ Size of Control memory = 32 words  
 5 bit each  
 (32 inlet, address requires 5 bits)

→ clock rate =  $2 \times 32 \times 8 \text{ kHz}$   
 $= 64 \times 8 = 512 \text{ kHz}$  } Bidirectional traffic  
 otherwise =  $32 \times 8 \text{ kHz}$

Q.2 $T_s = 125 \mu s$ 

Each pulse = 125 ns

Bidirectional traffic = 2 pulses =  $2 \times 125 \text{ ns}$ Subscribers =  $\frac{125 \mu s}{2 \times 125 \text{ ns}} = 500$ Q.31) Address lines =  $\log_2 32 = 5 \text{ bit}$ 

2) Data line = Always 8 bit (sample converted to 8 bit)

3) Data memory = (depends on Seq. Operation)  
(DM)

= O/p read operation is Seq.

= 32 outlets will read 1 by 1

(from DM, each DM will carry 8 bit sample)

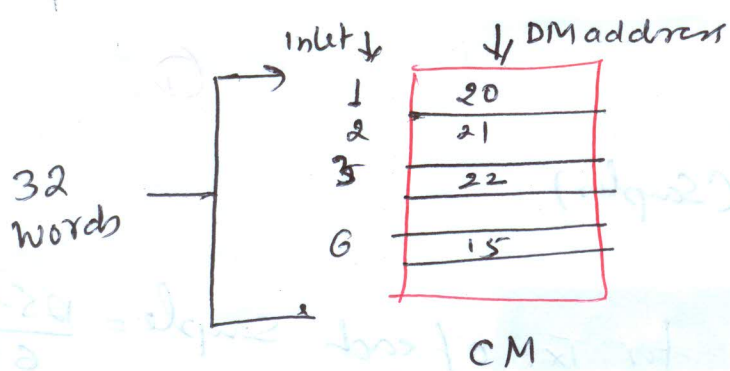
Size = 32 location  $\times$  8 bit4) CM size =  $32 \times 8 \text{ bit}$ 

depend on Random Operation

= 32 inlets has to be written in DM

based on address given by CM

=  $32 \times 5 \text{ bit}$



Data of 1 will be written 20th location of DM, 20th outlet will read. So  $1 \leftrightarrow 20$  connection achieved etc. (2)

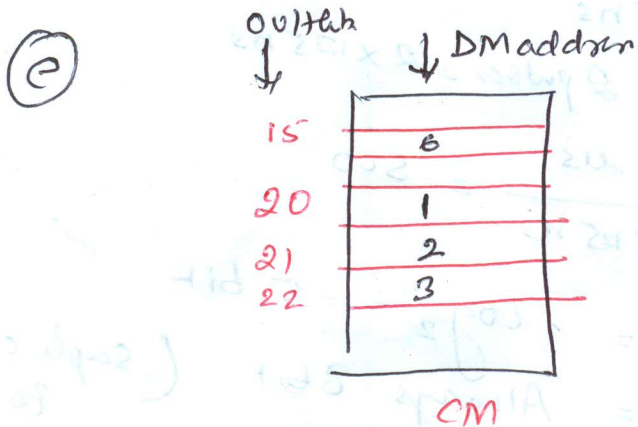
Q.4.

(a) Address line =  $\log_2 (\text{DM locations})$   
 $= \log_2 32 = 5$

(b) Data lines = 8

(c) DM =  $32 \times 8$  bit

(d) CM =  $32 \times 5$  bit



Q.5

32 X 64 Switch

Seq write / Random Read

→ 32 inlet written Seq. So DM will contain 32 location, 8bit each.

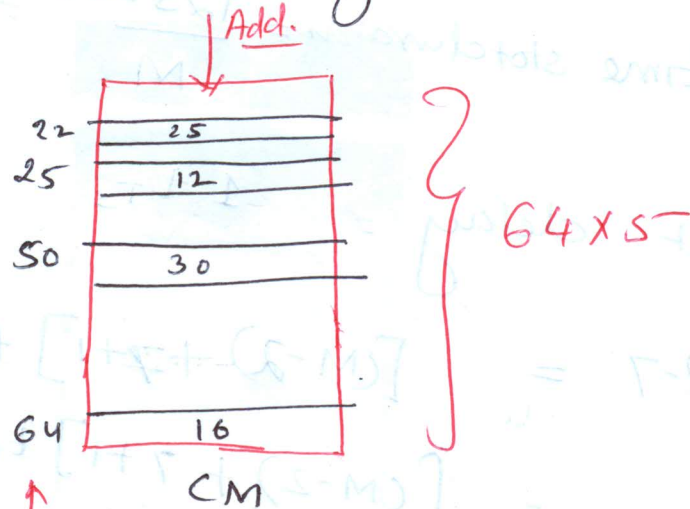
DM size =  $32 \times 8$  bit  
 Data lines = 8

→ 64 outlets read data randomly  
 CM contains = 64 location for each outlet  
 location contains address of DM, DM has 32 location so addressing then requires 5 bit

→ CM Size =  $64 \times 20 \log_2^{32} = 64 \times 5 \text{ bit}$

→ Address line =  $20 \log_2^{(\text{DM location})} = 20 \log_2^{32} = 5$

(3)



32x64

Q-6

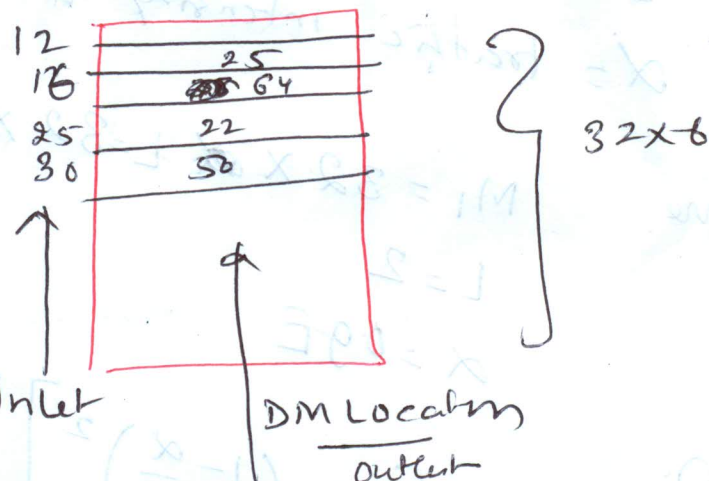
~~64x32~~ Switch Seq Read / Random write operation.

→ DM Size =  $64 \times 8 \text{ bit}$

→ Address line =  $20 \log_2^{64} = 6 \text{ bit}$

→ Data lines = 8 bit

→ CM Size =  $32 \times 6 \text{ bit}$





(4)

(7)

$$\text{bank} = 1 = M$$

$$\text{channel/slots} = 32 = M$$

$$\text{time slot duration} = \frac{125 \mu s}{M} = t_{Ts}$$

$$\rightarrow \text{inheret delay} = 1 t_{Ts}$$

$$\begin{aligned} \rightarrow \text{for } 2-7 &= [(M-2) + 7 + 1] t_{Ts} \\ &= [(M-2) + 7 + 1] t_{Ts} \end{aligned}$$

$$\text{for } 3-4 = [(M-3) + 4 + 1] t_{Ts}$$

$$\text{for } 1-1 = t_{Ts}$$

(8)

$$P_B (T_{ST}) = \left[ 1 - (1 - \alpha/L)^2 \right]^{M_1}$$

$M_1$  = time slot on o/p side of TSI switch.

$$L = M_1/M = \text{exp/concentration factor}$$

$$\alpha = \text{traffic intensity on a link}$$

$$\rightarrow \text{here } M_1 = 32 \times 2 = 64$$

$$L = 2$$

$$\alpha = 0.9E$$

$$P_B = \left[ 1 - \left( 1 - \frac{\alpha}{L} \right)^2 \right]^{M_1}$$