POSSESSION OF MOBILES IN EXAM IS UFM PRACTICE

Name: _____ **Enrolment No:** _____

Jaypee Institute of Information Technology, NOIDA

End Semester Examination – Even Semester 2023-24

B.TECH VI Semester

Course Title: Digital Hardware Design **Maximum Time: 2 Hr**

Course Code: 17B1NEC741 **Maximum Marks: 35**

CO1	Recall the concept of sequential circuits and state machines
CO2	Discuss advanced adders and multiplier circuits
CO3	Demonstrate the concept of VHDL and FSM in digital circuit design
CO4	Illustrate the concept of different ways of pulse or pattern generation.
CO5	Design asynchronous sequential digital circuits using flow table method.

Q1. A system is having one input and one output. Output becomes 1 and remains 1 thereafter when at least two 0's and at least two 1's has occurred as inputs, regardless of the order of occurrence. Draw state diagram of the system. [CO1(Remembering, Marks 5]

Q2. Design frequency divider by 5 circuit with50% duty cycle. Show complete design steps.

[CO4(Analyzing), Marks 5]

Q3. Explain the working of 4-bit Carry Select Adder (CSA) with proper block diagram?

[CO2 (Understanding, Marks 5]

Q4. Using Radix-2 Booth Multiplier Technique, show the computation of AxB for A= 1011 and B=0011 where A and B are in 2's complement form. [CO2(Understanding, Marks 5]

Q5. An asynchronous circuit is having two inputs (D and G) with output Z. The value of Output Z is same as that of D when G=1 otherwise no changes. Find primitive flow table and reduced flow table and design the circuit using basic logic gates. [CO5(Evaluating, Marks 7]

Q6. Write VHDL code for the state diagram given in Fig.1. [CO3 (Applying), Marks 4]

Q7. From the transition table given in Fig.2, identify the type of race present in system. T and C represent inputs and y1y2 represent states of the system. [CO5(Evaluating, Marks 4]

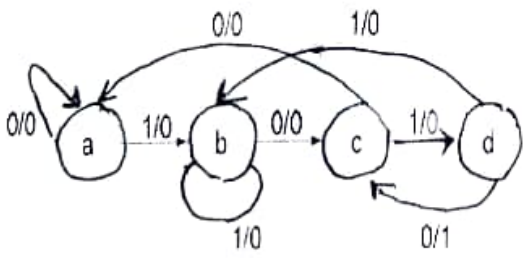

Fig.1

TC

y_1y_2	00	01	11	10
a = 00	10	(00)	(00)	11
b = 01	(01)	00	10	(01)
c = 11	01	(11)	(11)	10
d = 10	(10)	(10)	00	(10)

Fig.2