Course Name: Digital Hardware Design
Course Code: 17B1NEC741

Pulse Generation Techniques-1

Dr. Arti Noor
Dean, Academic Affairs
Electronics and Communication Engineering,
Jaypee Institute of Information Technology, Noida

Introduction

- Pulse Train or sequence generator is one kind of digital logic circuit.
- It is a system that generates a prescribed sequence of bits synchronized with a clock.

- A special kind of sequence generator is a binary counter.
- Pulse train can be generated using either direct logic or indirect logic.
- In direct logic the output is taken directly from a FF output
- In indirect logic, it is generated using extra circuitry or decoding circuit along with FF.

Direct Logic Approach

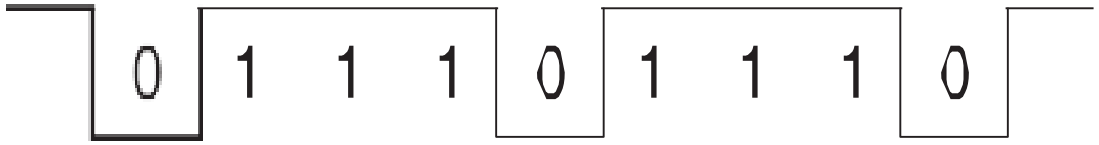
Steps:

1. Inspect the pulse train. Decide the number of unique states and no. of FFs required. List the sequence in 1s and 0s. The list may begin from anywhere on the train. Identify No. of unique states required and so FFs number required.

2. 1's and 0's sequence will form LSB of state assignment. If unique states are not possible with the least no. of FFs such that no. of states $N<2^n$, increase FFs.

1. Design the counter. The O/P is at the Q or Q' of LSB FF.

Example1: Design using JK FF.



0 1 1 1 0 1 1 10.....

It can be seen that pulse is of 4-bit like 1 0 1 1, 0 1 1 1, 1 1 1 0, 1 1 0 1

Write the sequence vertically in LSB position

LSB
0
1
1
1

Assign states using 2 FFs. Results in no unique 4 states

FF states	
	LSB
0	0
0	1
1	1
?	1

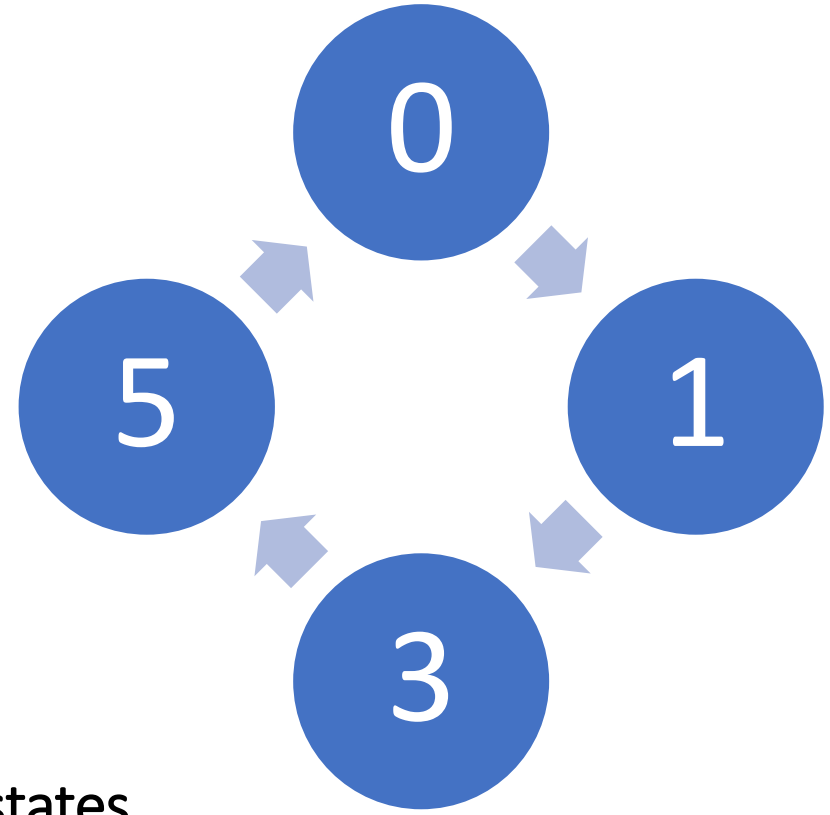
Try states using 3 FFs(8 states). Only four states are required and remaining 4 states will be invalid.

FF states			Equivalent Decimal
		LSB	
0	0	0	0
0	0	1	1
0	1	1	3
1	0	1	5

Example1: Design using JK FF.

The State diagram for is as shown below:

Sequence : 0 1 1 1

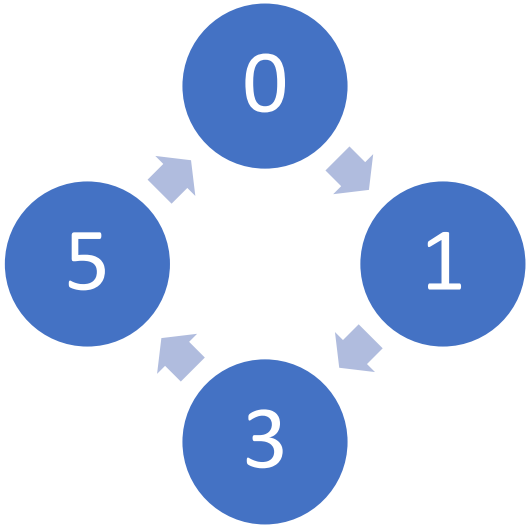


With Four unique valid states

Example1: Design using JK FF.

The State transition table for JK FF

Sequence : 0 1 1 1



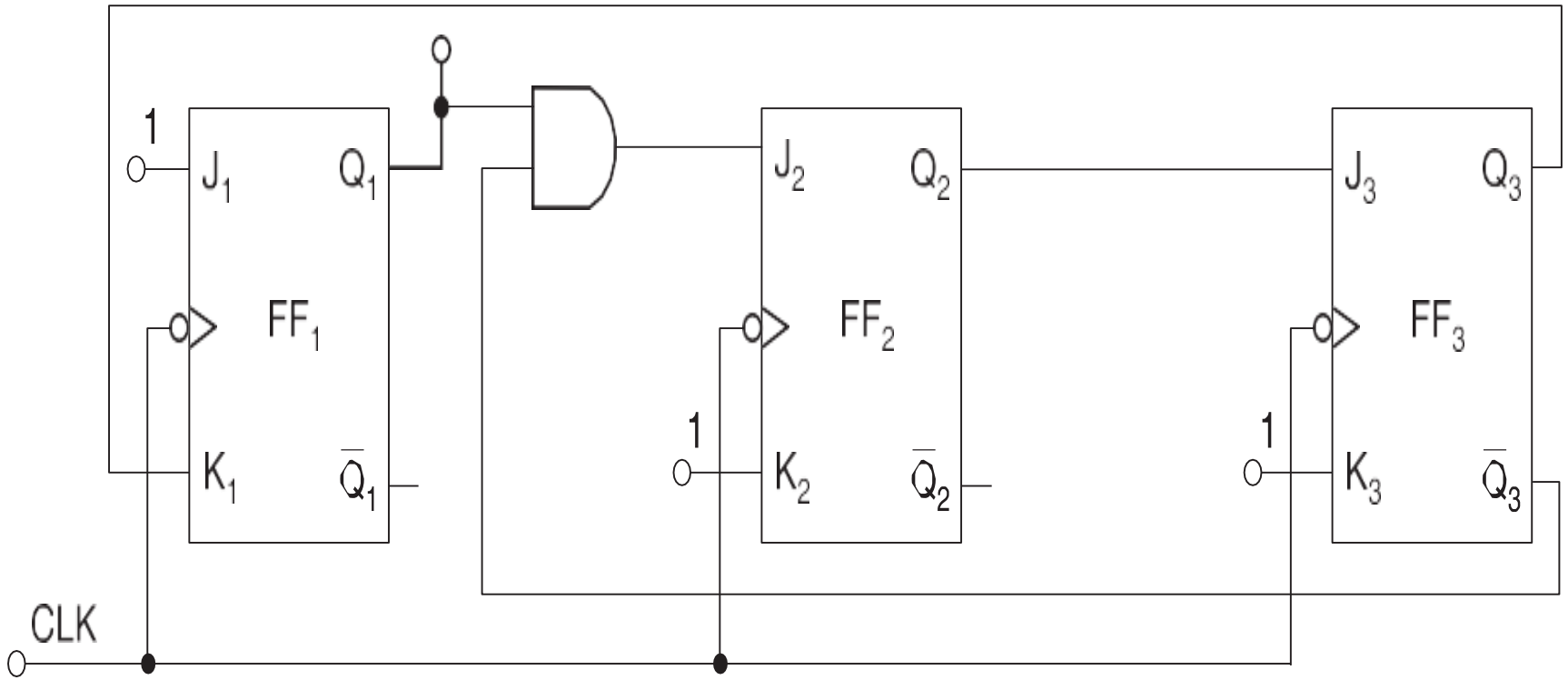
Present states			Next states			Required Excitation					
Q3	Q2	Q1	Q3+	Q2+	Q1+	J3	K3	J2	K2	J1	K1
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	1	0	x	1	x	x	0
0	1	1	1	0	1	1	x	x	1	x	0
1	0	1	0	0	0	x	1	0	x	x	1

Q	*Qnext*	*J*	*K*
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

J3=Q2, K3=1; J2=Q3'Q1, K2=1; J1=1, K1=Q3

Example1: Design using JK FF.

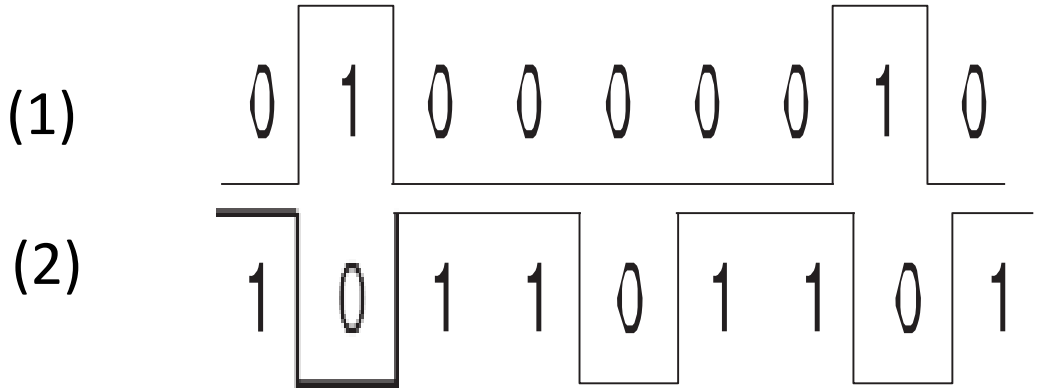
J3=Q2, K3=1; J2=Q3'Q1, K2=1; J1=1, K1=Q3



Logic Diagram of Pulse Train Generator

Direct Approach- Generating Multiple Pulses

Example2:

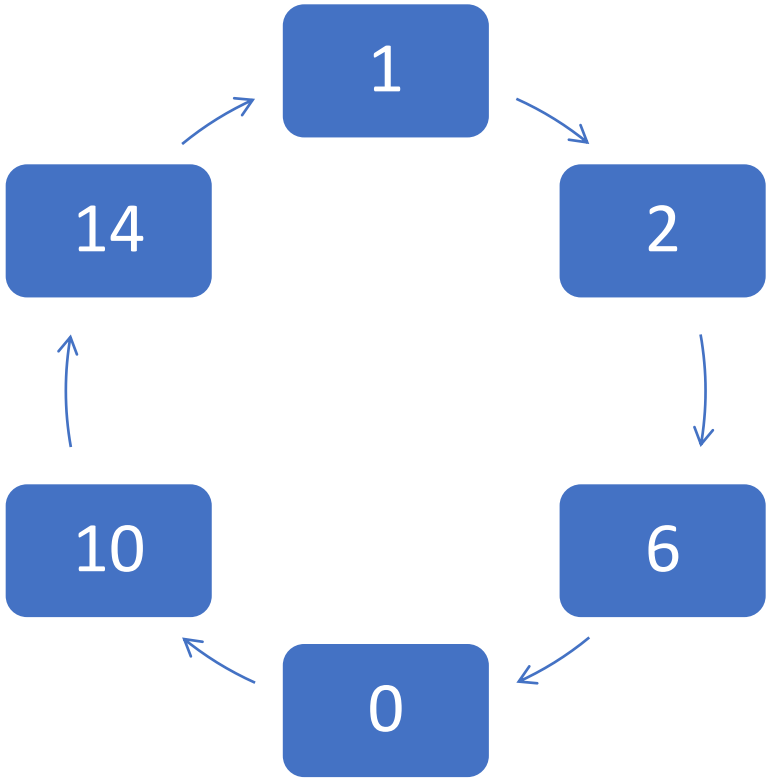


3 FF states (Q1 is ist o/p & Q2 2nd o/p)			4 FF States(Q1 is ist o/p & Q2 2nd o/p)				Equivalent Decimal Value
Q3	Q2	Q1	Q4	Q3	Q2	Q1	
0	0	1	0	0	0	1	1
0	1	0	0	0	1	0	2
1	1	0	0	1	1	0	6
0	0	0	0	0	0	0	0
?	1	0	1	0	1	0	10
?	1	0	1	1	1	0	14

Direct Approach- Generating Multiple Pulses

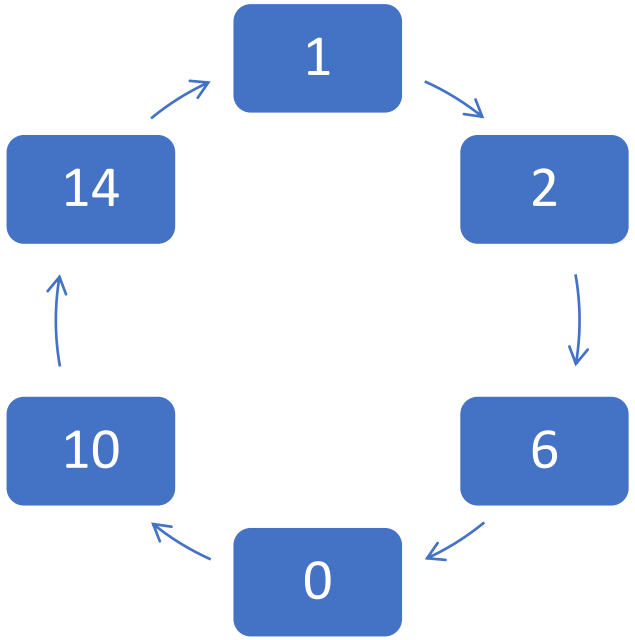
Example2:

The State Transition Graph



Direct Approach- Generating Multiple Pulses

Example2:



The State transition table for JK FF

PS				NS				Required excitation							
Q_4	Q_3	Q_2	Q_1	Q_4	Q_3	Q_2	Q_1	J_4	K_4	J_3	K_3	J_2	K_2	J_1	K_1
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	1	1	0	0	X	1	X	X	0	0	X
0	1	1	0	0	0	0	0	0	X	X	1	X	1	0	X
0	0	0	0	1	0	1	0	1	X	0	X	1	X	0	X
1	0	1	0	1	1	1	0	X	0	1	X	X	0	0	X
1	1	1	0	0	0	0	0	X	1	X	1	X	1	1	X

$J_4 = \overline{Q}_2\overline{Q}_1$, $K_4 = Q_3$

$J_3 = Q_2$, $K_3 = 1$

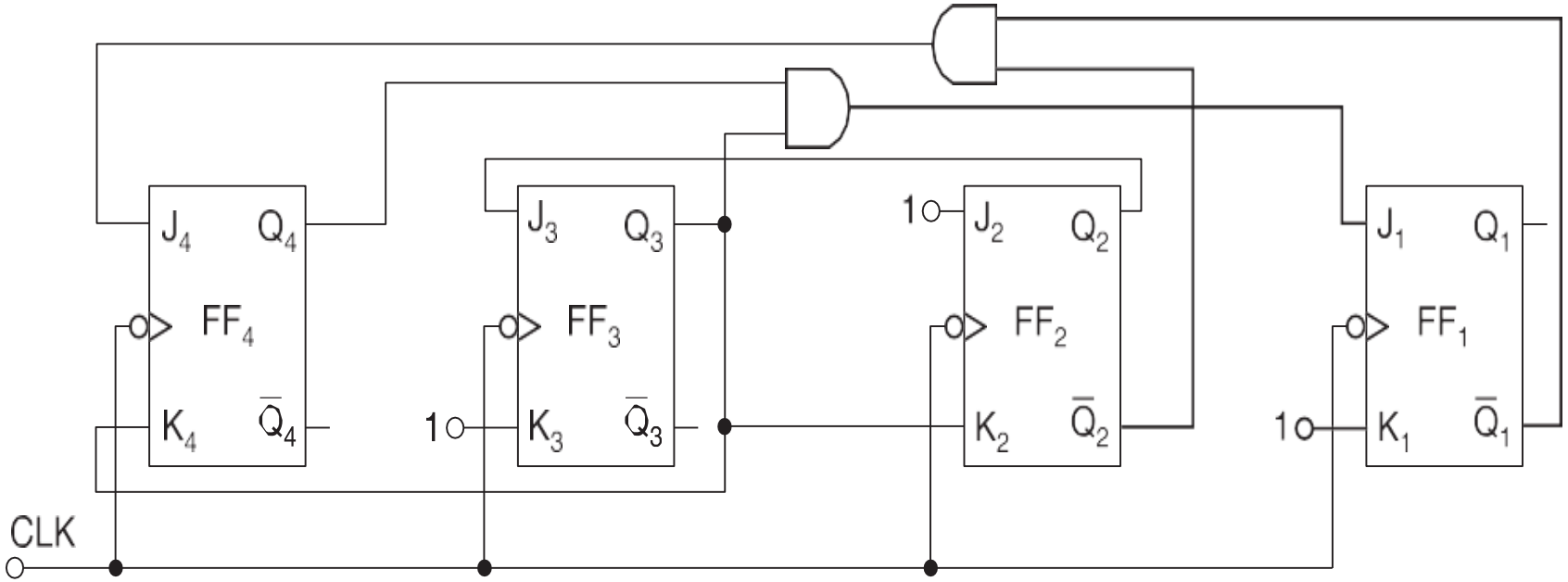
$J_2 = 1$, $K_2 = Q_3$

$J_1 = Q_4Q_3$, $K_1 = 1$

Direct Approach- Generating Multiple Pulses

Example2:

$$J_4 = \overline{Q}_2\overline{Q}_1, \quad K_4 = Q_3$$
$$J_3 = Q_2, \quad K_3 = 1$$
$$J_2 = 1, \quad K_2 = Q_3$$
$$J_1 = Q_4Q_3, \quad K_1 = 1$$



Logic Diagram of Pulse Train Generator