POSSESSION OF MOBILES IN EXAM IS UFM PRACTICE

Name: _____ Enrolment No: _____

Jaypee Institute of Information Technology, NOIDA

Test-1 Examination – 2024

B.TECH VI Semester

Course Title: Digital Hardware Design

Course Code: 17B1NEC741

Maximum Time: 1 Hr

Maximum Marks: 20

CO1	Recall the concept of sequential circuits and state machines
CO2	Discuss advanced adders and multiplier circuits
CO3	Demonstrate the concept of VHDL and FSM in digital circuit design
CO4	Illustrate the concept of different ways of pulse or pattern generation.
CO5	Design asynchronous sequential digital circuits using flow table method.

Q1. In state design, if the states are as given name as follows: S_0, S_2, S_5, S_6, S_{15}, than the minimum number of flip flop needed to implement it will be: _____

[CO1 (Remembering), Marks 1]

Q2

(a) FSM shown in Fig.1 is for _____ overlapping sequence detector.

(b) Converting Mealy machine FSM given in Fig.1 to Moore machine. Show steps clearly.

(c) Indicate the missing transitions at states b and c for FSM given in Fig.2 to work as overlapping type sequence detector for "100".

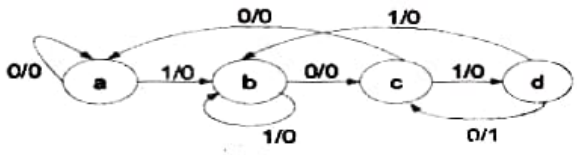

Fig.1

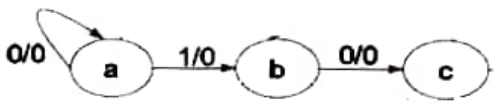

Fig.2

[CO3 (Applying), Marks [1+3+1]

Q3. Draw Mealy FSM for a sequential network which investigates an input sequence X and produces an output Z=1 if the total number of 1's received is even and the sequence "10" have occurred atleast once. [CO3 (Applying), Marks 5]

Q4. (a) Find out equivalent state in state table given in Fig.3 using implication chart method.

(b) Which state assignment is best out of those given in Fig. 4(a) and Fig. 4(b). Give reason.

PS	NS X=0	NS X=1	Z X=0	Z X=1
A	B	C	0	1
B	A	E	1	0
C	D	A	0	1
D	C	E	1	0
E	A	F	1	0
F	E	F	0	1

Fig.3

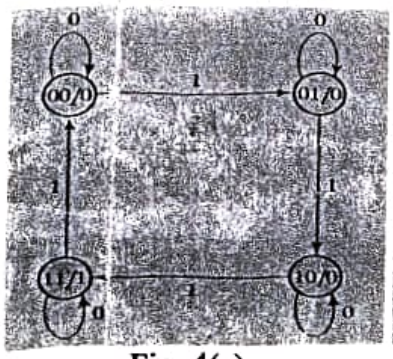

Fig. 4(a)

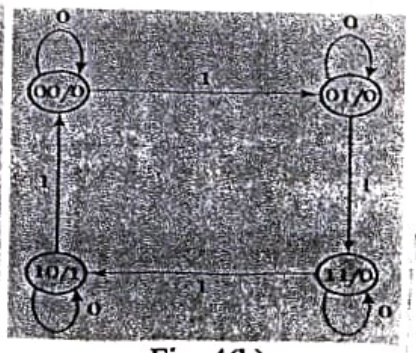

Fig. 4(b)

[CO3 (Applying), Marks 6+3]