JAYPEE INSTITUE OF INFORMATION TECHNOLOGY
Electronics and Communication Engineering
Course: VLSI Design
Course Code: 18B11EC315

Tutorial-4

1. For a CMOS inverter with a power supply voltage of V_{DD} = 5 V, determine the fall time, which is defined as the time elapsed between the time point at which V_{out} = V_{DD}*90% and the time point at which V_{out} = V_{DD} *10%. Use both the average-current method and the differential equation method for calculating the fall time. Assume output load capacitance is 1 pF. The nMOS transistor parameters are given as:
(i) $\mu_n C_{ox}$ = 20 $\mu A/V^2$
(ii) $(W/L)_n$ = 10
(iii)$V_{t,n}$ = 1.0 V

2. Consider a CMOS inverter, with the following device parameters:
(i) $V_{t0,n}$ = 0.8 V
(ii) $V_{t0,p}$= -1.0 V
(iii) W_{min} =1.2μm L = 0.6 μm

Design this CMOS inverter by determining the channel widths W_n and W_p of the nMOS and pMOS transistors, to meet the following performance specifications:

(a) V_{th} = 1.5 V for V_{DD} = 3 V
(b) Propagation delay times $\boldsymbol{t_{PHL}} \leq$ 0.2 ns and $\boldsymbol{t_{PLH}} \leq$ 0.15 ns,
(c) A falling delay of 0.35 ns for an output transition from 2 V to 0.5 V,
Assume a combined output load capacitance of 300 fF and an ideal step input.

3. For the RC network shown in Fig. 1, calculate the Elmore delay from In to Out1 and from In to Out2.

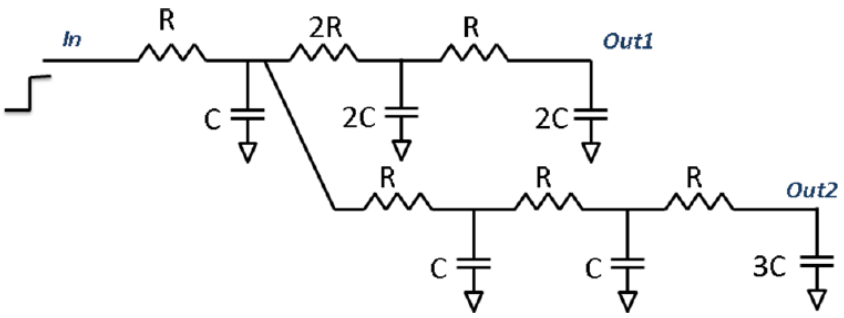

Fig. 1. Diagram of a RC network

4. For a CMOS inverter, assume that:
(i) V_{DD} = 2.5 V, (ii) k'_n = 115 μA/V^2, (iii) $L_n = L_p$= 0.25 μm, (iv)$V_{to,n}$ = 0.4 V, (v) $V_{to,p}$= -0.4 V, (vi) k'_p = 30 μA/V^2

Find W_p/W_n such that $\boldsymbol{t_{PHL} = t_{PLH}}$