JAYPEE INSTITUTE OF INFORMATION TECHNOLOGY

SECTOR -128,

NOIDA

VLSI LAB MANUAL

EXPERIMENT NO: 1

AIM: Introduction of Cadence tool, Schematic Editor, Layout Editor and Transient analysis of RC circuit.

TOOLS REQUIRED: PC,CADENCE TOOLS

PROCEDURE:

1-Introduction

This lab is a tutorial on Cadence Virtuoso, which is the simulation tool we will use for the rest of the semester. The official program name is Virtuoso, but the common name among users is just Cadence. We will use the name Cadence in this class.

Cadence Setup and Launch

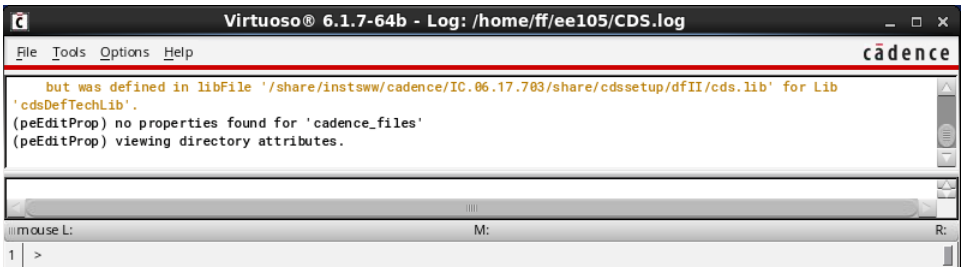
- Make sure your system is connected to JIIT network
- Right click on desktop and open Terminal.
- Then type following commands

  csh ←

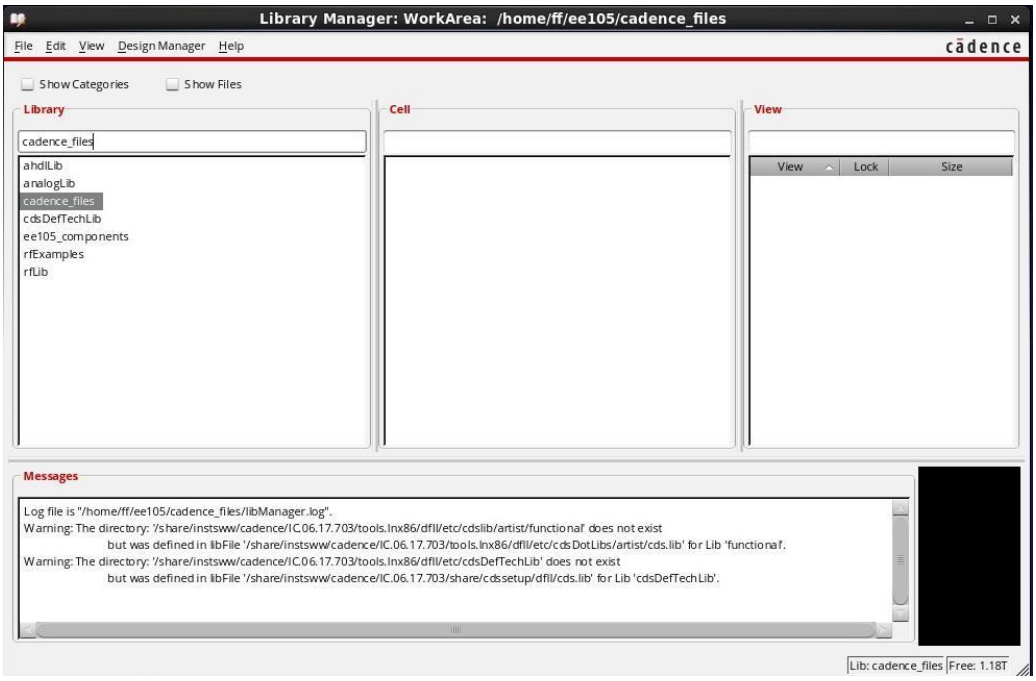
  source /home/install/cshrc ←
- A new window will be open then type here

  Virtuoso &←

After opening Cadence, you'll see the main window: -



Go to Tools->Library Manager, it should open the following window: -



The hierarchy in Cadence is:
Library (left side) -> Cell (middle) -> View (right).
A library contains multiple cells, and each cell contains multiple views. The ***libraries*** that we will use in this tutorial are: -

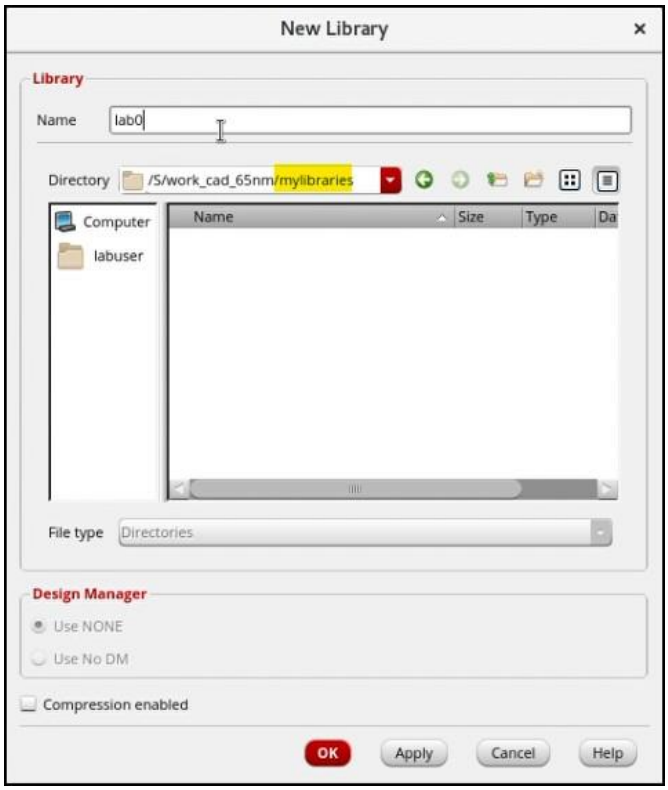
- **analogLib** - the basic analog components (resistors, capacitors, voltage and current sources, etc)
- **umc65ll** - the actual components that we will use in the lab (transistors, diodes, opamps, ...). Wewon't use them in this tutorial.
- **lab0** - your designs

The ***views*** that we will use for each cell are: -

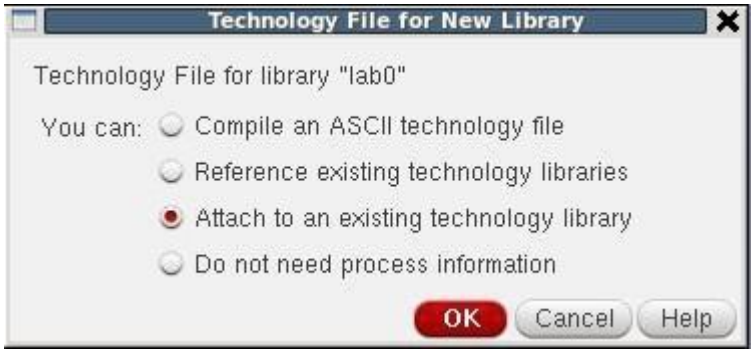
- **schematic** - the actual circuit, the components and interconnections
- **spectre** - the simulation setup
- **symbol** - the appearance of the cell in another schematic view

Creating a new Library: -

To create a new library, go to the library manager and click File → New → Library. A new windowwill pop up. Go into "**my libraries**" folder & type "**lab0**" in the name field and press OK.



At this point, Cadence will prompt you for something called a Technology File. The technology file is collection of information and libraries that define the layers and devices available for a given process technology.



For this class, we will use gpdk 180 technology file. Therefore, go ahead and choose 'Attach to an existing technology library'.

Creating a new schematic: -

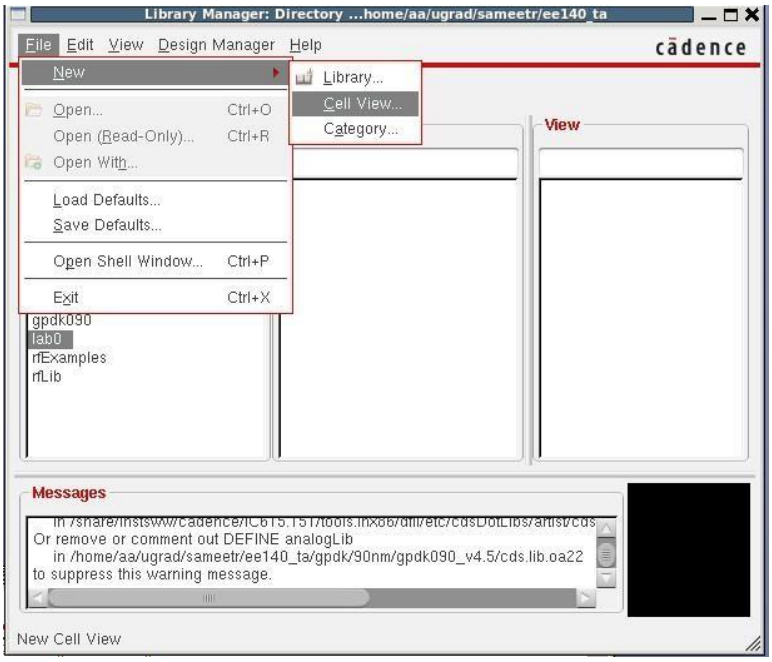
To create a new schematic design:

Click on the **lab0** library in the

Library Manager. File -> New ->

Cell View

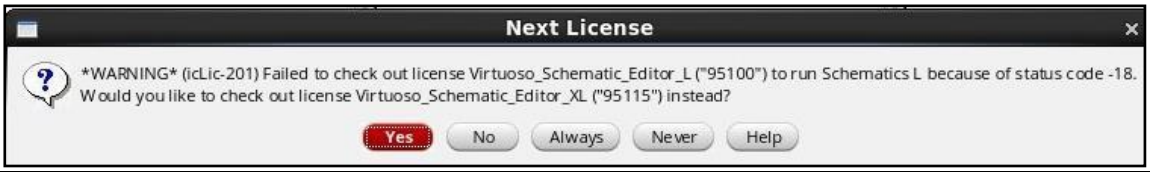
A new window pops up, but it may be at the background: -



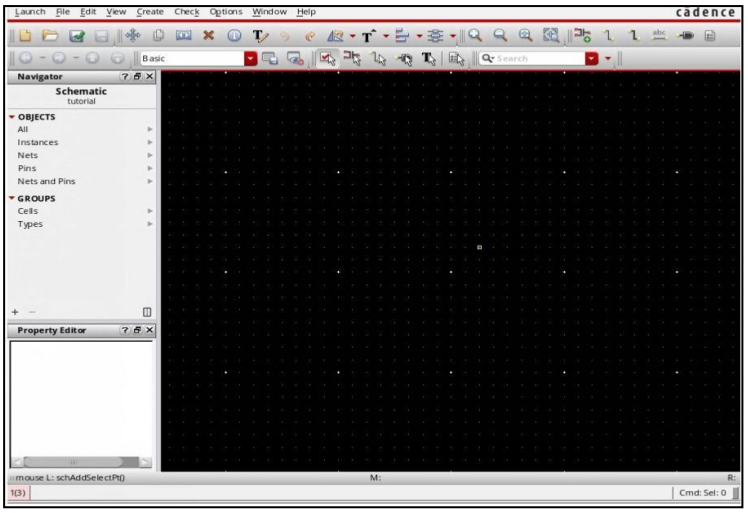
This is a general tip in Cadence - if you expect a window to open and it's not there, check the taskbar!

We will give it a name "tutorial", the type should be "schematic". Note that you can make cells in any available library by choosing proper one from **'Library'** (if you have permissions to edit).

Click OK. The following window will open:

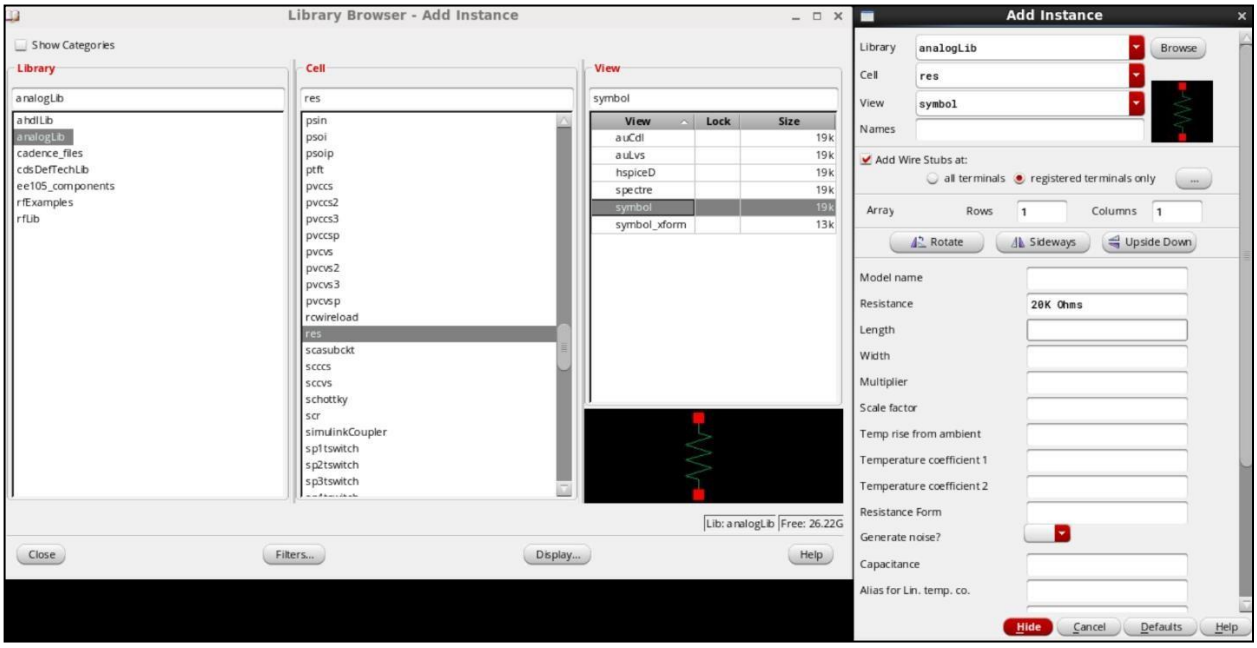


Click "Always" to avoid getting this message later. The schematic window will open:
This is the main window where we'll draw our circuit. Generally, we won't use the menus, but key board shortcuts.



Adding components: -To add an element, click "i". The following window will appear: -

You can type the library, cell and view names, or click Browse:
Select "analogLib" library, "res" cell and "symbol" view. Another window will open:



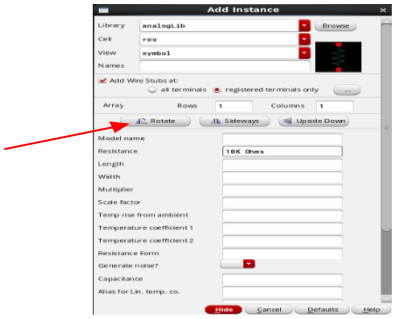
Here you specify the parameters of the component. A resistor has a single parameter (resistance), change it to 20kΩ.

In Cadence you don't have to write the units (Ohms, volts, etc.). For the resistance, type 20k and hit Tab. The Ohms will be automatically completed. The useful prefixes in Cadence are single letters: p - pico, n - nano, u - micro, m - milli, k - kilo, M - mega, G – giga.

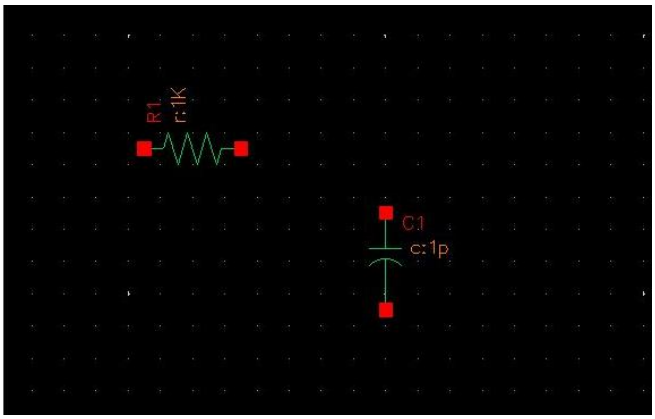
Click on the schematic window to place the resistor. The useful components in the analogLib library are:

res	Resistor
cap	Capacitor
gnd	Ground
vdc/idc	DC voltage/current source
vsin/isin	Sinusoidal voltage/current source
vpulse/ipulse	Square-wave voltage/current source
iprobe	Current meter

Now add another resistor of 10kΩ. Click "Rotate" to make it horizontal and place it on the schematic:



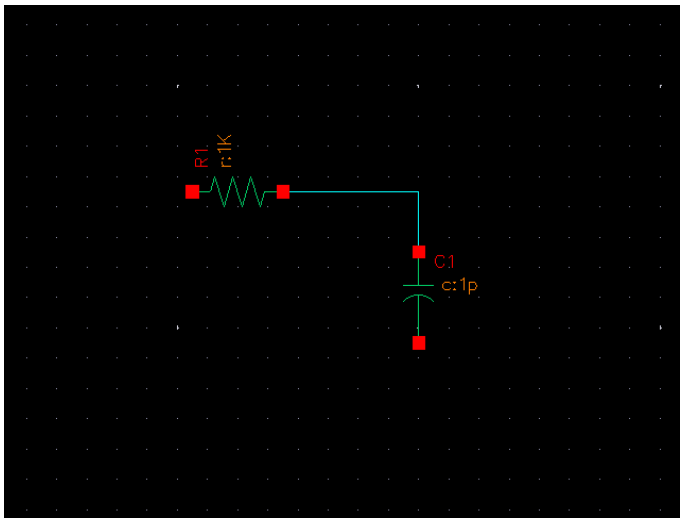
Your schematic should look like this:



Adding wires and labels: -

To connect the resistors with a wire, click "w". Click on the first terminal to connect, and then on the next terminal which you want connect.

To create a wire label, click "l" (lowercase L). Type out and click on the wire. Click Esc. Nowyou have the following schematic:



Labels can be used to connect nodes. If you want to connect two nodes in your circuit, you can give them the same label, without connecting them with a wire. It is usually useful for large circuits, to reduce the number of wires. Labels are also useful for output expressions, as we will see later.

Other useful shortcuts Components: - click on the desired component, then click:

- **c** - copy component
- **m** - move component (preserves the wire connections)
- **Shift+M** - move component (without the wire connections)
- **q** - edit component properties (same window as the add component window)
- **f** - fits the circuit to fit the screen
- **mouse scroll** - zoom in and out
- **z** - selects area to zoom
- **Shift+X** - check and save. Check that all nodes are connected properly. If you have errors, you have to fix them to simulate the circuit. You can run simulations if you have warnings. Pay attention to the warnings, usually they indicate a problem in your circuit, like unconnected nodes.

2-Transient simulation of RC circuit: -

The RC circuit shown in fig. is a low pass filter having 3-dB cut-off frequency is f_c, where $f_c = 1/2\pi RC$

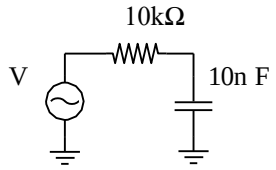


Figure 1: RC circuit

A capacitor has the ability to store an electrical charge and energy. The voltage across the capacitor is related to the charge by the equation V=Q/C for steady state values, or expressed as an instantaneous value dv=dq/C.

We will study the transient response of the RC circuit, which is the response to a sudden change in voltage.
In this experiment, we apply a pulse waveform to the RC circuit to analyze the transient response of the circuit. The pulse-width relative to a circuit's time constant determines how it is affected by an RC circuit.

Time Constant (τ): A measure of time required for certain changes in voltages and currents in RC and RL circuits. Generally, when the elapsed time exceeds five time constants (5τ) after switching has occurred, the currents and voltages have reached their final value, which is also called steady-state response.
The time constant of an RC circuit is the product of equivalent capacitance and the Thévenin resistance as viewed from the terminals of the equivalent capacitor.

$$\tau = RC$$

A Pulse is a voltage or current that changes from one level to the other and back again. If a waveform's high time equals its low time, it is called a square wave. The length of each cycle of a pulse train is termed its period (T).

The pulse width (tp) of an ideal square wave is equal to half the time period. The relation between pulse width and frequency is then given by,

$$f = 1/2t_p$$

From Kirchoff's laws, it can be shown that the charging voltage VC (t) across the capacitor is given by:

$$V(t) = V(1 - e^{-t/RC}),\ t \geq 0$$

Where, V is the applied source voltage to the circuit for $t \geq 0$. $\tau = RC$ is the time constant.
The response curve, showing capacitor charging for Series RC circuit to a step input with time axis normalized by τ is shown in Fig. 2.

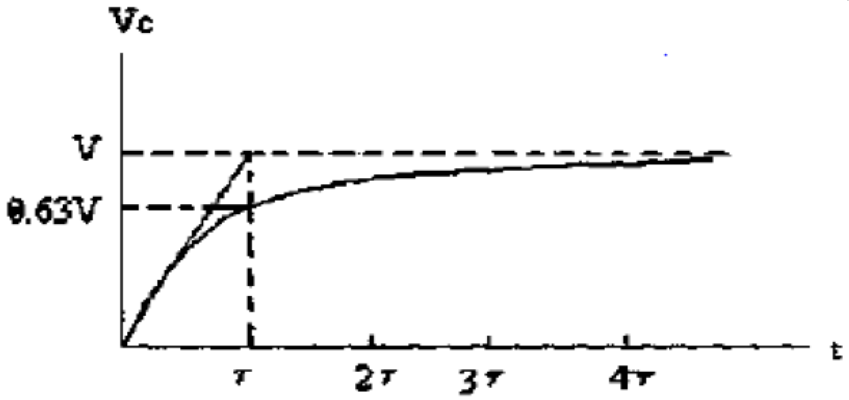
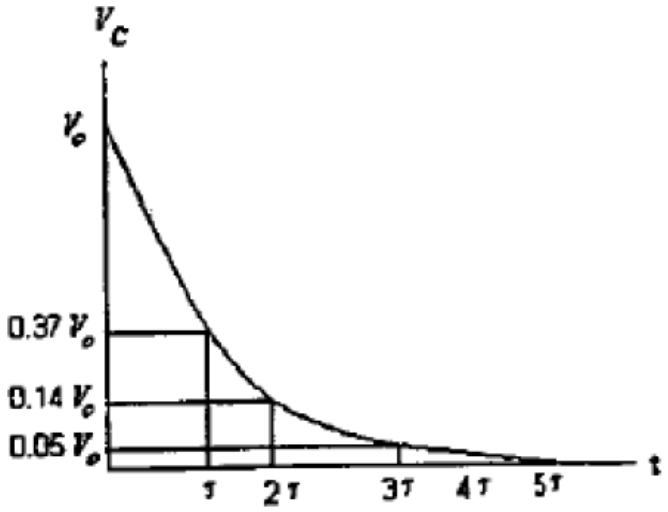


Fig. 2.

The discharge voltage for the capacitor is given by:

$$V(t) = V_o e^{-t/RC}\,,\ t \geq 0$$

Where V_o is the initial voltage stored in capacitor at t = 0, and τ=RC is time constant. The response curve is a decaying exponentials as shown in Fig. 3.



t	$e^{-t/\tau}$
τ	0.37
2τ	0.14
3τ	0.05
4τ	0.02
5τ	0.01

Fig. 3.

Now you can design the following RC circuit, Click Shift+X to check and save your schematic.

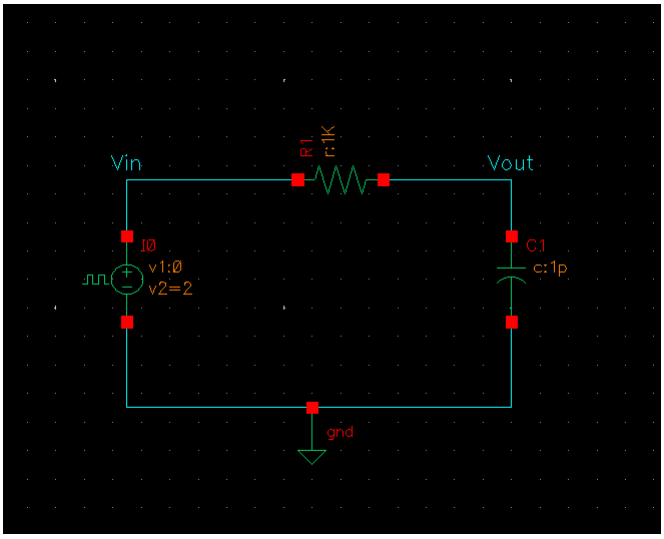
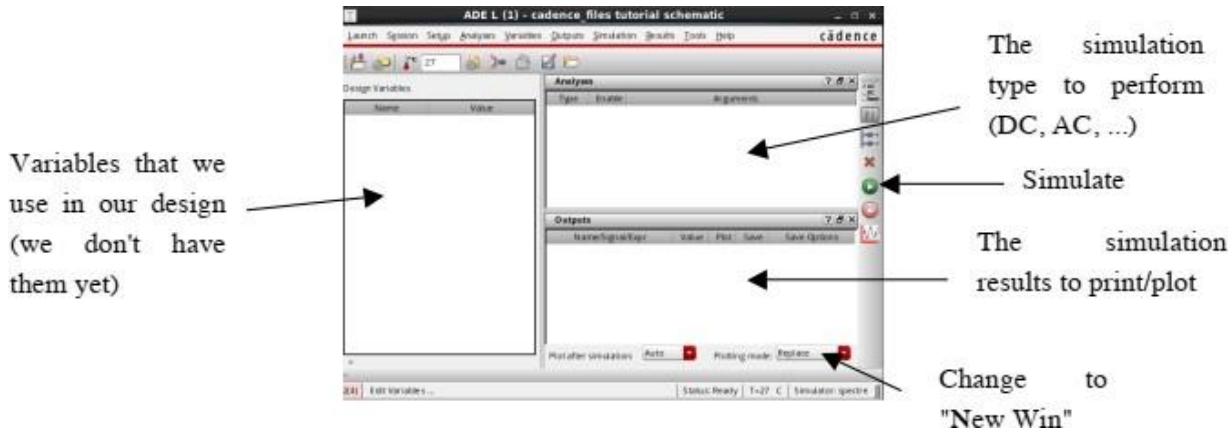


Fig. 1: Design RC circuit

To open the simulation window, click Launch -> ADE L. You will see the following window:
- Click "Always" to avoid getting this message later.



The ADE window will open:

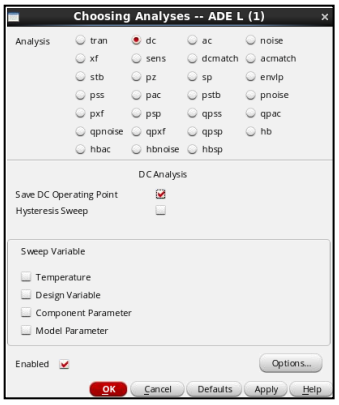
The Analysis box - specifying the simulation type

In the Analysis box: right click -> Edit.

Here we select the different simulation types for our schematic. The useful simulations in our class are:

- **dc** - DC simulation. Only DC sources are used, and the results are DC voltages and DC currents. This is in general a non-linear analysis (unless we only have linear components, like in our case).
- **ac** - AC simulation. This is a linear phasor analysis of the circuit. The simulation result is a phasor (magnitude and phase) of the voltages and the currents in our circuit. We can use it to calculate the transfer function from the input to the desired output. Here we define the frequency range to perform the simulation.
- **tran** - transient simulation. This is a non-linear time-domain simulation. The simulation results are time-domain waveform of the voltages and the currents in our circuit.

In this part of the tutorial we will perform a DC simulation. Select dc, and check "Save DC operatingpoint":



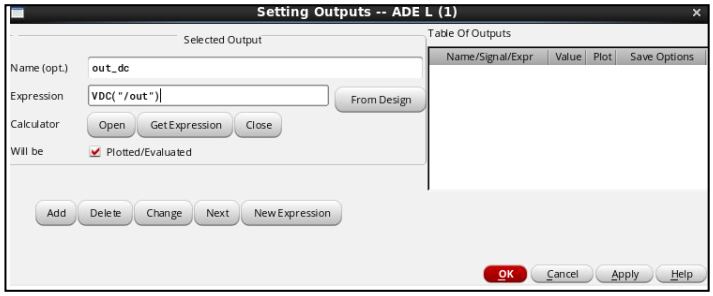
Click OK.

The Outputs box - specifying the simulation outputs

After performing the simulation, we should specify the results that we are interested in.In the Outputs box: right click -> Edit.

In the Name section type: out_dc.

In the Expression section, type: V_{DC}("/out"):



Click OK.

We created an output expression named "out_dc" for the DC voltage at the node "out".

A very useful tool in Cadence for the output expressions syntax is the calculator. In the main ADE window: Tools -> Calculator. At the bottom, you have a list of the various functions that can be performed on the simulation results. If you are not sure about the command syntax, the Calculator is a very useful place to start.

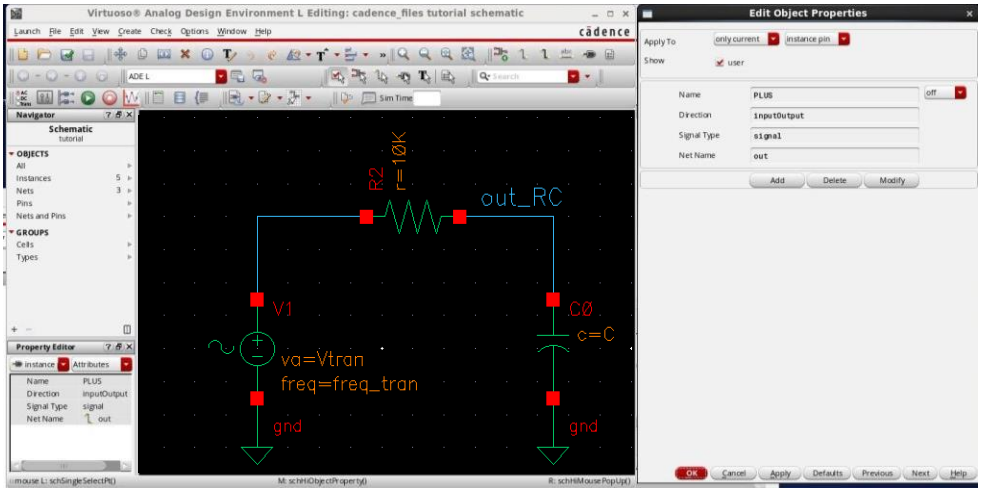
The syntax for the output expressions is:

V_{DC}/I_{DC}	DC voltage/current (dc analysis)
VF/IF	AC voltage/current (ac analysis)
VT/IT	Transient voltage/current (tran. analysis)

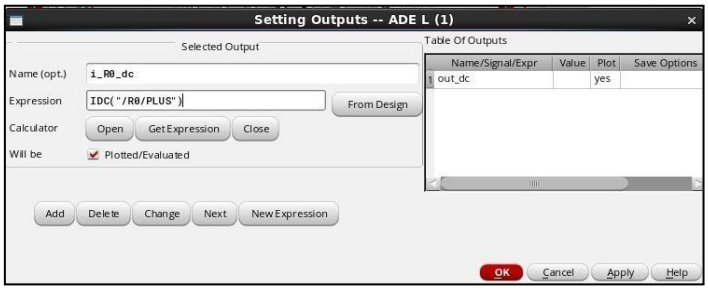
For voltage outputs, the syntax is V_{DC} ("**/node_name**"). For current output, the syntax is I_{DC} ("**/component_name/terminal name**").

In our circuit to see the terminal name of the 10k resistor connected to "out", click on it (the redsquare) and press **q**.

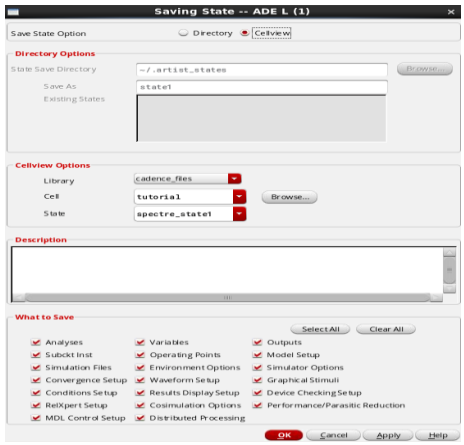
You will see the following window:



So, the component name is R0 and the terminal name is PLUS. For the output DC current through thisnode add the following output expression: I_{DC}("/R0/PLUS"):



Another option is to click on idc in the Calculator, and then click on the resistor terminal.To save your simulation setup: Session -> Save State. At the top change to "Cell view":



Click OK. It will a view named "spectre_state1" in the "tutorial" cell.

Click the "play" button to perform the simulation. You should see the simulated DC voltage and current at the Value column. Add the screenshot of the ADE window with the simulated result to your lab worksheet.

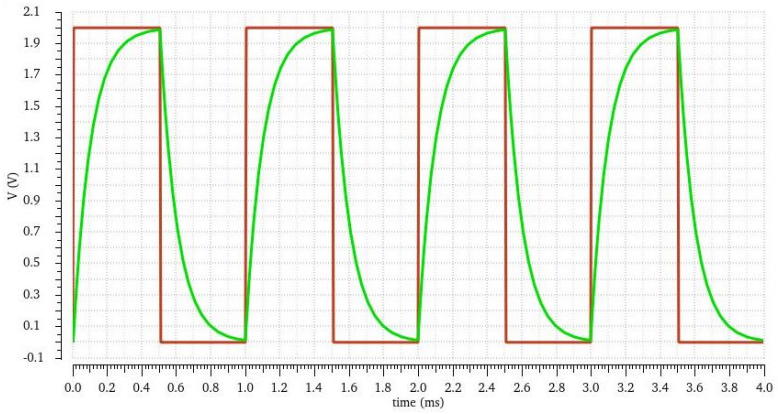


Fig. 5 -Transient response of RC circuit.

EXPERIMENT NO: - 2

AIM: - To study the I-V characteristics of NMOS and PMOS transistors.

TOOLS REQUIRED: PC,CADENCE TOOLS

CIRCUIT DIAGRAM: - NAND Gate Schematic

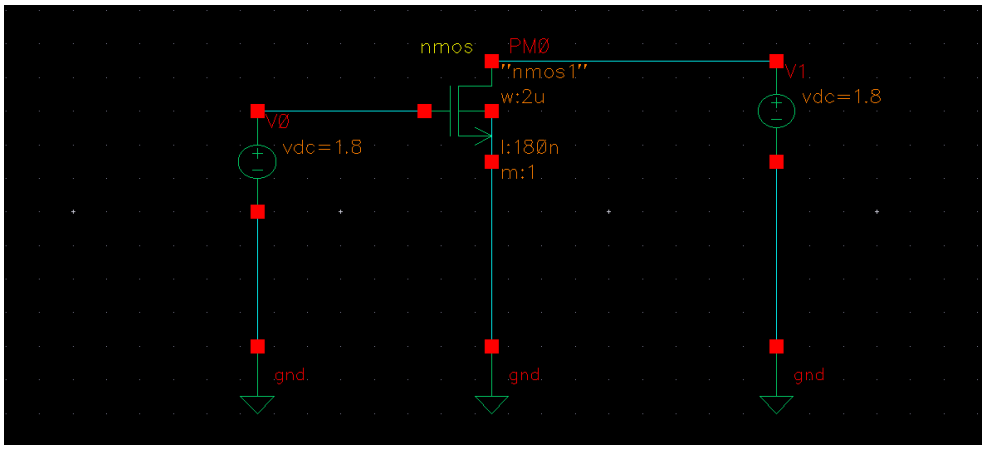


Fig. 1- Test Setup for the NMOS Transistor

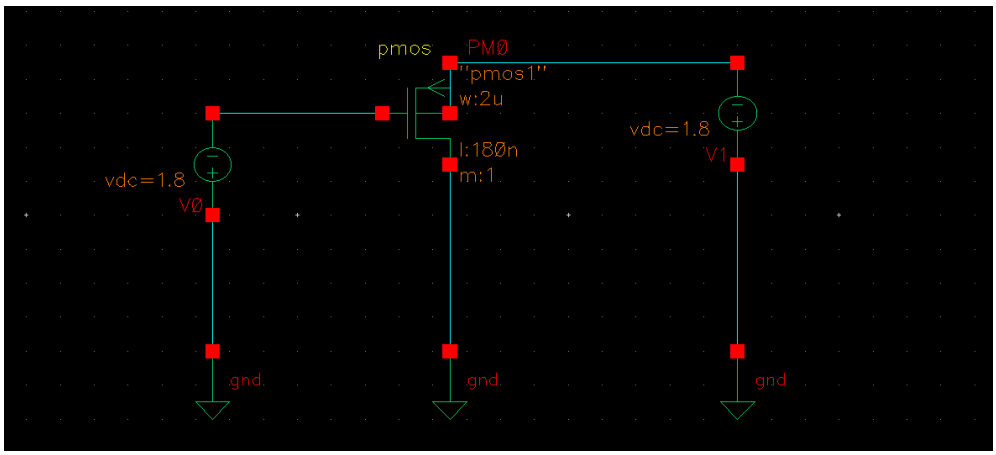


Fig. 2-Test Setup for the PMOS Transistor

Procedure: -

(1)Creating a Schematic Cell view

In this section we will learn how to open new schematic window in the new library and build the NAND schematic as shown in the figure at the start of this lab.

- In the CIW or Library manager, execute **File – New – Cellview**.
- Set up the new file form cell name and schematic view.
- Click **OK** when done the above settings. A blank schematic window is designappears.

(a) Adding Components to schematic

- In the nand schematic window, click the **Instance** fixed menu icon to display the Add Instance form.(You can also execute **Create — Instance** or press **i**.)
- Click on the **Browse** button. This opens up a Library browser from which you can select components and the **symbol** view. You will update the Library Name, Cell Name, and the property values as you place each component.
- After you complete the Add Instance form, move your cursor to the schematic window and click **left** to place a component.

If you place a component with the wrong parameter values, use the **Edit— Properties— Objects** command to change the parameters. Use the **Edit— Move** command if you place components in the wrong location.
You can rotate components at the time you place them, or use the **Edit— Rotate** command after they are placed.

- After entering components, click **Cancel** in the Add Instance form or press **Esc** with yourcursor in the schematic window.

(b) Adding pins to Schematic

- Click the **Pin** fixed menu icon in the schematic window. You can also execut **Create — Pin** or press ***P.***
- The Add pin form appears.
- Type the pin name in the Add pin form in the exact order leaving space between the pin names. Make sure that the direction field is set to **input/output/inputOutput** when placing the **input/output/inout** pins respectively and the Usage field is set to **schematic**.
- Select **Cancel** from the Add – pin form after placing the pins.
  In the schematic window, execute **Window— Fit** or press the **f** bindkey.

(c) Adding Wires to a Schematic

- Click the **Wire (narrow)** icon in the schematic window.
- You can also press the ***w*** key, or execute **Create — Wire (narrow).**
- In the schematic window, click on a pin of one of your components as the first point for your wiring. A diamond shape appears over the starting point of this wire.
- Complete the wiring and when done wiring press **ESC** key in the schematic window.

Saving the Design

- Click the ***Check and Save*** icon in the schematic editor window.
- Observe the CIW output area for any errors.

(2) Starting the Simulation Environment

- In the schematic window, execute **Launch – ADE L .**
- The **Virtuoso Analog Design Environment (ADE)** simulation window appears.

(a) Choosing Analyses

- In the Simulation window (ADE), click the **Choose - Analyses** icon. You can also execute **Analyses - Choose.**
- To setup for transient analysis :
  In the Analysis section select- **dc**

(b) Selecting Outputs for Plotting

- Execute **Outputs – To be plotted – Select on Schematic** in the simulation window.
- Follow the prompt at the bottom of the schematic window, Click on output net $\mathbf{I_D}$. Press **ESC** with the cursor in the schematic after selecting it.

(c) Running the Simulation

- Execute **Simulation – Netlist and Run** in the simulation window to start the Simulation orthe icon, this will create the netlist as well as run the simulation.
- When simulation finishes, the DC plots automatically will be popped up along withlog file.

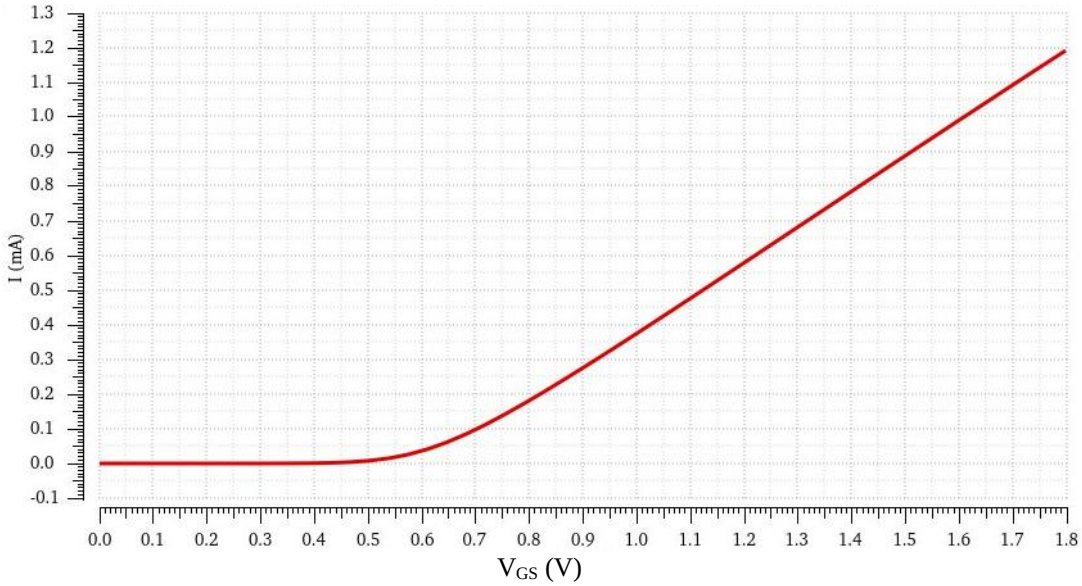


Fig. 3 Input transfer characteristics of NMOS

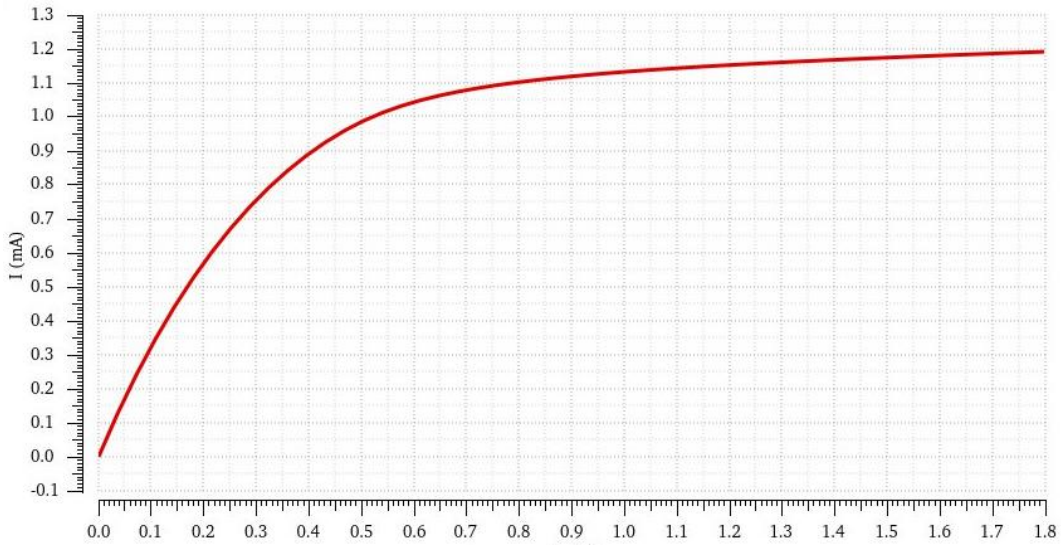


Fig. 4 Input transfer characteristics of PMOS

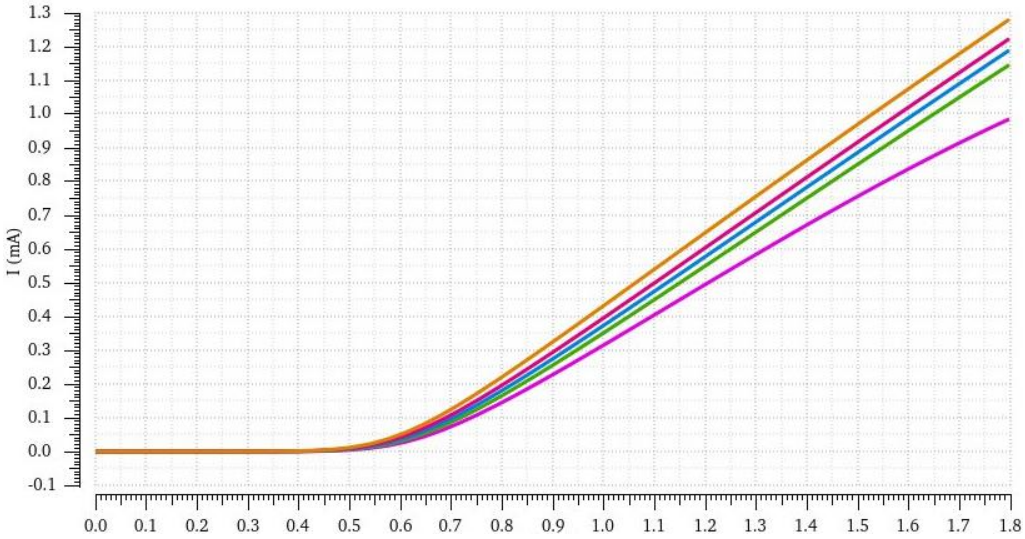


Fig. 5: Parametric Plot of the NMOS Transistor

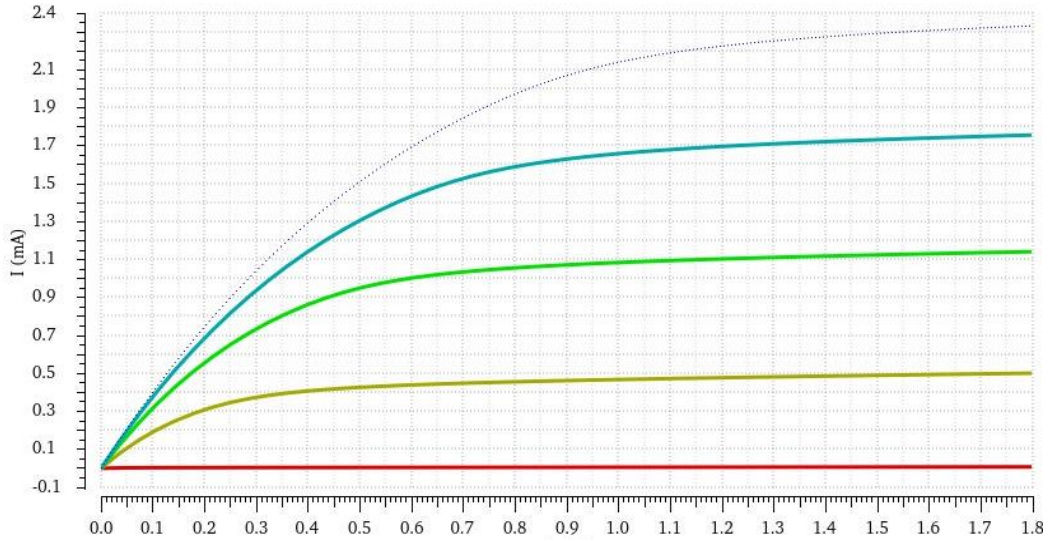


Fig. 6: Parametric Plot of the NMOS Transistor

RESULT: -

EXPERIMENT NO: 3

AIM: To obtain the NMOSFET parameters: k_n, V_{to}, V_t, γ and λ.

TOOLS REQUIRED: PC,CADENCE TOOLS

Theory of Transistor Operation: -

MOS transistors are the fundamental devices of CMOS integrated circuits. The schematic symbols for anNMOS and PMOS transistor are illustrated in Figure 1 and Figure 2, respectively.

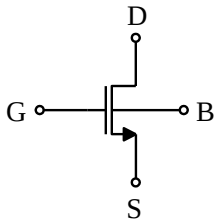


Fig. 1: NMOS Transistor

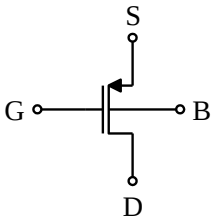


Fig. 2: PMOS Transistor

A cross sectional view of an NMOS transistor is shown in Figure 3. When the potential difference between the source (S) and the Drain (D) is small (~0 V), and a large potential (> V_{T0}) is applied between the gate (G) and source, the transistor will be operating in the linear or ohmic region. The positive gate potential causes electrons to gather below the surface of the substrate near the gate in a process called "inversion". This region of mobile charge forms a "channel" between the source and drain. The amount ofcharge is a function of the gate capacitance (C_{ox}) and the gate-to-source overdrive voltage:

$$Q_m = C_{ox}(V_{GS} — V_{T0})$$

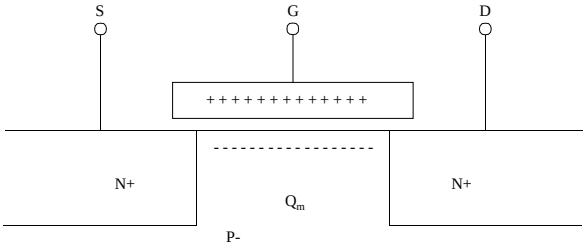


Fig. 3: Cross-Sectional View of an NMOS Transistor

The term V_{T0} is the threshold voltage. When the gate-to-source voltage (V_{GS}) exceeds this value, an inversion region is formed. Before reaching the inversion region, as the gate-to-source voltage is increased, the transistor passes through the accumulation region where holes are repelled from and electrons are attracted to the substrate region under the gate. Immediately before inversion, the transistor reaches the depletion region (weak-inversion) when the gate to source voltage is approximately equal to the threshold voltage. In this region a very small current flows.

In the linear region, the MOSFET acts a voltage controlled resistor. Resistance is determined by V_{GS}, transistor size, and process parameters.

When the drain-to-source voltage (V_{DS}) is increased, the quantity and distribution of mobile charge carriersbecomes a function of V_{DS} as well. Now the total charge is given by:

$$Q_m = C_{ox}(V_{GS} - V_T - V_{DS})$$

The threshold voltage (now denoted as V_T) becomes a function of V_{DS}. This distribution of this charge is such that Q_m is greater near the source and less near the drain. To find the channel conductance, the charge must be recast as a function of position $Q_m(y)$ and integrated from the source to drain. Since the charge isa function of V_{DS}, the conductance depends on V_{DS}. The channel current becomes:

$$I_D = \mu_0 C_{OX} \frac{W}{L}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}$$

or

$$I_D = KP\frac{W}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS}$$

As V_{DS} increases, eventually the drain current saturates, That is, an increase in V_{DS} does not cause anincrease in current. The saturation voltage depends on V_{GS} and is given by:

$$V_{DS(sat)} = V_{GS} - V_T$$

The equation of the drain current becomes:

$$I_D = \frac{1}{2}KP\frac{W}{L}(V_{GS} - V_T)^2$$

At this point the transistor is operating in the saturation region. This region is commonly used for amplification applications. In saturation, I_D actually depends weakly on V_{DS} with the parameter λ. Also, thethreshold voltage depends on the bulk-to-source voltage (V_{BS}) through the parameter γ. A better equation for the MOSFET (that includes the effects of V_{BS}) in saturation is given by:

$$I_D = \frac{1}{2}KP\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

When V_{GS} is less than the threshold voltage, the channel also conducts current. This region of operation is called weak-inversion or sub-threshold conduction. It is characterized by an exponential relationship between V_{GS} and I_D. Also, when V_{GS} becomes very large the charge carrier's velocity no longer increases with the applied voltage. This region is known as velocity saturation and has an I_D that depends linearly on V_{GS} as opposed to the quadratic relation shown above.

Figure 4 is a three-dimensional cross-sectional view of a MOSFET. Notice in the figure the overlap between the gate region and the active regions. The overlap forms parasitic capacitors C_{GS} and C_{GD}.

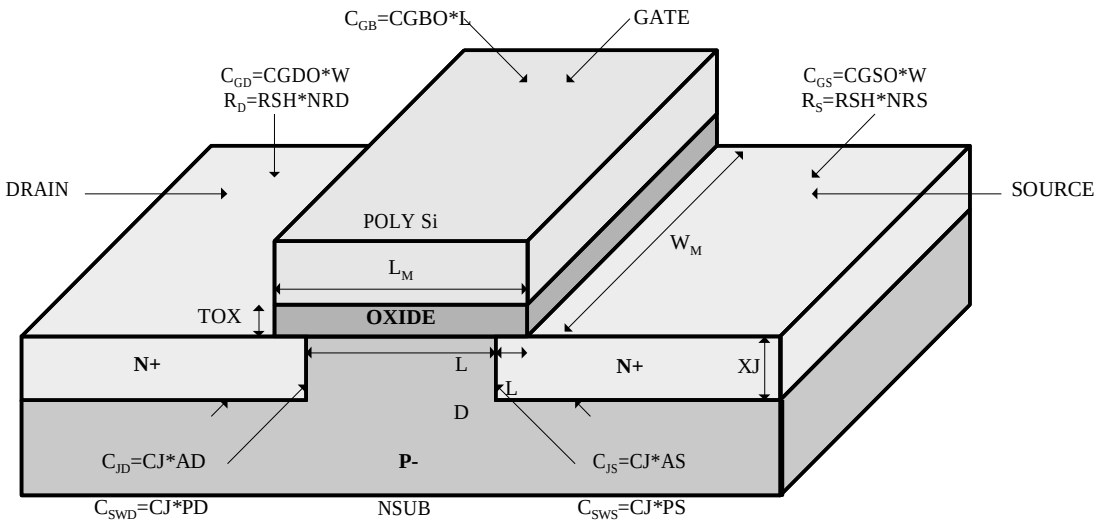


Fig. 4: Physical Structure of a MOSFET

The reverse-biased junctions between the active regions and the bulk form the parasitic capacitors C_{DB} and C_{SB}. The conductivity of the active regions forms the parasitic resistors R_D and R_S. A schematic symbol with these parasitic elements is illustrated in Figure 5.

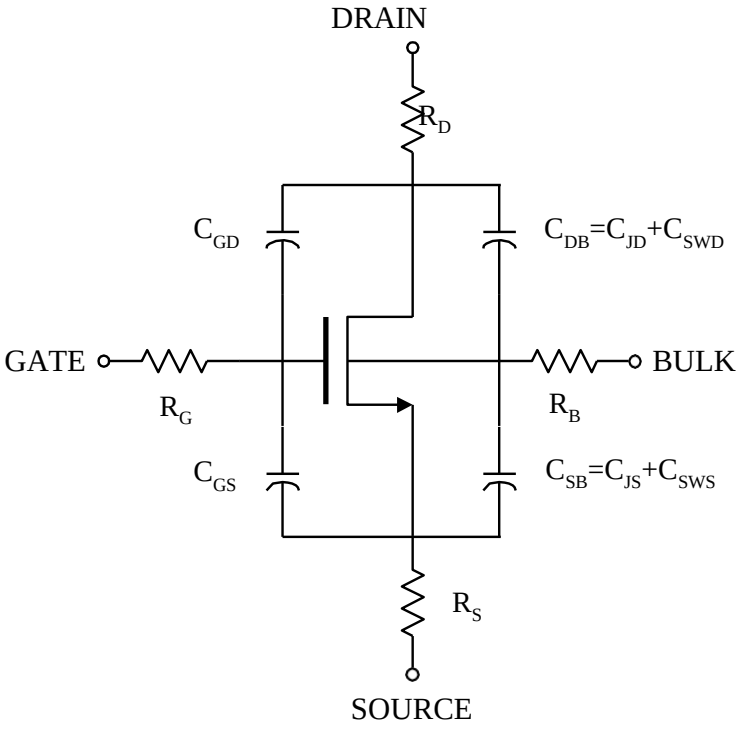


Fig. 5: MOSFET Parasitic Resistors and Capacitors

Device Characterization

To characterize the MOSFETs so that hand calculations can be done in the future, simulations need to be done to measure KP, V_{T0}, λ and γ. These parameters will be used in future labs, project and other assignments. We will be performing the calculation of the four parameters on two different device sizes for each of the two types of MOSFETs so that parameter variation may be observed. The test setups for the NMOS is shown in Figure 6.

Measuring λ

To measure λ you need to do a DC sweep of V_{DS} and plot I_D as shown in Figure 7. Each curve represents a different V_{GS} value. Any one of these curves can be used to calculate λ. Make sure that V_{BS} is 0V for this simulation. The formula for calculating λ given two points on the saturation portion of a single curve is:

$$\lambda = \frac{I_{D2} - I_{D1}}{I_{D1}V_{DS2} - I_{D2}V_{DS1}}$$

Measuring V_{T0}

V_{T0} can also be obtained from Figure 7. Using the saturation portion of two curves with equal V_{DS} then V_{T0} can be calculated as:

$$V_{T0} = \frac{V_{GS1} - V_{GS2}\sqrt{\frac{I_{D1}}{I_{D2}}}}{1 - \sqrt{\frac{I_{D1}}{I_{D2}}}}$$

Measuring K_p

Knowing λ and V_{T0}, K_P can easily be found from the equation for a MOSFET drain current in the saturationregion. A little algebra gives that K_P is:

$$KP = \frac{2I_D}{\frac{W}{L}(V_{GS} - V_{T0})^2(1 + \lambda V_{DS})}$$

Measuring γ

To obtain γ you must first give the transistor a non-zero V_{BS}. Next, calculate the new V_T using the same procedure that you used to obtain V_{T0} where $2\Phi_F = 0.7$ V. γ is given as:

$$\gamma = \frac{V_T - V_{T0}}{\sqrt{|2\Phi_F| + |V_{BS}|} - \sqrt{|2\Phi_F|}}$$

Additional Notes

While in graph mode, you can use the "M" key to insert a marker. The "A" and "B" keys will insert markersas well, except they will give the dx, dy and slope between the two points. The "H" key will generate a horizontal bar, and the "V" key will generate a vertical bar.

CIRCUIT DIAGRAM:

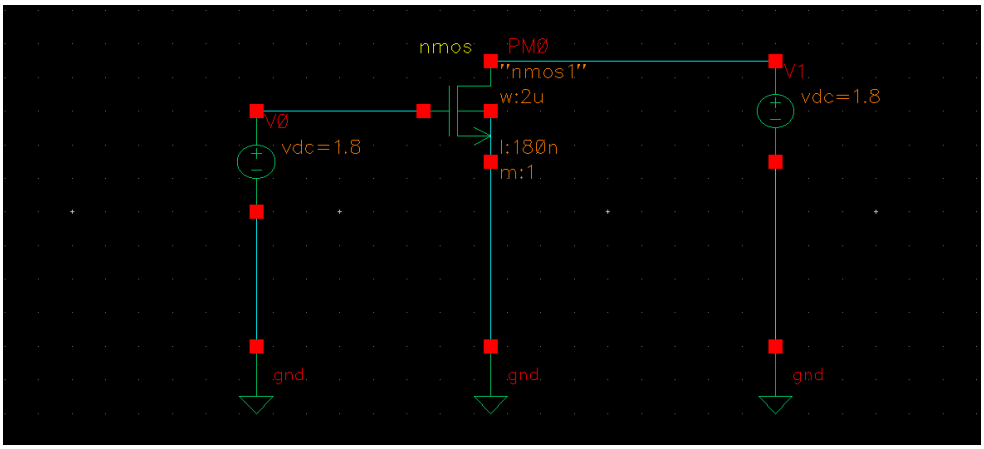


Fig. 6- Test Setup for the NMOS Transistor

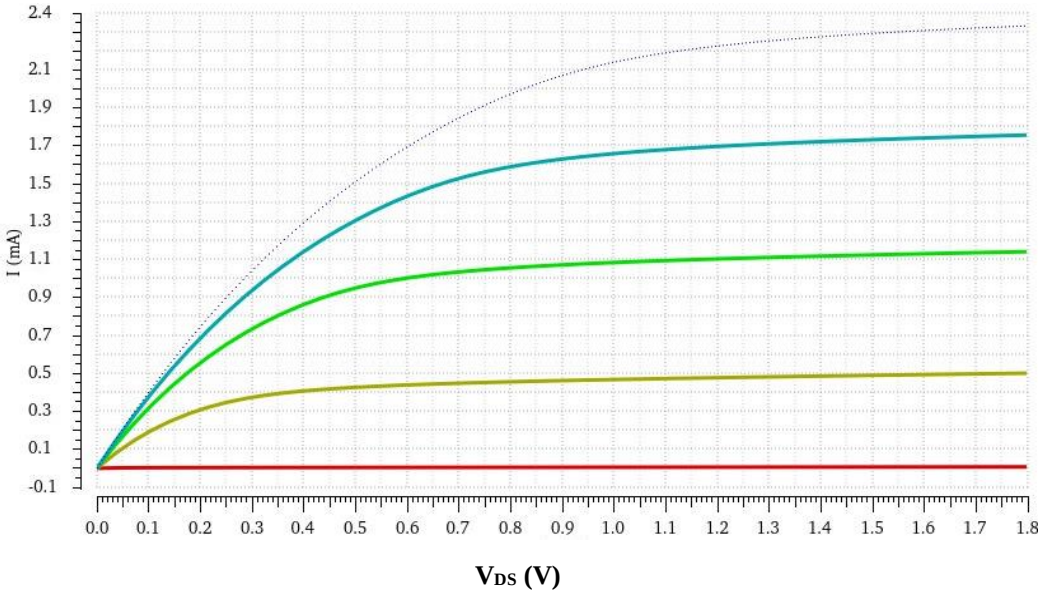


Fig. 7: Parametric Plot of the NMOS Transistor

RESULT: -

EXPERIMENT NO: - 4

AIM: - To analyze the voltage transfer characteristics (VTC) of resistive-load NMOS inverter and calculate V_{OH}, V_{OL}, V_{IH}, V_{IL} and V_{th}.

TOOLS REQUIRED: PC,CADENCE TOOLS

CIRCUIT DIAGRAM: - NAND Gate Schematic

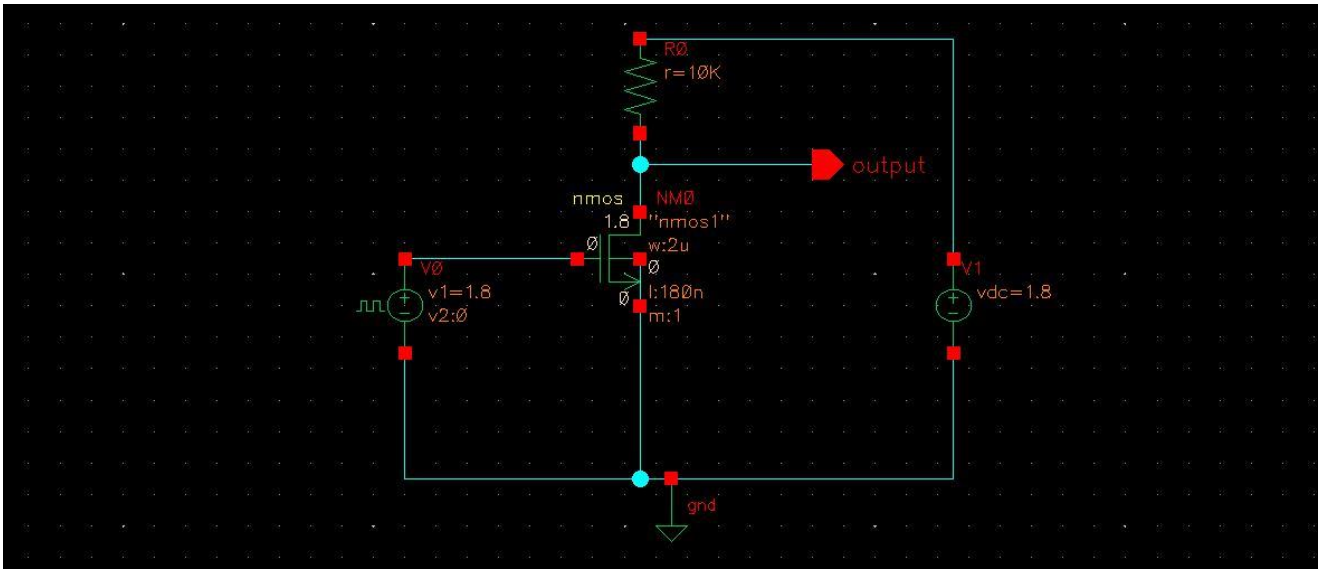


Fig. 1- Test Setup for the NMOS Transistor

Procedure: -

(1)Creating a Schematic Cell view

In this section we will learn how to open new schematic window in the new library and build the inverter schematic as shown in the figure at the start of this lab.

- In the CIW or Library manager, execute **File – New – Cellview**.
- Set up the new file form cell name and schematic view.
- Click **OK** when done the above settings. A blank schematic window for the **inverter** designappears.

(a) Adding Components to schematic

- In the nand schematic window, click the **Instance** fixed menu icon to display the AddInstance form.(You can also execute **Create — Instance** or press **i**.)
- Click on the **Browse** button. This opens up a Library browser from which you can select components and the **symbol** view. You will update the Library Name, Cell Name, and theproperty values as you place each component.
- After you complete the Add Instance form, move your cursor to the schematic window andclick **left** to place a component.

If you place a component with the wrong parameter values, use the **Edit— Properties— Objects** command to change the parameters. Use the **Edit— Move** command if you placecomponents in the wrong location.
You can rotate components at the time you place them, or use the **Edit— Rotate** command afterthey are placed.

- After entering components, click **Cancel** in the Add Instance form or press **Esc** with yourcursor in the schematic window.

(b) Adding pins to Schematic

- Click the **Pin** fixed menu icon in the schematic window. You can also execut **Create — Pin** or press ***P.***
- The Add pin form appears.
- Type the pin name in the Add pin form in the exact order leaving space between the pin names. Make sure that the direction field is set to **input/output/inputOutput** when placingthe **input/output/inout** pins respectively and the Usage field is set to **schematic**.
- Select **Cancel** from the Add – pin form after placing the pins.
  In the schematic window, execute **Window— Fit** or press the **f** bindkey.

(c) Adding Wires to a Schematic

- Click the **Wire (narrow)** icon in the schematic window.
- You can also press the ***w*** key, or execute **Create — Wire (narrow).**
- In the schematic window, click on a pin of one of your components as the first point for yourwiring. A diamond shape appears over the starting point of this wire.
- Complete the wiring and when done wiring press **ESC** key in the schematic window.

Saving the Design

- Click the ***Check and Save*** icon in the schematic editor window.
- Observe the CIW output area for any errors.

(2) Starting the Simulation Environment

- In the schematic window, execute **Launch – ADE L .**
- The **Virtuoso Analog Design Environment (ADE)** simulation window appears.

(a) Choosing Analyses

- In the Simulation window (ADE), click the **Choose - Analyses** icon. You can also execute **Analyses - Choose.**
- To setup for transient analysis : In the Analysis section select- **dc**

(b) Selecting Outputs for Plotting

- Execute **Outputs – To be plotted – Select on Schematic** in the simulation window.
- Follow the prompt at the bottom of the schematic window, Click on output net $\mathbf{I_D}$. Press **ESC** with the cursor in the schematic after selecting it.

(c) Running the Simulation

- Execute **Simulation – Netlist and Run** in the simulation window to start the Simulation orthe icon, this will create the netlist as well as run the simulation.
- When simulation finishes, the DC plots automatically will be popped up along withlog file.

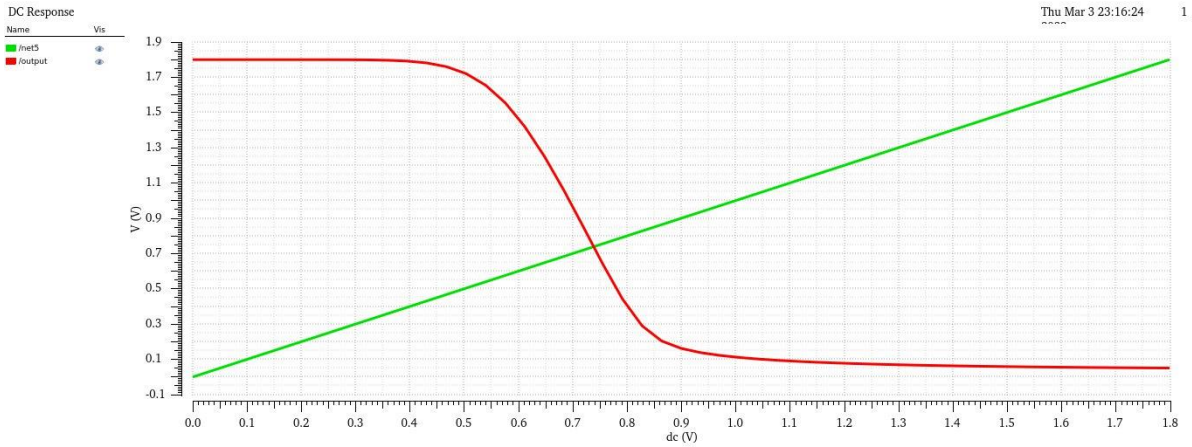


Fig. 2 transfer characteristics of resistive-load NMOS inverter

RESULT: -

EXPERIMENT NO: 5 & 6

AIM: (5) To analyze the voltage transfer characteristics (VTC) of CMOS inverter and calculate VOH, VOL, VIH, VIL and Vth.

(6) To analyze the transient response of CMOS inverter and calculate the propagation delay, rise time and fall time.

TOOLS REQUIRED: PC, CADENCE TOOLS.

CIRCUIT DIAGRAM:

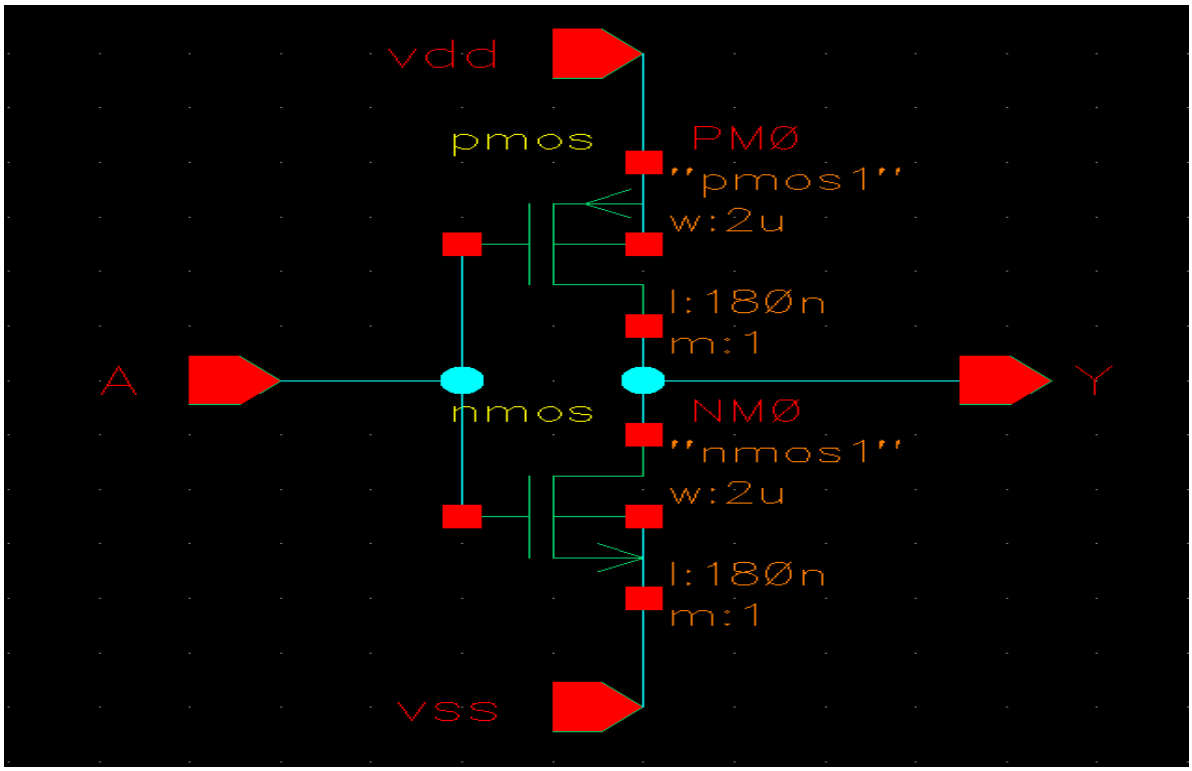


Fig. 1: Schematic of inverter

PROCEDURE:

Schematic Entry:

Objective: To create a library and build a schematic of an Inverter

Below steps explain the creation of new library "**myDesignLib**" and we will use the same throughout this course for building various cells that we going to create in the next labs. Execute **Tools – Library Manager** in the CIW or Virtuoso window to open Library Manager.

Creating a New library:

- In the Library Manager, execute **File - New – Library**. The new library form appears.

- In the "New Library" form, type "**myDesignLib**" in the Name section.In the field of Directory section, verify that the path to the library is set to **~/Database/cadence_analog_labs_613** and click **OK**.

  Note: A technology file is not required if you are not interested to do the layouts for the design.

- In the next "**Technology File for New library**" form, select option **Attach to an existing techfile** and click **OK**.

- In the "**Attach Design Library to Technology File**" form, select **gpdk180** from the cyclic field and click **OK**.

- After creating a new library you can verify it from the library manager.
  - If you right click on the "**myDesignLib**" and select properties, you will find that **gpdk180** library is attached as techlib to "**myDesignLib**".

Creating a Schematic Cell view

In this section we will learn how to open new schematic window in the new **myDesignLib**" library andbuild the inverter schematic as shown in the figure at the start of this lab.

- In the CIW or Library manager, execute **File – New – Cell view**.
- Set up the New file form as follows:Do not edit the **Library path file** and the one above might be different from the path shown in your form.

- Click **OK** when done the above settings. A blank schematic window for the **Inverter** design appears.

Adding Components to schematic

- In the Inverter schematic window, click the Instance fixed menu icon to display the Add Instance form. 
- **Tip:** You can also execute **Create — Instance** or press **i**.
- Click on the **Browse** button. This opens up a Library browser from which you can select components and the **symbol** view .You will update the Library Name, Cell Name, and the property values given in the table on the next page as you place each component.
- After you complete the Add Instance form, move your cursor to the schematic window and click **left** to place a component.
- This is a table of components for building the Inverter schematic.

Library name	**Cell Name**	**Properties/Comments**
gpdk180	pmos	For M0: Model name = pmos1, **W= wp**, L=180n
gpdk180	nmos	For M1: Model name = nmos1, W= 2u, L=180n

- If you place a component with the wrong parameter values, use the **Edit— Properties— Objects** command to change the parameters.
- Use the **Edit— Move** command if you place components in the wrong location.

- You can rotate components at the time you place them, or use the **Edit— Rotate** command after they are placed.

Adding pins to Schematic

- Click the **Pin** fixed menu icon in the schematic window. You can also execute **create — Pin** or press ***p***.  The Add pin form appears.
- Type the following in the Add pin form in the exact order leaving space between the pin names.

Pin Names	Direction
vin	Input
vout	Output

- Make sure that the direction field is set to **input/output/inputOutput** when placing the **input/output/inout** pins respectively and the Usage field is set to **schematic**.
- Select **Cancel** from the Add – pin form after placing the pins. In the schematic window, execute **Window— Fit** or press the **f** bindkey.

Adding Wires to a Schematic

Add wires to connect components and pins in the design.

- Click the **Wire (narrow)** icon in the schematic window.
- You can also press the ***w*** key, or execute **Create — Wire (narrow).**
- In the schematic window, click on a pin of one of your components as the first point for your wiring. A diamond shape appears over the starting point of this wire.
- Follow the prompts at the bottom of the design window and click **left** on the destination point for your wire. A wire is routed between the source and destination points.
- Complete the wiring as shown in figure and when done wiring press **ESC** key in the schematic window to cancel wiring.

Saving the Design

- Click the **Check and Save** icon in the schematic editor window.
- Observe the CIW output area for any errors.

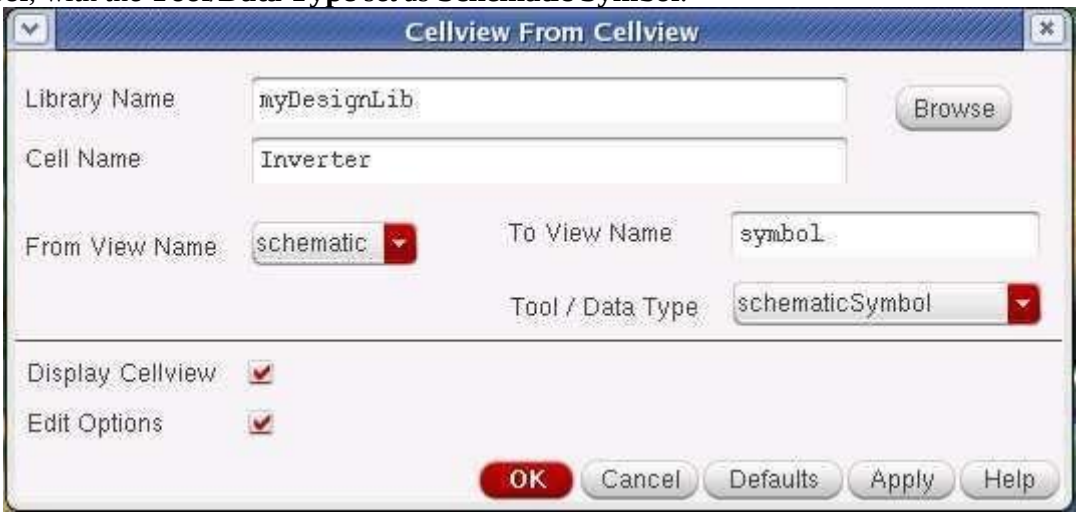
Symbol Creation

In this section, you will create a symbol for your inverter design so you can place it in a test circuit for simulation. A symbol view is extremely important step in the design process. The symbol view must exist for the schematic to be used in a hierarchy. In addition, the symbol has attached properties (cds Param) that facilitate the simulation and the design of the circuit.

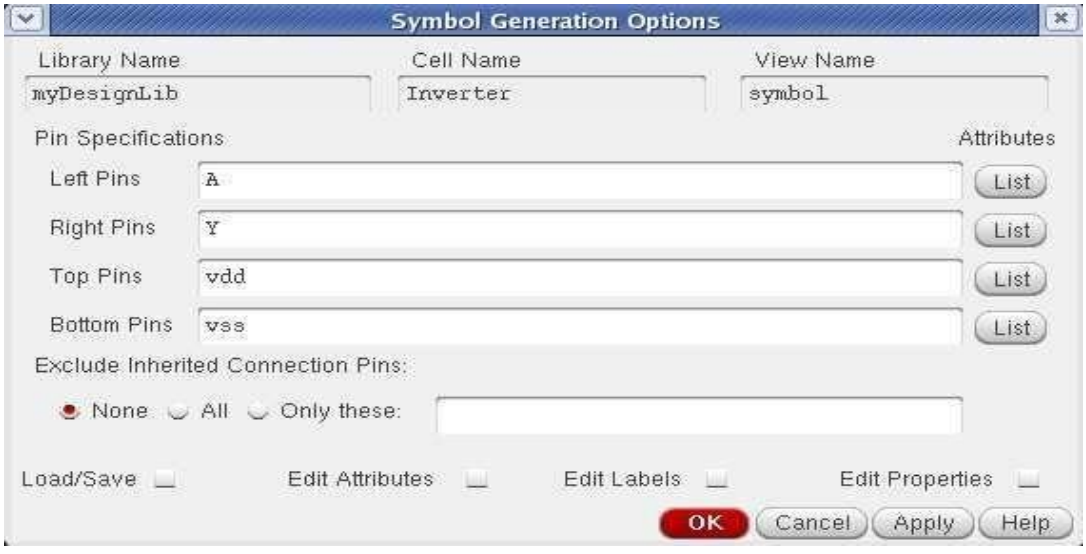
- In the Inverter schematic window, execute **Create — Cellview— From Cellview**.
- The **Cellview From Cellview** form appears. With the Edit Options function active, you can control the

appearance of the symbol to generate.

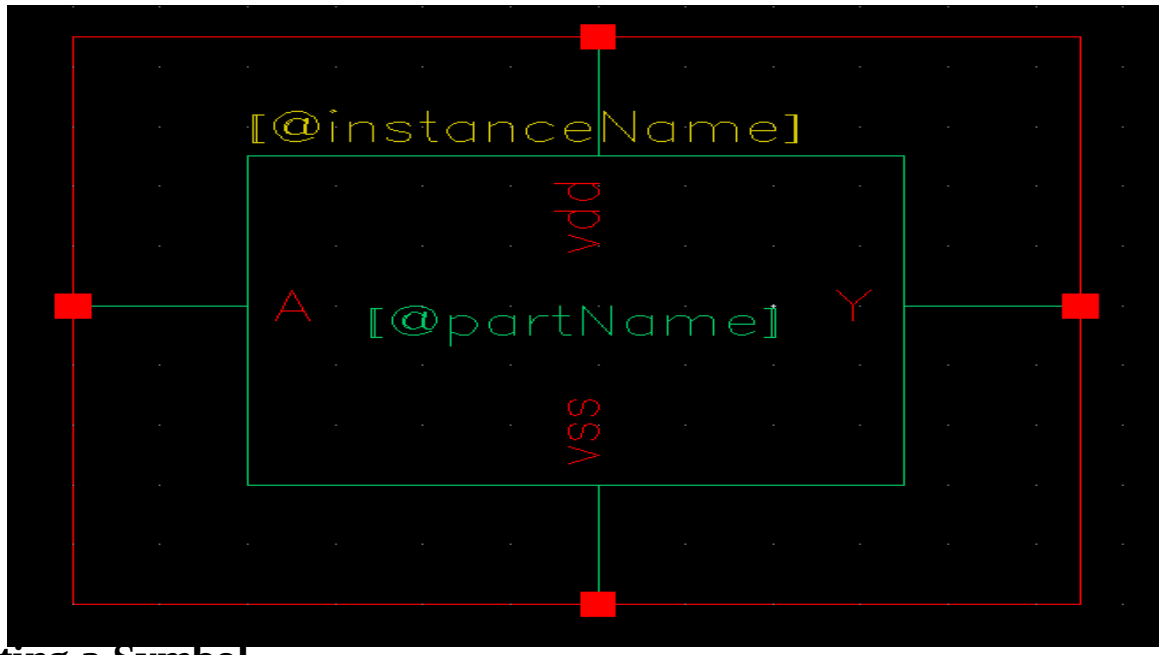
- Verify that the **From View Name** field is set to **schematic**, and the **To View Name** field is set to **symbol**, with the **Tool/Data Type** set as **Schematic Symbol**.



- Click **OK** in the **Cellview From Cellview** form.
- The Symbol Generation Form appears.
- Modify the **Pin Specifications** as follows:



- Click **OK** in the Symbol Generation Options form.
- A new window displays an automatically created Inverter symbol as shown here.



Editing a Symbol

In this section we will modify the inverter symbol to look like a Inverter gate symbol.

Move the cursor over the automatically generated symbol, until the green rectangle is highlighted, click

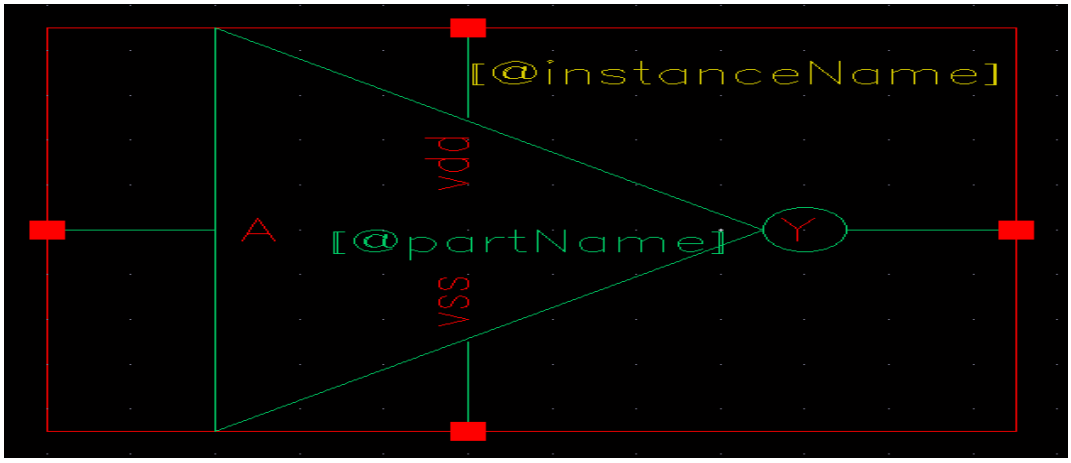
left to select it.

- Click **Delete** icon in the symbol window, similarly select the red rectangle and delete that.
- Execute **Create – Shape – polygon**, and draw a shape similar to triangle.
- After creating the triangle press ***ESC*** key.
- Execute **Create – Shape – Circle** to make a circle at the end of triangle.
- You can move the pin names according to the location.
- Execute **Create — Selection Box**. In the Add Selection Box form, click
- **Automatic**.A new red selection box is automatically added.
- After creating symbol, click on the ***save*** icon in the symbol editor window to save the symbol. In the symbol editor, execute **File — Close** to close the symbol view window.

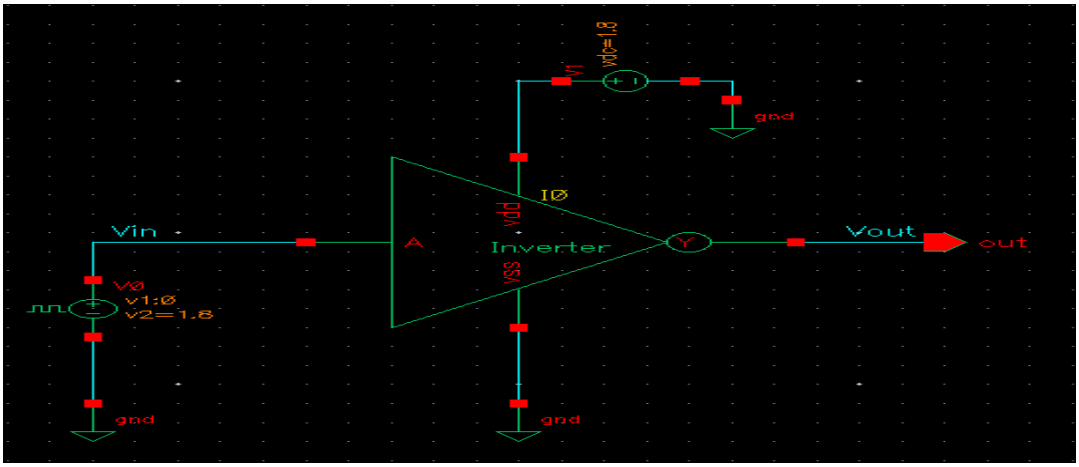
Building the Inverter_Test Design: Creating the Inverter_Test Cellview

You will create the Inverter_Test cellview that will contain an instance of the Inverter cellview. In the nextsection, you will run simulation on this design

- In the CIW or Library Manager, execute **File— New— Cellview**.
- Set up the New File form as follows:



- Click **OK** when done. A blank schematic window for the **Inverter_Test** design appears.



Building the Inverter_Test Circuit

- Using the component list and Properties/Comments in this table, build the Inverter_Test schematic.

Library name	Cellview name	Properties/Comments
myDesignLib	Inverter	Symbol

analogLib	vpulse	v1=0, v2=1.8,td=0 tr=tf=1ns,ton=10n, T=20n
analogLib	vdc, gnd	vdc=1.8

Note: Remember to set the values for V_{DD} and V_{SS}. Otherwise; your circuit will have no power.Add the above components using **Create — Instance** or by pressing **I**.

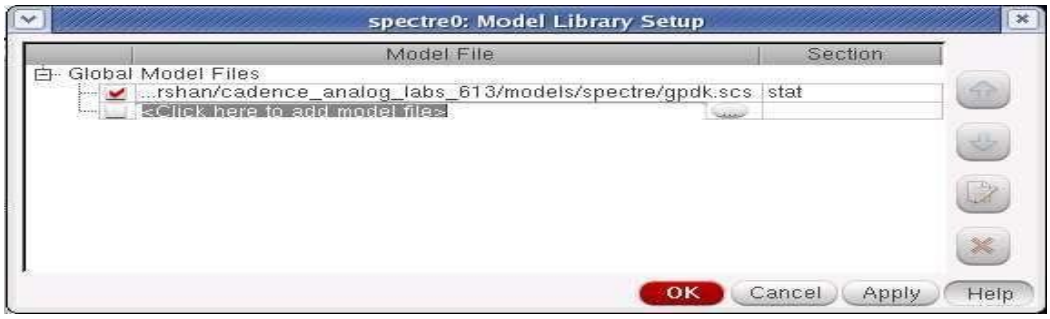
- Click the **Wire (narrow)** icon and wire your schematic.
- **Tip:** You can also press the **w** key, or execute **Create— Wire (narrow)**.
- Click **Create — Wire Name** or press **L** to name the input **(Vin)** and output **(Vout)** wires as in the below schematic.
- Click on the **Check and Save** icon to save the design.
- The schematic should look like this.
- Leave your **Inverter_Test** schematic window open for the next section.
- **Analog Simulation with Spectre:** To set up and run simulations on the Inverter_Test design
- In this section, we will run the simulation for Inverter and plot the transient, DC characteristics and we will do Parametric Analysis after the initial simulation.
- **Starting the Simulation Environment:**Start the Simulation Environment to run a simulation.
- In the **Inverter_Test** schematic window, execute
- **Launch – ADE L:**The Virtuoso Analog Design Environment (ADE) simulation window appears**.**

Choosing a Simulator

- Set the environment to use the **Spectre® tool**, a high speed, highly accurate analog simulator. Use this simulator with the **Inverte*r_Test*** design, which is made-up of analog components.
- In the simulation window (ADE), execute Setup— Simulator/Directory/Host.
- In the Choosing Simulator form, set the Simulator field to **spectre** (Not spectreS) and click **OK**.

Setting the Model Libraries:

- The Model Library file contains the model files that describe the nmos and pmos devices during simulation.
- In the simulation window (ADE), Execute **Setup - Model Libraries.** The Model Library Setup form appears. Click the **browse** button to add **gpdk.scs** if notadded by default as shown in the **Model Library Setup** form.
- **Remember** to select the section type as **stat** in front of the gpdk.scs file. Your Model Library Setup window should now looks like the below figure.



To view the model file, highlight the expression in the Model Library File field and Click **Edit F**

- To complete the Model Library Setup, move the cursor and click **OK**. The Model Library Setup allows you to include multiple model files. It also allows you to use the Edit button to view the model file.

Choosing Analyses

This section demonstrates how to view and select the different types of analyses to complete the circuitwhen running the simulation.

- In the Simulation window (ADE), click the **Choose - Analyses** icon.

You can also execute **Analyses - Choose.**

The Choosing Analysis form appears. This is a dynamic form, the bottom of the form changes based onthe selection above.

- To setup for transient analysis
  - **a.** In the Analysis section select **tran**
  - **b.** Set the stop time as **200n**
  - **c.** Click at the **moderate** or **Enabled** button at the bottom, and then click Apply.

- To set up for DC Analyses:
  - a. In the Analyses section, select **dc**.

b. In the DC Analyses section, turn on **Save DC Operating Point.**

c. Turn on the **Component Parameter**.

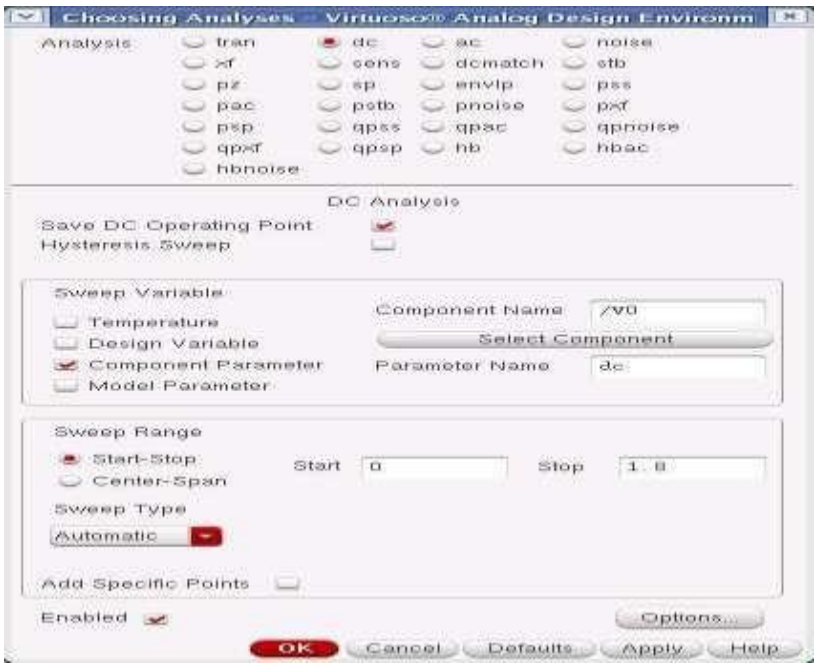
d. Double click the **Select Component**, Which takes you to the schematic window.

e. Select input signal **vpulse source** in the test schematic window.

f. Select **"DC Voltage"** in the **Select Component Parameter** form and click OK.

g. In the analysis form type **start** and **stop** voltages as **0** to **1.8** respectively.

h. Check the enable button and then click **Apply.**



- Click ***OK*** in the Choosing Analyses Form.

Setting Design Variables

Set the values of any design variables in the circuit before simulating. Otherwise, the simulation will notrun.

- In the Simulation window, click the **Edit Variables** icon.
- The Editing Design Variables form appears.
- Click **Copy From** at the bottom of the form. The design is scanned and all variables found in the design are listed. In a few moments, the **wp** variable appears in the Table of Design variables section.
- Set the value of the **wp** variable: With the **wp** variable highlighted in the Table of Design Variables, click on the variable name **wp** and enter the following:

Value(Expr)	2u

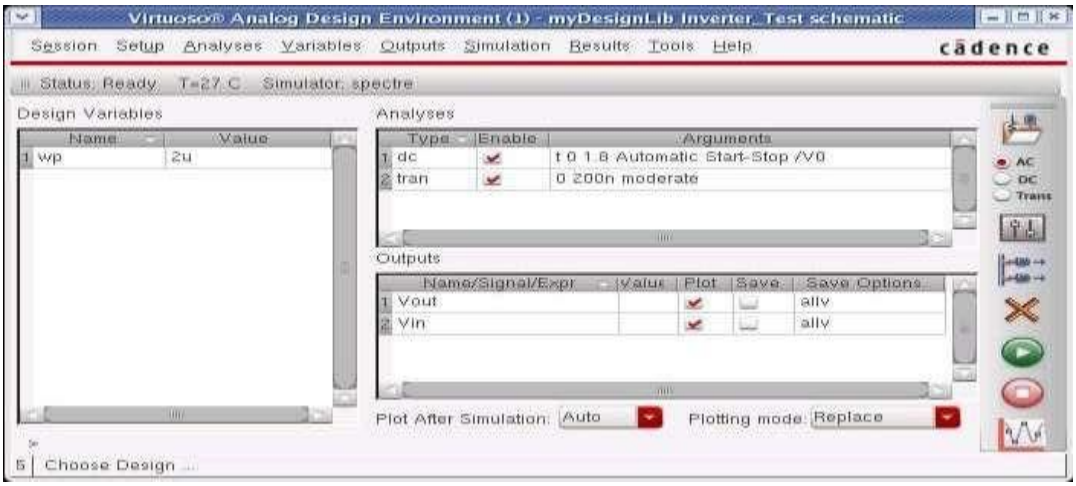
Click **Change** and notice the update in the Table of Design Variables.

- Click **OK** or **Cancel** in the Editing Design Variables window.

Selecting Outputs for Plotting

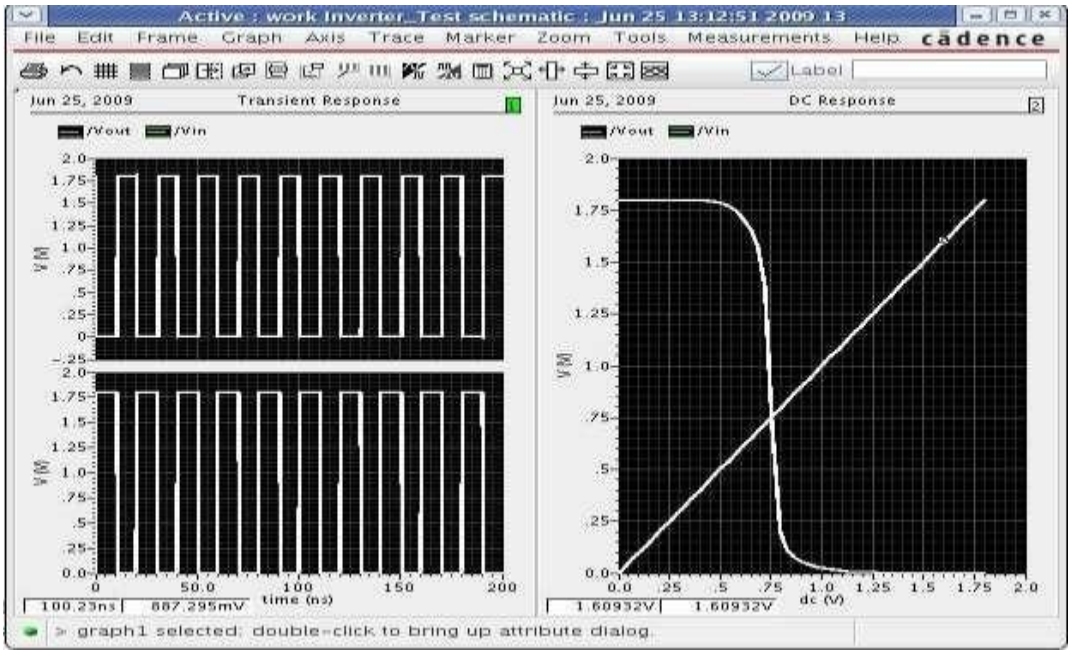
- Execute **Outputs – To be plotted – Select on Schematic** in the simulation window.
- Follow the prompt at the bottom of the schematic window, Click on output net **Vout**, input net **Vin** of the Inverter. Press **ESC** with the cursor in the schematic after selecting it.

Does the simulation window look like this?



Running the Simulation:

- Execute **Simulation – Netlist and Run** in the simulation window to start the
- Simulation or the icon, this will create the netlist as well as run the simulation.
- When simulation finishes, the Transient, DC plots automatically will be popped up along with log file.



Saving the Simulator State

We can save the simulator state, which stores information such as model library file, outputs, analysis, variable etc. This information restores the simulation environment without having to type in all of settingagain.

- In the Simulation window, execute **Session – Save State**. The Saving State form appears.
- Set the **Save as** field to **state1_inv** and make sure all options are selected under what to save field.
- Click **OK** in the saving state form. The Simulator state is saved.

Loading the Simulator State

- From the ADE window execute **Session – Load State.**
- In the Loading State window, set the State name to **state1_inv** as shown

- Click **OK** in the Loading State window.

Parametric Analysis

- Parametric Analysis yields information similar to that provided by the Spectre® sweep feature, except the data is for a full range of sweeps for each parametric step. The Spectre sweep feature provides sweep data at only one specified condition.

- You will run a parametric DC analysis on the **wp** variable, of the PMOS device of the Inverter design by sweeping the value of **wp**.

- Run a simulation before starting the parametric tool. You will start by loading the state from the previous simulation run.

- Run the simulation and check for errors. When the simulation ends, a single waveform in the waveform window displays the DC Response at the **Vout** node.

Starting the Parametric Analysis Tool

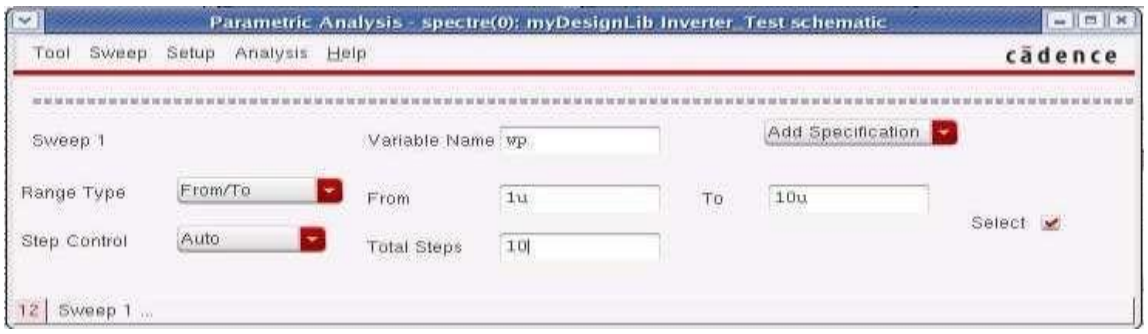
- In the Simulation window, execute **Tools—Parametric Analysis**. The Parametric Analysis form appears.
- In the Parametric Analysis form, execute **Setup—Pick Name for Variable—Sweep 1**.

A selection window appears with a list of all variables in the design that you can sweep. This list includes the variables that appear in the Design Variables section of the Simulation window.

- In the selection window, double click left on **wp**.The Variable Name field for Sweep 1 in the Parametric Analysis form is set to **wp**.
- Change the Range Type and Step Control fields in the Parametric Analysis form as shown below:

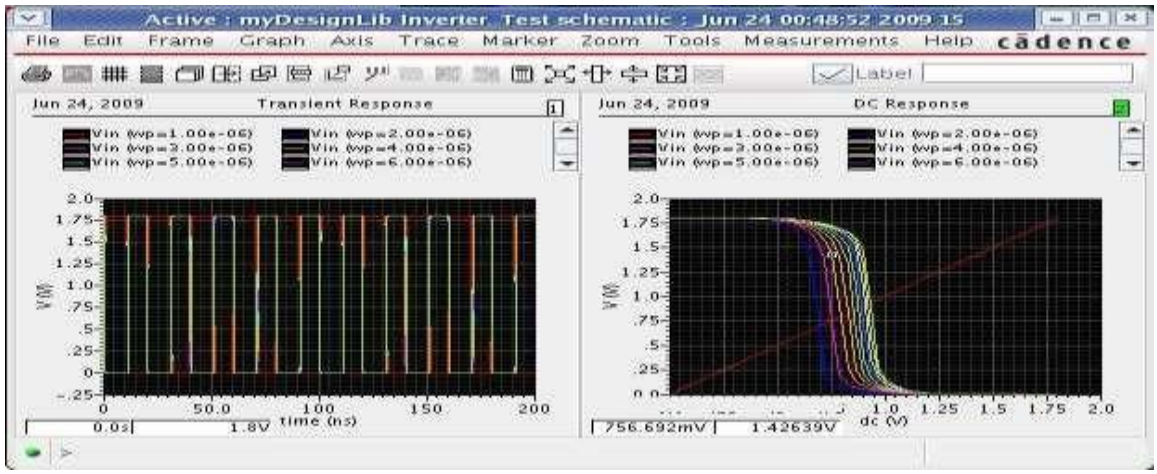
Range Type	**From/To**	From	**1u**	To	**10u**
Step Control	**Auto**	Total Steps	**10**		

These numbers vary the value of the **wp** of the pmos between 1um and 10um at ten evenly spacedintervals.



- Execute **Analysis—Start**.

The Parametric Analysis window displays the number of runs remaining in the analysis and the current value of the swept variable(s). Look in the upper right corner of the window. Once the runs are completed the wavescan window comes up with the plots for different runs.



Note: Change the wp value of pmos device back to 2u and save the schematic before proceeding to the next section of the lab. To do this use edits property option.

RESULT: Designed and verified the static (VTC) and dynamic characteristics of a digital CMOS inverter.

CONCLUSION: -

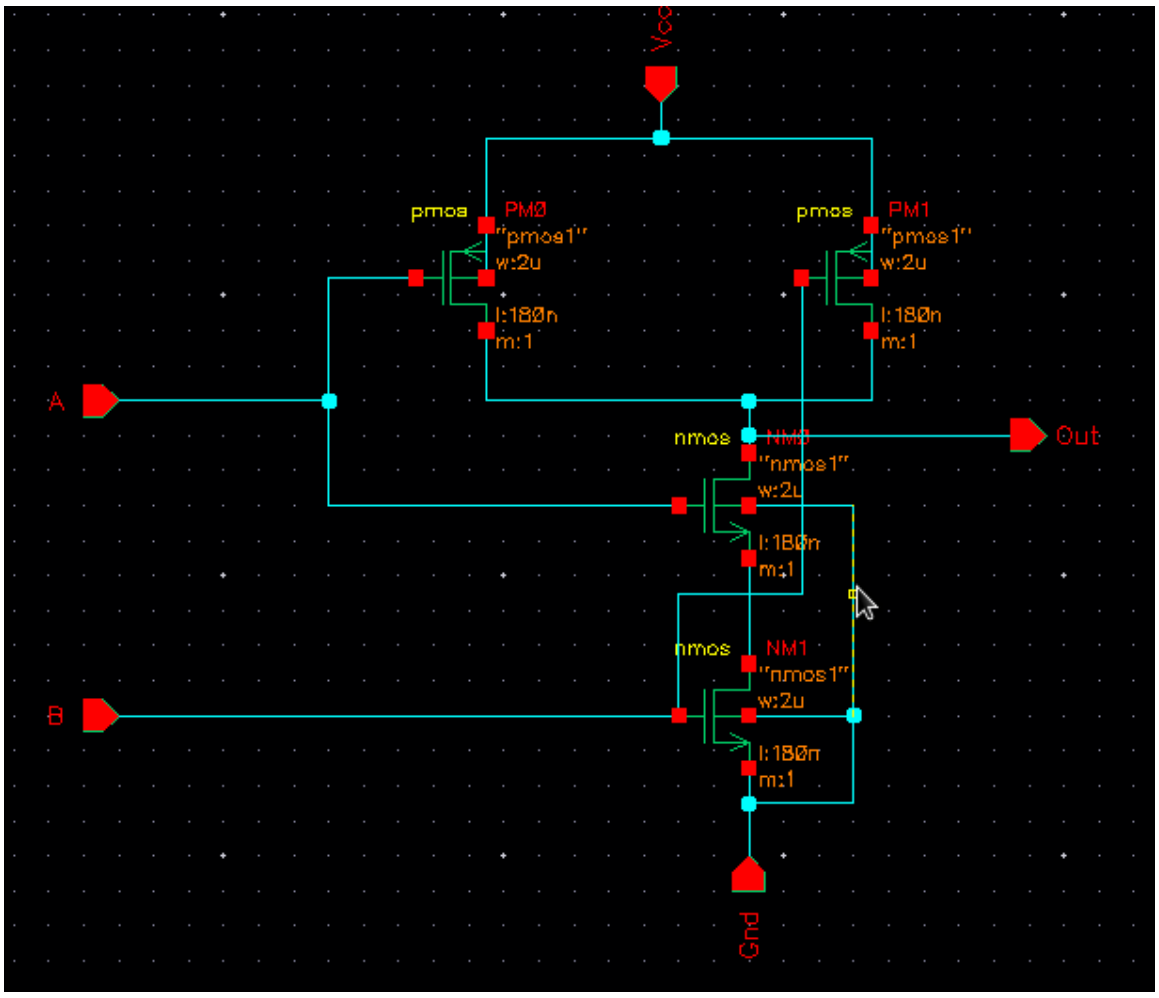
EXPERIMENT NO :- 7

AIM: - To simulate the following logic gates and verify the truth tables:

(a) Two-input NAND
(b) Two-input NOR

TOOLS REQUIRED: PC,CADENCE TOOLS

CIRCUIT DIAGRAM: - (a) Two-input NAND Gate Schematic



Procedure: -

(1)Creating a Schematic Cellview

In this section we will learn how to open new schematic window in the new library and build the NAND schematic as shown in the figure at the start of this lab.

- In the CIW or Library manager, execute **File – New – Cellview**.
- Set up the new file form cell name and schematic view.
- Click **OK** when done the above settings. A blank schematic window for the **NAND** designappears.

(a) Adding Components to schematic

- In the nand schematic window, click the **Instance** fixed menu icon to display the AddInstance form.(You can also execute **Create — Instance** or press **i**.)
- Click on the **Browse** button. This opens up a Library browser from which you can select components and the **symbol** view . You will update the Library Name, Cell Name, and theproperty values as you place each component.
- After you complete the Add Instance form, move your cursor to the schematic window and click **left** to place a component.

If you place a component with the wrong parameter values, use the **Edit— Properties— Objects** command to change the parameters. Use the **Edit— Move** command if you place components in the wrong location.
You can rotate components at the time you place them, or use the **Edit— Rotate** command after they are placed.

- After entering components, click **Cancel** in the Add Instance form or press **Esc** with yourcursor in the schematic window.

(b) Adding pins to Schematic

- Click the **Pin** fixed menu icon in the schematic window. You can also execut **Create — Pin** or press ***P***
- The Add pin form appears.
- Type the pin name in the Add pin form in the exact order leaving space between the pin names. Make sure that the direction field is set to **input/output/inputOutput** when placing the **input/output/inout** pins respectively and the Usage field is set to **schematic**.
- Select **Cancel** from the Add – pin form after placing the pins.

In the schematic window, execute **Window— Fit** or press the **f** bindkey.

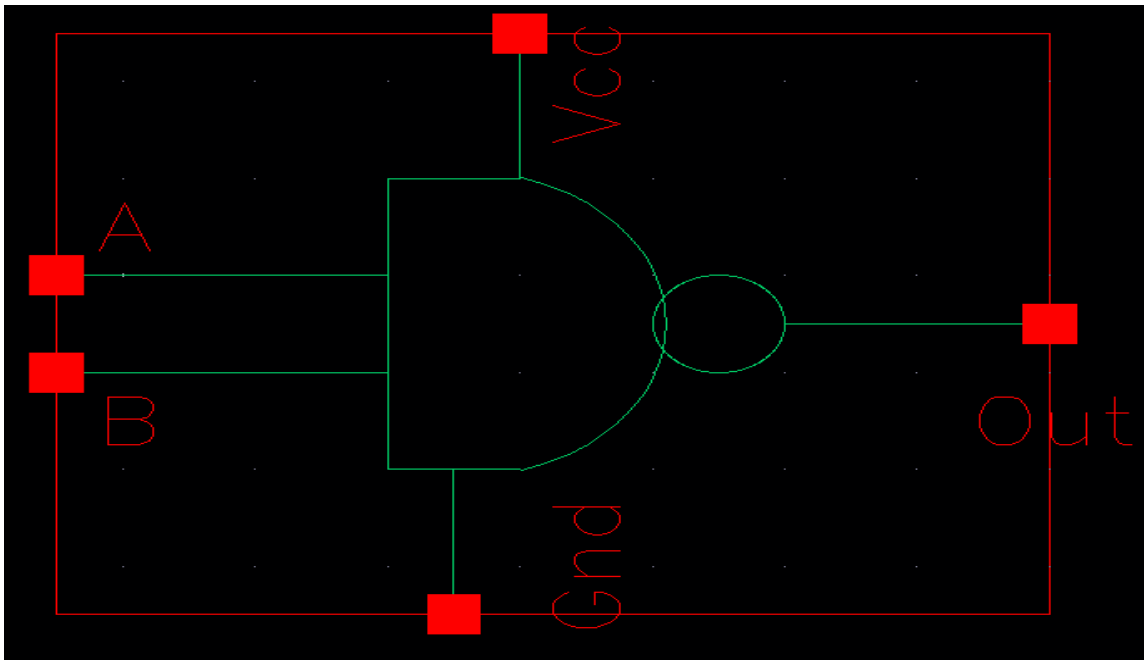
(c) Adding Wires to a Schematic

- Click the **Wire (narrow)** icon in the schematic window.
- You can also press the ***w*** key, or execute **Create — Wire (narrow).**
- In the schematic window, click on a pin of one of your components as the first point for your wiring. A diamond shape appears over the starting point of this wire.
- Complete the wiring and when done wiring press **ESC** key in the schematic window.

Saving the Design

- Click the ***Check and Save*** icon in the schematic editor window.
- Observe the CIW output area for any errors.

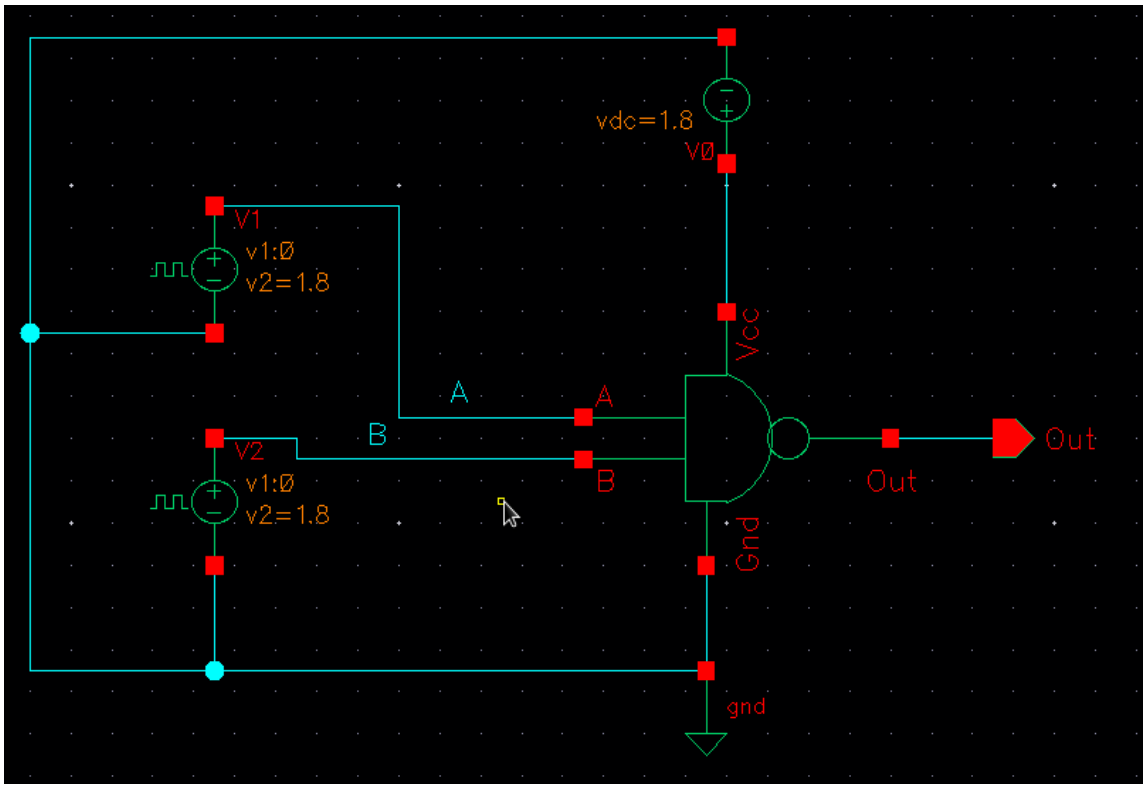
(2) NAND Gate Symbol



(a) Symbol Creation

- In the nand schematic window, execute **Create — Cellview— From Cellview**.
- The **Cellview From Cellview** form appears. With the Edit Options function active, you cancontrol the appearance of the symbol to generate.
- Verify that the **From View Name** field is set to **schematic**, and the **To View Name** field is setto **symbol**, with the **Tool/Data Type** set as **SchematicSymbol.**
- Click **OK** in the **Cellview From Cellview** form.
- The Symbol Generation Form appears & Modify the **Pin Specifications.**
- Click **OK** in the Symbol Generation Options form.
- A new window displays an automatically created NAND GATE symbol.

(3) NAND Gate Test Circuit



(a) Creating the NAND_Test Cellview

You will create the NAND_Test cellview that will contain an instance of the Inverter cellview. In the next section, you will run simulation on this design .

- In the CIW or Library Manager, execute **File— New— Cellview**.
- Set up the New File form as cell name schematic view.
- Click **OK** when done. A blank schematic window for the **NAND_Test** design appears.

(b) Building the NAND_Test Circuit

- Using the component list and Properties/Comments in this table, build the **NAND_Test** schematic.

Library name	**Cellview name**	**Properties/Comments**
Your library	NAND	symbol
analogLib	Vpulse	V1= 0v, V2= 1.8v, pw= 40ns, period= 20ns
analogLib	Vpulse	V1= 0v, V2= 1.8v, pw= 20ns, period= 20ns
analogLib	Vdd, gnd	Vdc= 1.8v

(4) Starting the Simulation Environment

- In the **NAND_Test** schematic window, execute **Launch – ADE L .**
- The **Virtuoso Analog Design Environment (ADE)** simulation window appears.

(a) Choosing Analyses

- In the Simulation window (ADE), click the **Choose - Analyses** icon. You can also execute **Analyses - Choose.**
- To setup for transient analysis :
  In the Analysis section select
  tran

Set the stop time as **200n**
Click at the **moderate** or **Enabled** button at the bottom, and then click **Apply**.

- Click ***OK*** in the Choosing Analyses Form.

(b) Selecting Outputs for Plotting

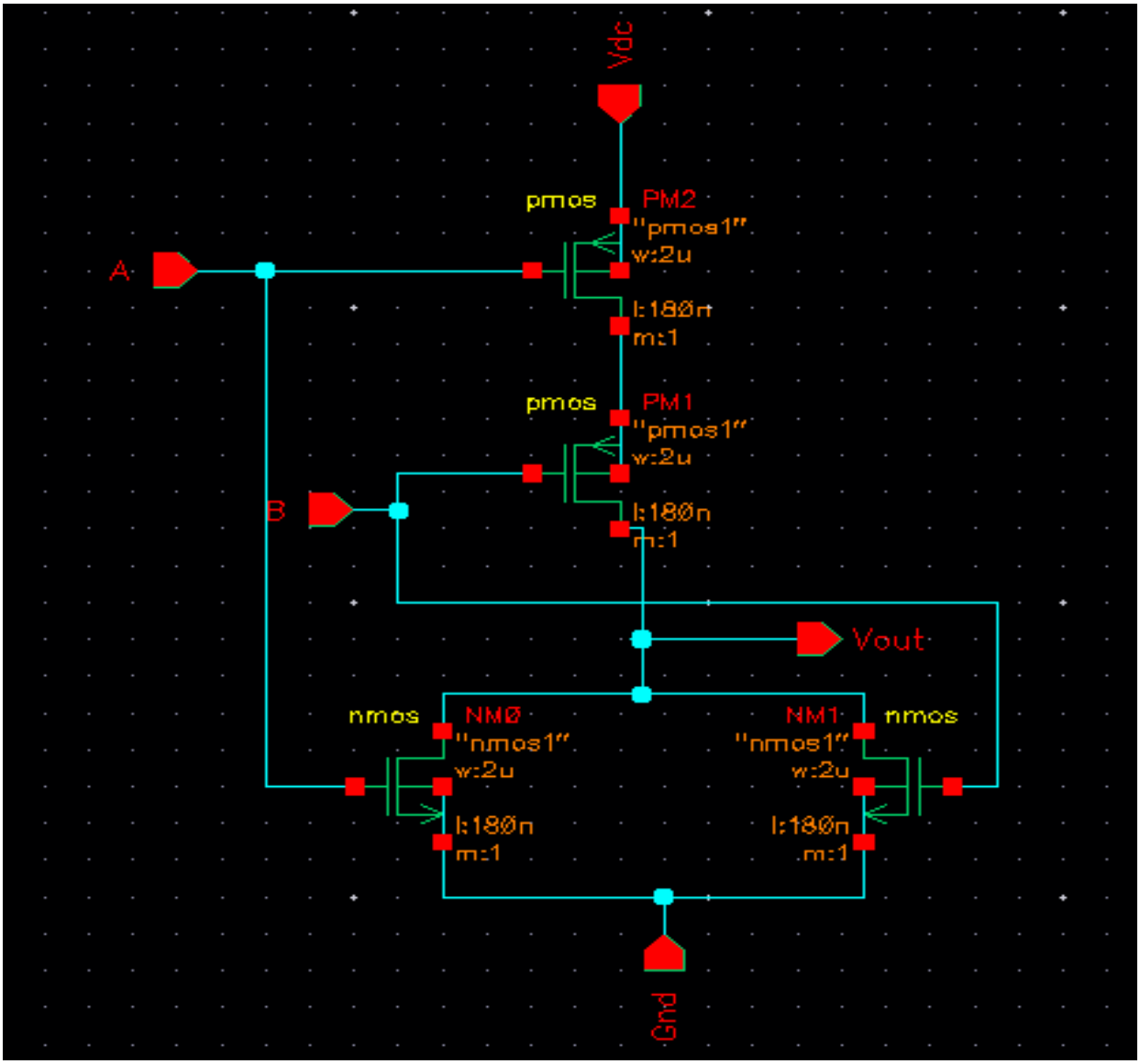
- Execute **Outputs – To be plotted – Select on Schematic** in the simulation window.
- Follow the prompt at the bottom of the schematic window, Click on output net **Vout**, input net **Vin** of the NAND. Press **ESC** with the cursor in the schematic after selecting it.

(c) Running the Simulation

- Execute **Simulation – Netlist and Run** in the simulation window to start the Simulation orthe icon, this will create the netlist as well as run the simulation.
- When simulation finishes, the Transient plots automatically will be popped up along with log file.

RESULT: -

CIRCUIT DIAGRAM:- (b) Two-input NOR Gate Schematic



Procedure: -

(1) Creating a Schematic Cell view

In this section we will learn how to open new schematic window in the new library and build the NOR schematic as shown in the figure at the start of this lab.

- In the CIW or Library manager, execute **File – New – Cellview**.
- Set up the New file form cell name and schematic view.
- Click **OK** when done the above settings. A blank schematic window for the **NOR** designappears.

(a) Adding Components to schematic

- In the nor schematic window, click the **Instance** fixed menu icon to display the Add Instanceform.(You can also execute **Create — Instance** or press **i**.)
- Click on the **Browse** button. This opens up a Library browser from which you can select components and the **symbol** view . You will update the Library Name, Cell Name, and theproperty values as you place each component.
- After you complete the Add Instance form, move your cursor to the schematic window and click **left** to place a component.

If you place a component with the wrong parameter values, use the **Edit— Properties— Objects** command to change the parameters. Use the **Edit— Move** command if you place components in the wrong location.
You can rotate components at the time you place them, or use the **Edit— Rotate** command after they are placed.

- After entering components, click **Cancel** in the Add Instance form or press **Esc** with yourcursor in the schematic window.

(b) Adding pins to Schematic

- Click the **Pin** fixed menu icon in the schematic window. You can also execut **Create — Pin** or press ***P***
- The Add pin form appears.

- Type the pin name in the Add pin form in the exact order leaving space between the pin names. Make sure that the direction field is set to **input/output/inputOutput** when placing the **input/output/inout** pins respectively and the Usage field is set to **schematic**.

- Select **Cancel** from the Add – pin form after placing the pins.
  In the schematic window, execute **Window— Fit** or press the **f** bindkey.

(c) Adding Wires to a Schematic

- Click the **Wire (narrow)** icon in the schematic window.

- You can also press the ***w*** key, or execute **Create — Wire (narrow).**

- In the schematic window, click on a pin of one of your components as the first point for your wiring. A diamond shape appears over the starting point of this wire.

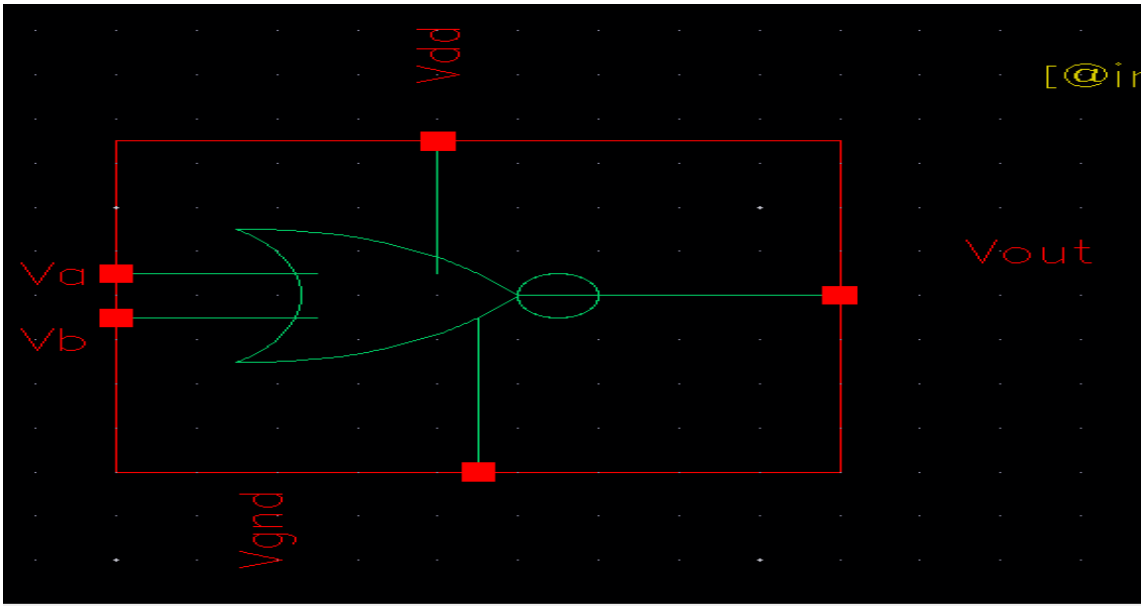
- Complete the wiring and when done wiring press **ESC** key in the schematic window.

Saving the Design

- Click the ***Check and Save*** icon in the schematic editor window.

- Observe the CIW output area for any errors.

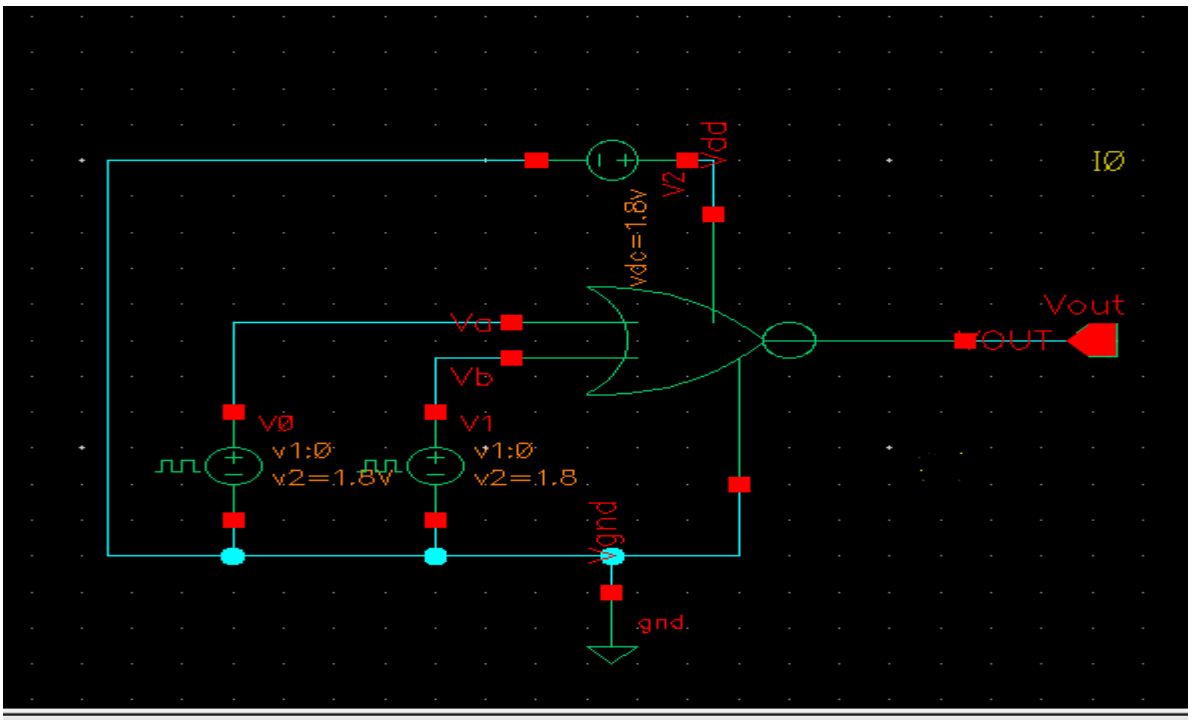
(2) NOR Gate Symbol



Symbol Creation

- In the NOR schematic window, execute **Create — Cellview— From Cellview**.
- The **Cellview From Cellview** form appears. With the Edit Options function active, you cancontrol the appearance of the symbol to generate.
- Verify that the **From View Name** field is set to **schematic**, and the **To View Name** field is setto **symbol**, with the **Tool/Data Type** set as **SchematicSymbol.**
- Click **OK** in the **Cellview From Cellview** form.
- The Symbol Generation Form appears & Modify the **Pin Specifications.**
- Click **OK** in the Symbol Generation Options form.
- A new window displays an automatically created NOR GATE symbol.

(3) NOR Gate Test



(a) Creating the NOR_Test Cellview

You will create the NOR_Test cellview that will contain an instance of the Inverter cellview. In thenext section, you will run simulation on this design .

- In the CIW or Library Manager, execute **File— New— Cellview**.
- Set up the New File form as cell name schematic view.
- Click **OK** when done. A blank schematic window for the **NOR_Test** design appears.

(b) Building the NOR_Test Circuit

- Using the component list and Properties/Comments in this table, build the **NOR_Test** schematic.

Library name	**Cellview name**	**Properties/Comments**
Your library	NOR	symbol
analogLib	Vpulse	V1= 0v, V2= 1.8v, pw= 40ns, period= 20ns
analogLib	Vpulse	V1= 0v, V2= 1.8v, pw= 20ns, period= 20ns
analogLib	Vdd, gnd	Vdc= 1.8v

(3) Starting the Simulation Environment

- In the **NOR_Test** schematic window, execute **Launch – ADE L .**
- The **Virtuoso Analog Design Environment (ADE)** simulation window appears.

(a) Choosing Analyses

- In the Simulation window (ADE), click the **Choose - Analyses** icon. You can also execute **Analyses - Choose.**

- To setup for transient analysis :
  In the Analysis section select
  tranSet the stop time as **200n**
  Click at the **moderate** or **Enabled** button at the bottom, and then click **Apply**.
- Click ***OK*** in the Choosing Analyses Form.

(b) Selecting Outputs for Plotting

- Execute **Outputs – To be plotted – Select on Schematic** in the simulation window.
- Follow the prompt at the bottom of the schematic window, Click on output net **Vout**, input net **Vin** of the NOR GATE. Press **ESC** with the cursor in the schematic after selecting it.

(c) Running the Simulation

- Execute **Simulation – Netlist and Run** in the simulation window to start the Simulation orthe icon, this will create the netlist as well as run the simulation.
- When simulation finishes, the Transient plots automatically will be popped up along with log file.

RESULT: -