POSSESSION OF MOBILES IN EXAM IS UFM PRACTICE

Name: _____ Enrolment No: _____

Jaypee Institute of Information Technology, NOIDA

Test-2 Examination –2024

B.TECH, VI Semester

Course Title: Digital Hardware Design **Maximum Time: 1 Hr**

Course Code: 17B1NEC741 **Maximum Marks: 20**

CO1	Recall the concept of sequential circuits and state machines
CO2	Discuss advanced adders and multiplier circuits
CO3	Demonstrate the concept of VHDL and FSM in digital circuit design
CO4	Illustrate the concept of different ways of pulse or pattern generation.
CO5	Design asynchronous sequential digital circuits using flow table method.

Q1. Design shift register based pulse train generator to generate the pulse train 101110. Show steps clearly. [CO4 (Analyzing), Marks 4]

Q2. Discuss design strategy for generating pulse sequences 100111 and 011101 simultaneously using indirect logic. [CO4 (Analyzing), Marks 4]

Q3. With reference to VHDL programming.

(a) When a port of a component is not connected to any signal, then which keyword is used to indicate the situation:_____

(b) Write down the value of y

```
SIGNAL x: STD_LOGIC:= '1';
SIGNAL y: STD_LOGIC_VECTOR (3 DOWNTO 0);
```

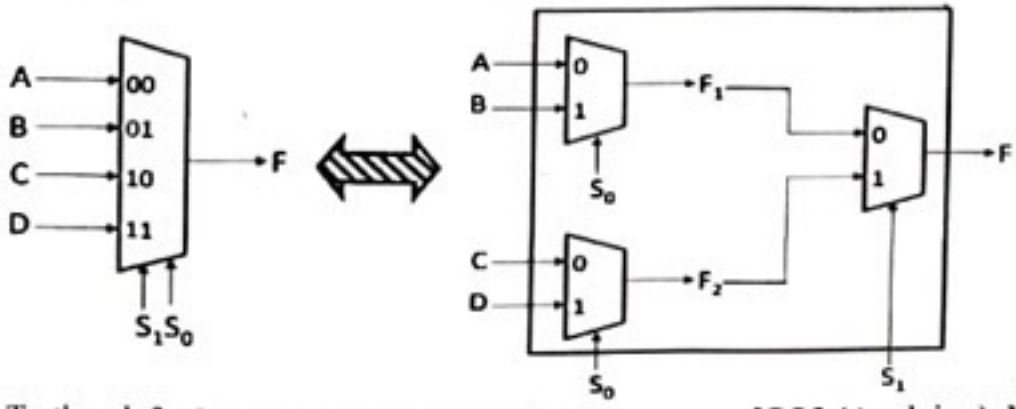
(i) y <= (1 => '1', OTHERS => '0') (ii) y < = "010" & x;

(c) What is the use of generate command?

(d) What does sensitivity list in process command mean?

(e) What flexibility generic command provides? [CO3 (Applying), Marks 5]

Q4. (a) Write VHDL code for 2X1 Mux using **if-then-else command**. Using the same 2X1 Mux as component, do structural coding for 4x1 Multiplexers shown below.



(b) Write Testbench for 2x1 Mux designed in part 4 (a). [CO3 (Applying), Marks 4+3]