JAYPEE INSTITUE OF INFORMATION TECHNOLOGY
Electronics and Communication Engineering
Course: VLSI Design
Course Code: 18B11EC315

Tutorial-3

Q1. Consider a CMOS inverter with given process trans-conductance parameters: k'_n=140 μA/V^2 , k'_p=60 μA/V^2 , $V_{to,n}$=0.7 V, $V_{to,p}$= - 0.7 V, V_{DD}=3 V.

(a) If the design is ideal and symmetrical, then find out the ratio of (W/L)p and (W/L)n. (b) Take the case when (W/L)p = (W/L)n, then find out the inverter threshold voltage.

Q2. A CMOS inverter is built in a process where k'_n=100 μA/V^2 , k'_p=42 μA/V^2 , $V_{to,n}$=0.7 V, $V_{to,p}$= - 0.8V and a power supply of V_{DD}=3.3 V is used. Calculate the inverter threshold voltage V_{th} if $(W/L)_n$=10 and $(W/L)_p$=14.

Q3. Find the ratio k_n/k_p needed to obtain a CMOS inverter threshold voltage of V_{th}=1.3 V with a power supply of 3 V. Assume that $V_{to,n}$=0.6 V and $V_{to,p}$ = -0.82. Find the relative device sizes if the mobility are related as: $\mu_n=2.2\mu_p$.

Q4. Consider the CMOS inverter circuit with V_{DD} = 3.3 V. The *I-V* characteristics of the nMOS transistor are specified as follows: when V_{GS} = 3.3 V, the drain current reaches its saturation level $\mathbf{I_{DSAT}}$ = 2 mA for $V_{DS} \geq$ 2.5 V. Assume that the input signal applied to the gate is a step pulse that switches instantaneously from 0 V to 3.3 V. Using the data above, calculate the delay time necessary for the output to fall from its initial value of 3.3V to 1.65V, assuming an output load capacitance of 300 fF.

Q.5. Consider a CMOS inverter, with the following device parameters:

(i) $V_{t0,n}$ = 0.8 V
(ii) $V_{t0,p}$= -1.0 V
(iii) W_{min} =1.2μm

Design this CMOS inverter by determining the channel widths W_n and W_p of the nMOS and pMOS transistors, to meet the following performance specifications:

(a) $V_{th} = 1.5$ V for $V_{DD} = 3$ V
(b) Propagation delay times $\boldsymbol{t_{PHL}} \leq 0.2$ ns and $\boldsymbol{t_{PLH}} \leq 0.15$ ns,
(c) A falling delay of 0.35 ns for an output transition from 2 V to 0.5 V,
Assume a combined output load capacitance of 300 fF and an ideal step input.

Q.6. For the RC network shown in Fig. 1, calculate the Elmore delay from In to Out1 and from In to Out2.

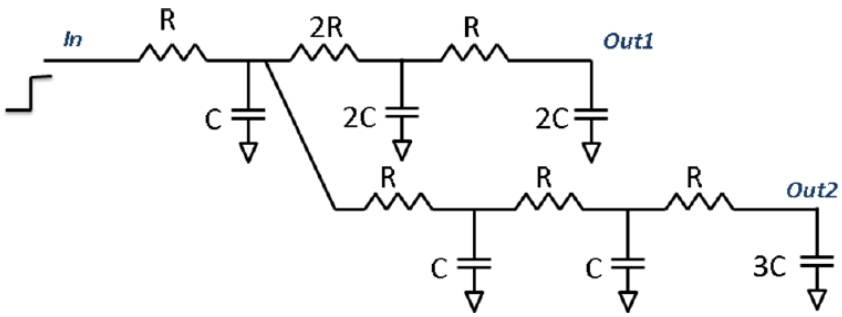

Fig. 1. Diagram of a RC network