Course Name: Digital Hardware Design
Course Code: 17B1NEC741

Shift Register Based Sequence Generator

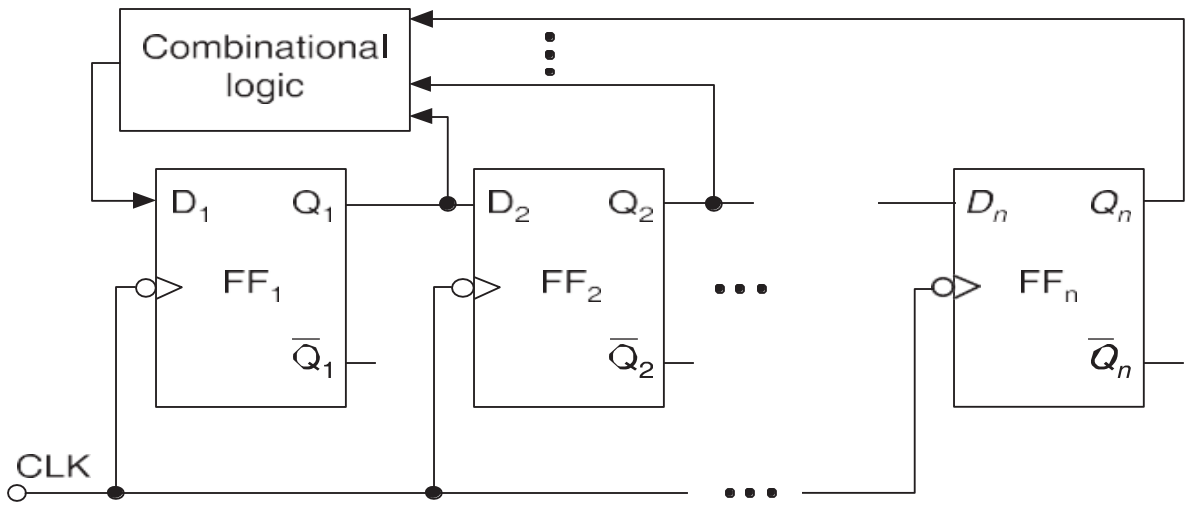
Dr. Arti Noor
Dean, Academic Affairs
Electronics and Communication Engineering,
Jaypee Institute of Information Technology, Noida

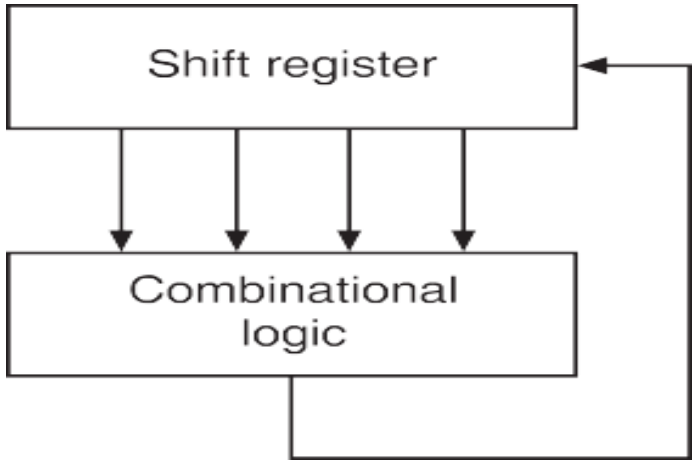
• Shift registers can be used to generate single pulse trains.

•A shift register is quite restrictive in the sense that it can't go from any one state to any other state of our choice.

•So, the pulse train need to be examined to see if it can be generated by shifting.

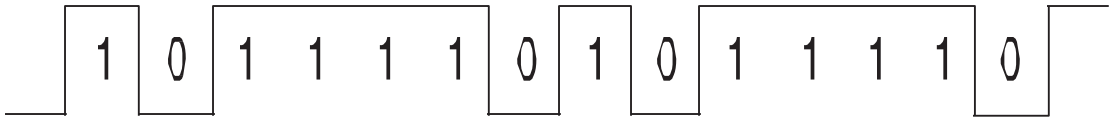
•General architecture is shown below:





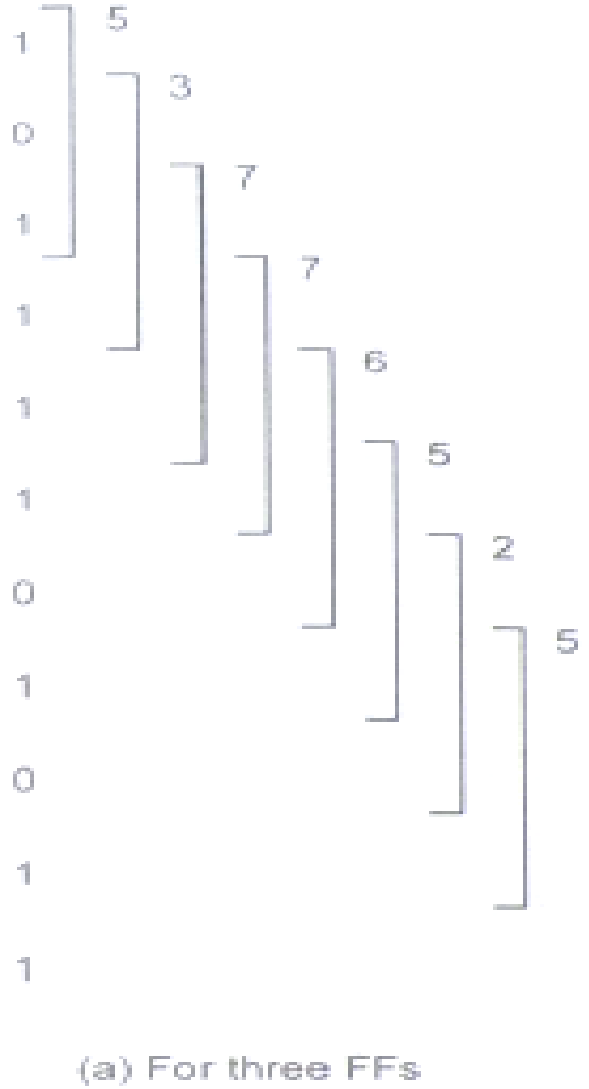
Example-1

Design a pulse train generator using a shift register.

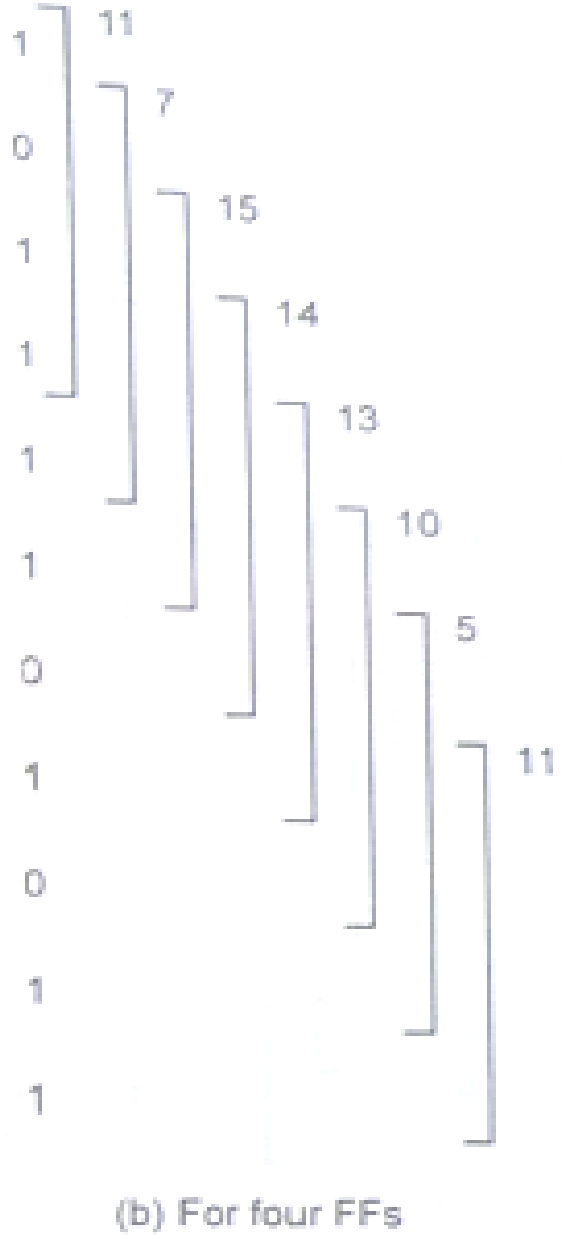


Considering sequence as 1011110

- Since pattern is of 7-bits, minimum of three FFs required.
- Write sequence 1011110 in vertical form.
- Make groups of 3-bit starting from the top bit and
- Write the states in decimal also.
- In 3-bit groups, it can be seen that states 7 and 5 are repeated.
- It means we can't get unique state by using 3-bit
- So make a group of 4-bits and observe again.



(a) For three FFs

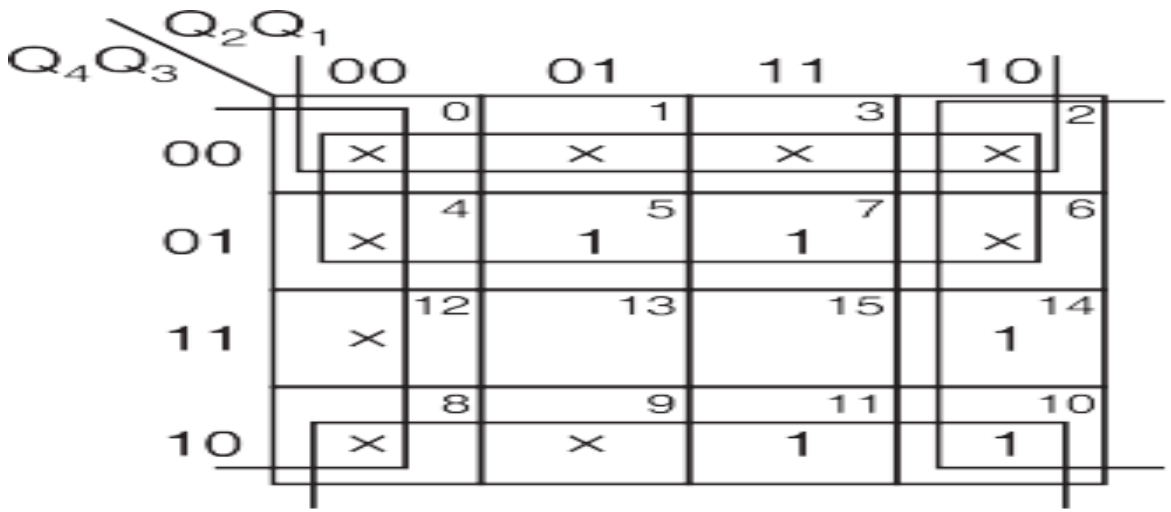


(b) For four FFs

- **The states are not repeated, i.e. seven unique states (11, 7, 15, 14, 13, 10, 5) can be obtained using four FFs.**
- **Make the truth table with the states of register and O/P of the combinational circuit which is to be fed as input to the shift register.**
- **For each state of a particular group of 4 bits, the next lower bit is O/P of the CLB.**
- **The unused nine states (0,1,2,,3,4,6,8,9,12) are invalid.**

Q_4	Q_3	Q_2	Q_1	f
1	0	1	1	1
0	1	1	1	1
1	1	1	1	0
1	1	1	0	1
1	1	0	1	0
1	0	1	0	1
0	1	0	1	1

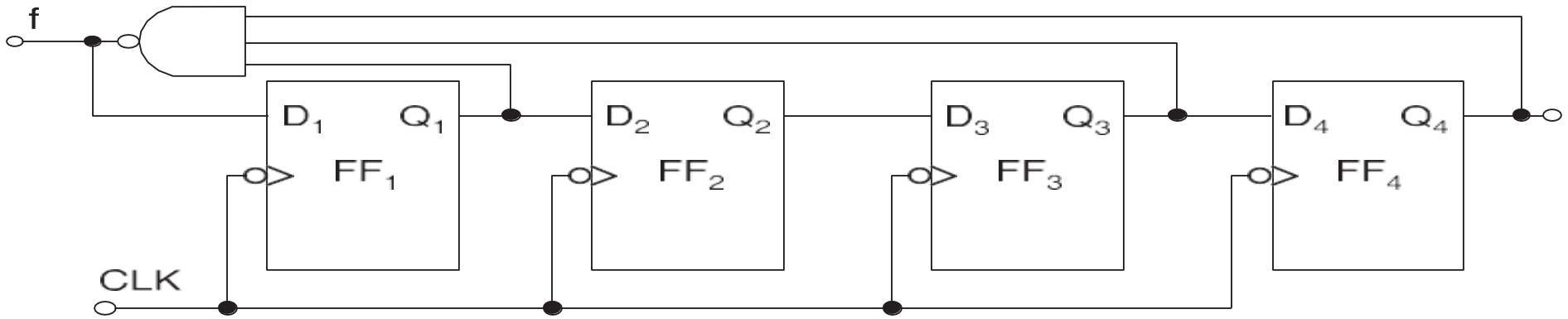
Truth Table



$$f = \overline{Q}_4 + \overline{Q}_3 + \overline{Q}_1 = \overline{Q_4 Q_3 Q_1}$$

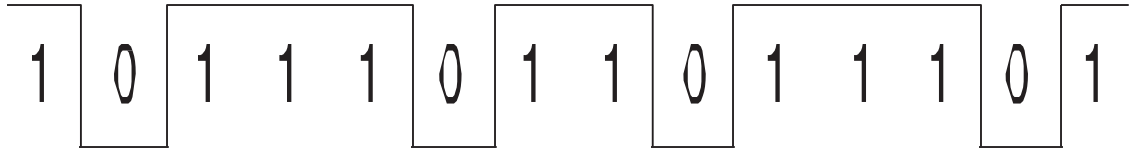
(a) K-map

Complete circuit diagram for pulse train generator for generating 1011110 using shift register technique



Example-2

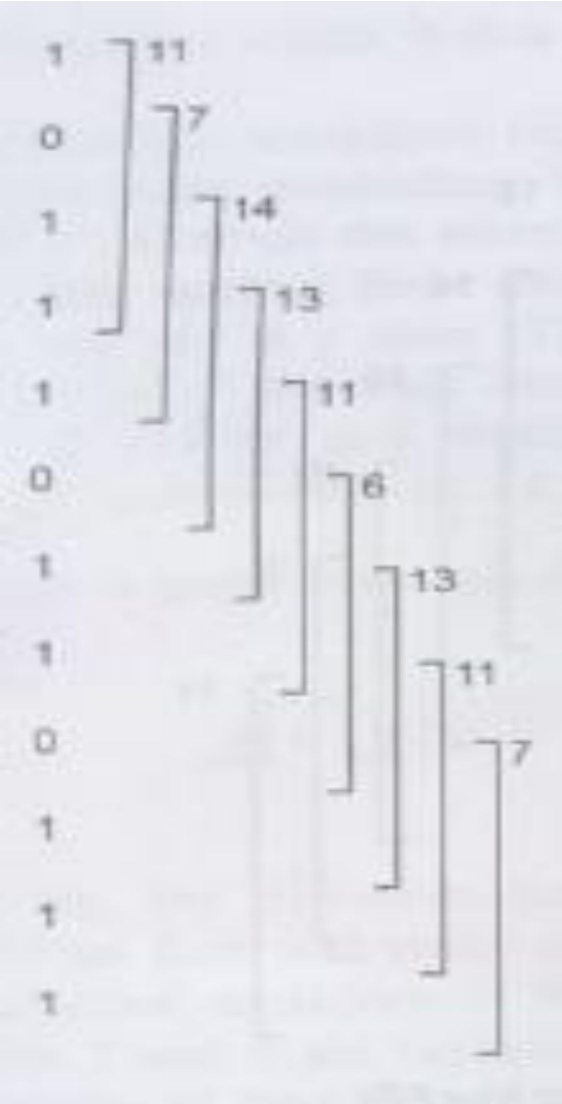
Design a pulse train generator using a shift register.



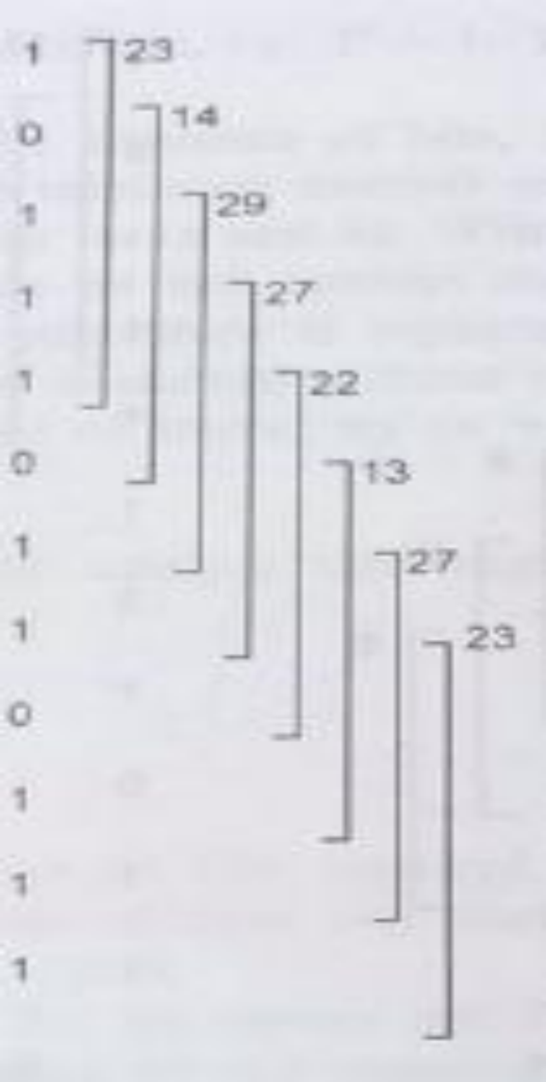
Considering sequence as 1011101

- Since pattern is of 7-bits, so we require minimum of three FFs
- Write sequence 1011101 in vertical form and
- Make groups of 3-bit starting from the top bit and
- Write the states in decimal also.
- In 3-bit groups, it can be seen that few states are repeated.
- It means we can't get unique 7-state by using 3-bit
- So make a group of 4-bits and observe again.

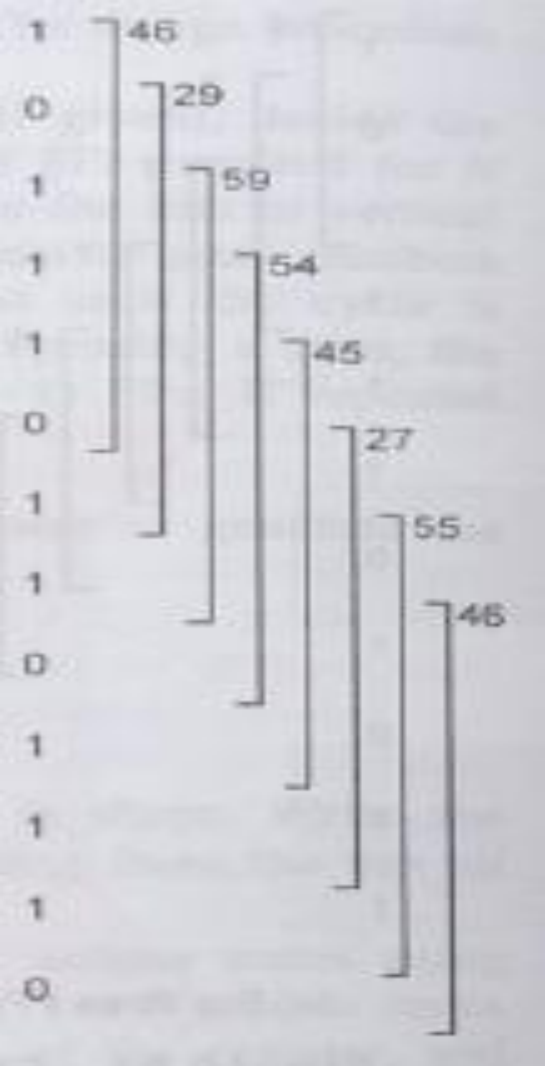
- In 4-bit and 5-bit groups, it can be seen that few states are repeated.
- It means we can't get unique 7-state by using 4 or 5-bit.
- So make a group of 6-bits and observe again



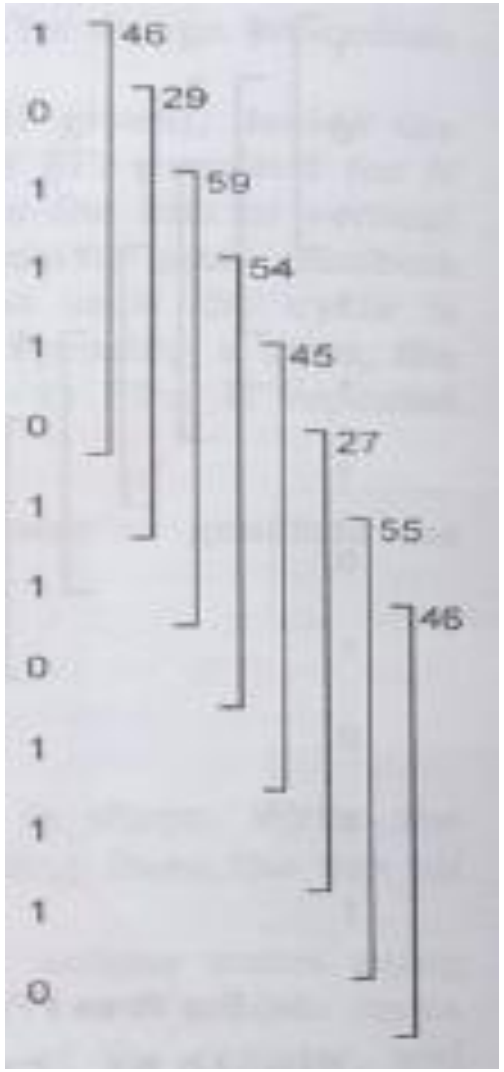
4-bit grouping



5-bit grouping



6-bit grouping



Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	f
0	1	1	1	0	1	1
1	0	1	1	1	0	1
1	1	0	1	1	1	0
0	1	1	0	1	1	1
1	0	1	1	0	1	1
1	1	0	1	1	0	1
1	1	1	0	1	1	0

f = Q6‘ + Q5’ Q4 + Q6 Q1’