VLSI Design
Moderate Assignment

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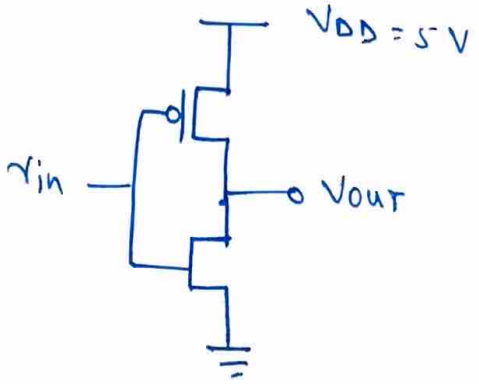
Q1.

Sol. Given,

$V_{Tn} = 1V \quad V_{Tp} = -1.5\,V$

$K_n = 100\,\mu A/V^2 \quad K_p = 50\,\mu A/V^2$



① $V_{OH} = 5V$, $V_{OL} = 0V$

② $V_{IL} = \dfrac{2V_{out} + V_{TP} - V_{DD} + K_R V_{Tn}}{1 + K_R}$

$K_R = \dfrac{K_n}{K_p} = 2$

$V_{IL} = \dfrac{2V_{out} - 1.5 - 5 + 2}{1+2}$

$V_{IL} = \dfrac{2}{3}V_{out} - \dfrac{1}{2} - \dfrac{5}{3} + \dfrac{2}{3} = \dfrac{2}{3}V_{out} - \dfrac{3}{2} = 0.66\,V_{out} - 1.5$

$2[0.66\,V_{out} - 1.5 - 1]^2 = 2[0.66\,V_{out} - 1.5 + 1.5 - 5]$

$(V_{out} - 5) - (V_{out} - 5)^2$

$(-1.2244)\,V_{out}^2 = -15\,V_{out} + 43.75$

$0 = 1.2244\,V_{out}^2 - 15\,V_{out} + 43.75$

$V_{IL} = 0.66 \times 4.78 - 1.5$

$V_{IL} = 1.6548.$

③ $V_{IH} = \dfrac{V_{DD} + V_{T0,P} + K_r(2V_{out} + V_{T0,n})}{1 + K_r}$

$V_{IH} = \dfrac{5 - 1.5 + 2(2V_{out} + 1)}{1+2} = 1.33\,V_{out} + 2.33$

$2[2(1.33\,V_{out} + 2.33)V_{out} - V_{out}^2] = (1.33\,V_{out} - 1.17)^2$

$2.5571\,V_{out}^2 + 6.2\,V_{out} - 1.3684 = 0$

$V_{out} = 0.2$

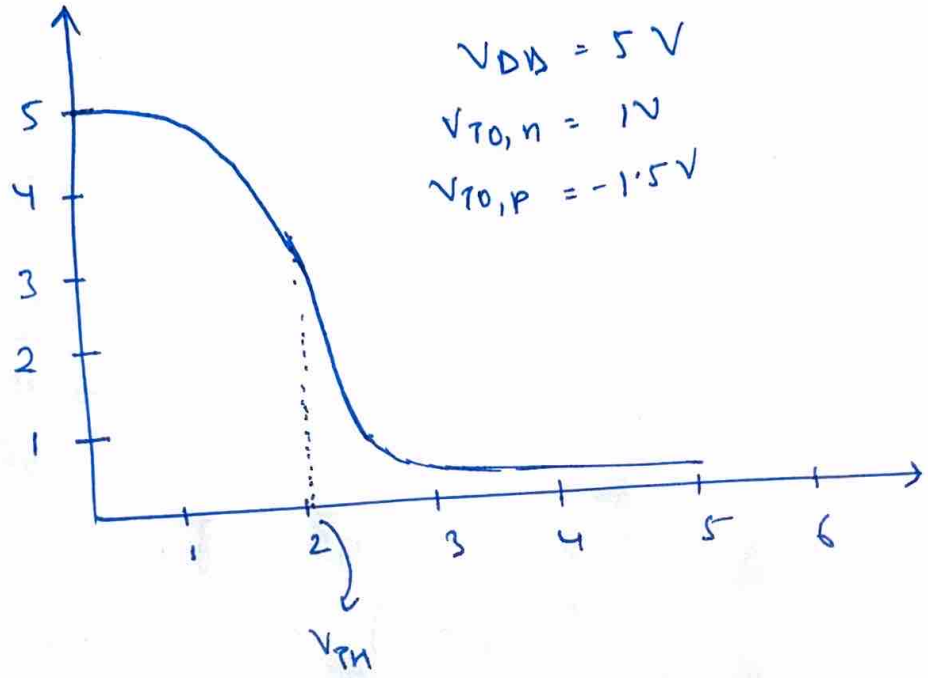
$V_{IH} = 1.33 \times 0.2 + 2.33$

$= 2.596\,V$

(4) $$V_{TH} = \frac{V_{TO,n} + \sqrt{1/K_r} \cdot (V_{DD} + V_{TO,p})}{(1 + \sqrt{1/K_r})}$$

$$V_{TH} = \frac{1 + \sqrt{1/2}\,(5 - 1.5)}{(1 + \sqrt{1/2})} = 2.035533$$

VTC Curve.



$V_{DD} = 5\,V$

$V_{TO,n} = 1V$

$V_{TO,P} = -1.5V$

VLSI Design
Assignment - 2

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Q1.

Sol. VHDL code for Half Adder.

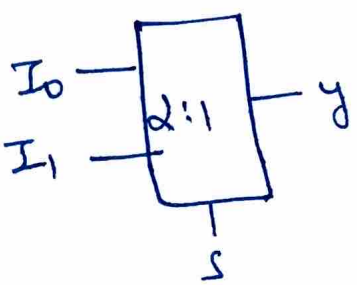
```
library IEEE ;
Use IEEE.STD_LOGIC_1164.ALL ;

entity HalfAdder is
    Port (
        A : in STD_LOGIC ;
        B : in STD_LOGIC ;
      Sum : out STD_LOGIC ;
    Carry : out STD_LOGIC
    );
end HalfAdder;

architecture Behavioral of HalfAdder is
begin
    Sum <= A xor B ;
  Carry <= A and B ;
end Behavioral;
```

Q2.

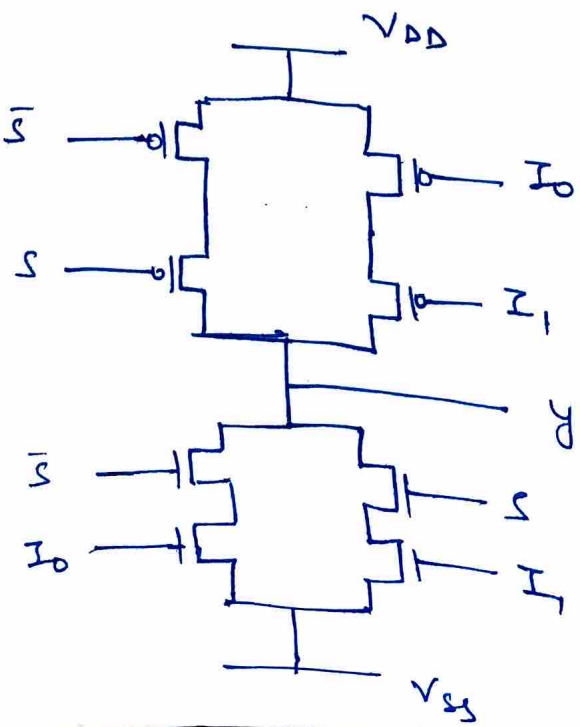
Sol.



$y = \bar{S} \cdot I_0 + S I_1$

Pull up ⇒ PMOS

Pull down ⇒ NMOS



Q3.

Sol. A 6T SRAM cell uses 6 transistors: 2 access transistors and 4 forming two cross-coupled inverters that store a bit.

Hold Operation	Write Operations	Read Operation.
• WL = 0 (Word line disabled). access transistors off • Inverters retain the stored bit • very low power (only leakage)	• BL and $\bar{BL}$ are driven with the data and its complement • WL = 1, enabling access • Bit line drivers force the new value into the cell. • Higher power due to switching	• BL and $\bar{BL}$ are driven with the data and its complement: • WL = 1, ~~enabling access~~. one bit line slightly discharges stored value. • A sense amplifier detects the differ

* Low Power Features.
  - No refresh needed (unlike DRAM)
  - CMOS inverters draw almost zero static power.
  - Minimal switching during read.
  - Efficient in hold state.