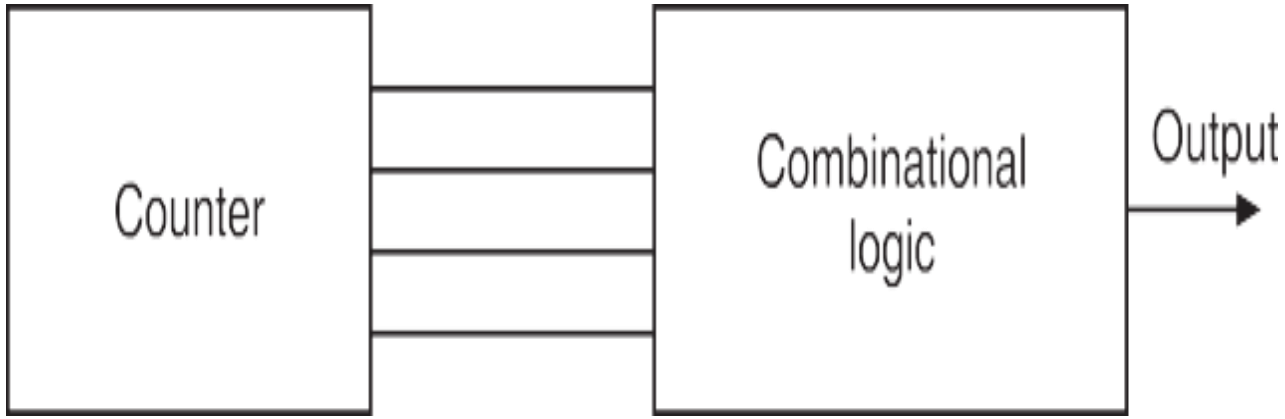
Course Name: Digital Hardware Design
Course Code: 17B1NEC741

Pulse Generation Techniques-2

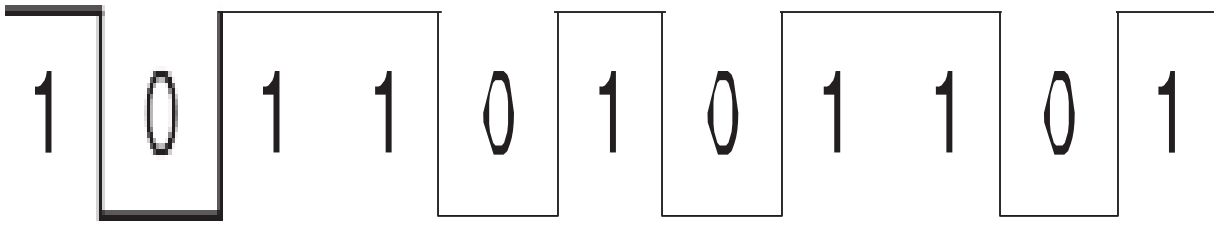
Dr. Arti Noor
Dean, Academic Affairs
Electronics and Communication Engineering,
Jaypee Institute of Information Technology, Noida

Indirect Logic Approach

1. In indirect approach the output is taken from decoder gate.
2. The block diagram is shown below. A combination of counter and Combinational logic is used for pulse train detection



Example: Generate the following pulse train using indirect logic.



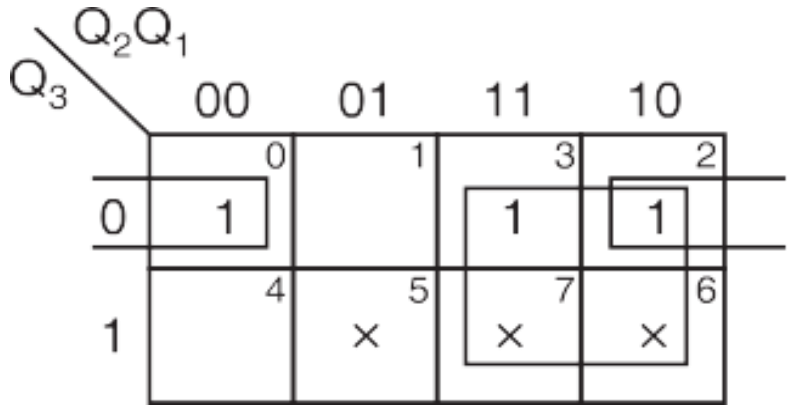
The sequence is 10110. it is 5-bit long so 5 unique states are required.
Any mod-5 counter may be used.

Example:

Use a simple ripple counter which goes through states 0,1,2,3,4,0…..
States 5,6,7 may not be used and are invalid or X.

Q_3	Q_2	Q_1	Output (f)
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	×
1	1	0	×
1	1	1	×

Truth table for output (f)

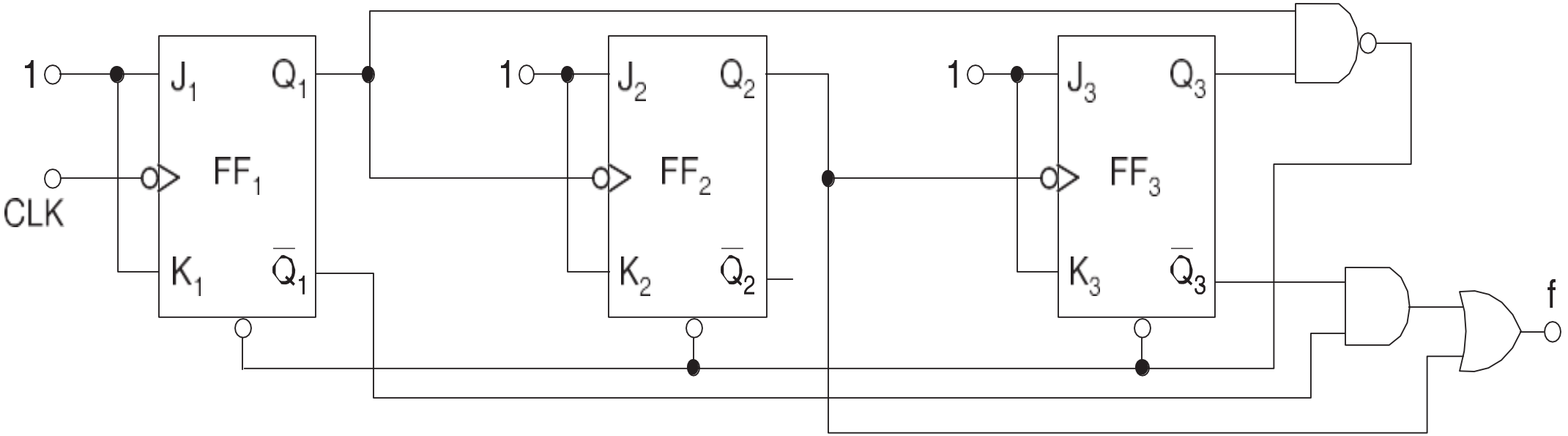


$$\text{Output, } f = Q_2 + \overline{Q}_3\overline{Q}_1$$

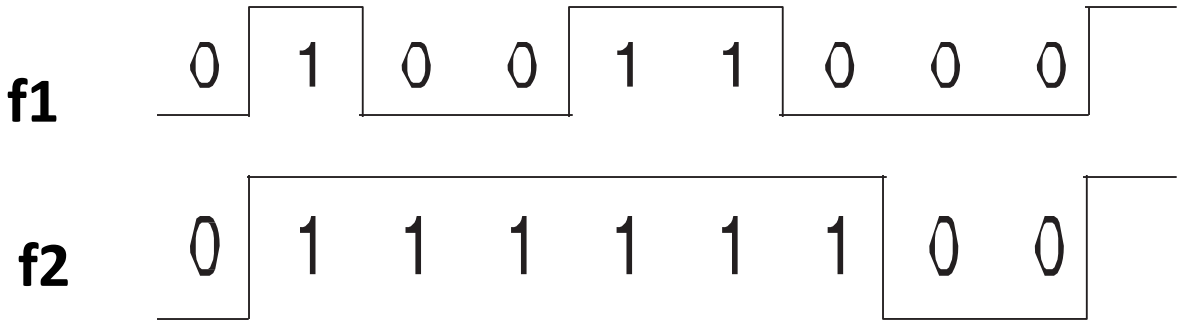
K-map and logic minimization

Example:

Logic block using mod-5 ripple counter



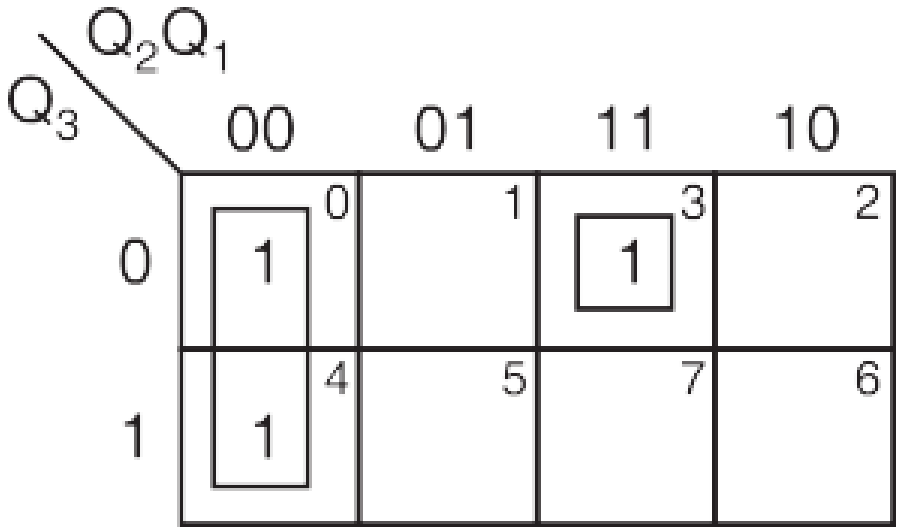
Example: Design a pulse generator using indirect logic to produce the following waveforms.



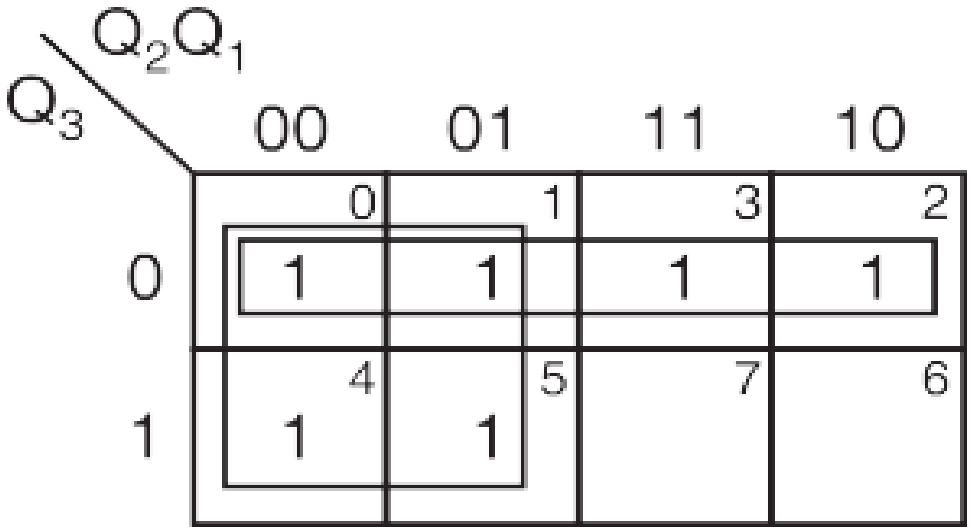
Use a simple ripple up counter which goes through 8 states

States	Q_3	Q_2	Q_1	f_1	f_2
0	0	0	0	1	1
1	0	0	1	0	1
2	0	1	0	0	1
3	0	1	1	1	1
4	1	0	0	1	1
5	1	0	1	0	1
6	1	1	0	0	0
7	1	1	1	0	0

K-map and logic minimization

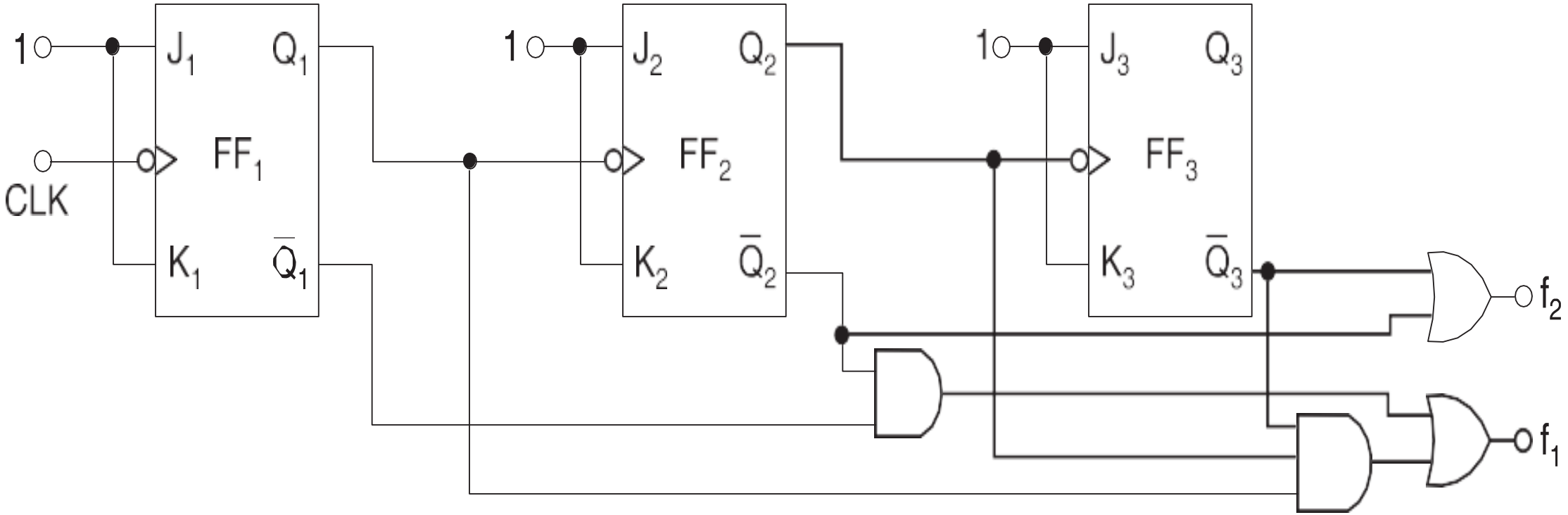


$$f_1 = \overline{Q}_2\overline{Q}_1 + \overline{Q}_3Q_2Q_1$$



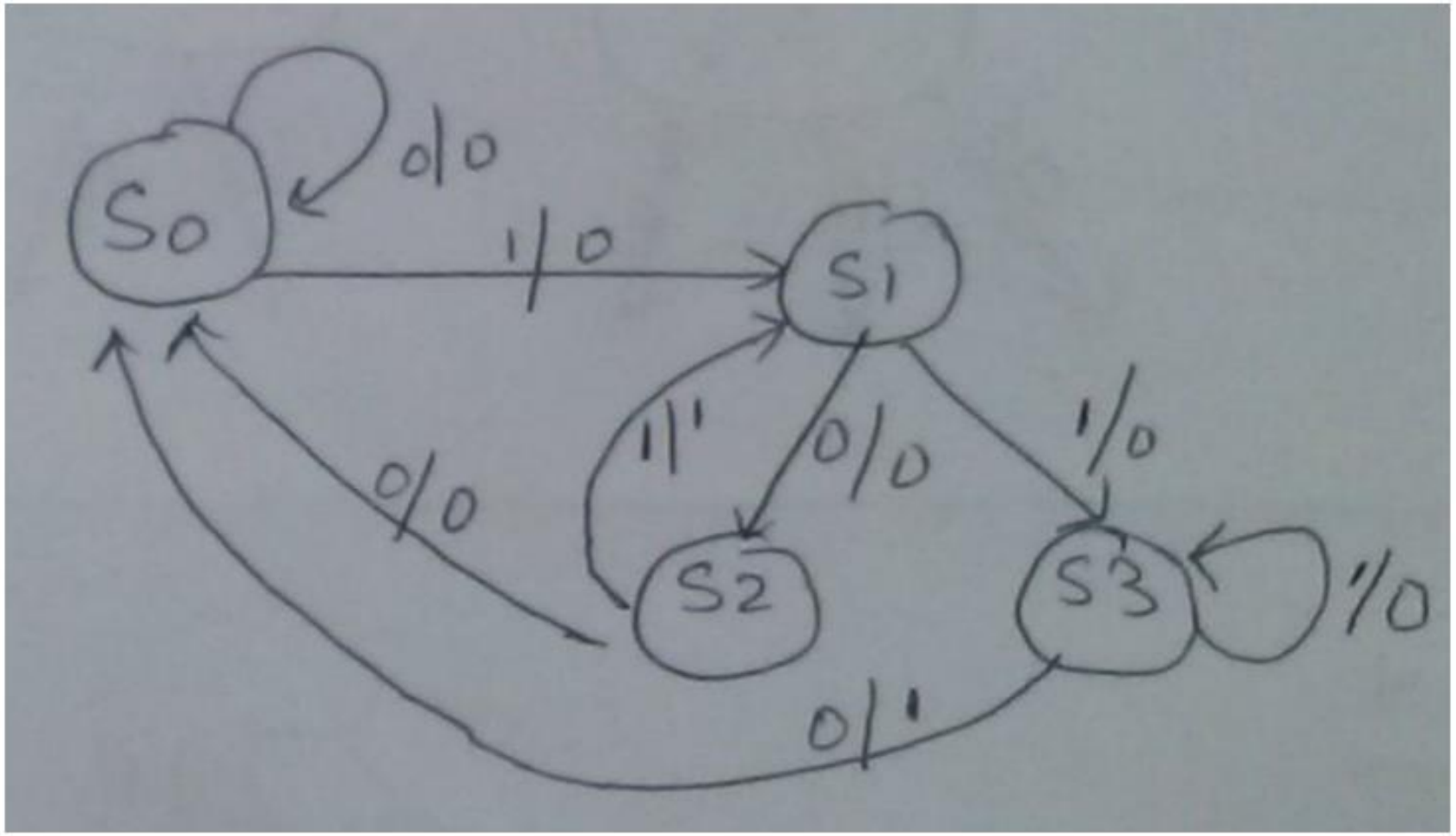
$$f_2 = \overline{Q}_2 + \overline{Q}_3$$

Logic block using ripple up counter



Practice Problems

Draw FSM for a system which is getting input bit serially and output is 1 when the present bit & past two bit contains even no of 1’s.


S0
S1
S2
S3
0/0
1/0
1/1
0/0
0/0
1/0
1/0
0/1