JAYPEE INSTITUE OF INFORMATION TECHNOLOGY
Electronics and Communication Engineering
Course: VLSI Design
Course Code: 18B11EC315

Tutorial-3

Q1. Consider a resistive-load inverter circuit with V_{DD}=5 V, k'n= 20 μA/V^2 , V_{t0}= 0.8 V, R_L= 200 KΩ, and *W/L* = 2. Calculate the critical voltages-V_{OL}, V_{OH}, V_{IL}, V_{IH} find the noise margins of the circuit.

Q2. Determine the value of (W/L) of nMOS for resistive load inverter, if

V_{OL}=0.6V, R=10 KΩ, V_{DD}=5V, $V_{th,n}$=1V, $\mu_n C_{ox}$=22μA/V^2

Q3. Consider a CMOS inverter with the given process transconductance parameters- k'n=140 μA/V^2 , k'p=60 μA/V^2 , V_{ton}=0.7 V, V_{top}= - 0.7 V, VDD=3 V.

(a) If the design is ideal and symmetrical, then find out the ratio of (W/L)p and (W/L)n.
(b) Take the case when (W/L)p = (W/L)n, then find out the inverter threshold voltage.

Q4. A CMOS inverter is built in a process where k'n=100 μA/V^2, k'p=42 μA/V^2, V_{ton}=0.7 V, V_{top}= - 0.8 V and a power supply of VDD=3.3 V is used. Calculate the inverter threshold voltage Vth if (W/L)n=10 and (W/L)p=14.

Q5. Find the ratio kn/kp needed to obtain a CMOS inverter threshold voltage of Vth=1.3 V with a power supply of 3 V. Assume that V_{ton}=0.6 V and V_{top}= - 0.82 V. What would be the relative device sizes if the mobility values are related by μ_n=2.2μ_p?