

Course Name: Digital Hardware Design
Course Code: 17B1NEC741



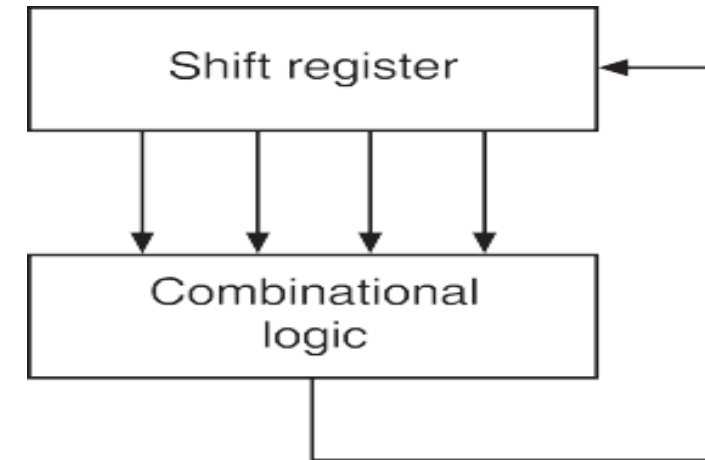
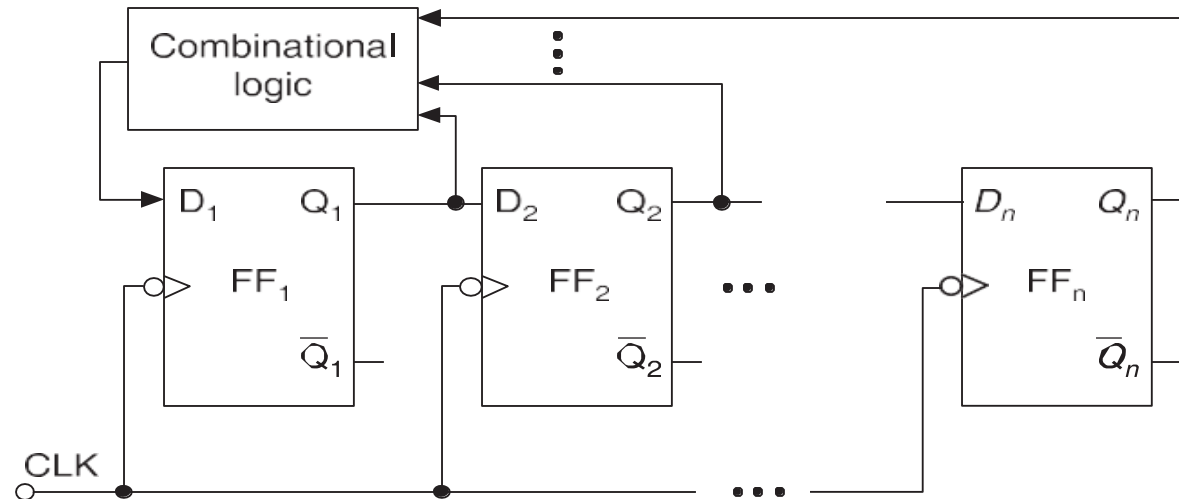
Shift Register Based Sequence Generator

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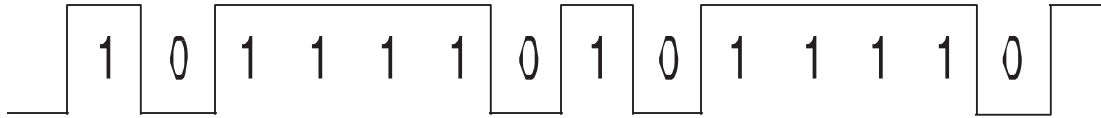
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- Shift registers can be used to generate single pulse trains.
- A shift register is quite restrictive in the sense that it can't go from any one state to any other state of our choice.
- So, the pulse train need to be examined to see if it can be generated by shifting.
- General architecture is shown below:



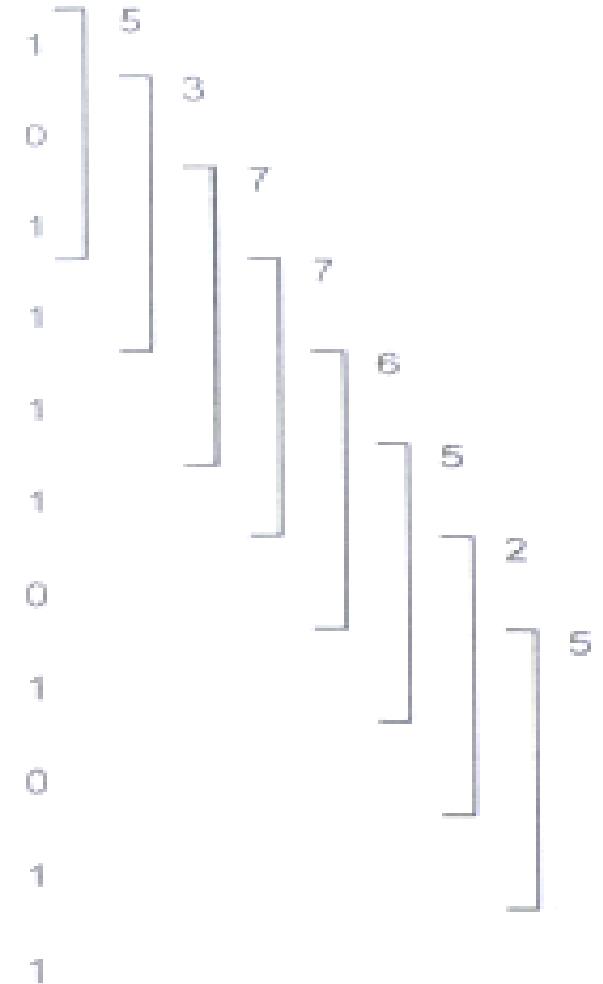
Example-1

Design a pulse train generator using a shift register.



Considering sequence as 1011110

- Since pattern is of 7-bits, minimum of three FFs required.
- Write sequence 1011110 in vertical form.
- Make groups of 3-bit starting from the top bit and
- Write the states in decimal also.
- In 3-bit groups, it can be seen that states 7 and 5 are repeated.
- It means we can't get unique state by using 3-bit
- So make a group of 4-bits and observe again.

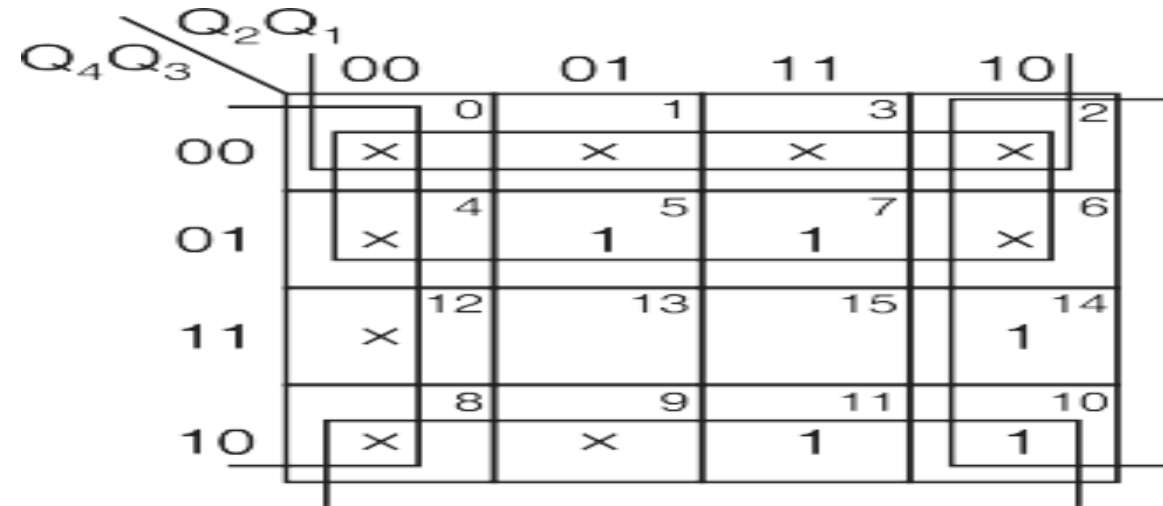




- The states are not repeated, i.e. seven unique states (11, 7, 15, 14, 13, 10, 5) can be obtained using four FFs.
- Make the truth table with the states of register and O/P of the combinational circuit which is to be fed as input to the shift register.
- For each state of a particular group of 4 bits, the next lower bit is O/P of the CLB.
- The unused nine states (0,1,2,,3,4,6,8,9,12) are invalid.

Q_4	Q_3	Q_2	Q_1	f
1	0	1	1	1
0	1	1	1	1
1	1	1	1	0
1	1	1	0	1
1	1	0	1	0
1	0	1	0	1
0	1	0	1	1

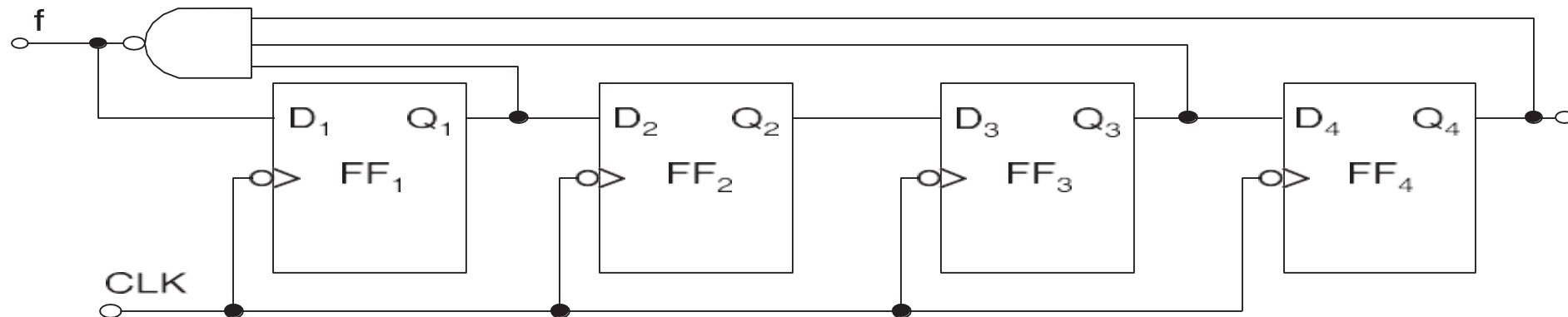
Truth Table



$$f = \bar{Q}_4 + \bar{Q}_3 + \bar{Q}_1 = \bar{Q}_4 Q_3 \bar{Q}_1$$

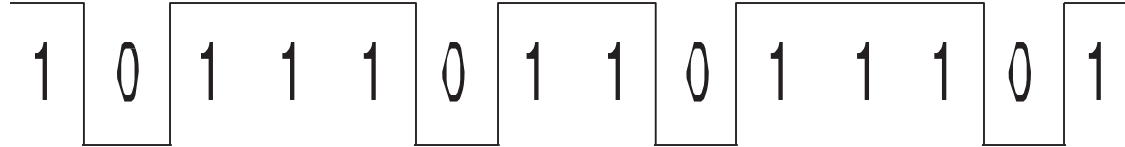
(a) K-map

Complete circuit diagram for pulse train generator for generating 1011110 using shift register technique



Example-2

Design a pulse train generator using a shift register.

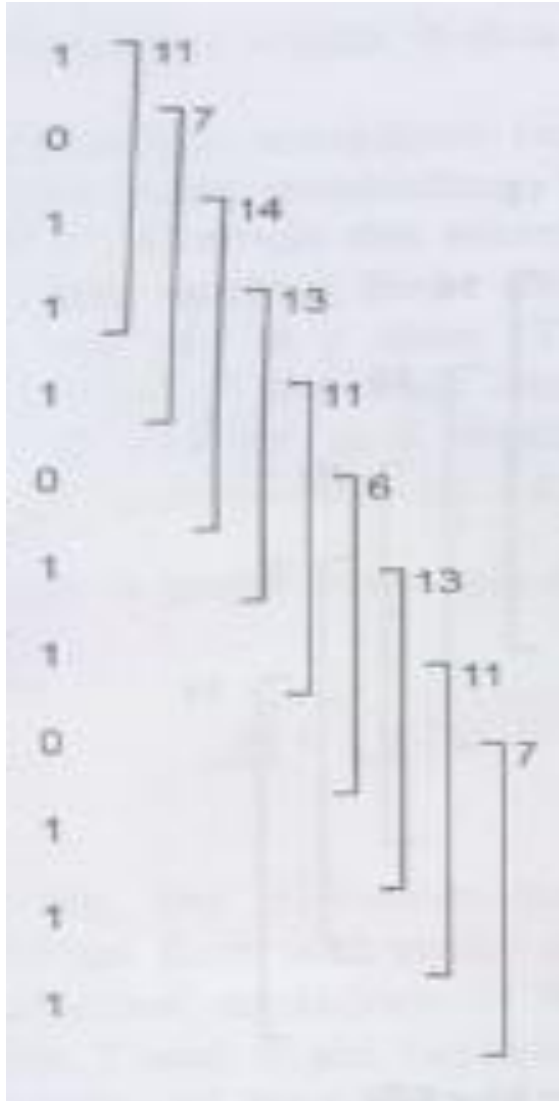


Considering sequence as 1011101

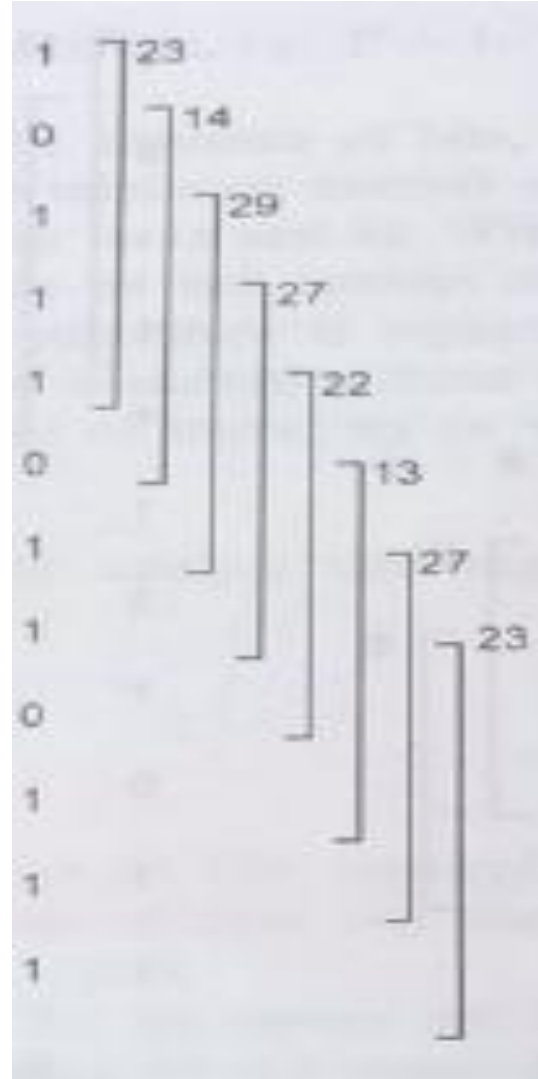
- Since pattern is of 7-bits, so we require minimum of three FFs
- Write sequence 1011101 in vertical form and
- Make groups of 3-bit starting from the top bit and
- Write the states in decimal also.
- In 3-bit groups, it can be seen that few states are repeated.
- It means we can't get unique 7-state by using 3-bit
- So make a group of 4-bits and observe again.



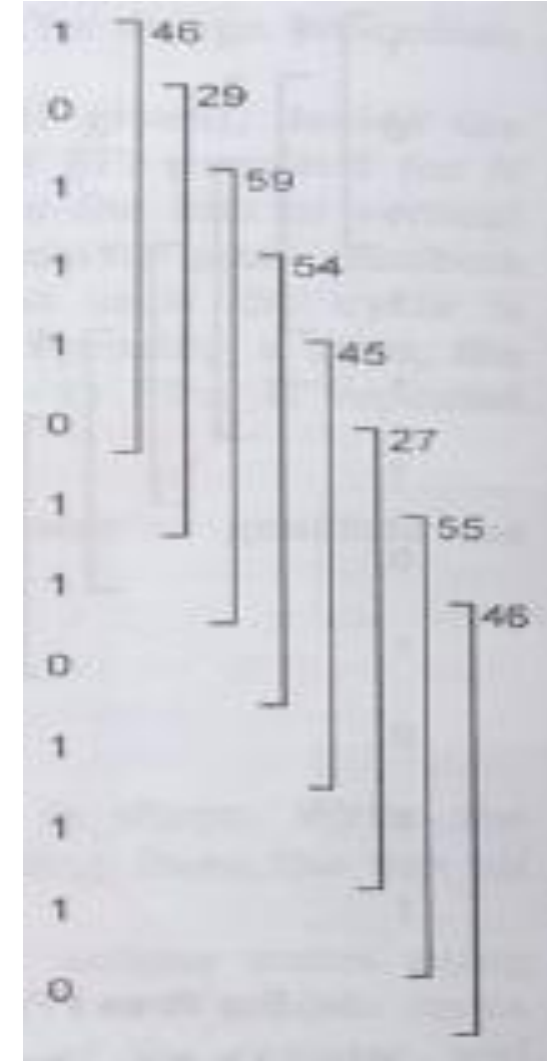
- In 4-bit and 5-bit groups, it can be seen that few states are repeated.
- It means we can't get unique 7-state by using 4 or 5-bit.
- So make a group of 6-bits and observe again



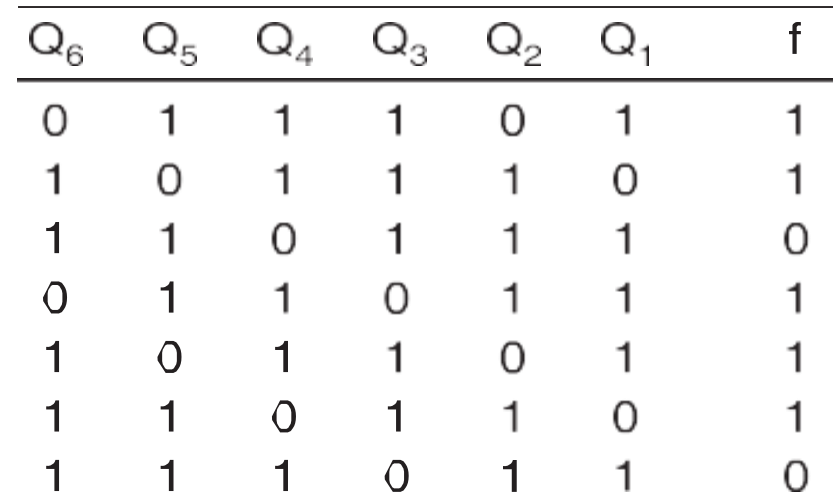
4-bit grouping



5-bit grouping



6-bit grouping



The diagram shows a 6-bit shift register composed of six D flip-flops, labeled FF_1 through FF_6 . Each flip-flop has a data input (D_i), a data output (Q_i), and an inverted data output (\bar{Q}_i). A common clock signal, labeled CLK , is connected to the clock input of every flip-flop. The inputs and outputs are configured as follows:

- The input signal f is connected to the D_1 input of FF_1 and to two 2-input AND gates.
- The output of the first AND gate is connected to the D_6 input of FF_6 .
- The output of the second AND gate is connected to the D_5 input of FF_5 .
- The Q_4 output of FF_4 is connected to the D_5 input of FF_5 .
- The \bar{Q}_5 output of FF_5 is connected to the D_6 input of FF_6 .
- The data output of each flip-flop is connected to the D input of the next flip-flop in the sequence: $Q_1 \rightarrow D_2$, $Q_2 \rightarrow D_3$, $Q_3 \rightarrow D_4$, $Q_4 \rightarrow D_5$, and $Q_5 \rightarrow D_6$.