JAYPEE INSTITUTE OF INFORMATION TECHNOLOGY, NOIDA
Electronics and Communication Engineering
Digital Hardware Design (17B1NEC741)
Tutorial Sheet: 2

Q1 [CO1] A FSM has one input and one output. The output becomes 1 and remains 1 thereafter when at least two 0's and at least two 1's have occurred as inputs, regardless of the order of occurrence .Draw state diagram.

Q2 [CO1] Design FSM for a system which gives output high when bit-1 is in majority in three bit number(overlapping is allowed).Assuming input is coming serially.

10101010101010110011111 => ……0111100

Q3 [CO1] Draw FSM for system which can detect either of the two sequences 110 & 0101(overlapping)

Q4 [CO1] Draw FSM for a system which is getting input bit serially and output is 1 when the present bit & past two bit contains even no of 1's.

Q5 [CO1] Draw FSM for palindrome checker for three bit(overlapping is allowed)

Q6 [CO1] Draw FSM for palindrome checker for 4-bit input .Assuming input is coming serially. It is of overlapping type.

Q7 [CO1] Draw an FSM for system which gives output high when the number of 0's or 1's in past two inputs is more the that of the respective bit present in current input assuming inputs are coming serially.

Q8 [CO1] Implement a two- input Mealy machine that produces a 1 at its single output when the values of the two inputs differ at the time of the previous clock pulse.

Q9 [CO1] A sequential circuit has one input (X) and one output (Z). Draw FSM for each of the give cases:

(a) The output Z=1 if and only if the total number of 1's received is divisible by three (for example 0, 3, 6…..)
(b) The output Z=1 if and only if the total number of 1's received is divisible by two (for example 0, 2, 4, 6…..)

Q10 [CO1] A sequential circuit has two inputs and two outputs. The inputs (X1X2) represent a 2-bit binary number, N. If the present value of N is greater than the previous value, then Z1=1.If the present value of N is less than the previous value, then Z2=1. Otherwise Z1, Z2 are 0. Draw FSM for the same.

Q11 [CO1] Draw FSM for system which takes 3 bit gray-code (MSB first) format and gives output its corresponding binary number.

Q12 [CO1] Design a sequence detector to detect the sequence 110 and output a '1' whenever the sequence is completed including overlapping sequences.

Example: Input: 1100010010011100111111000100111……

Output: 0010000000000010000000100000000……

Q13 [CO1] Draw FSM for system which takes 3 bit binary number (MSB first) and gives output its gray-code equivalent

Q14 [CO1] A Mealy sequential network has two inputs & one output. If the total no of 0's received is ≥4 and at least 3 pairs of input have occurred, then the output should be one coincident with the last input pair in the sequence. Whenever a 1 output occurs, the network resets. Drive state diagram & state table.

Input: X1= 1110001110001100010

X2= 1000001111110100010

Output Z = 0001001000001001001

Q15 [CO1] A sequential network has an input X and two outputs S and V. X represents a 4-bit binary number N which is input least significant bit first. S represents a 4-bit binary number equal to N+2, which is output least significant bit first. At the time fourth input occurs, V=1 if N+2 is too large to be represented by four bits; otherwise V=0. The network always resets after the fourth bit of X is received. Find FSM for the same.

EXAMPLE: X=0111

S=0000(since 14+2=16, and requires 5-bits)

V=0001

Q16 [CO1] Design a Mealy sequential network, which adds 5 to a binary number in the range 0000 through 1010.

Q17 [CO1] A sequential network is having an input signal X and an output signal Z. The output is the same as the input was two clock periods previously. Draw FSM for the same.

Example

X=0101101011010001….

Z= 0001011010110100….