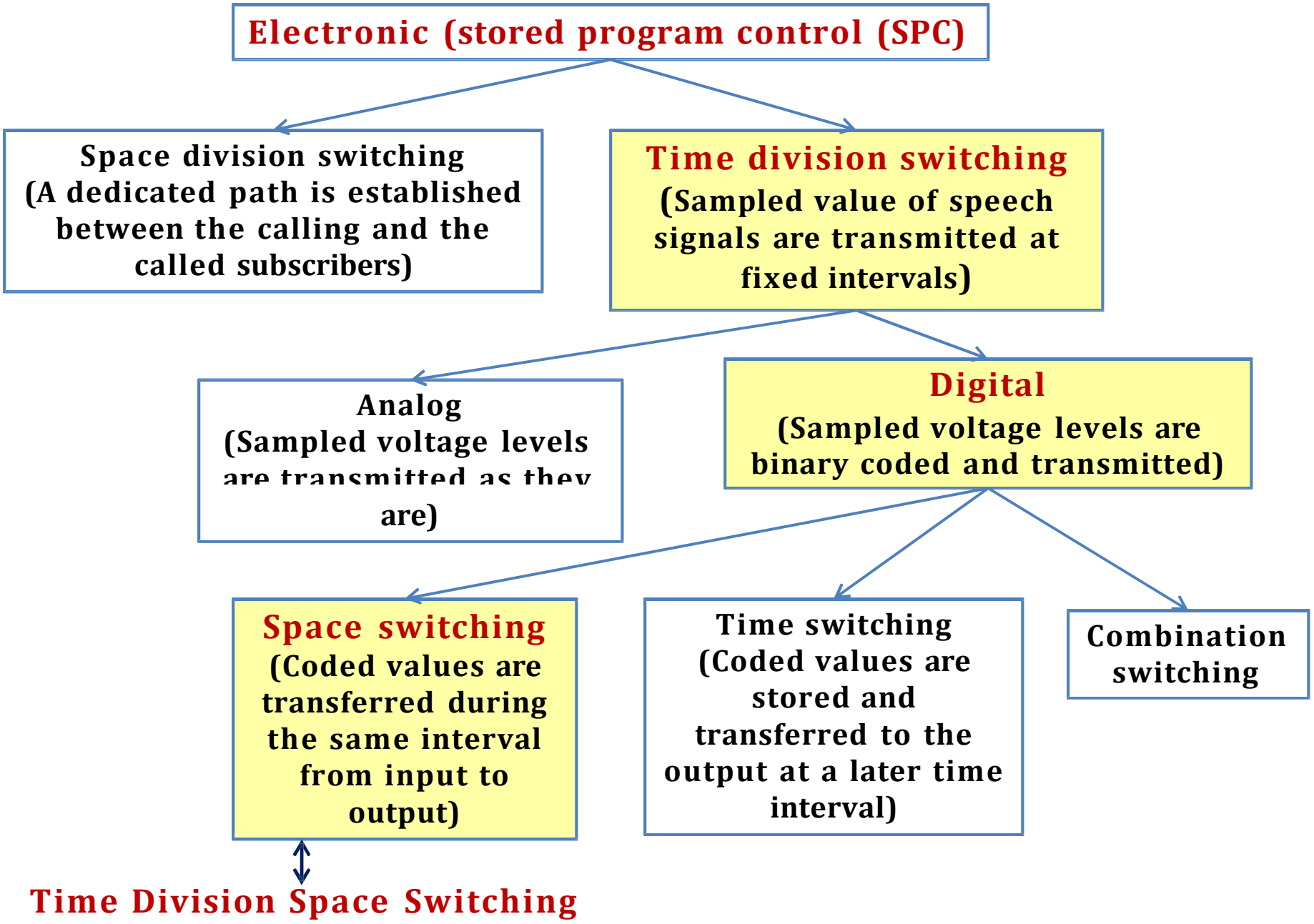
Telecommunication Networks
15B11EC611

Time Division Switching

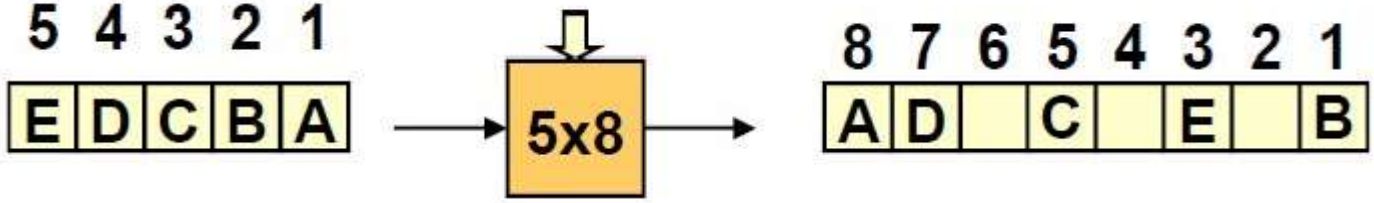

Electronic (stored program control (SPC)
Space division switching
(A dedicated path is established between the calling and the called subscribers)
Time division switching
(Sampled value of speech signals are transmitted at fixed intervals)
Analog
(Sampled voltage levels are transmitted as they are)
Digital
(Sampled voltage levels are binary coded and transmitted)
Space switching
(Coded values are transferred during the same interval from input to output)
Time switching
(Coded values are stored and transferred to the output at a later time interval)
Combination switching
Time Division Space Switching

Digital Time & Space Switch

- Switching can be done in two ways:
  - Time switching
  - Space switching

Time switch

• Contents of time slot are transferred to another time slot in the PCM stream. E.g.



Channel A is moved to time slot 8

Channel B is moved to time slot 1

Channel C is moved to time slot 5

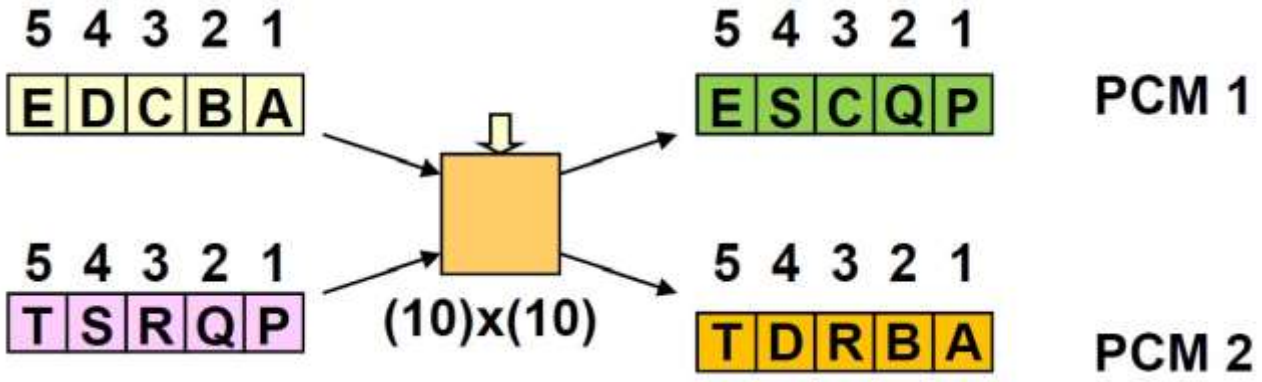
Channel D is moved to time slot 7

Channel E is moved to time slot 3

Digital Time & Space Switch

Space switch

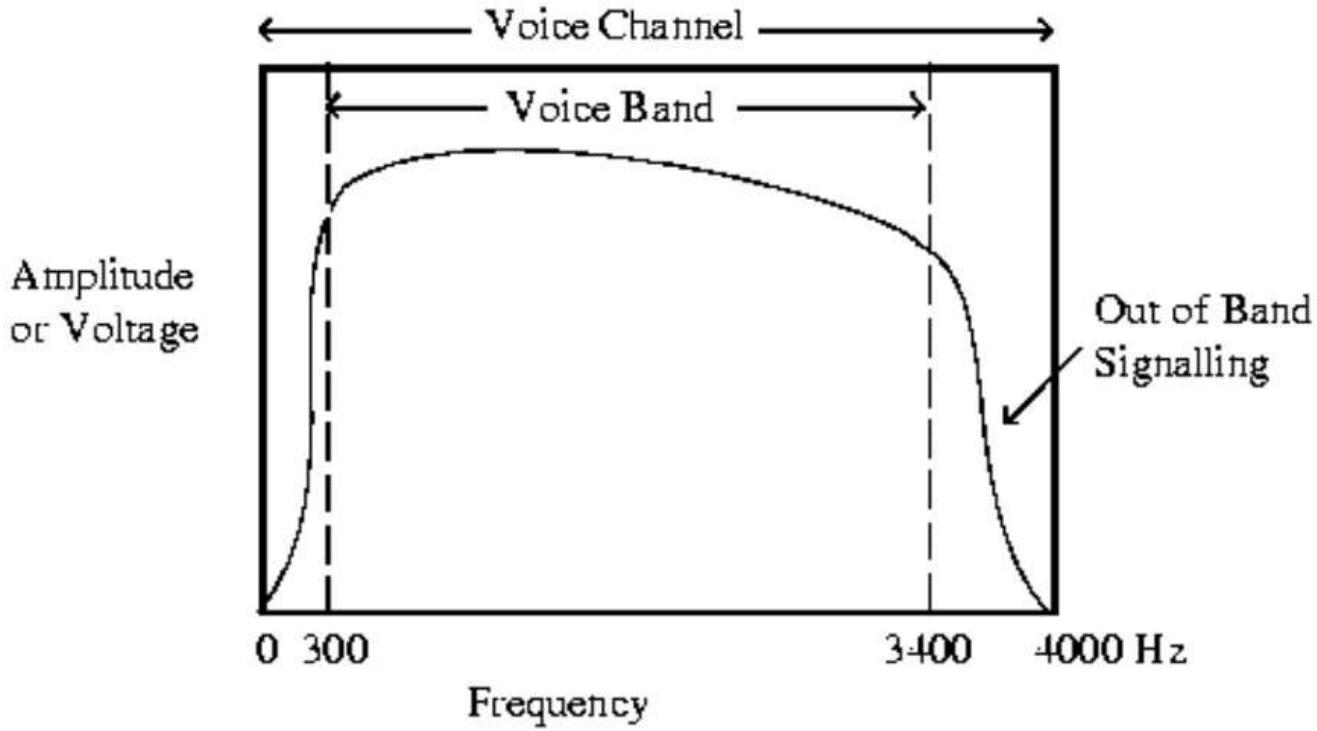
• Contents of a time slot are transferred to the same time slot in another PCM stream. E.g.



- Channels A, B, D are moved to respective time slots of PCM stream 2.
- Channels P, Q, S are moved to respective time slots of PCM stream 1.

Voice Channel Communications

- **Audio Frequency range: 20 Hz – 20 kHz Human ear is capable to perceive**
- **Human speech covers the frequency range of 100 to 7000 Hz**
- **But research has shown that the intelligence part of human speech is carried in the 300 - 3400 Hz range. This range is called the Voice Band.**



Voice Channel Communications

- Analog voice transmission Effect of NOISE and INTERFERENCE is most apparent during speech pauses

- Digital transmission overcome many of the problems faced in analog systems
  - rejection of crosstalk is superior
  - ability to support non-voice services
  - easy data encryption and performance monitoring

- Disadvantage Require greater bandwidth

- The Nyquist Theorem states that to accurately reproduce an analog signal with a digital signal, the analog signal must be sampled a minimum of 2x the highest frequency of the analog signal.

- $f_s \geq 2$ H , f_s = sampling frequency, H = highest frequency component in the input analog waveform

Voice Channel Communications

- For the Voice Channel (0 to 4 kHz) to be digitized, we must sample the Voice Channel at 2x the highest frequency (4 kHz) which would be 8 kHz.

- This means that as soon as you digitize an analog signal, you must immediately double the bandwidth.

✓ Aliasing effect □ if f_s < 2 H, overlapping of sidebands produce

- With 8 kHz sampling rate, a sample occurs every 125 microseconds

Time Division Switching (TDS)

In digital transmission

- sampled value of speech are sent as pulse amplitude modulated (PAM) values or pulse code modulated (PCM) binary words.

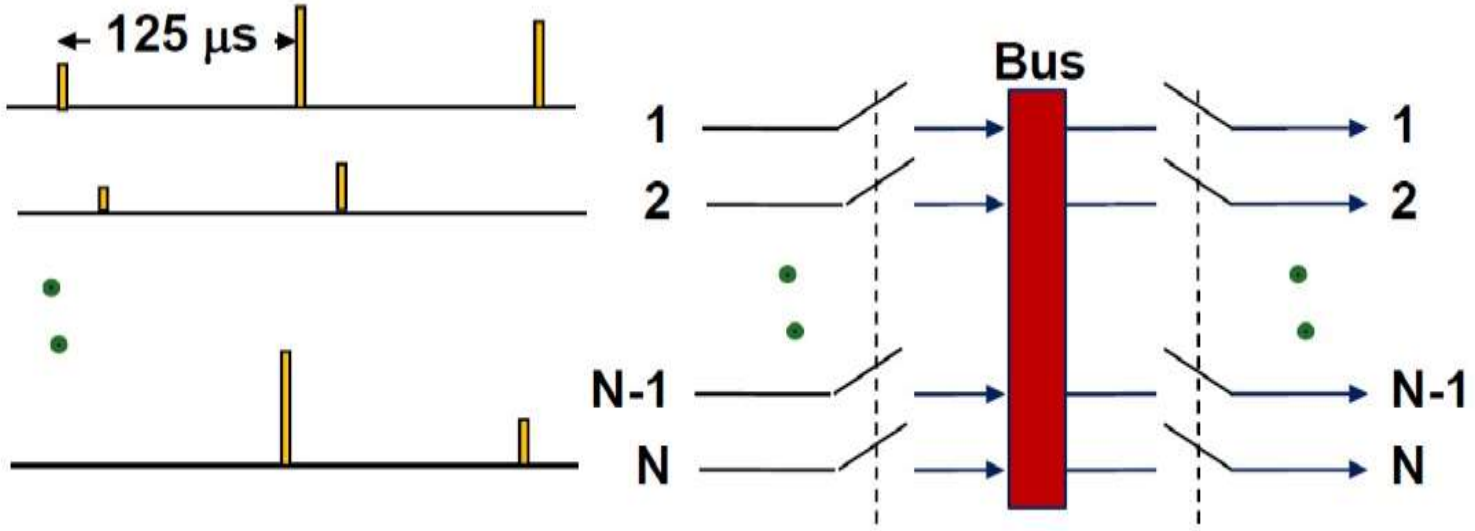
- **With 8 kHz sampling rate, a sample occurs every 125 microseconds**

- In digital domain, a sample can be passed from an inlet to an outlet in a few microsecond or less, through a switching elements.
- As a results, during 125 microseconds sampling interval, a dedicated switching elements remain unused.

Principle of TDS

- If we can establish a dynamic control mechanism whereby a switching element can be assigned to a number of inlet-outlet pairs on time-division basis.
- In other words, a switching elements can be shared by number of simultaneously active speech circuits

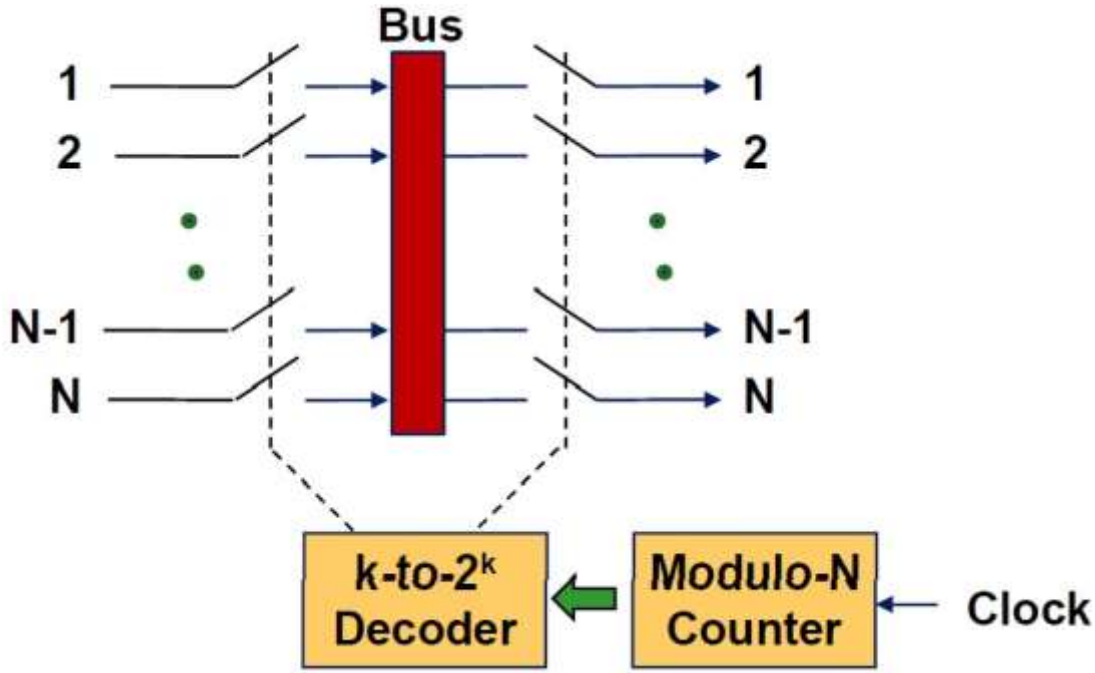
BASIC TIME DIVISION SPACE SWITCHING



- Bus is time-shared between N-inlets and N-outlets.
- Inlets carry PAM or PCM samples of voice channel.
  - Sample of a voice channel are at 125 µs interval.

- When PAM samples are switched, the bus is analog in nature and if the binary samples are switched, a digital bus is used.

BASIC TIME DIVISION SPACE SWITCHING



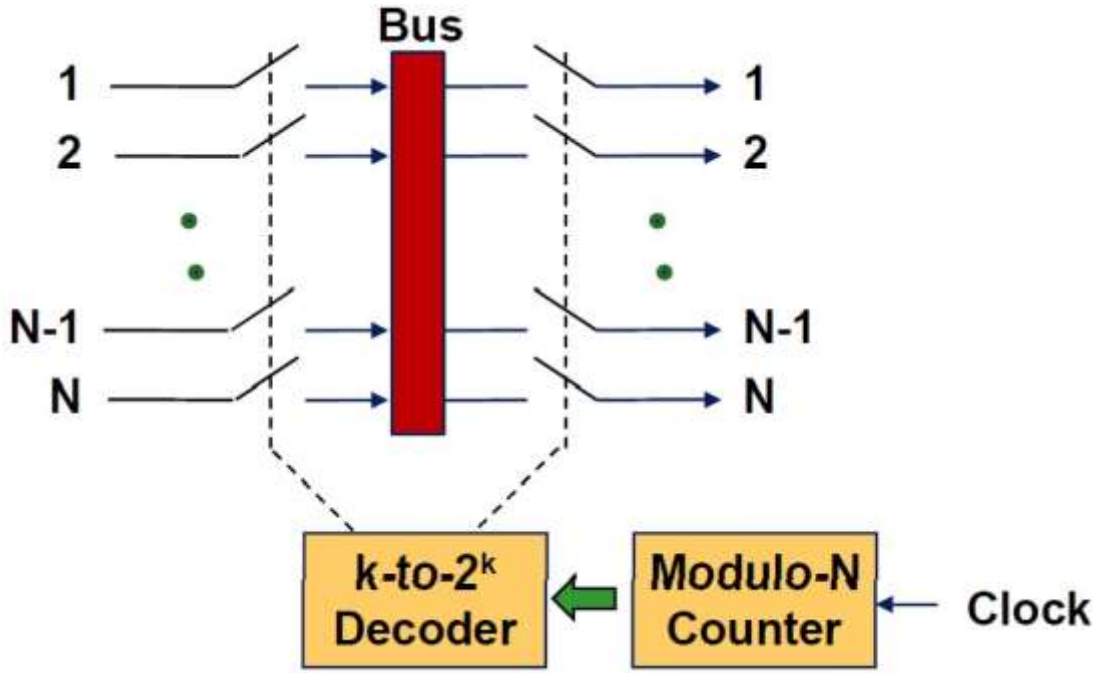
- Access to/from bus is controlled by k-to-2k decoder. E.g. If decoder input is 0010, inlet-2 & oulet-2 are connected to the bus.

- Inlets & outlets are cyclically switched by the decoder.
  - One voice sample of each inlet is transferred to the connected outlet in one cycle.

N and k are related by the equation $\lceil \log_2 N \rceil = k$

Symbol $\lceil \rceil$ $\lceil \rceil$ Ceiling function that gives the lowest integer equal to or higher than the quantity inside the symbol

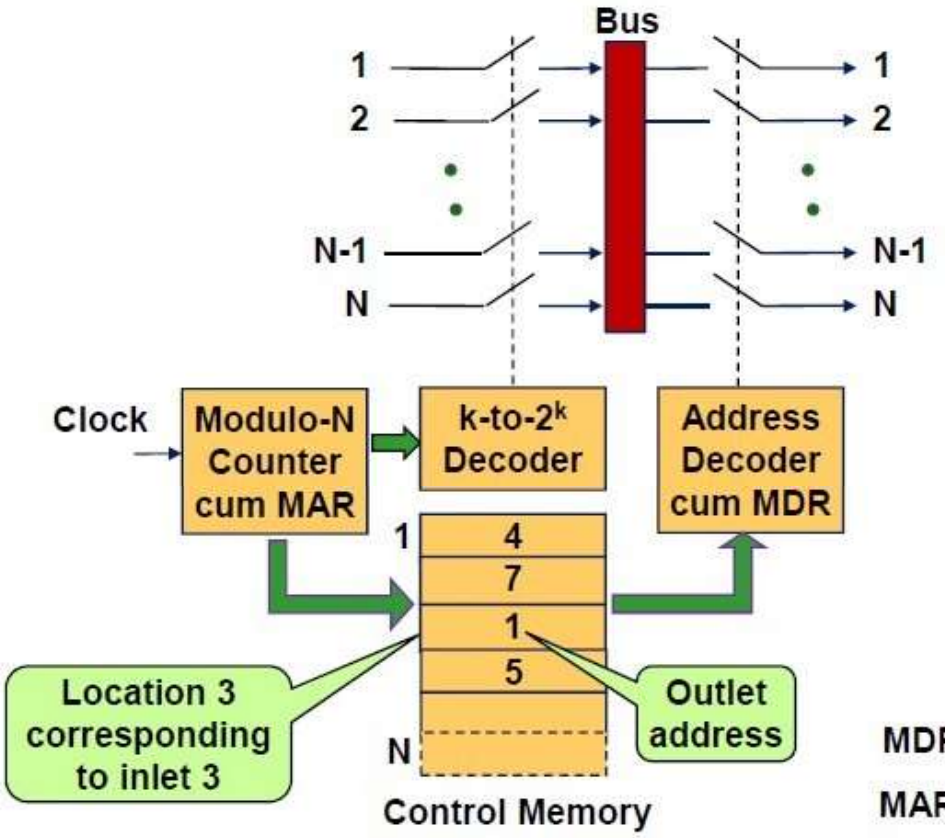
BASIC TIME DIVISION SPACE SWITCHING



- Number of simultaneous possible conversations (SC) is
  - $SC = 125/t_s$ where t_s is time in μs to set up connection and transfer the sample.
- In this configuration, i^{th} inlet is always switched to i^{th} outlet. The switch is non-blocking so long as number of inlets $N \leq SC$.
- But it lacks full availability as it is not possible to connect any inlet to any outlet.

Note: If we make one of the control memory based, then full availability can be obtained.

Input Controlled Time Division Space Switch with Full Availability



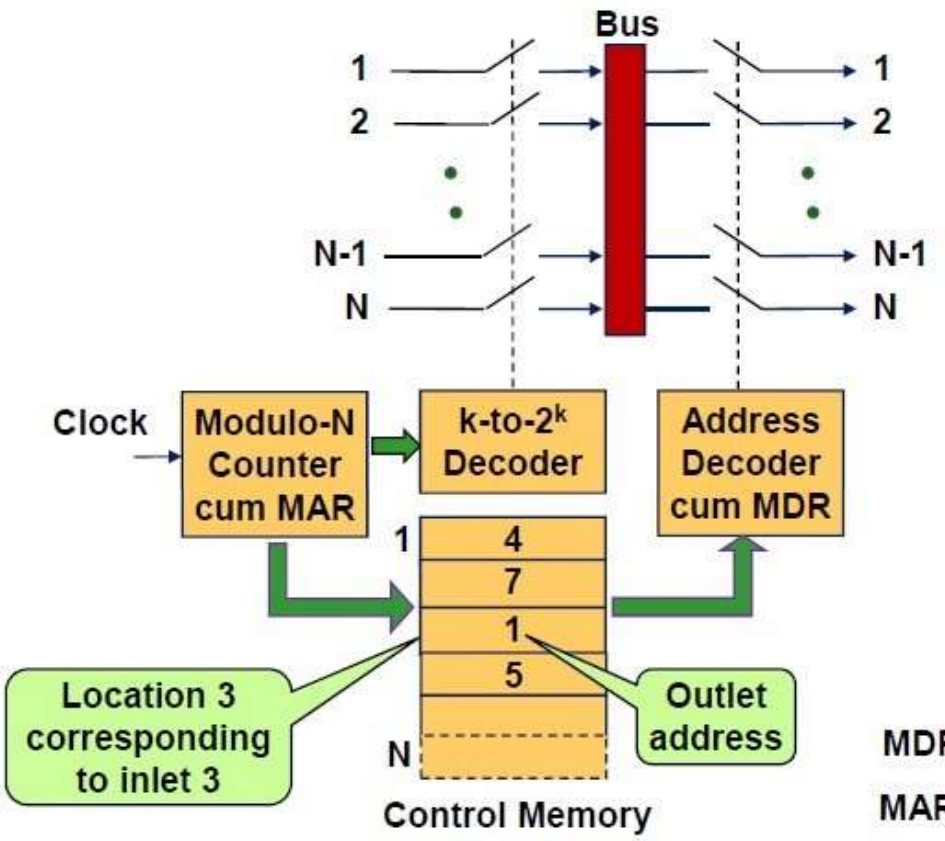
- The input side is cyclically controlled all the subscriber lines are scanned irrespective of whether they are active or not.
- On output side, there is a control memory which contains the address of the outlets

MDR : Memory Data Register

MAR : Memory Address Register

- An address sequence 4-7-1-5 stored in location 1, 2, 3, and 4 of the control memory inlet 1 is connected to outlet 4, inlet 2 to outlet 7, and so on
- The modulo-N counter of the cyclic control also acts as MAR of the control memory.

Input Controlled Time Division Space Switch with Full Availability



- **For an active inlet, the corresponding outlet address is read out and passed to the address decoder which also acts as MDR of control memory.**
- **The decoder output enable the proper outlet to be connected to the bus.**
- **The sample value is then transferred from the inlet to the outlet**

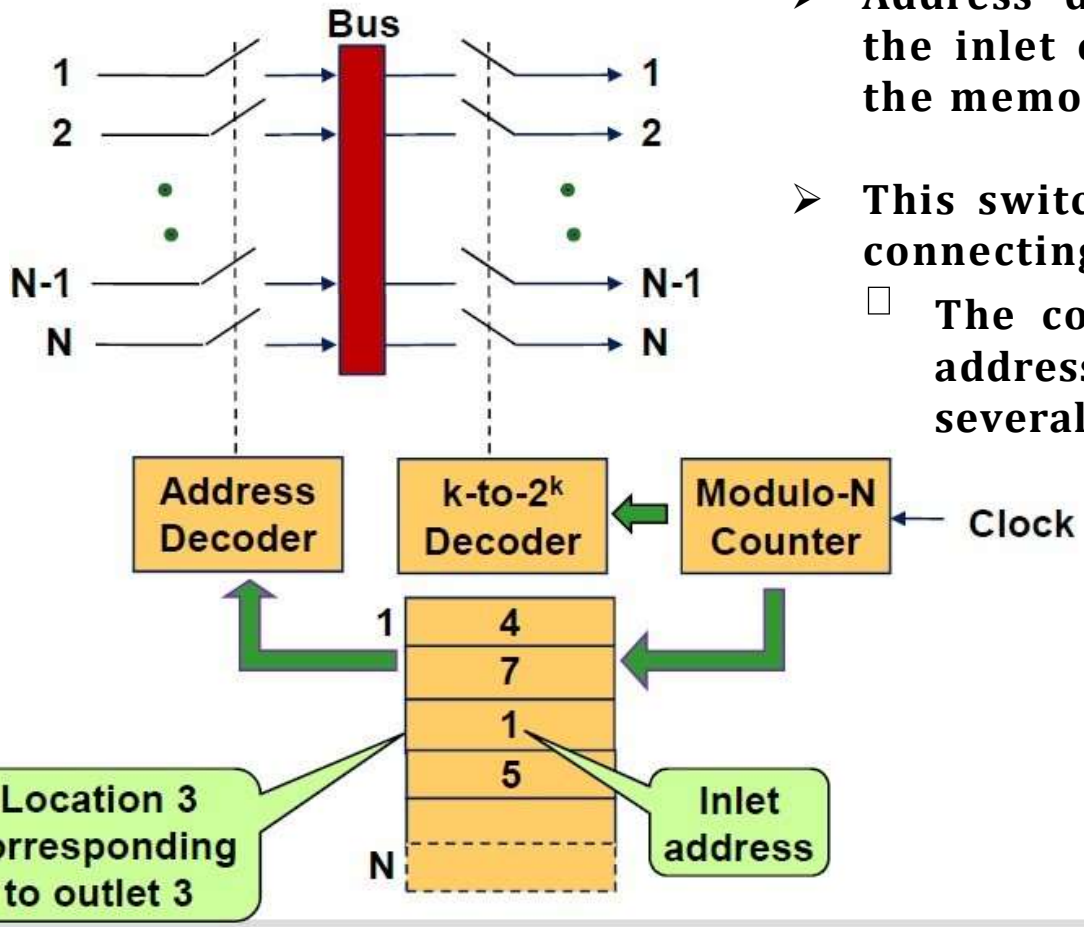
MDR : Memory Data Register

MAR : Memory Address Register

- **In case an inlet is not active, corresponding entry in control memory is null**
- **Any inlet can be switched to any outlet (full availability).**

Output Controlled Time Division Space Switch with Full Availability

- In this alternative configuration, control memory contains inlet address.
- The outlets are cyclically connected to the bus.



- Address decoder connects to the bus the inlet corresponding to the entry in the memory.
- This switch is capable of broadcast i.e. connecting one inlet to several outlets
  - The control memory contains the address of the common inlet in several memory locations.

TIME DIVISION SPACE SWITCHING

- For both input and output-controlled configurations, the number of inlets or outlets N, which is equal to the switching capacity, is given by

$$N = SC = 125/(t_i + t_m + t_d + t_t)$$

Where
t_i = Time to increment the modulo-N counter.
t_m = Time to read control memory.
t_d = Time to decode address and select the inlet/outlet.
t_t = Time to transfer the voice sample from inlet to outlet.

- The required clock rate for N inlets is 8N Kbps as N inlets/outlets are to be switched in 125 µs.

TIME DIVISION SPACE SWITCHING

- The use of cyclic control in input or output control restricts the number of subscribers due to scanning of all lines irrespective of whether they are active or not.
- Full cyclic scanning of all the inlets/outlets in both the input and output controlled configurations restricts the capacity of the switch.
  - In practice, only about 20% of the inlets may be active at any point of time. **Scanning inactive inlets is wasteful**.
- More efficient configuration is possible by using control memory both for the inlets and outlets.
  - This configuration is called **memory controlled time division space switch**.

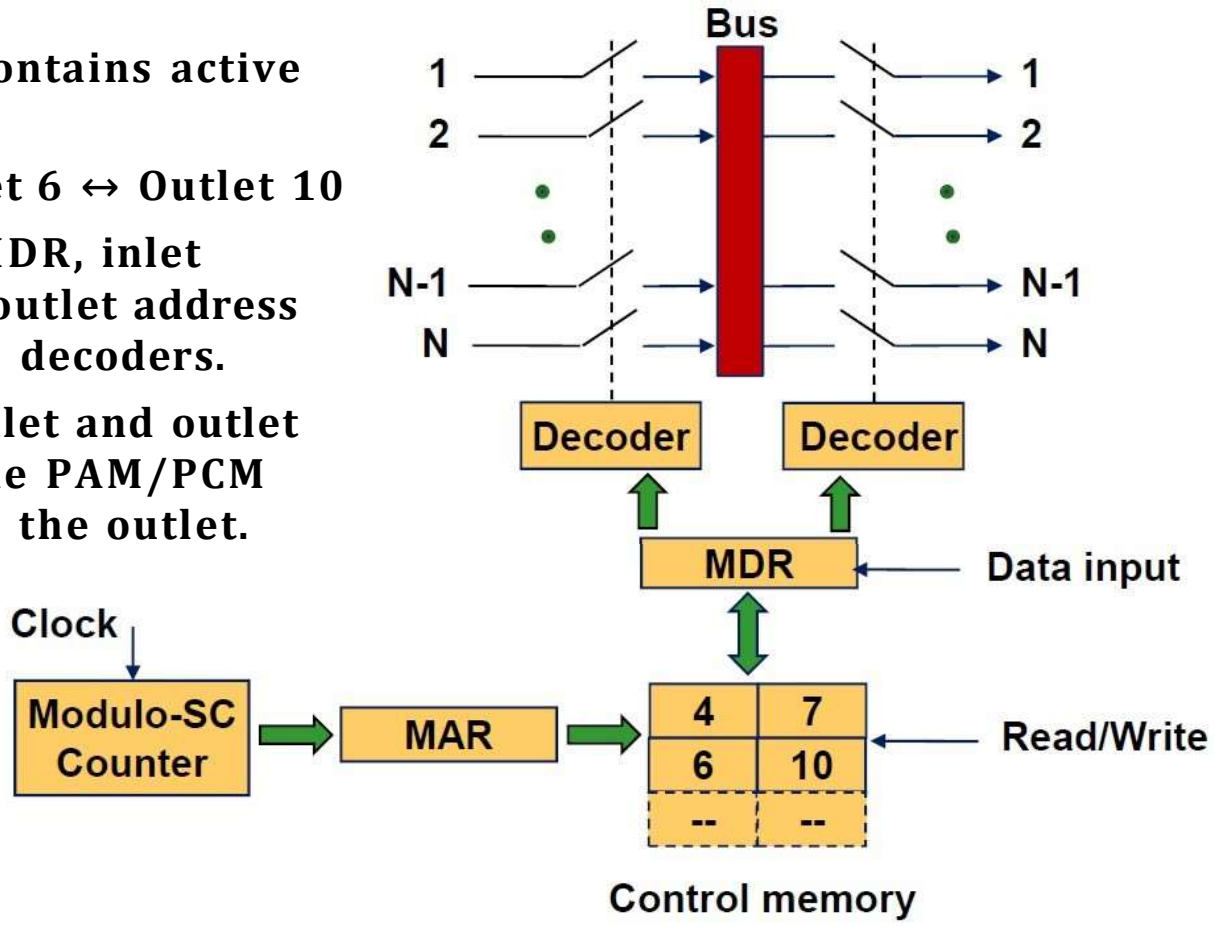
TIME DIVISION SPACE SWITCHING

Memory Controlled Time Division Space Switch

- Here, control memory contains active inlet-outlet pairs. E.g.

  Inlet 4 ↔ Outlet 7, Inlet 6 ↔ Outlet 10

- With the help of MAR/MDR, inlet address and associated outlet address are fed to the respective decoders.
- Decoders connect the inlet and outlet to the bus for passing the PAM/PCM sample from the inlet to the outlet.



- For a new connection,
  - addresses of inlet i and outlet j are entered into free location in control memory.
  - memory location address is updated in MAR.
- When the connection terminates, respective entries in the control memory and MAR entries are erased.

TIME DIVISION SPACE SWITCHING

Memory Controlled Time Division Space Switch

Switching capacity $SC = 125/(t_i + t_m + t_d + t_t)$

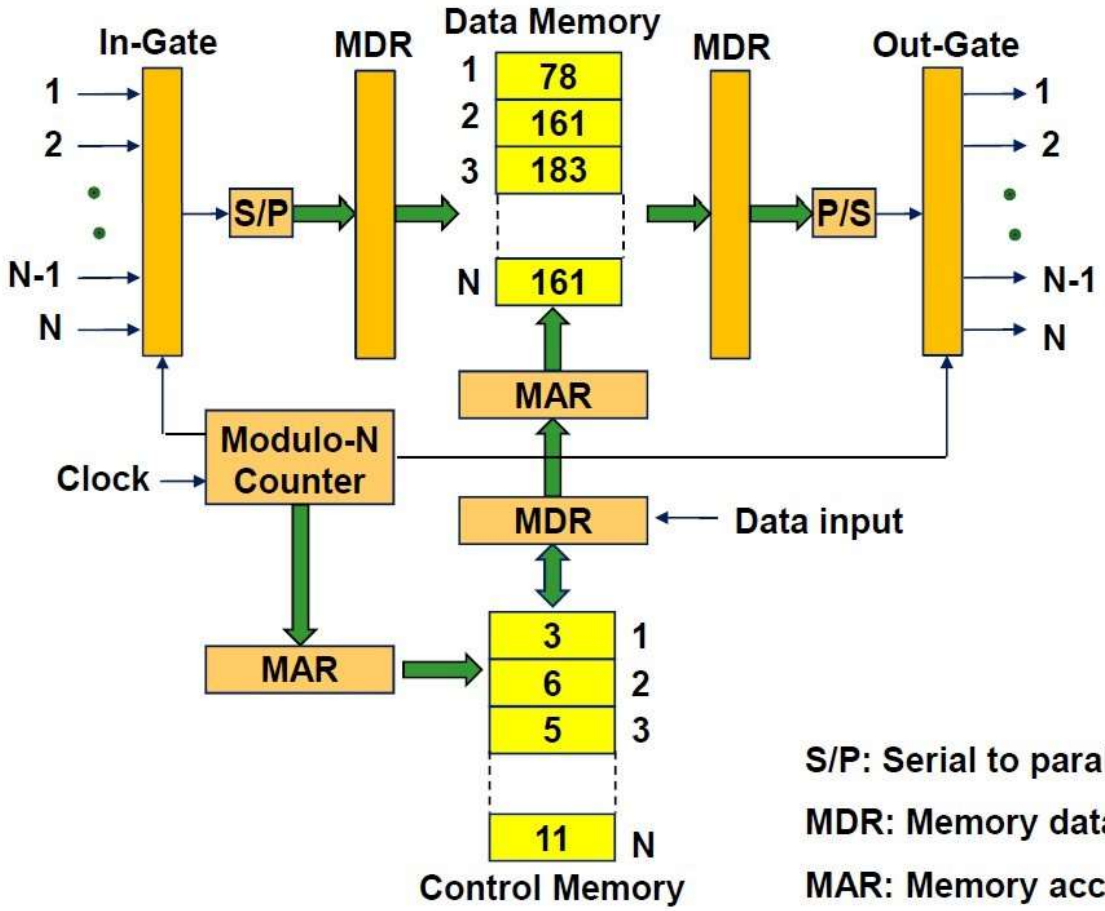
Clock rate = 8 SC KHz

Note: **Here the number of words in the control memory and the size of the modulo counter are equal to the switching capacity of the network, and have no relation to the number of subscribers connected to the network**

Time Division Time Switching

Basic Time Division Time Switching

- Another way of organizing time division switching use a memory block in place of bus
- There is no physical connection between inlets and outlets.
- Information is not transferred in real time. It is first stored in the memory and later transferred to the outlet.
- Time switching requires storage of voice sample in memory. Therefore, voice sample is always PCM



S/P: Serial to parallel converter

MDR: Memory data register

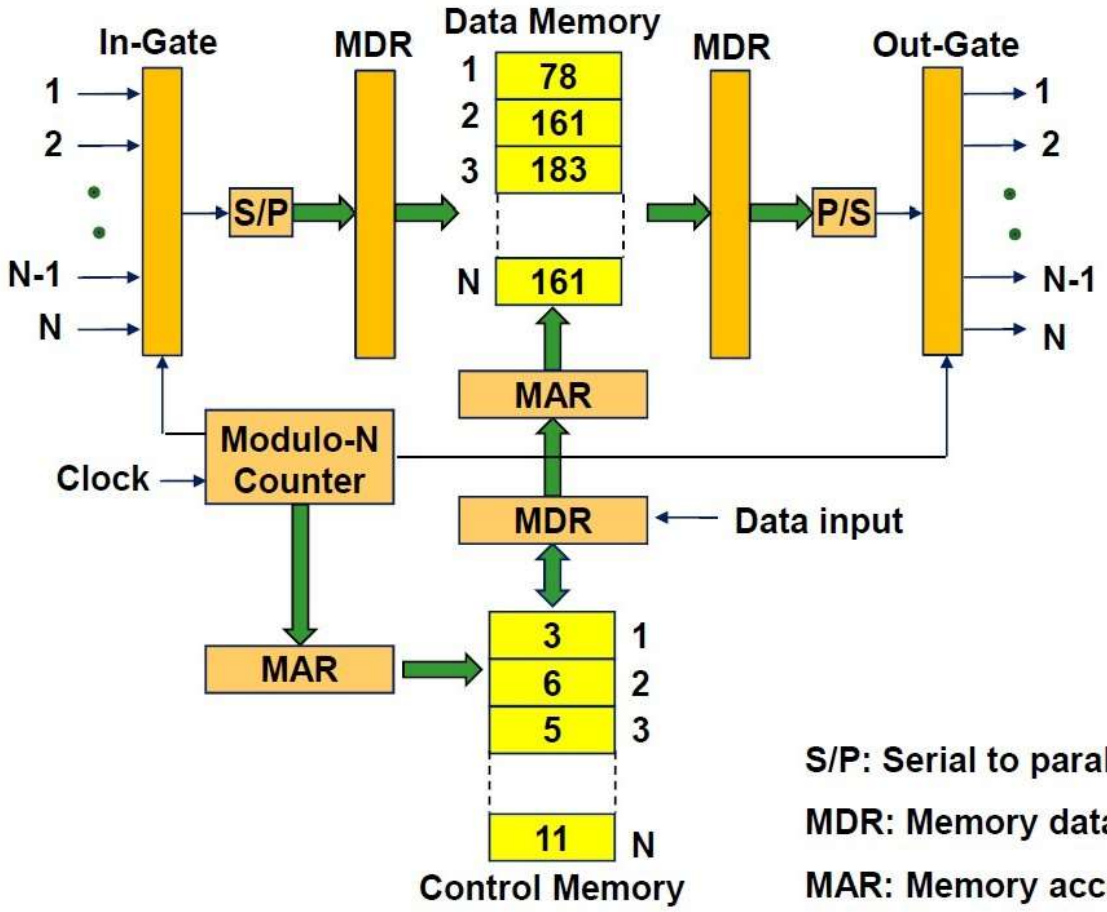
MAR: Memory access register

- Serial-to-parallel (S/P) and parallel-to-serial (P/S) are required as
  - PCM stream is serial data and
  - Memory read/write function handles parallel data.

Basic Time Division Time Switching

- Memory data register (MDR) is a single register but for convenience separate MDRs are shown for input and output sides.

- Since there is one MDR, Gating mechanism is required to connect the required inlet/outlet to the common MDR. This is done by the in-gate and out-gate units.



S/P: Serial to parallel converter

MDR: Memory data register

MAR: Memory access register

- In place of the bus, we have Data Memory.
  - N-inlets write N words of PCM in data memory.
  - Each of these words is read out to the outlet from the data memory.

Basic Time Division Time Switching

- A Time Division Time Switch can be controlled in any of the three ways:
  1. Sequential write/random read.
  2. Random write/sequential read.
  3. Random input/random output.

- refer to the Data Memory (DM).
- In both cases, the inlets and outlets are scanned sequentially.
- In the last case, the inlets and outlets are scanned randomly, and the DM is accessed sequentially.

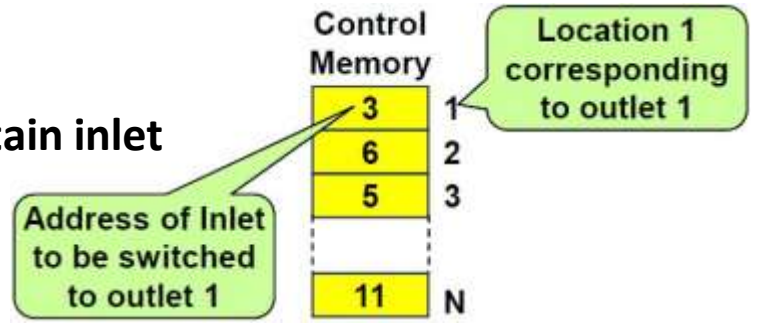
- The above three forms of control have two modes of operation:
  1. Phased operation.
  2. Slotted operation.

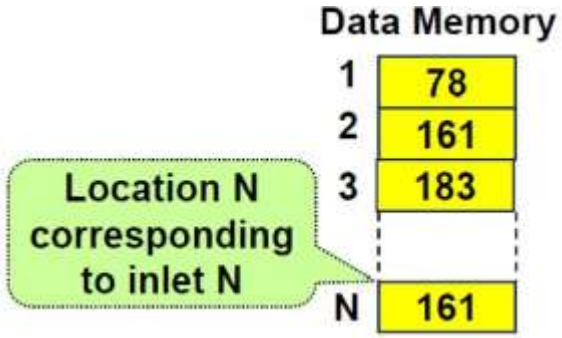
Sequential Write/Random Read

Sequential Write/Random Read

Phased Mode

- To start with, control memory locations 1 to N contain inlet addresses corresponding to 1 to N outlets.



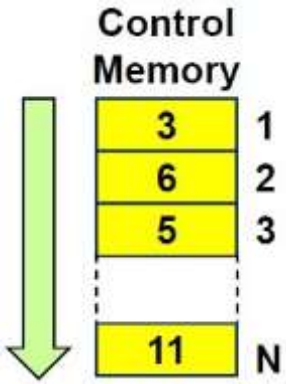


Phase 1

N-inlets are scanned sequentially & data is stored sequentially in Data Memory locations 1 to N.

Phase 2

- Control memory locations 1 to N are read sequentially to get the inlet addresses.
- Data is read from corresponding data memory location & transferred to the outlet.



E.g.

First location contains address '3', and '183' in location 3 of data memory is transferred to outlet 1.

Sequential Write/Random Read

Phased Mode

- In the 1st phase, one memory write is involved per inlet whereas
- In the 2nd phase, two memory reads, one at control memory and the other at the data memory , are involved per outlet
- The time taken for the two-phase operation t_s is given by
  - $t_s = N\ t_d + N\ (t_d + t_c)$
    - t_d = read/write time for the data memory
    - t_c = read/write time for the control memory
- If $t_d = t_c = t_m$ $\square$ $t_s = 3Nt_m$
- Since the entire operation is to be completed within 125 µs $\square$ the number of subscribers can be expressed as
- $t_s = 3Nt_m = 125$ µs $\square$ $N = 125/3t_m$

Example: A 32 X 32 basic time division time switch is operating in sequential write/random read mode. Find the following

1. Number of data lines
2. Number of address lines
3. Size of data memory
4. Size of control memory
5. Design the control memory for the following connections of input & output

   1 ……..20 2 ……..21 3 ……..22

   6 ……..15

Solution:

1. Number of data lines: 8 (always sample converted to 8-bit)

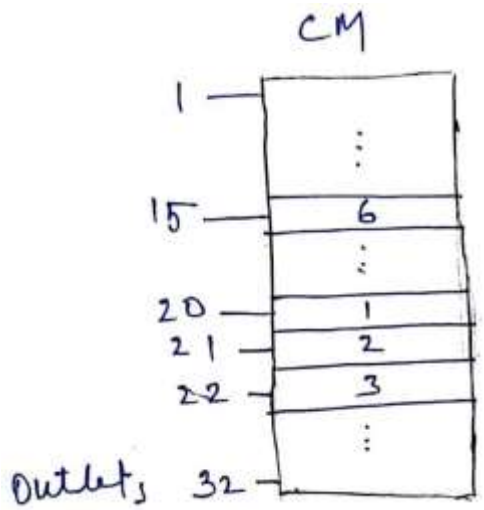
2. Number of address lines: $= \log_2(DM\ \ Locations)$

$$= \log_2(32) = 5$$

3. Size of data memory = 32 x 8 = 256 bits

4. Size of control memory = 32 x 5 = 160 bits

5. Design of control memory (CM)



Example: **A 32 X 64 basic time division time switch is operating in sequential write/random read mode. Find the following**

1. **Number of data lines**
2. **Number of address lines**
3. **Size of data memory**
4. **Size of control memory**
5. **Design the control memory (CM) and data memory (DM) for the following connections of input & output**

   30……α……..50 **12……β……..25** **25……γ……..22**

   16……δ……..64

Solution:

1. **Number of data lines: 8 (always sample converted to 8-bit)**

2. **Number of address lines:** $= \log_2(DM\ \ Locations)$

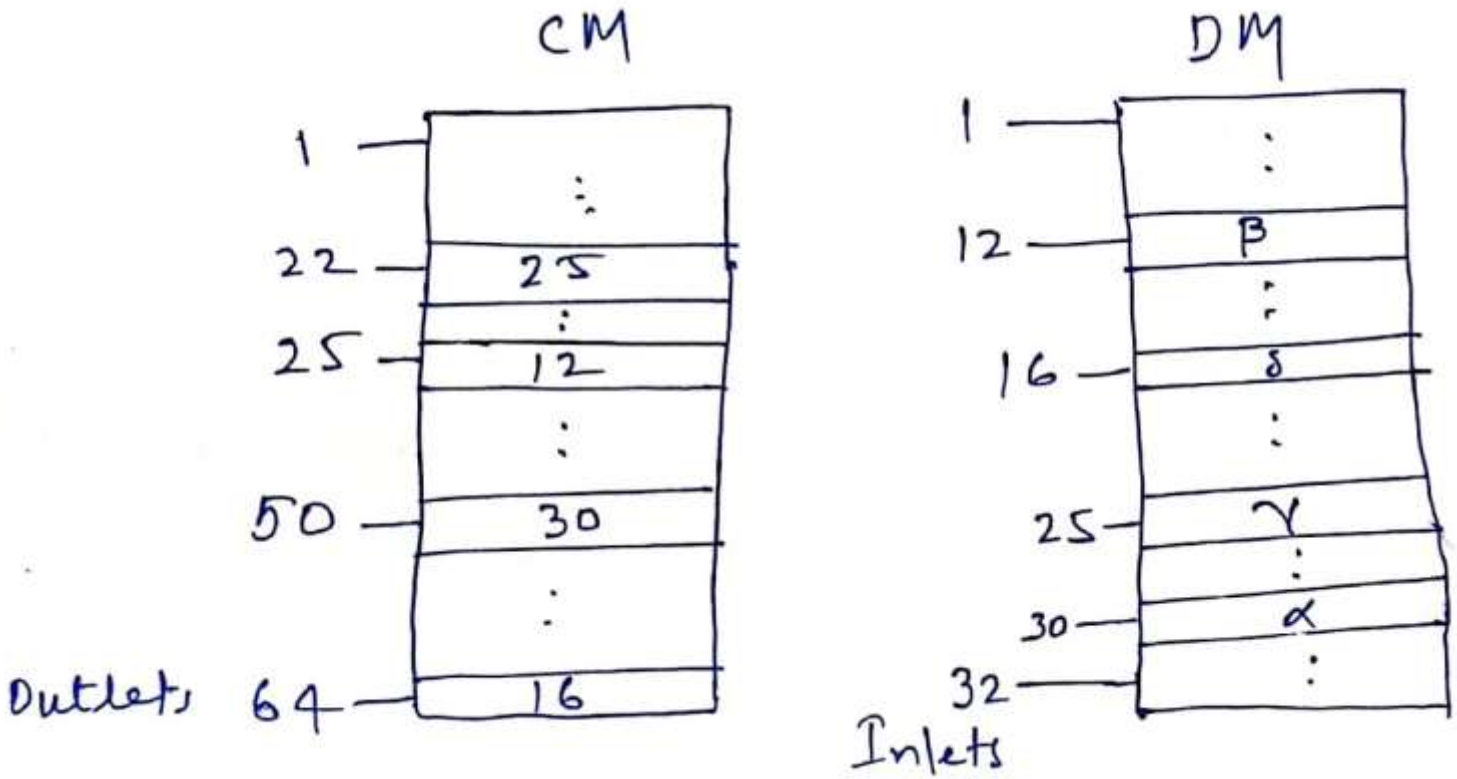
$$= \log_2(32) = 5$$

3. **Size of data memory = 32 x 8 = 256 bits**

4. **Size of control memory = 64 x 5 = 320 bits**

Solution:

5. Design of control memory(CM) and data memory (DM)

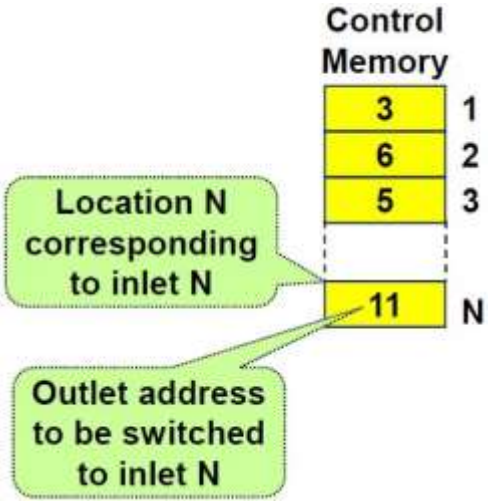


Random Write/Sequential Read

Random Write/Sequential Read

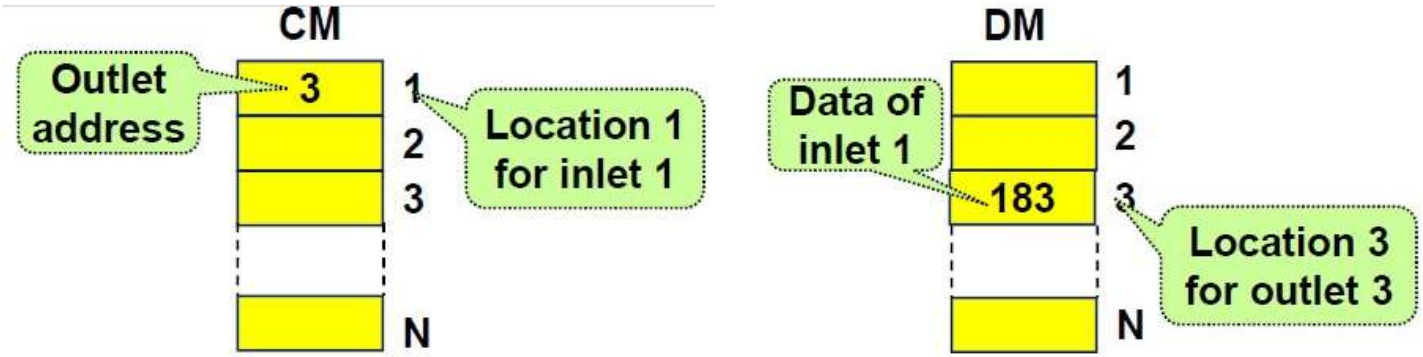
Phased Mode

To start with, CM locations 1 to N contain outlet addresses corresponding to 1 to N inlets.



Phase 1

– CM is scanned sequentially to determine outlet address corresponding to each inlet.
– Inlet data is entered into the corresponding outlet location of DM



E.g.
– 1st CM location has 3. It implies data of 1st inlet is to sent to outlet 3.
– If voice sample data of 1st inlet is 183. Then 183 is entered into location 3 of DM.

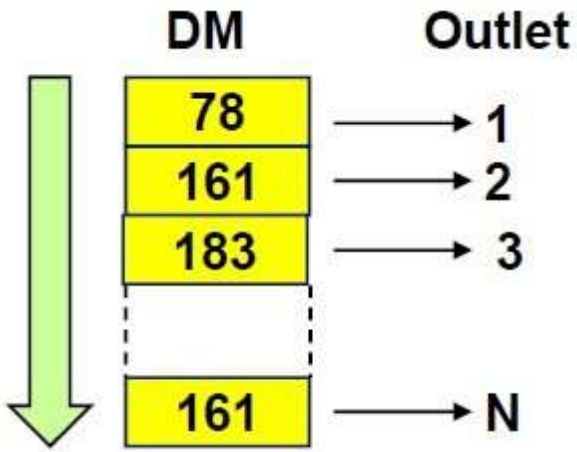
Random Write/Sequential Read

Phased Mode

Phase 2

– DM is read sequentially and data is transferred to respective outlet. E.g.

’78’ is sent to outlet ‘1’
‘161’ is sent to outlet ‘2’



Random Write/Sequential Read

Phased Mode

- Phase 1 has one read (CM) and one write (DM) operation. Phase 2 has one read (DM) operation.
- Time taken for two phase operation is

  $t_s = N(t_m + t_m) + Nt_m = 3Nt_m$

  where t_m is time to read/write (CM/DM).
- Phase 1 & 2 must be completed in 125 μs. Therefore,

  $t_s = 125$ $\qquad$ $N = 125/(3t_m)$

Example: A 128 X 64 basic time division time switch is operating in sequential read/random write mode. Find the following

1. Number of data lines
2. Number of address lines
3. Size of data memory
4. Size of control memory
5. Design the control memory for the following connections of input & output

   110……..11 2……..8 96……..54

   127……..63

Solution:

1. Number of data lines: 8 (always sample converted to 8-bit)

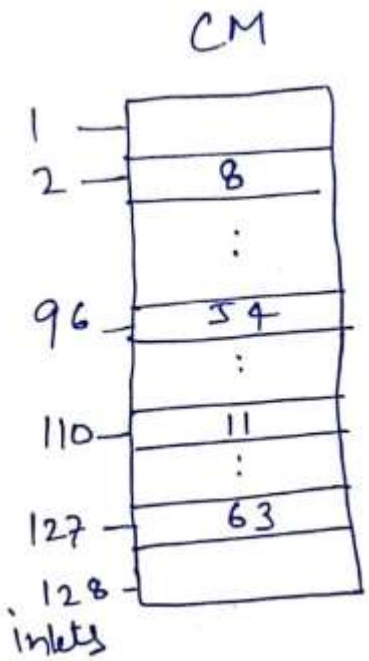
2. Number of address lines: $= \log_2(DM\ \ Locations)$

   $= \log_2(64) = 6$

3. Size of data memory = 64 x 8 = 512 bits

4. Size of control memory = 128 x 6 = 768 bits

5. Design of control memory (CM)



Example: **A 32 X 64 basic time division time switch is operating in sequential read/random write mode. Find the following**

1. **Number of data lines**
2. **Number of address lines**
3. **Size of data memory**
4. **Size of control memory**
5. **Design the control memory for the following connections of input & output**

   30……..50 **12……..25** **25……..22**

   16……..64

Solution:

1. **Number of data lines: 8 (always sample converted to 8-bit)**

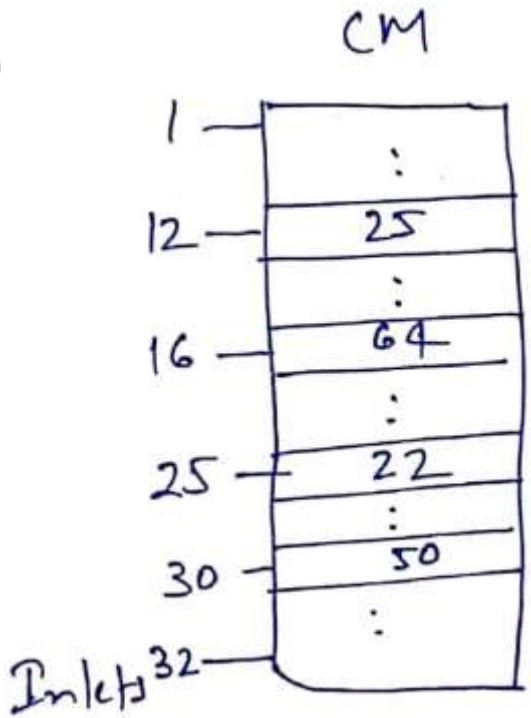
2. **Number of address lines:** $= \log_2(DM\ \ Locations)$

$$= \log_2(64) = 6$$

3. **Size of data memory = 64 x 8 = 512 bits**

4. **Size of control memory = 32 x 6 = 192 bits**

5. **Design of control memory (CM)**



Random Input/Random Output

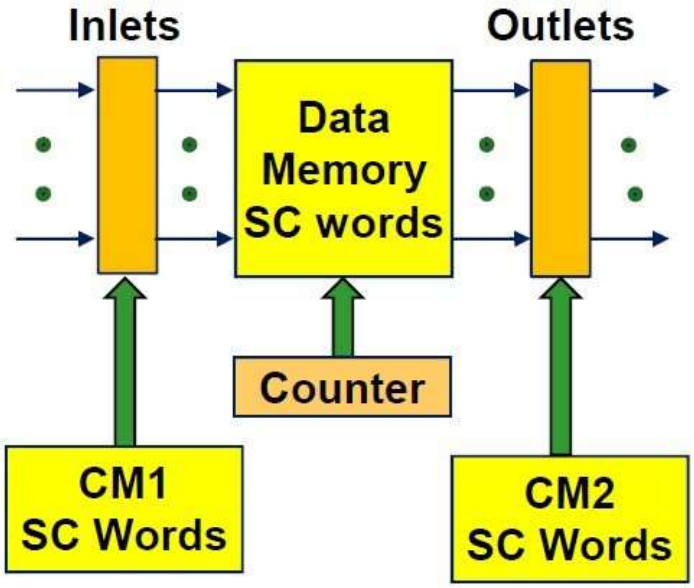
- In both sequential write/random read and random write/sequential read, all the inlets and the outlets are scanned irrespective of whether they are active or not.

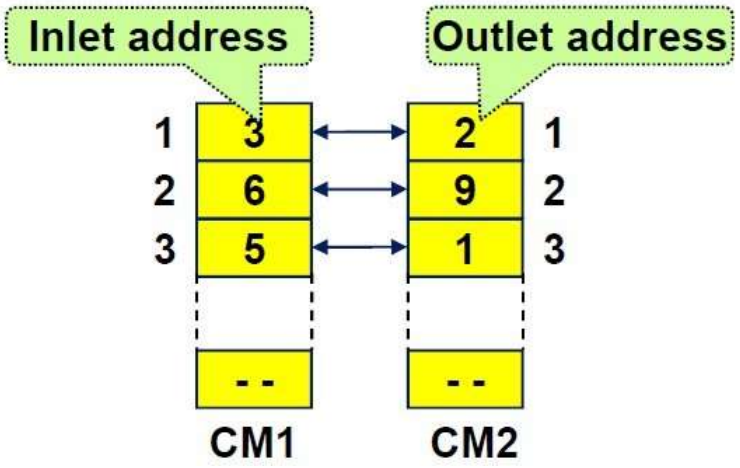
- Scanning inlets/outlets is limits the number of subscribers due to read/write operations that performed in 125-µs interval.

- If we have a scheme whereby only the active subscribers are scanned, then the total number of subscribers can be increased. This scheme refer to Random input/random output.

Random Input/Random Output

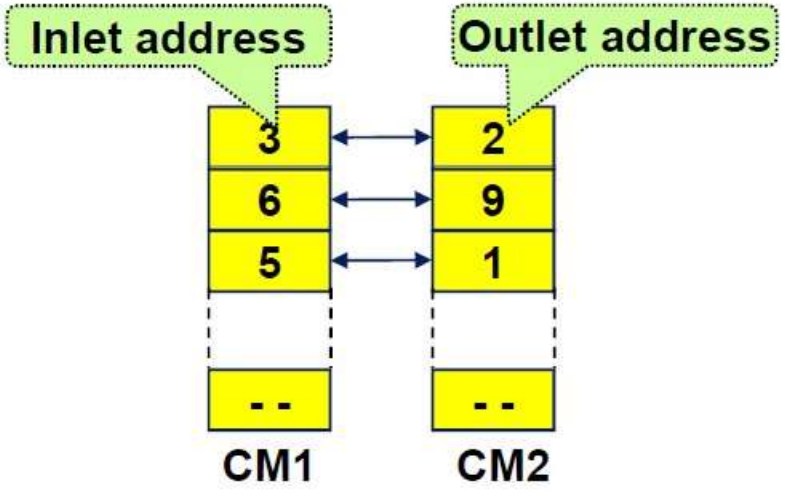
- In random input/random output control, only active inlets/outlets are scanned, thereby increasing capacity of the switch.
- Control Memory CM1 and CM2 hold addresses of active inlets and outlets respectively.
- If address of an active inlet is placed in location *x of* CM1, address of the connected outlet is placed in location *x of CM2.*

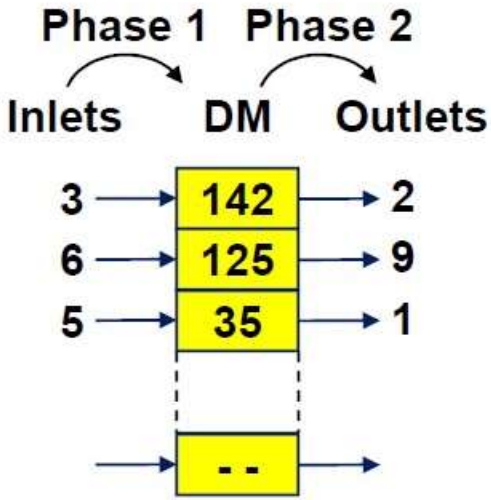




Random Input/Random Output

Phased Mode



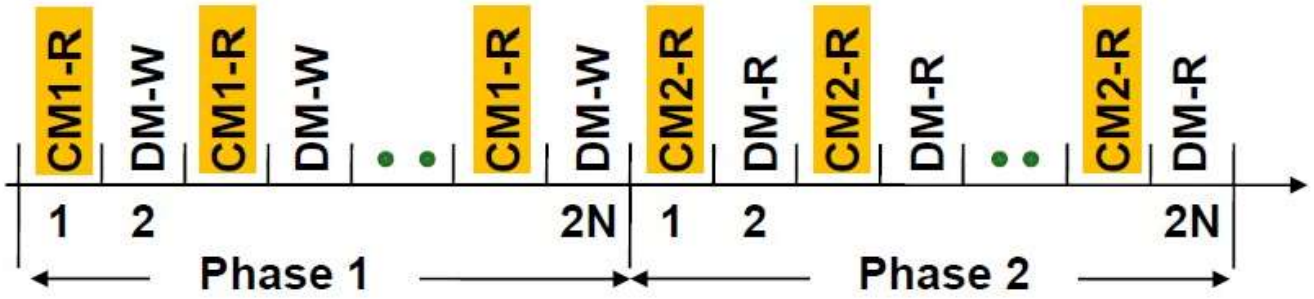


- Phase 1
  - Inlet addresses in CM1 are read one by one. Data from respective inlet is transferred to DM starting from the first location.
- Phase 2
  - Outlet addresses in CM2 are read one by one. Data from DM is transferred to these outlets.

Random Input/Random Output

- There is one read and one write operation in phase 1.
- There are two read operations in phase 2.
- System capacity (SC) is

$$SC = 125/(4t_m)$$




THANK YOU