JAYPEE INSTITUTE OF INFORMATION TECHNOLOGY, NOIDA
Electronics and Communication Engineering
Digital Hardware Design (17B1NEC741)
Tutorial Sheet: 3

Q1 [CO1] A sequential network is having input X & output Y & Z. YZ represents a 2 bit binary numbers equal to the number of pairs of adjacent 1's that have been received as inputs. For example the input sequence 0110 contains one pair, the sequence 01110 contains two pairs & the sequence 0110111 contains three pairs of adjacent 1's.The network resets when the total number of pairs of 1's received reaches 4. Find a Mealy machine FSM for the same.

Example:
Input X 0101101110010101011101101100 10…..
Output Y 0000000111111111110000000011111…..
Z 0000111011111111111000011100000…

Q2 [CO1] A Mealy machine Network has one input & one output. When the sequence 011 occurs, the output becomes 1 & remains 1 until the sequence 011 occurs again, in which the output returns to 0. The output then remains 0 until 011 occurs a third time .This keeps on going. Find FSM for the above problem using minimum states.

Example: Input 01011010110100111……
Output 00001111100000011…..

Q3 [CO1] Design a Mealy sequential network which investigates an input sequence X and which will produce an output of Z=1 if the total number of 1's received is even (consider zero is to be an even number of 1's) and 0's received is odd .

Example: X 1010100110101011010…..
Z 0010000000100010001…..

Q4 [CO1] A system is getting input bit serially & two outputs Z1, Z2. Z1 is 1 every time the sequence 011 is detected and Z2 is 1 only if the sequence 101 is detected before 011 is detected. Find FSM for the above problem using minimum states.

Example: Input 01011010110100111……
Output Z1 00001000000000100……
Z2 00010000000000000……

Q5 [CO1] Design a Mealy sequential network which investigates an input sequence X and produces an output Z=1 if the total number of 1's received is even (consider zero is to be an even number of 1's) and the sequence 01 have occurred atleast once.