POSSESSION OF MOBILES IN EXAM IS UFM PRACTICE.

Name Shashwat Singhal **Enrollment No.** 21102039

Jaypee Institute of Information Technology, Noida
T1 Examination, 2024
B. Tech VI, Semester

Course Title : VLSI Design
Course Code : 18B11EC315

Maximum Time : 1 Hr
Maximum Marks : 20

COs	Course Outcome	Cognitive Levels
CO1	Understand VLSI design flow, VLSI design style, digital system modeling using Verilog-HDL.	Understanding Level (C2)
CO2	Apply MOSFET models for circuits simulation and its effect on scaling.	Applying Level (C3)
CO3	Analyze the concept of static and dynamic characteristics of MOS inverters, combinational and sequential circuits	Analyzing Level (C4)
CO4	Explain and evaluate dynamic logic circuits, stick diagram, layout and different types of semiconductor memories.	Evaluating Level (C5)

Note: Attempt all the questions and assume suitable data if required.

Q. 1: Explain the various VLSI design styles. Also draw the VLSI design flow chart.

(CO1: Understanding Level (C2), 4 Marks)

Q. 2: Derive the expression for I_D in saturation mode for N-channel MOSFET with channel length modulation effect along with suitable diagrams.

(CO2: Applying Level (C3), 5 Marks)

Q. 3: A MOS transistor was fabricated on an n-type substrate with a bulk doping density of $N_D = 10^{15}\,cm^{-3}$, gate doping density (n-type poly) $N_D = 10^{22}\,cm^{-3}$, $Q_{ox} = q.2 \times 10^{10}\,cm^{-2}$ and gate oxide thickness is 0.2 μm. Calculate threshold voltage at room temperature for V_{SB}=0V. (Use: $\varepsilon_{si} = 11.7\varepsilon_0, \varepsilon_{ox} = 3.9\varepsilon_0, \varepsilon_0 = 8.85 \times 10^{-14} F/cm, n_i = 1.45 \times 10^{10}\,cm^{-3}, q = 1.6 \times 10^{-19}\,C$).

(CO2: Applying Level (C3), 5 Marks)

Q. 4: An n-channel enhancement type MOSFET having parameters W= 5 μm, Y= 10 μm, x_j= 2 μm and t_{ox}= 40 nm. The substrate is doped with doping concentration of $1 \times 10^{14}\,cm^{-3}$ and source/drain doped with doping concentration of $2 \times 10^{20}\,cm^{-3}$. The sidewall (p+) doping is $2 \times 10^{15}\,cm^{-3}$. Find the drain-substrate junction capacitance C_{db} if voltage equivalent factor K_{eq}= $K_{eq(sw)}$= 0.52 when substrate bias is 0V and drain voltage is changing from 0.5V to 5V. (Use $\varepsilon_{si} = 11.7\varepsilon_0, \varepsilon_{ox} = 3.9\varepsilon_0, \varepsilon_0 = 8.85 \times 10^{-14} F/cm, n_i = 1.45 \times 10^{10}\,cm^{-3}, q = 1.6 \times 10^{-19}\,C$).

(CO2: Applying Level (C3), 6 Marks)

POSSESION OF MOBILES IN EXAM IS UFM PRACTICE

Name Shashwat Singhal Enrollment No. 21102022

Jaypee Institute of Information Technology, Noida
Test-2 Examination, 2024
B.Tech. VI Semester

Course Title: VLSI Design
Course Code: 18B11EC315

Maximum Time: 1 Hr
Maximum Marks: 20

COs	Course Outcome	Cognitive Levels
CO1	Understand VLSI design flow, VLSI design style, digital system modeling using Verilog-HDL.	Understanding Level(C2)
CO2	Apply MOSFET models for circuits simulation and its effect on scaling	Applying Level(C3)
CO3	Analyze the concept of static and dynamic characteristics of MOS inverters, combinational and sequential circuits	Analyzing Level(C4)
CO4	Explain and evaluate dynamic logic circuits, stick diagram, layout and different types of semiconductor memories.	Evaluating Level(C5)

Note: Attempt all the questions.

[CO3] Q1. (a) Design a CMOS Inverter with the following parameters: **3+2=5 Marks**

nMOS: $V_{to,n}$=0.6V, $\mu_n C_{ox}$=60μA/V²

pMOS: $V_{to,p}$= - 0.8V, $\mu_p C_{ox}$=20μA/V²

Supply Voltage=3V, λ=0

By determining (W/L) ratio of nMOS and pMOS transistor such that switching threshold V_{th}=1.5V.

(b) Draw VTC plot and explain region of operation of CMOS inverter using VTC plot.

[CO3] Q2. Consider a CMOS inverter with a power supply V_{DD}=5V. Determine the time delay elapsed between the time point at which $V_{out}=V_{80\%}$=4V and the time point at which $V_{out}=V_{20\%}$=1V. Use both Average current method and Time domain(differential equation) method for calculation of time delay. The output load Capacitor=1pF and nMOS parameters are: $\mu_n C_{ox}$=20μA/V², $(W/L)_n$=10, $V_{to,n}$=1.5V **2+4=6 Marks**

[CO3] Q3. (a) Find Elmore Interconnect Delay $\tau_{(V1-V2)}$ in Fig 1. **2+2=4 Marks**

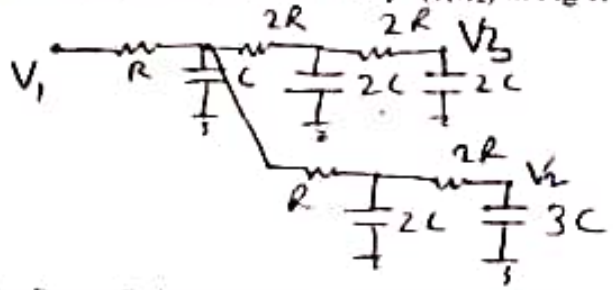

Fig 1.

(b) Derive Power Delay Product of CMOS Inverter.

[CO4] Q4. Realize Boolean function $Z = \overline{A(D+E)+BC}$ using CMOS technology. Find out the common Euler's path and draw optimized stick diagram of the given function. **5 Marks**

POSSESSION OF MOBILES IN EXAM IS UFM PRACTICE.

Name. Shashaat Singhal Enrollment No. 21102022

Jaypee Institute of Information Technology, Noida
End Term Examination, 2024
B.Tech., 6th Semester

Course Title: VLSI Design **Maximum Time: 02 Hrs**
Course Code: 18B11EC315 **Maximum Marks: 35**

CO1	Understand VLSI design flow, VLSI design styles, digital systems modelling using Verilog-HDL.
CO2	Apply MOSFET models for circuits simulation and its effect on scaling
CO3	Analyse the concept of static and dynamic characteristics of MOS inverters, combinational and sequential circuits.
CO4	Evaluate dynamic logic circuits, stick diagram, layout and different types of semiconductor memories.

Note: Attempt all the questions. Assume suitable data if necessary.

Q. 1: (a) Draw and explain Y-chart design hierarchy.
(b) Write the Verilog code for 4:1 Multiplexer using Data flow Modelling.
[CO1 (Understanding), 3+4 Marks]

Q. 2: An NMOS transistor is fabricated with the substrate doping of $N_A = 1 \times 10^{16}\ cm^{-3}$, polysilicon doping $N_D = 1 \times 10^{20}\ cm^{-3}$, and oxide interface charge density is $2 \times 10^{10}\ cm^{-3}$.
(a) Calculate the oxide capacitance (C_{OX}) for the un-implanted transistor with the threshold voltage (V_T) of $0.41\ V$.
(b) To achieve $V_T = 3\ V$ and $V_T = -3\ V$, determine the concentration of impurities to be implanted along with the type of impurities?
[CO2 (Applying), 4+3 Marks]

Q. 3: (a) Implement the given function $F(A, B, C, D) = \overline{(A + B)} . \overline{(C + D)}$ using CMOS.
(b) Consider a CMOS inverter with the following parameters:
NMOS: $V_{t_{on}} = 0.6\ V$, $\mu_n C_{OX} = 60\ \mu A/V^2$, $(W/L)_n = 8$
PMOS: $V_{t_{op}} = -0.7\ V$, $\mu_p C_{OX} = 25\ \mu A/V^2$, $(W/L)_p = 12$
The power supply voltage $V_{DD} = 3.3\ V$. Calculate the switching threshold voltage and noise margin high $(NM)_H$ of the circuit.
[CO3 (Analyzing), 2+5 Marks]

Q. 4: (a) Draw the circuit diagram of CMOS-based D-Latch and discuss its working.
(b) Analyze 2-input XOR gate using CMOS transmission gates.
[CO3 (Analyzing), 4+3 Marks]

Q. 5: (a) Explain Lambda (λ) layout design rules in detail.
(b) Explain the operation of SRAM cell with suitable diagram and waveform.
[CO4 (Evaluating), 3+4 Marks]

POSSESSION OF MOBILES IN EXAM IS UFM PRACTICE.

Name Shashwat Singhal **Enrollment No.** 21102022

Jaypee Institute of Information Technology, Noida

T-1 Examination, 2024

B. Tech 6th Semester

Course Title: Telecommunication Networks **Maximum Time: 1 Hour**

Course Code: 15BITEC611 **Maximum Marks: 20 Marks**

C315.1	To understand the basic concepts of Telecommunication network model, Traffic engineering and switching technology. Also to understand various mechanisms involved in OSI model, TCP/IP and LAN access protocols, ATM and ISDN.	Understanding (C2)
C315.2	To apply the concepts of traffic engineering, switching technologies and various network protocols for solving network related problems.	Applying (C3)
C315.3	To analyze the link utilization and data packet generated after incorporation of data link error control and flow control mechanisms.	Analyzing (C4)
C315.4	To apply the concept of subnetting for creating and assigning address blocks in a network. Applying various routing algorithms to create routing table for communication between two nodes.	Creating (C6)

Q1.[CO2] A call processor in an exchange requires 120 ms to complete 1 process of the call. What is the BHCA rating for the processor? If the exchange is capable of carrying 720 E of traffic, what is CCR? Assume call holding time is 2 mins. **[4 Marks]**

Q2.[CO2] For a 3-stage switching network having 256 inlets and 256 outlets, find out minimum number of switching elements, if the switch is: **[4 Marks]**

a) blocking switch

b) non-blocking switch

Q3.[CO2] A 64x32 basic time division switch is operating in sequential read/random write mode. Find the following: **[4 Marks]**

a) Number of address lines

b) Number of data lines

c) Size of data memory

d) Size of control memory

e) Contents of control memory for following connections of input and output:

50.....30

5.....2

23.....28

16.....32

Q4.[CO1] Explain the working of a memory-controlled time division space switch with the help of a suitable diagram. **[4 Marks]**

Q5.[CO1] Derive the expression of blocking probability for a 3-stage network. **[4 Marks]**

POSSESION OF MOBILES IN EXAM IS UFM PRACTICE.

Name Shashwat Singhal **Enrollment No.** 21102022

Jaypee Institute of Information Technology, Noida
T2 Examination, 2024
B. Tech 6th Semester

Course Title: Telecommunication Networks **Maximum Time: 1 Hr**
Course Code: 15B11EC611 **Maximum Marks: 20**

Upon completion of the course student will be able:
CO1: To understand the basic concepts of Telecommunication network model, traffic engineering and switching technology. Also, to understand various mechanisms involved in OSI model, TCP/IP and LAN access protocols, ATM and ISDN.
CO2: To apply the concepts of traffic engineering, switching technologies and various network protocols for solving network related problems.
CO3: To analyze the link utilization and data packet generated after incorporation of data link error control and flow control mechanisms.
CO4: To apply the concept of subnetting for evaluating address blocks in a network. Applying various routing algorithms to predict routing path for communication between two nodes.

Note: All questions are compulsory.

Q1.**[CO3]** Illustrate the frame format of HDLC protocol. Analyze the control field for I-frame and S-frame in a HDLC protocol. **[5 Marks]**

Q2.**[CO3]** Given the data-word 1010011010 and the divisor 10111,
(a) Show the generation of the codeword at the sender site (using binary division)
(b) Show how to determine an error at the receiver site (if error is introduced in LSB of transmitted code) **[5 Marks]**

Q3.**[CO3]** Derive the utilization factor for Go-Back N ARQ. **[5 Marks]**

Q4.**[CO4]** An ISP is granted a block of addresses starting with 150.80.0.0/12. The ISP wants to distribute its block to three sub blocks as follows:
(a) The first sub block has 256 customers, each need 256 addresses.
(b) The second sub block has 256 customers, each need 128 addresses.
(c) The third sub block has 128 customers, each need 64 addresses.
Design the sub blocks, also find out range of IP addresses which is still available after these allocations. **[5 Marks]**

POSSESION OF MOBILES IN EXAM IS UFM PRACTICE.

Name Shaurya Singhal **Enrollment No.** 21102022

Jaypee Institute of Information Technology, Noida
End Semester Examination, 2024
B.Tech, VI Semester

Course Title: Telecommunication Networks **Maximum Time: 2 Hrs**
Course Code:15B11EC611 **Maximum Marks: 35**

CO1	To understand the basic concepts of Telecommunication network model, traffic engineering and switching technology. Also, to understand various mechanisms involved in OSI model, TCP/IP and LAN access protocols, ATM and ISDN.
CO2	To apply the concepts of traffic engineering, switching technologies and various network protocols for solving network related problems.
CO3	To analyze the link utilization and data packet generated after incorporation of data link error control and flow control mechanisms.
CO4	To apply the concept of subnetting for evaluating address blocks in a network. Applying various routing algorithms to predict routing path for communication between two nodes.

Note: Attempt all the questions.

Q1. A TST switch supports 32 trunks of 16 channels each. A time expansion factor of 4 and a single stage space switch are used. What is the blocking probability of the switch if the channel loading is 0.9 E per channel? **[CO2(Applying), 4 Marks]**

Q2. Consider the use of 1000 bit frames in a 1 Mbps satellite channel with a 200 ms delay. What is the maximum link utilization for
a) Stop and Wait ARQ b) Selective Reject ARQ with window size 127
c)Go back-N ARQ with window size 511
Assume the probability of a single frame to be in error is 0.01. **[CO3(Analysing), 6 Marks]**

Q3. As shown in fig. 1, frames are generated at node A and sent to node C through node B. Considering full duplex lines between the nodes with no errors having data rate between A and B of 100 Kbps, propagation delay is 10 μs/mile for both lines, all data frames are 1000 bit long(ACK frames are separate frames of negligible length), a sliding window protocol with a window size of 3 is used between A & B, and stop & wait is used between B & C. Determine the minimum transmission rate required between nodes B and C so that the buffers of bode B are not flooded. **[CO3(Analysing), 5 Marks]**

Fig. 1

Q4. For the network graph shown in fig. 2, deduce the shortest path tree using Dijkstra Algorithm. Assume 'A' as root node. **[CO4(Evaluating), 5 Marks]**

Q5. Derive throughput of pure ALOHA and slotted ALOHA protocol and sketch the throughput vs offered load graph. **[CO1(Understanding), 5 Marks]**

Q6. Discuss the ATM layers and their functions in detail. What is the relationship between TPs, VPs and VCs? Explain with the help of suitable diagram. **[CO1(Understanding), 5 Marks]**

Q7. How does CSMA/CD protocol inform the stations about the collision? Illustrate with the help of a flow diagram. **[CO1(Understanding), 5 Marks]**

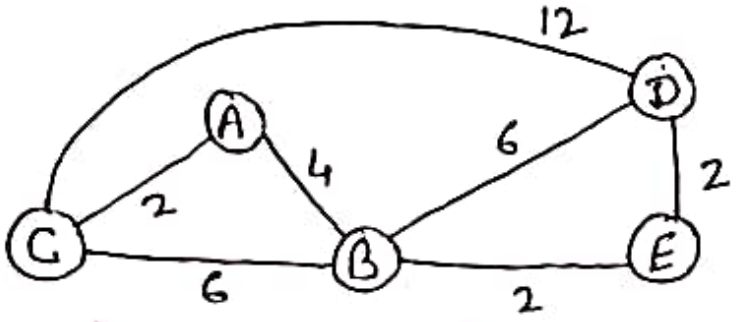

Fig. 2

POSSESSION OF MOBILES IN EXAM IS UFM PRACTICE.

Name Shashwat Singhal **Enrollment No.** 21102029

Jaypee Institute of Information Technology, Noida

T1 Examination, Even Sem 2024

B.Tech VI Semester

Course Title: Semiconductor Devices and Circuits **Maximum Time: 1 hr**
Course Code:23BT12EC311 **Maximum Marks:20**

After the completion of this course, students will be able to

CO1	To recall the basics of semiconductor physics and diodes
CO2	To explain the basics of energy band diagram and optical absorption properties for various two terminal devices
CO3	To apply the concept of semiconductor physics to design the special purpose diodes, transistors and thyristors
CO4	To analyze the operation of different logic families such as bipolar, unipolar and hybrid.

Note: All questions are compulsory.

1. Explain the formation of energy band diagram using two atoms of silicon semiconductor. Also explain the energy momentum diagram

CO1 (Remembering) 2+1 =3 marks

2. Explain in details the tunnel diode with the help of energy band diagram. Also plot its current voltage characteristics

CO2 (Understanding) 3+1= 4 marks

3. Calculate the probability that an energy state 3KT above fermi level is occupied by an electron provided that T=300 kelvin.

$\frac{1}{1+e^{(E-E_F)}}$

CO1 (Remembering) 2 marks

4. Explain the Schottky diode in details. Also explain the ohmic contact in details.

CO2 (Understanding) 3+2 =5 marks

5. Explain heterojunction and its types with the help of energy band diagrams.

CO2 (Understanding) 2 marks

6. Discuss the built-in potential for p-n junction diode at zero applied bias. Find the approximate value of built in potential provided that doping level is tripled on both the sides.

CO2 (Understanding) 3+2= 4 marks

**********End of question paper**********

POSSESION OF MOBILES IN EXAM IS UFM PRACTICE.

Name Shashwat Singhal **Enrollment No.** 22103029

Jaypee Institute of Information Technology, Noida

T2 Examination, Even Semester 2024
B.Tech 6th Semester

Course Title: Semiconductor Devices and Circuits **Maximum Time: 1 hour**
Course Code: 23B12EC311 **Maximum Marks: 20**

	Course Outcomes	Cognitive levels
CO1	Recall the basics of semiconductor physics and devices.	Remembering [C1]
CO2	Explain the basics of the energy band diagram and optical absorption properties for various two terminal devices	Understanding [C2]
CO3	Apply the concept of semiconductor physics to design the special purpose diode, transistors and thyristors.	Applying [C3]
CO4	Analyse the operation of different logic families such as Bipolar, Unipolar and Hybrid.	Analyzing [C4]

All the questions are mandatory.

Q1. Explain the operation of LED. State any two-factors affecting the efficiency of the LED. **(2+1=3 marks)**
Understanding (CO2)

Q2. Explain the photon absorption in details. Explain the photoluminence and electroluminence in details. **(2+1=3 marks)**
Understanding (CO2)

Q3. Differentiate between photoconductor and photodiode. Explain the operation and applications of varactor diode. **(1+2=3 marks)**
Applying (CO3)

$\mu_p = 450$
$\mu_n = 1350$.

Q4. Calculate the photoconductor gain of n type silicon photoconductor with a length = 140 um, area of 10^{-6} cm^2, minority carrier life time of 1 us and voltage of 12 V. **(3 marks)**

Applying (CO3)

Q5. (a) Explain Gunn diode while using gun effect and its oscillator.

(b) For the value of R_{mm}=10 ohms, R_p=1 ohm and Cj= 2nf. Determine the maximum resistance cut off frequency of the tunnel diode. **(4 +2=6 marks)**

Applying (CO3)

Q6. Consider a silicon semiconductor that is illuminated with the photons of energy 1.40 electron volts. Determine the thickness of the material such that 90 percent of the energy is absorbed. **(2 marks)**

Understanding (CO2)

POSSESSION OF MOBILES IN EXAM IS UFM PRACTICE

Name ...Shashwat Singhal

Enrollment No. ...21102022

Jaypee Institute of Information Technology, Noida
End-Term Examination, Even Sem 2024
B. Tech, VIth Semester

Course Title: Semiconductor Devices and Circuits **Max Time: 02 Hrs**
Course Code: 23B12EC311 **Max Marks: 35**

Course Outcomes: At the end of the course, students will be able to:

CO1	Recall the basics of semiconductor physics and devices.
CO2	Explain the basics of energy band diagram and optical absorption properties for various two terminal devices.
CO3	Apply the concept of semiconductor physics to design the special purpose diode, transistors and thyristors.
CO4	Analyse the operation of different logic families such as Bipolar, Unipolar and Hybrid.

Note: Attempt all the questions.

Q1. Define the built-in potential voltage. Calculate V_{bi} in a silicon P-N junction at T=300K for $N_A = 2\times10^{15}$ cm^{-3} and $N_D = 2\times10^{16}$ cm^{-3}. Consider the intrinsic semiconductor concentration (n_i) for silicon is 10^{14} cm^{-3}. **[CO1 (Remembering), 4 Marks]**

Q2. Describe the charge flow in a forward-biased Schottky barrier diode. Draw the energy-band diagram of zero-biased, reverse-biased and forward-biased Schottky diode.

[CO2 (Understanding), 6 Marks]

Q3. Describe the concept of excess carrier generation and recombination. Calculate the generation rate of GaAs electron-hole pairs at T=300K. Assume that the photon intensity at a particular point is $I_V(x) = 0.06$W/cm^2 for wavelength $\lambda = 0.75\mu$m, $\alpha = 0.9\times10^{16}$, and carrier life time $\tau = 10^{-8}$ s.

[CO2 (Understanding), 5 Marks]

Q4. Explain the vertical power bipolar transistor. Determine the required current, voltage and power rating of a power BJT as shown in figure 1. The parameters are $R_C = 10\Omega$ and $V_{CC} = 35$V. Also draw the load line and maximum power curve. **[CO3 (Applying), 6 Marks]**

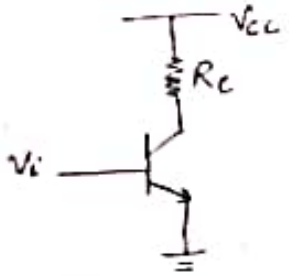

figure 1

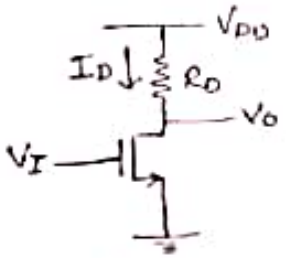

figure 2

Q5. Explain the working of double-diffused MOS (DMOS) transistor. For the common source circuit as shown in figure 2, determine the required current, voltage and power rating of MOSFET for (a) $R_D = 12\Omega$, $V_{DD} = 24$V and (b) $R_D = 8\Omega$, $V_{DD} = 40$V. **[CO3 (Applying), 6 Marks]**

Q6. Explain how the gate terminal of a semiconductor controlled rectifier can control the switching characteristics. **[CO3 (Applying), 3 Marks]**

Q7. Explain the working of BiCMOS inverter circuit. Draw the minimum CMOS transistor network that implements the functionality of Boolean equation F= ((AB+CD)E)'. **[CO4 (Analyzing), 5 Marks]**