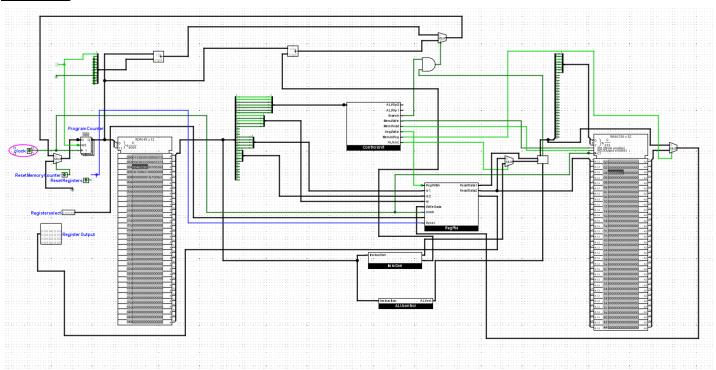
# **PROCESSOR**

Anup Lal Nayak 2022CS51827 Lucky Ahirwar 2022CS52049

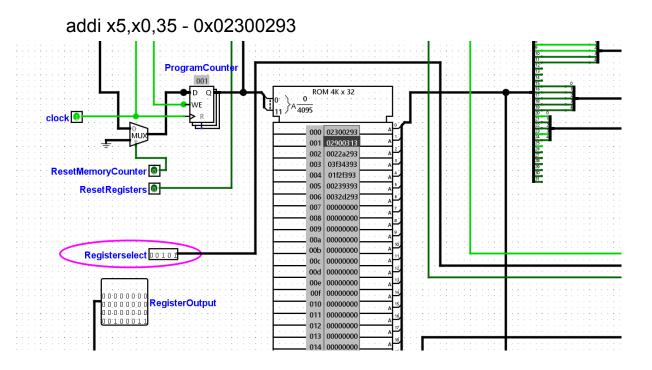
### **Design Decisions:**

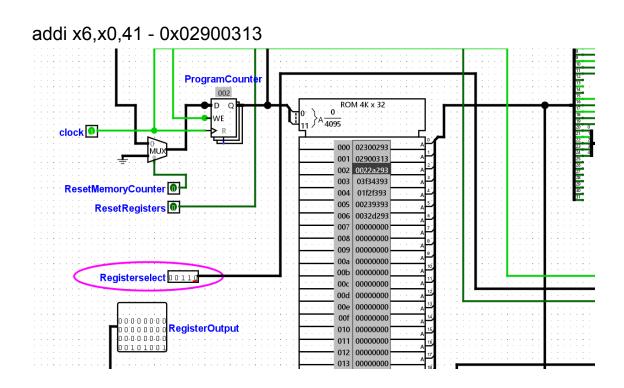
- 1. We used instruction memory address width as 12 bit since keeping it as 24 bits was taking 160mb of memory and we could not submit that on moodle.
- 2. We are storing instruction memory at increments of 1.
- 3. We made separate inputs for resetting the register file and resetting the program counter.

### **TESTING**:

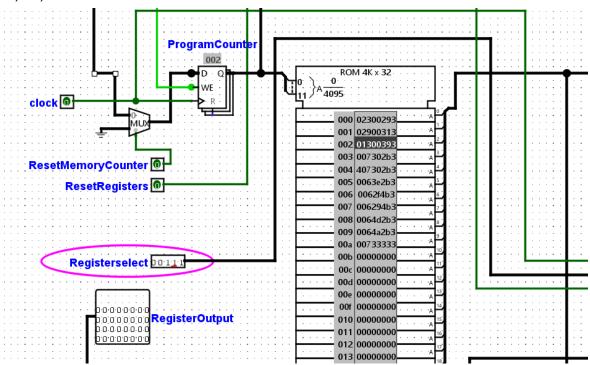


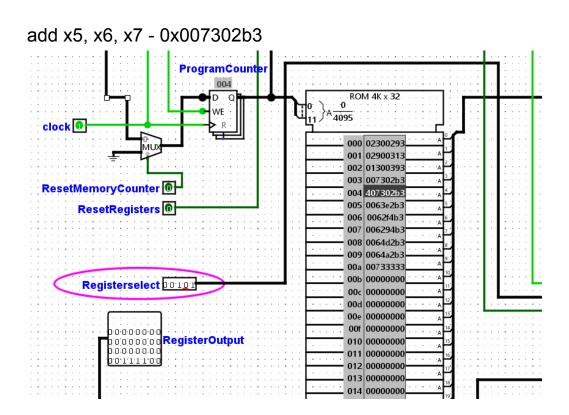
### 1. R TYPE INSTRUCTIONS



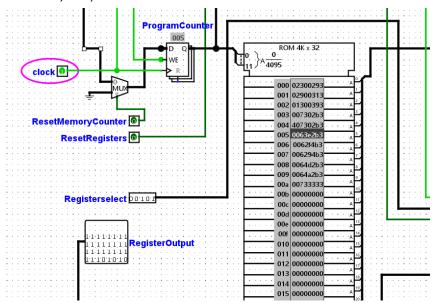


addi x7,x0, 19 - 0X01300393

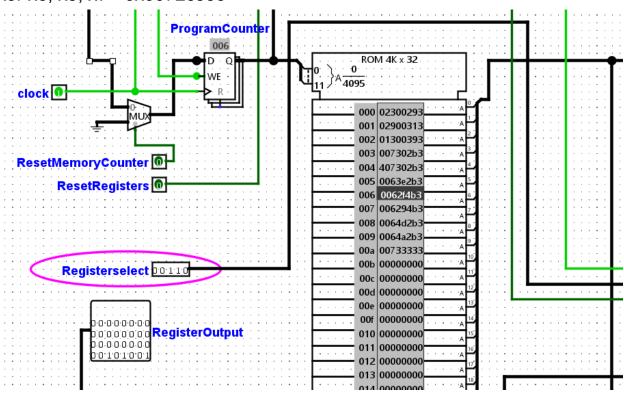


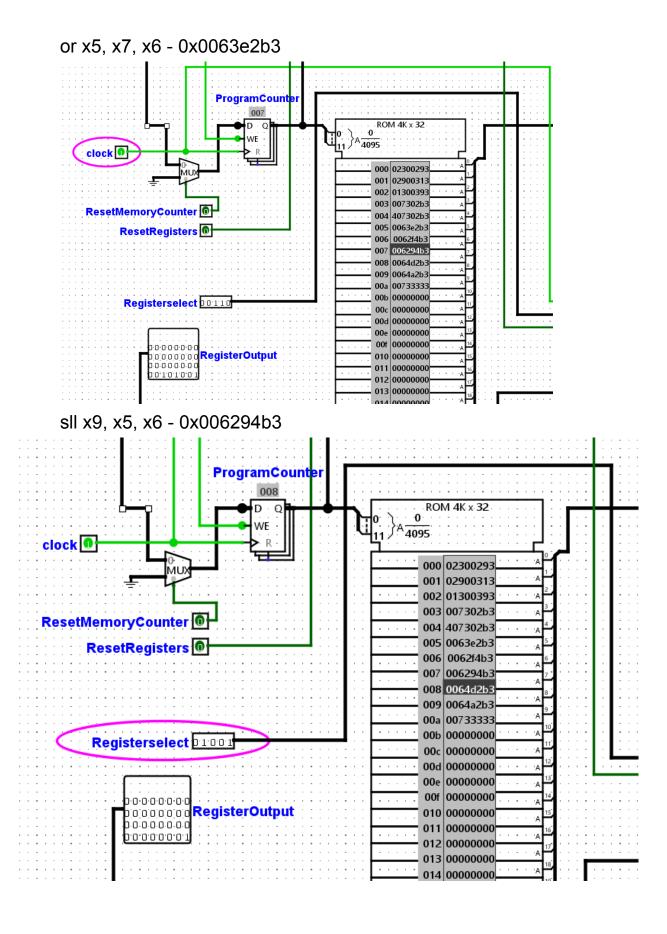


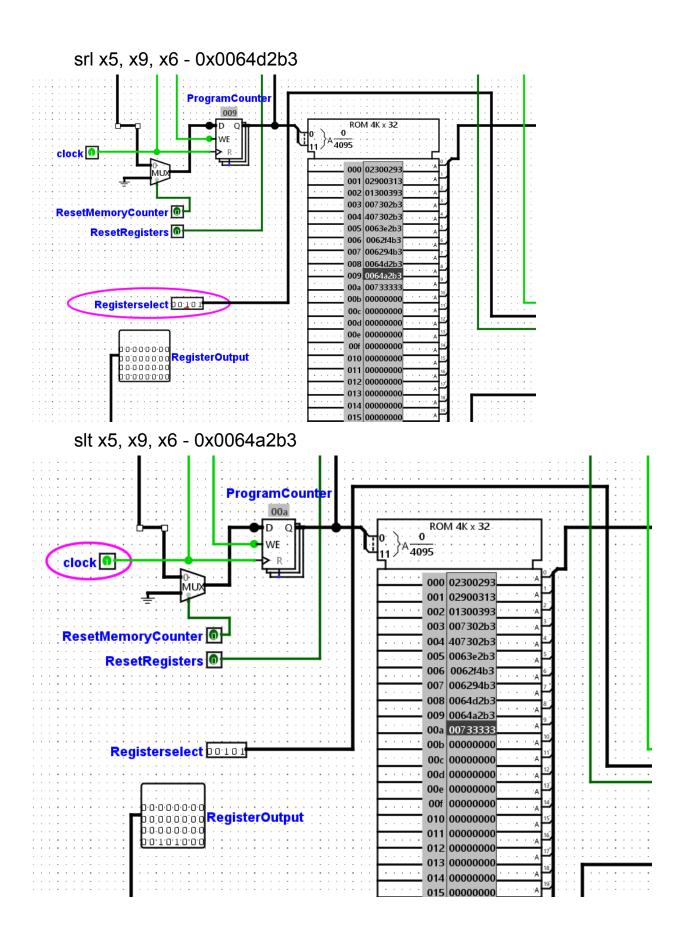
sub x5, x6, x7 - 0x407302b3

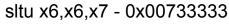


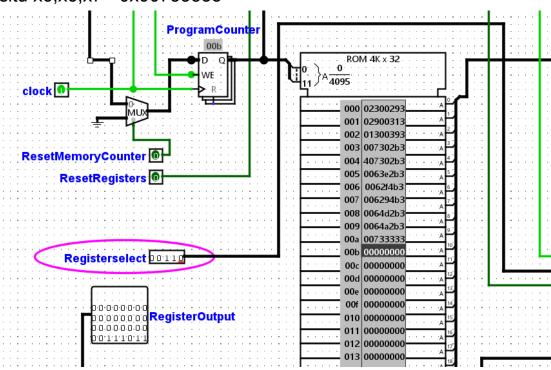
## xor x6, x5, x7 - 0x0072c333



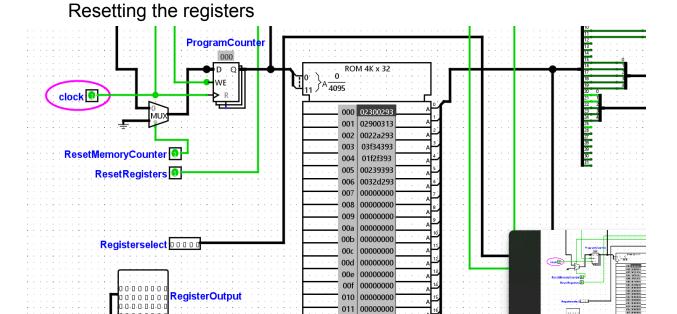




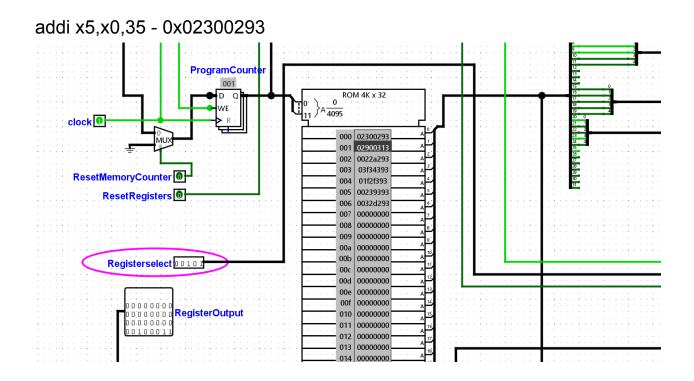


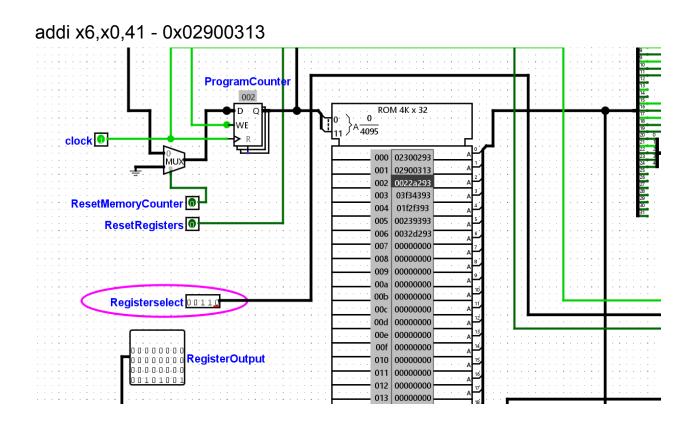


### 2. I TYPE INSTRUCTIONS

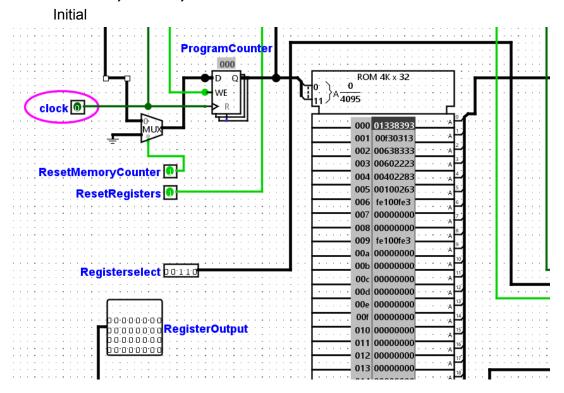


012 00000000

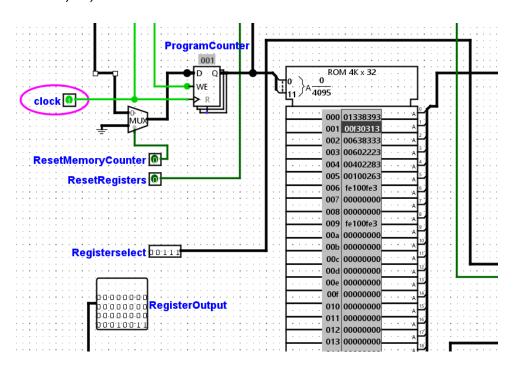




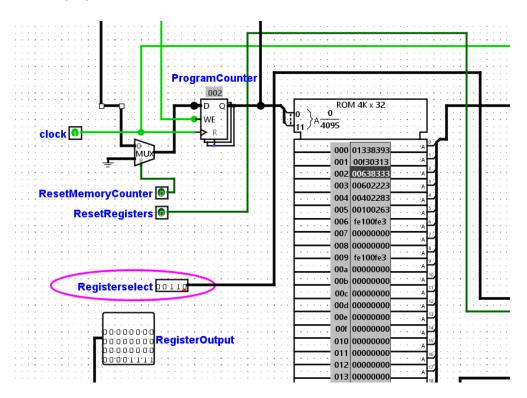
## 3. STORE, LOAD, BRANCH



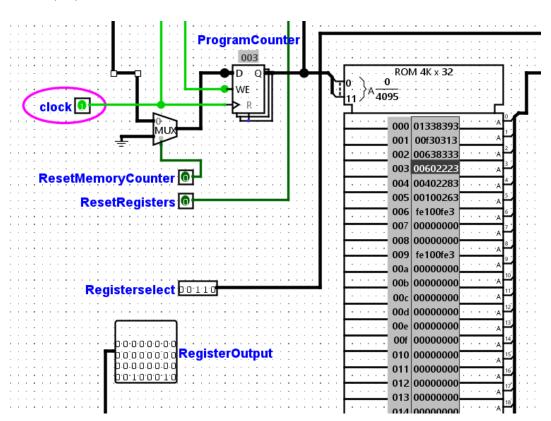
#### **ADDI x7, x7, 1**



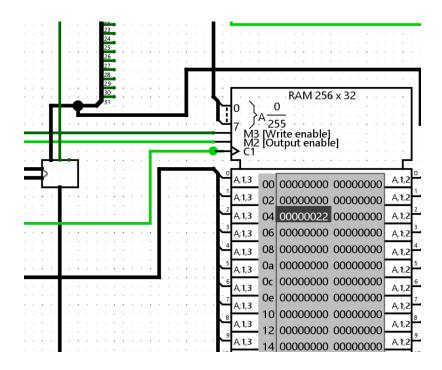
#### **ADDI x6,x6,15**



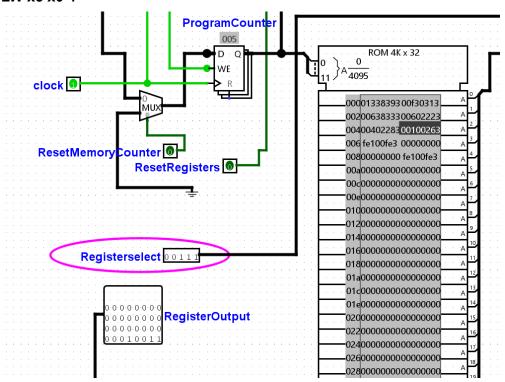
ADD x6,x7,x6

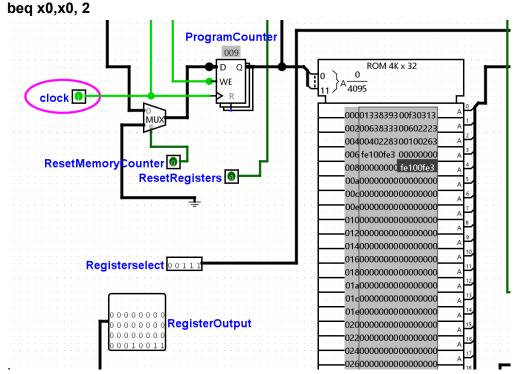


sw x0 4 x6









eq x0,x0,-2 **ProgramCounter** 007 ROM 4K x 32 0 A 4095 clock 1 .0000133839300f30313 .0020063833300602223 0040040228300100263 006 fe100fe3 00000000 ResetMemory Counter 10 008000000000 fe100fe3 ResetRegisters 0 00e00000000000000000 -0100000000000000000 -01200000000000000000 .0140000000000000000 0160000000000000000 Registerselect 0.0 1.1 1 0180000000000000000 01a00000000000000000 01e00000000000000000 0.0.0.0.0.0.0 o o o o o o o <mark>RegisterOutput</mark> 02000000000000000000 0.0.0.0.0.0.0.0.0 02200000000000000000 0.0.0.1.0.0.1.1 02400000000000000000 -02600000000000000000 .0280000000000000000