PROCESSOR

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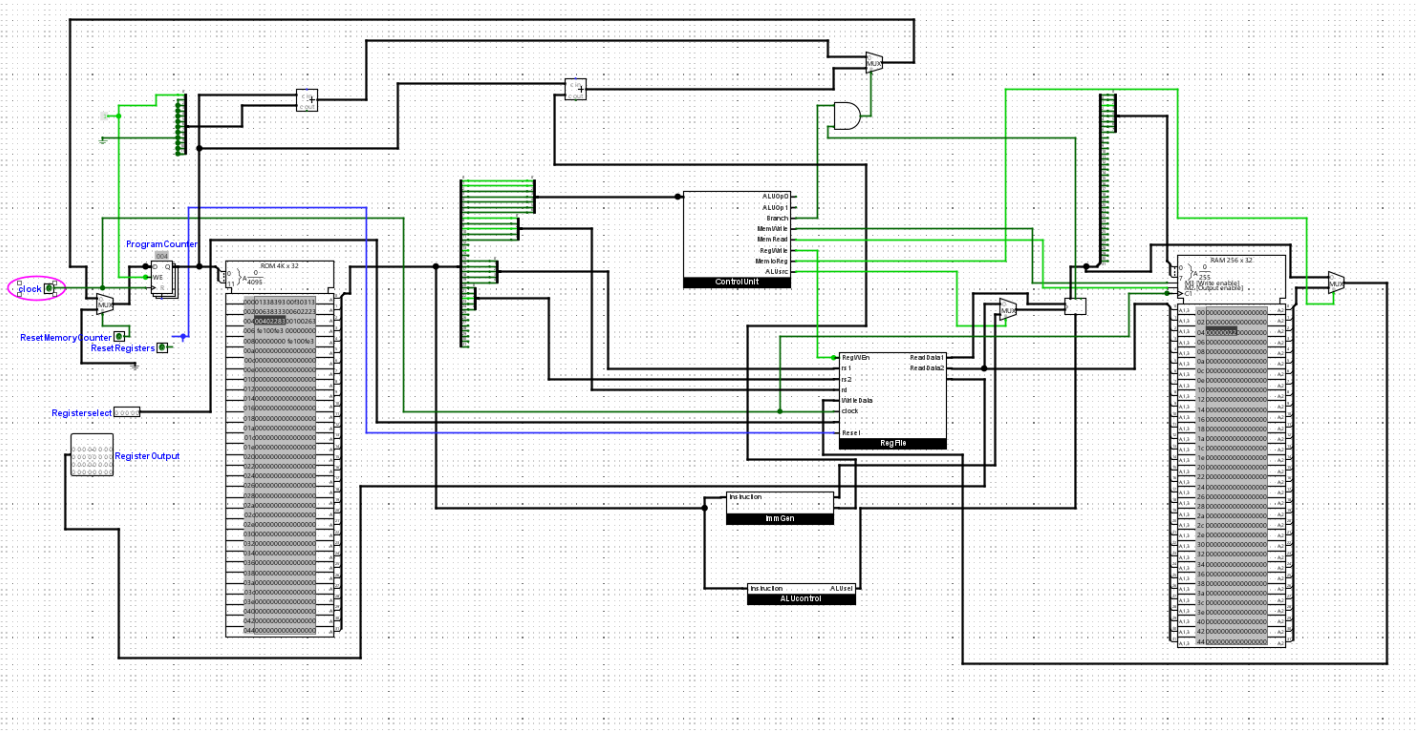
Lucky Ahirwar 2022CS52049

Design Decisions:

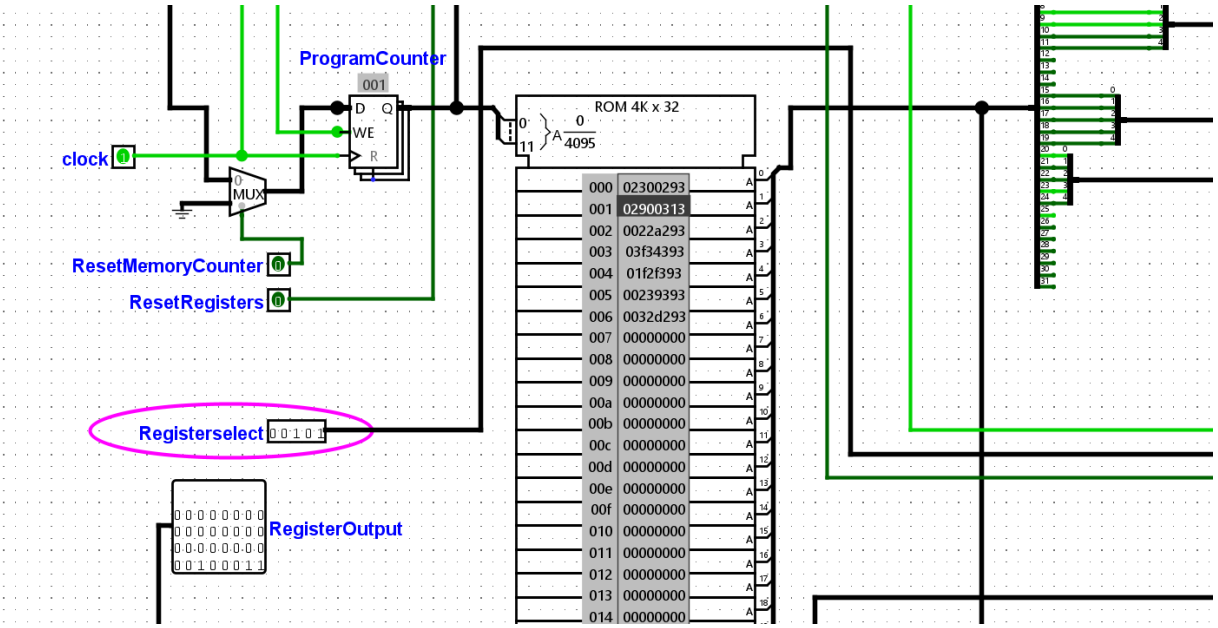
1. We used instruction memory address width as 12 bit since keeping it as 24 bits was taking 160mb of memory and we could not submit that on moodle.
2. We are storing instruction memory at increments of 1.
3. We made separate inputs for resetting the register file and resetting the program counter.

TESTING:

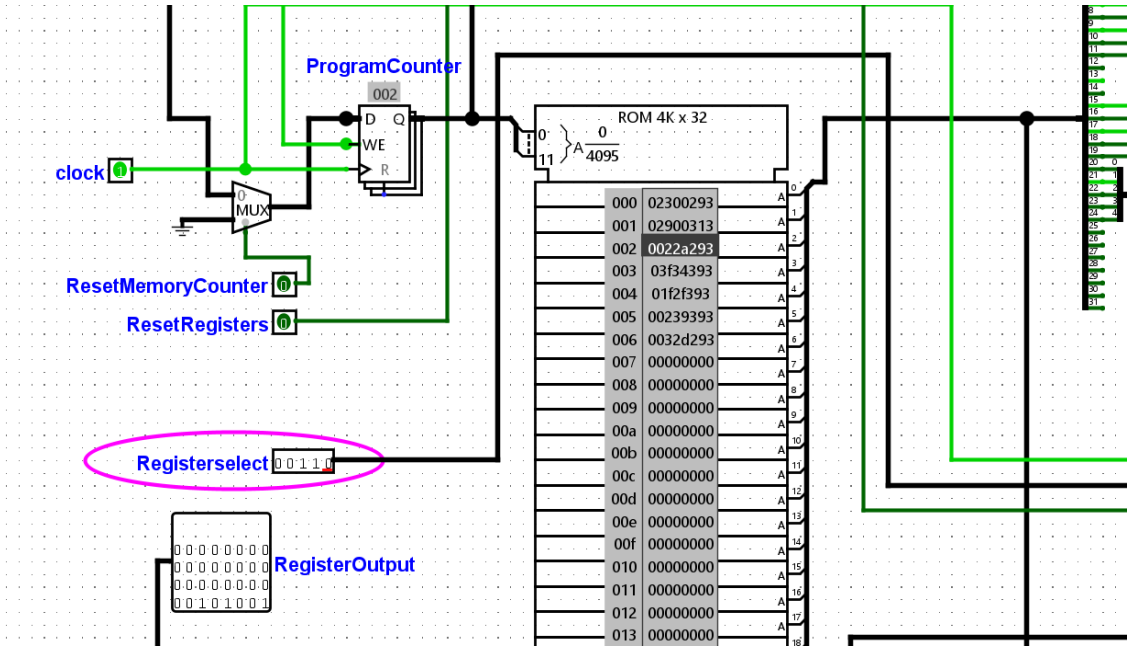


1. R TYPE INSTRUCTIONS

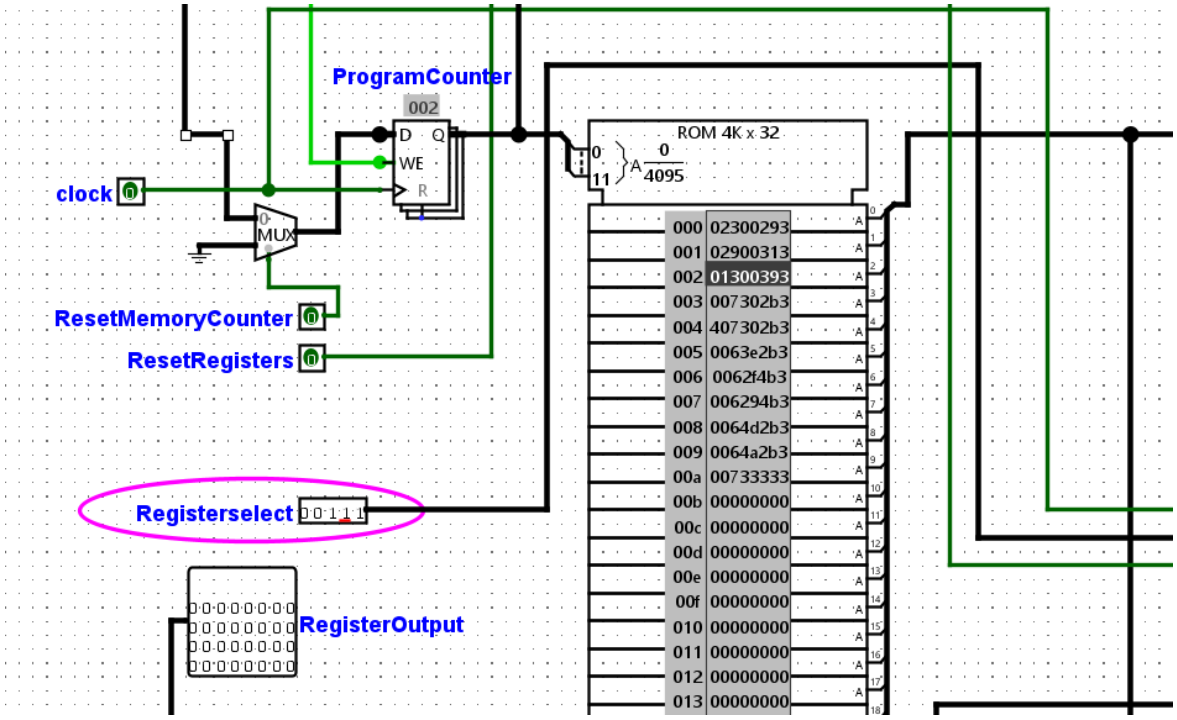
addi x5,x0,35 - 0x02300293



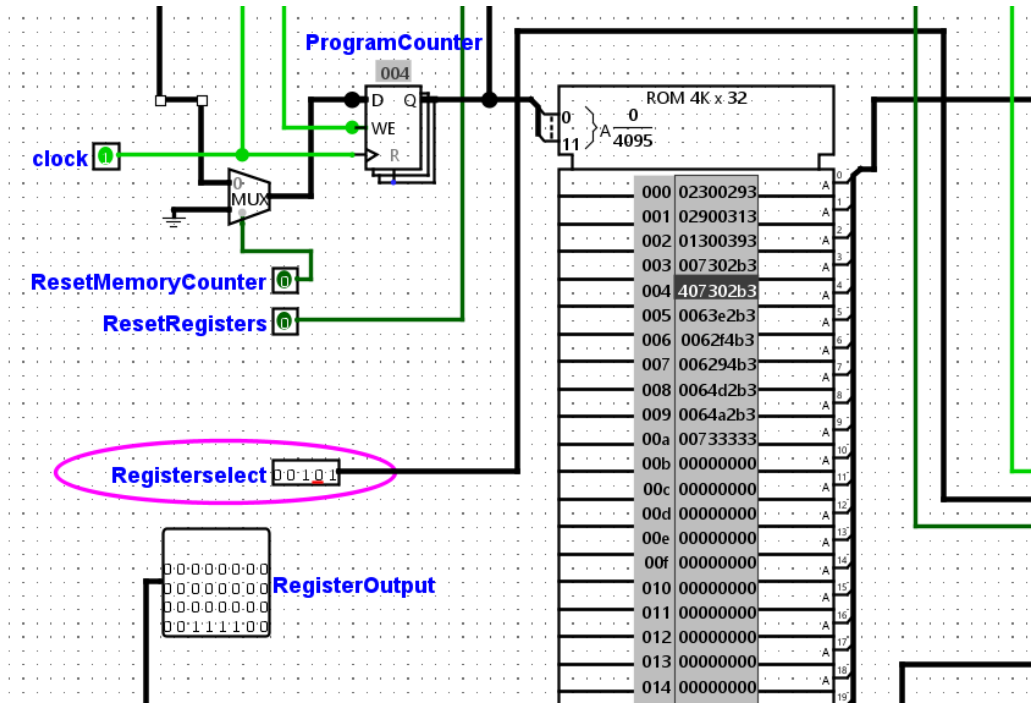
addi x6,x0,41 - 0x02900313



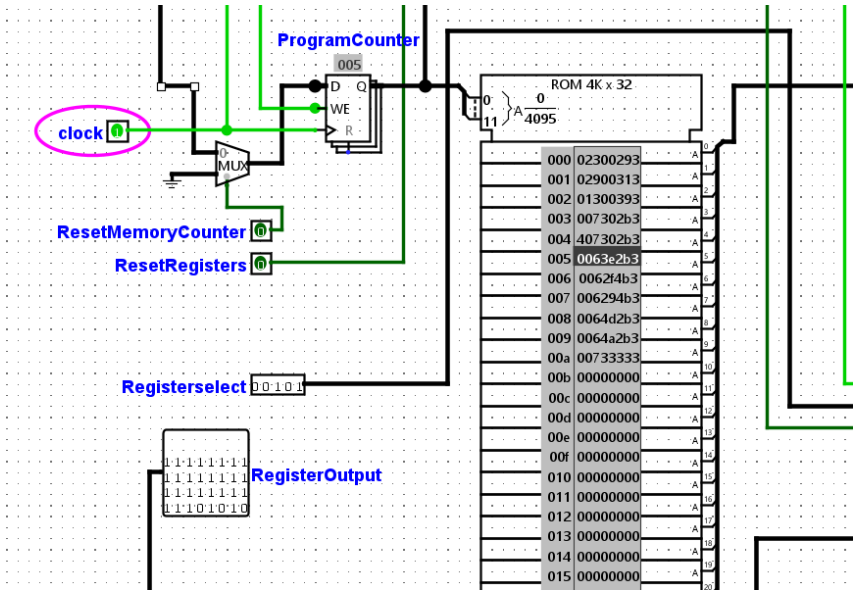
addi x7,x0, 19 - 0X01300393



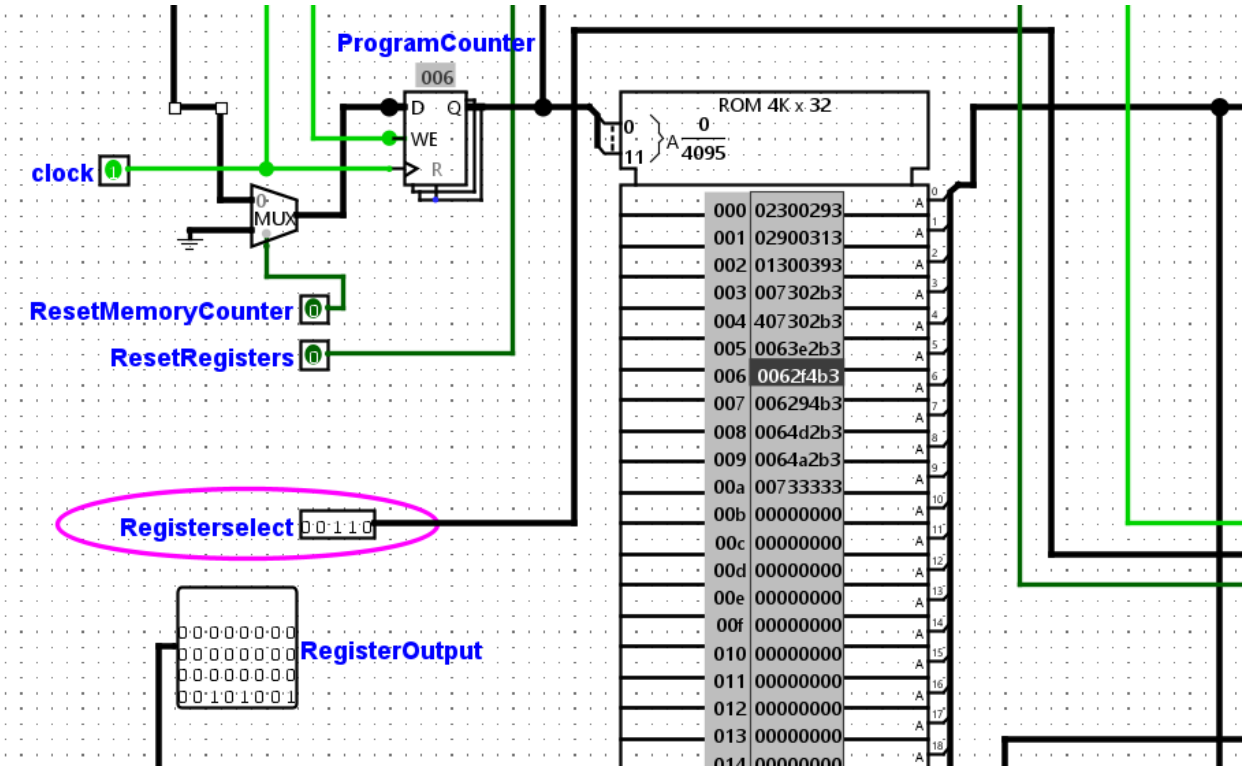
add x5, x6, x7 - 0x007302b3



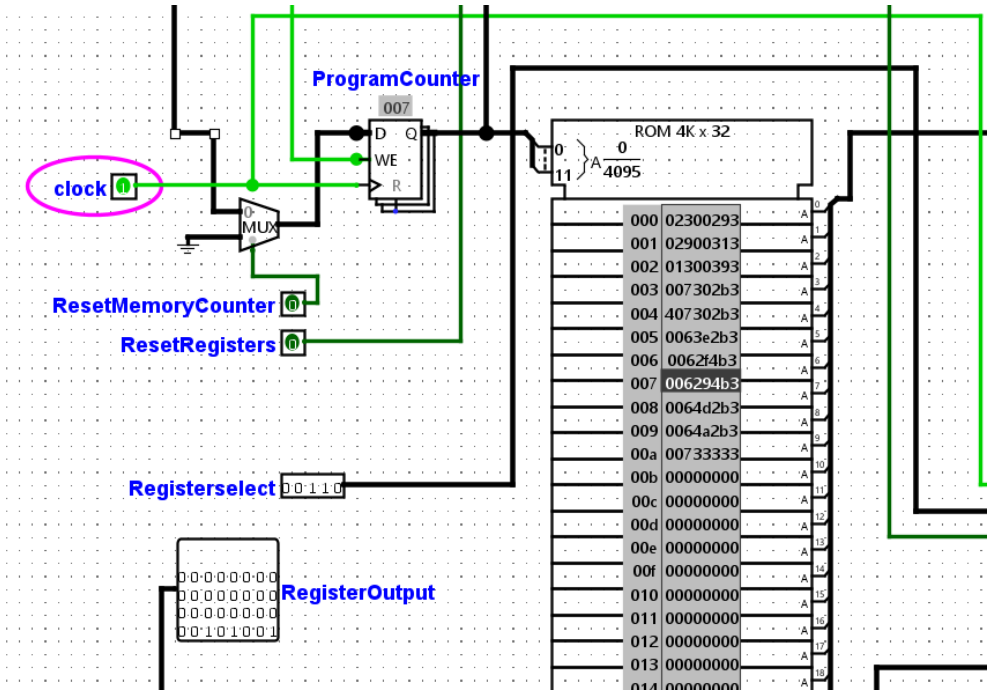
sub x5, x6, x7 - 0x407302b3



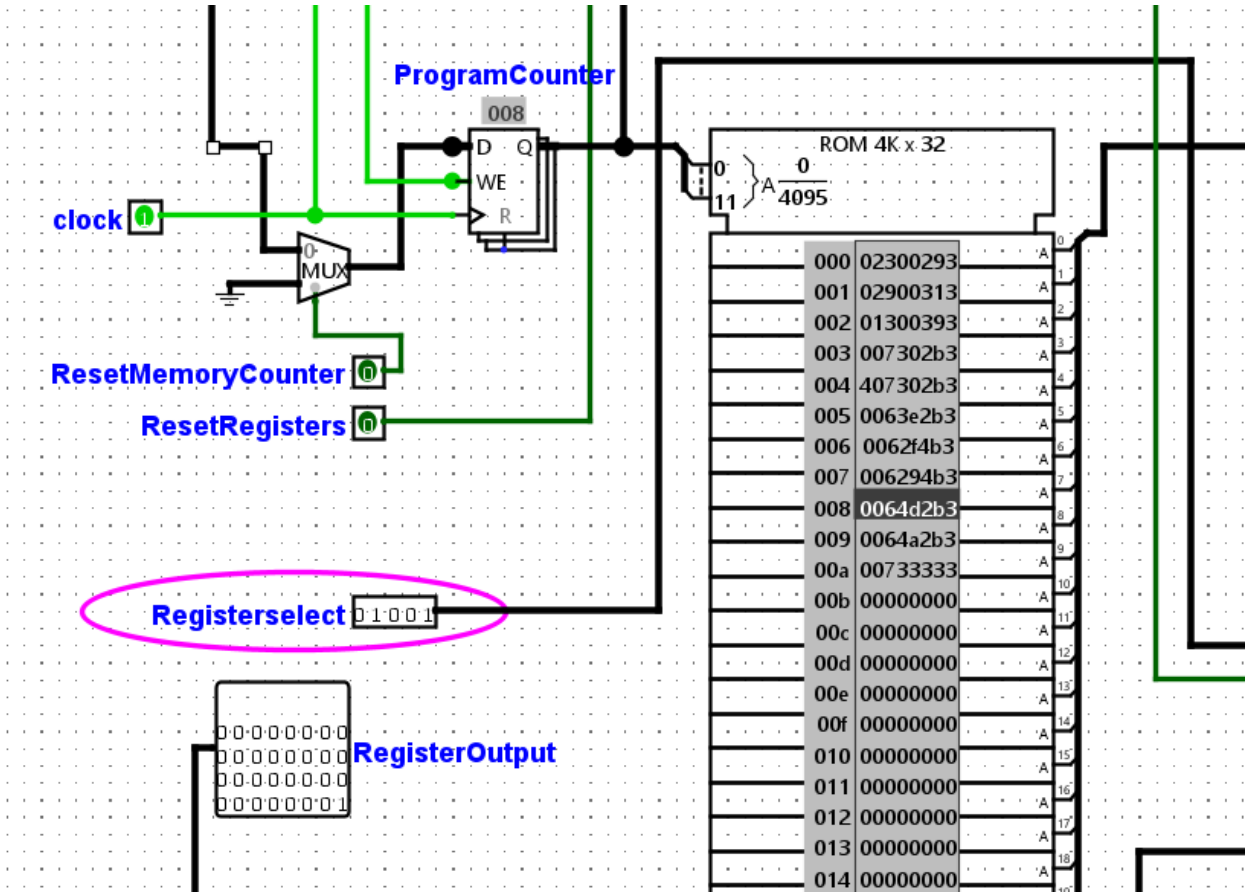
xor x6, x5, x7 - 0x0072c333



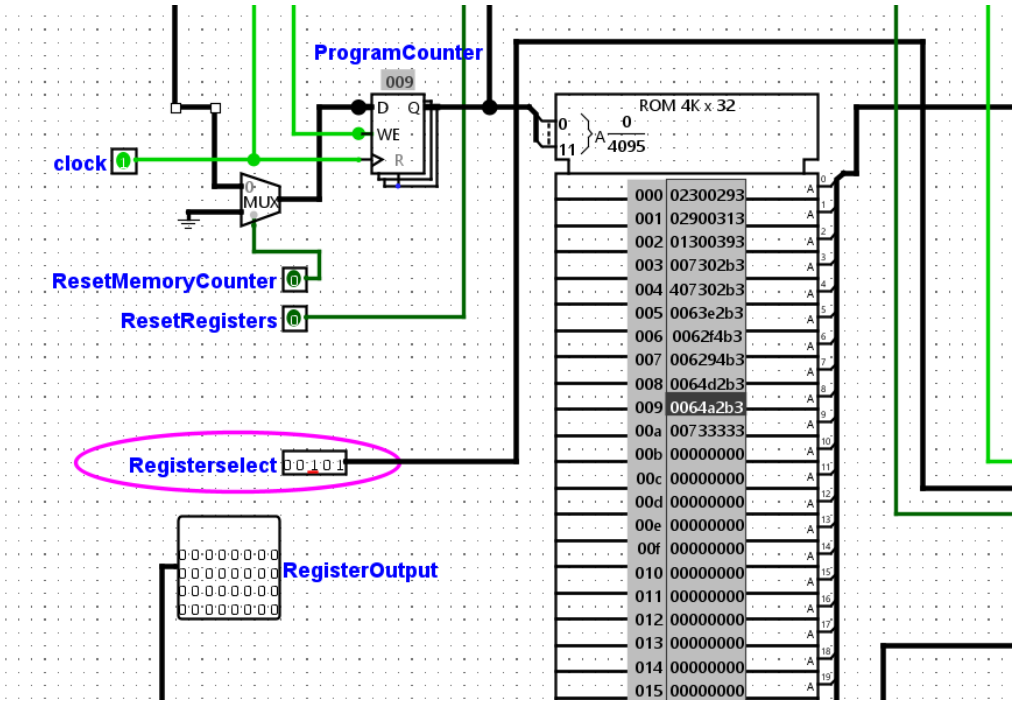
or x5, x7, x6 - 0x0063e2b3



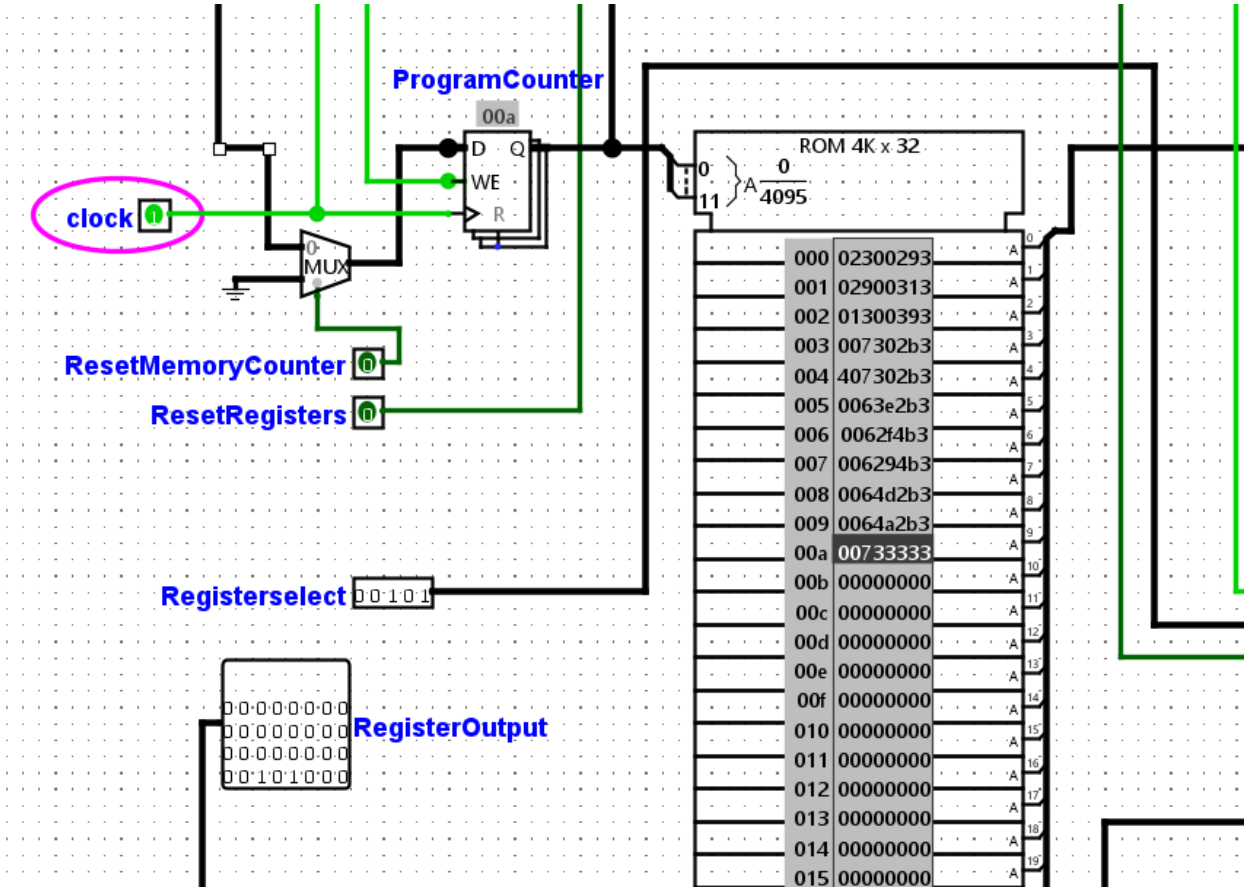
sll x9, x5, x6 - 0x006294b3



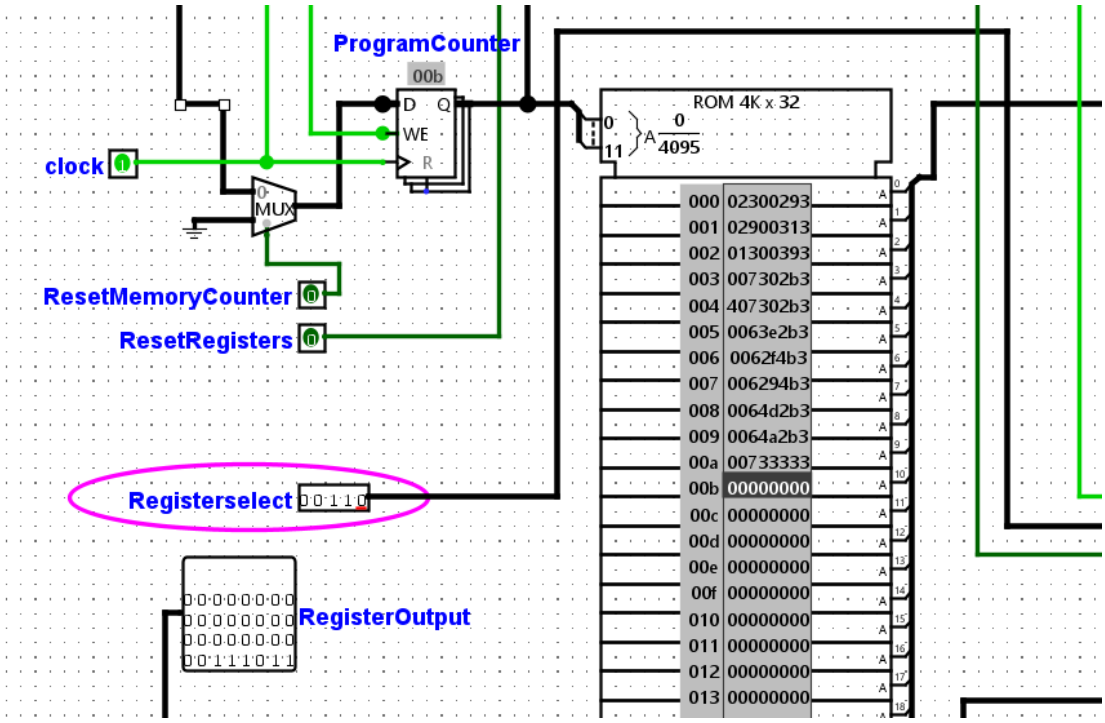
srl x5, x9, x6 - 0x0064d2b3



slt x5, x9, x6 - 0x0064a2b3

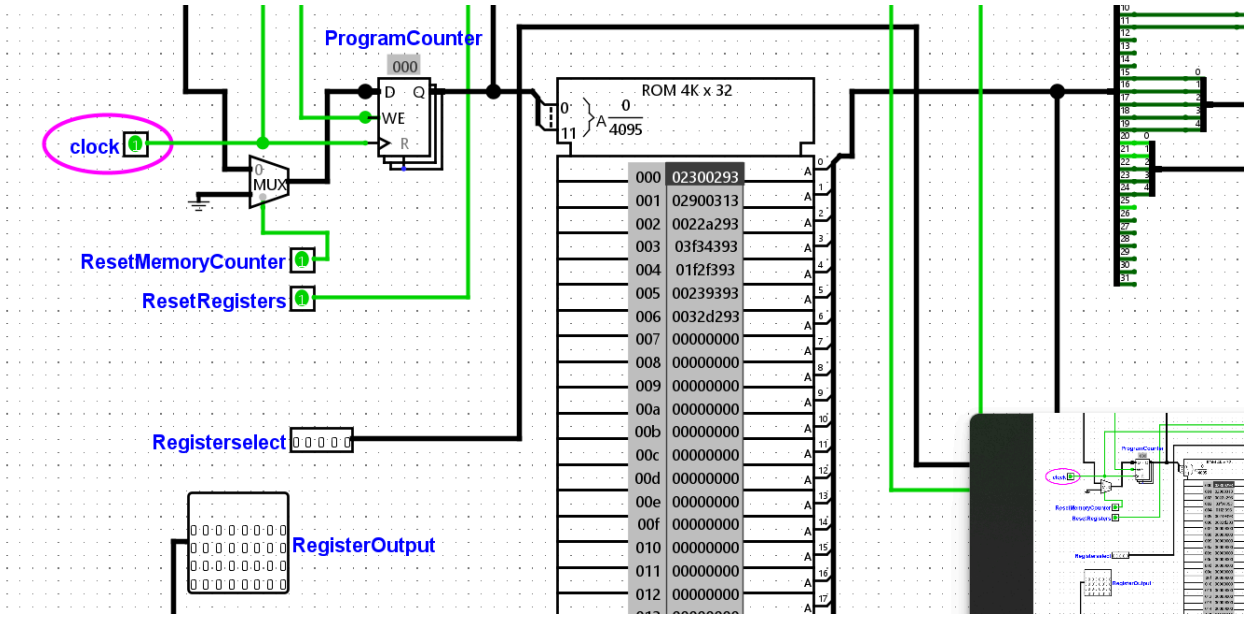


sltu x6,x6,x7 - 0x00733333

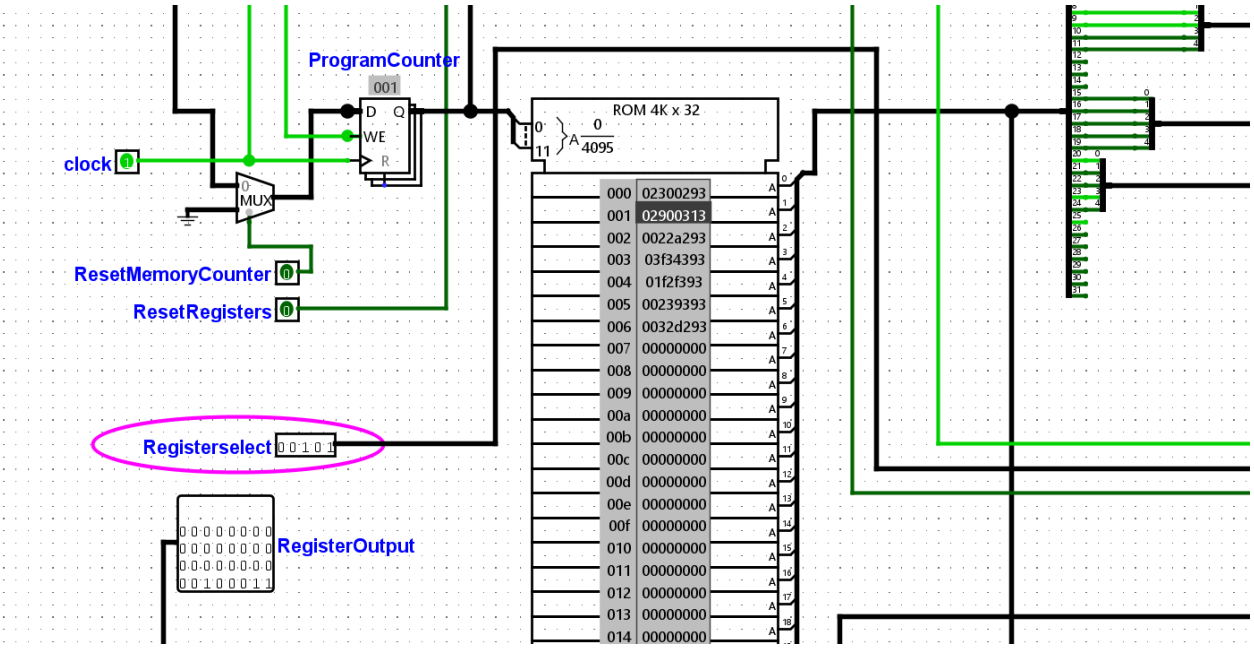


2. I TYPE INSTRUCTIONS

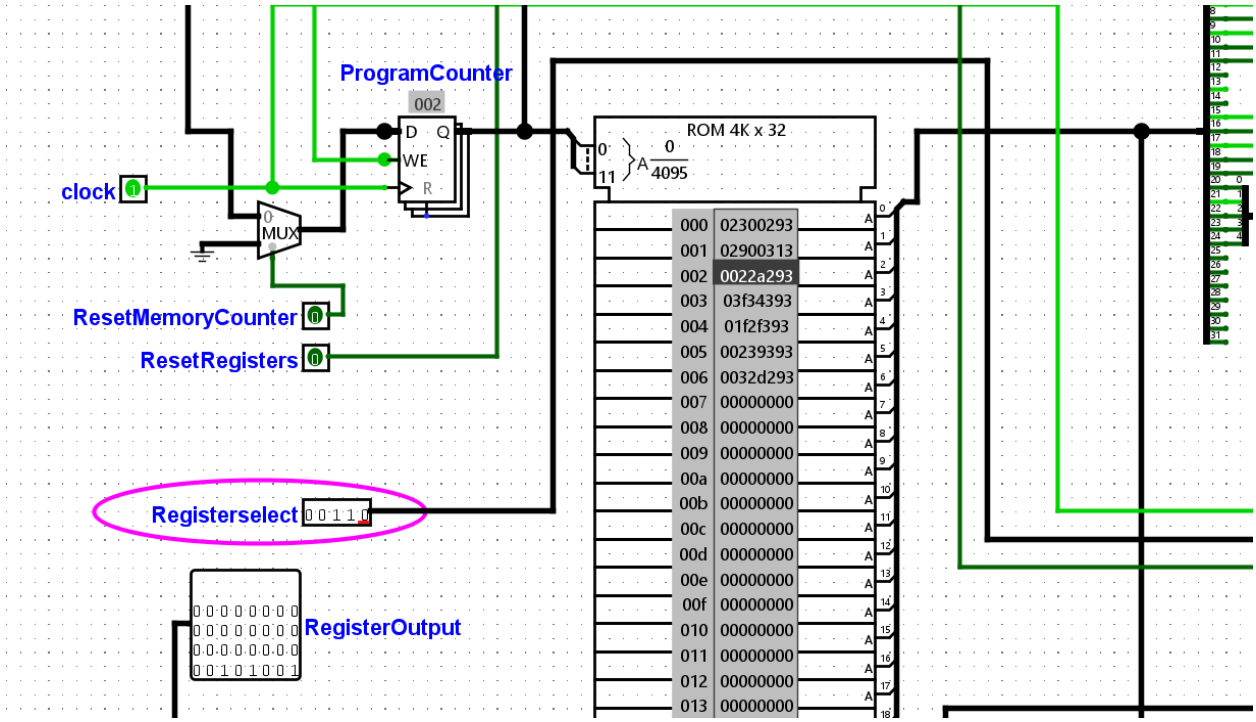
Resetting the registers



addi x5,x0,35 - 0x02300293

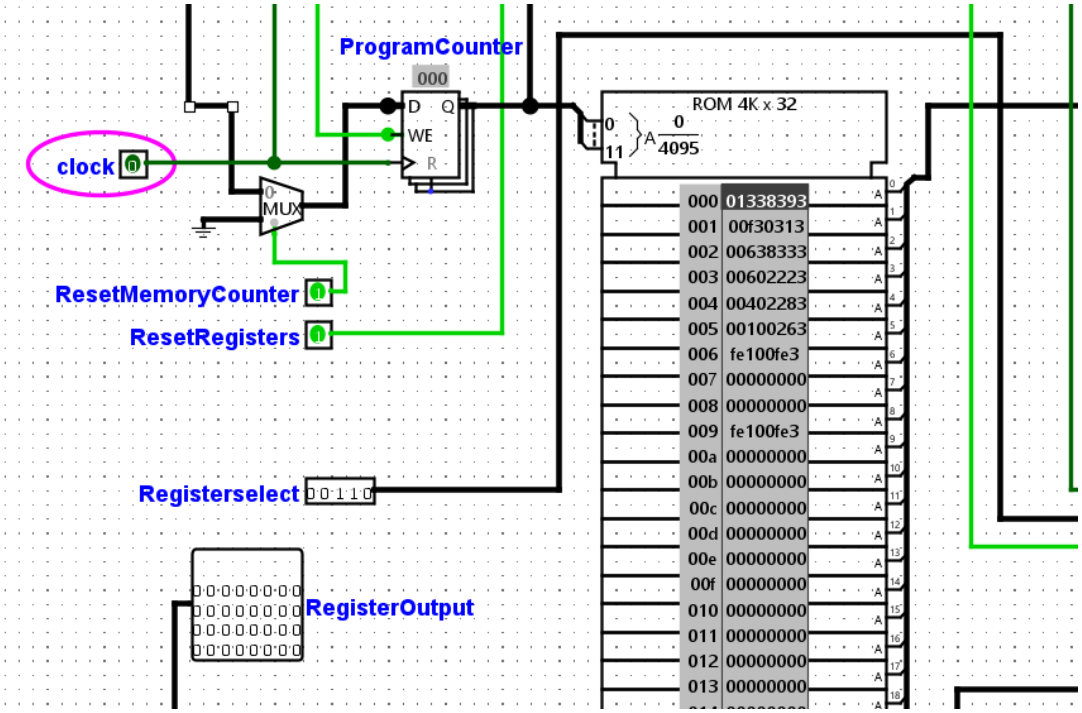


addi x6,x0,41 - 0x02900313

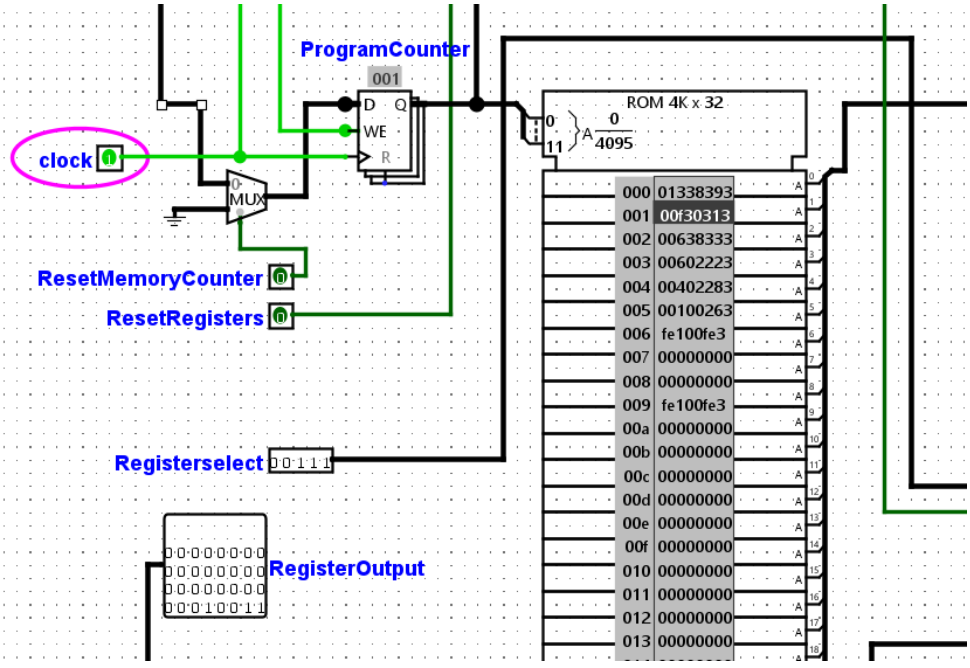


3. STORE, LOAD, BRANCH

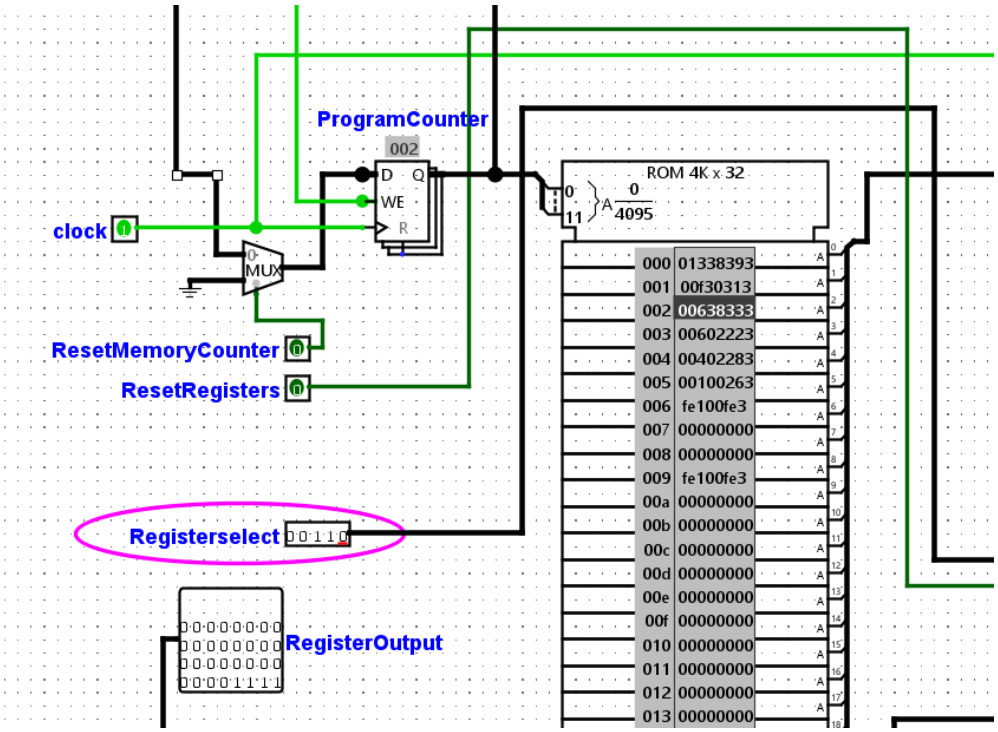
Initial



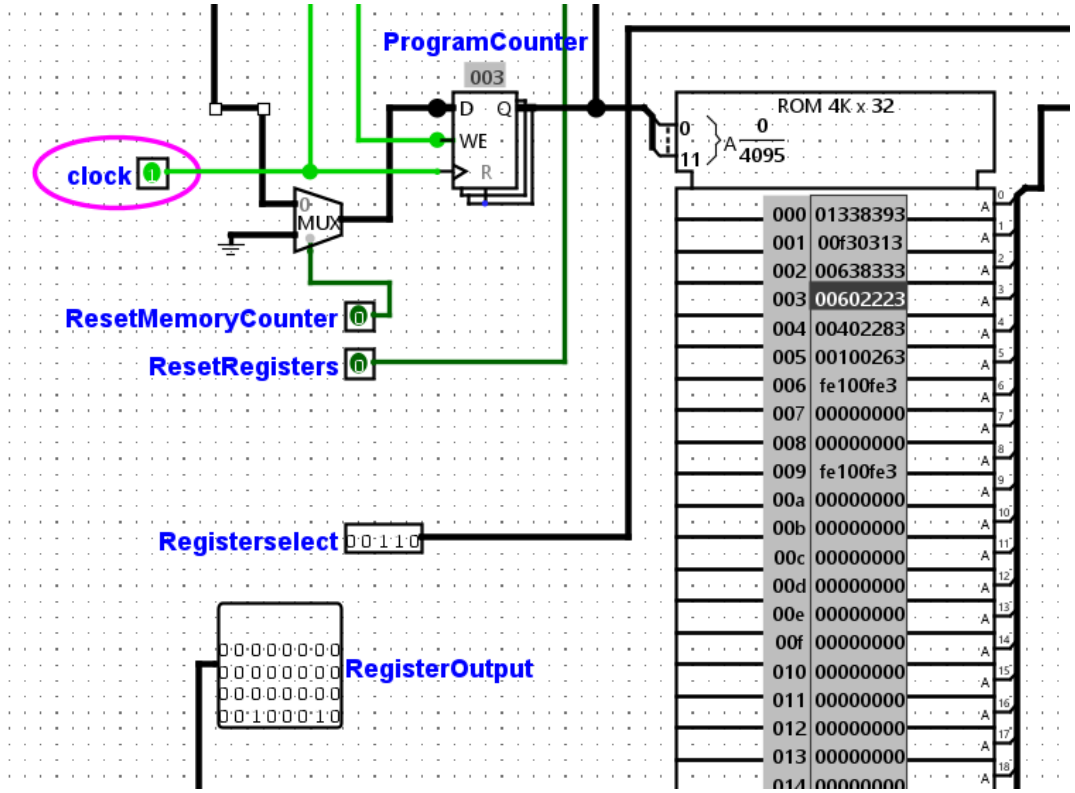
ADDI x7, x7, 1



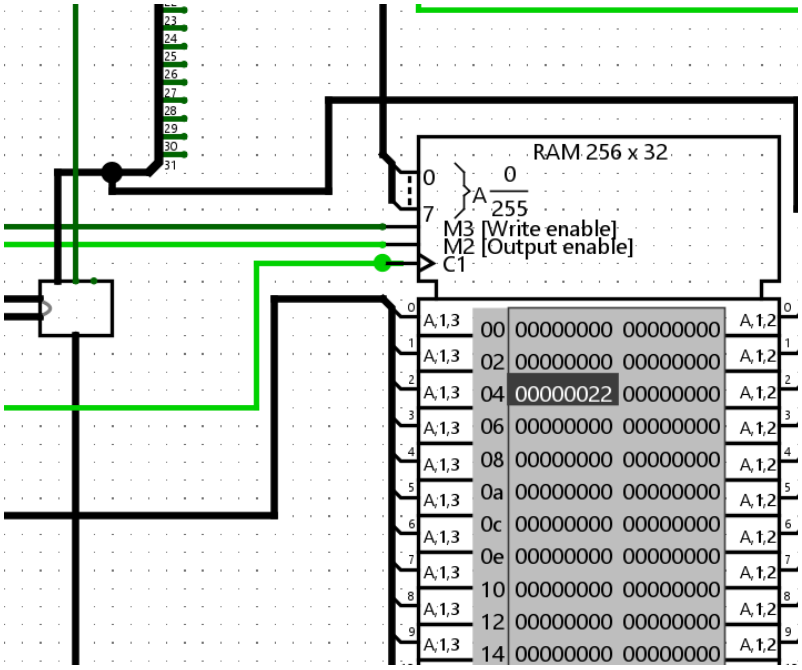
ADDI x6,x6,15



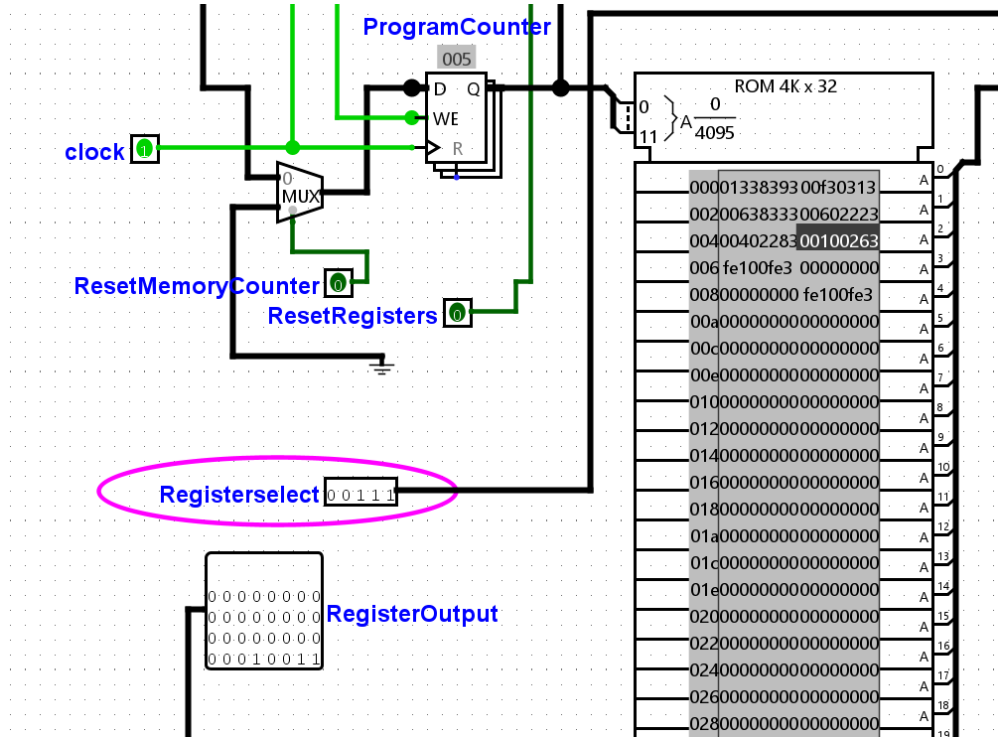
ADD x6,x7,x6



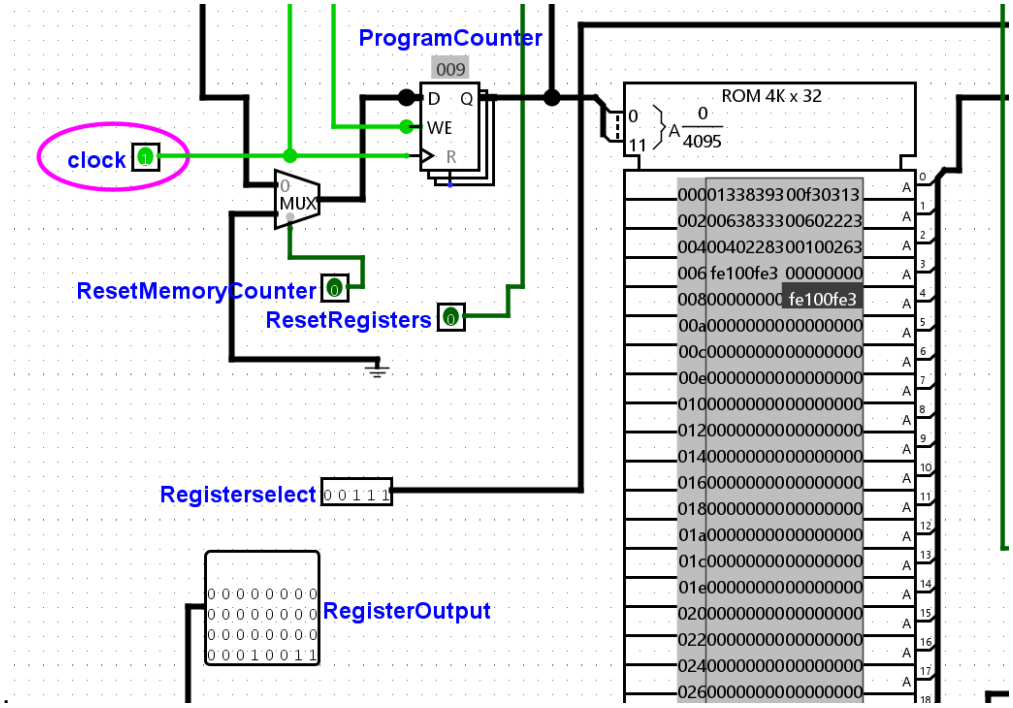
sw x0 4 x6



LW x5 x0 4



beq x0,x0, 2



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eq x0,x0,-2