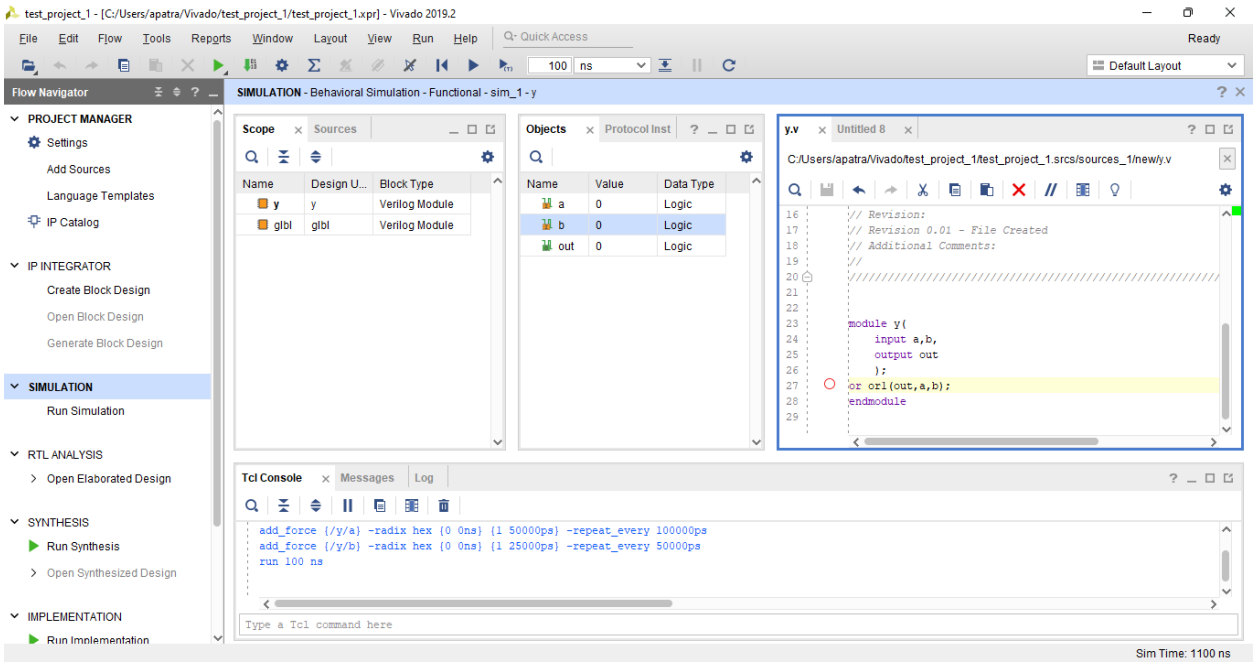
1. OR Gate


test_project_1 - [C:/Users/apatra/Vivado/test_project_1/test_project_1.xpr] - Vivado 2019.2
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RTL ANALYSIS
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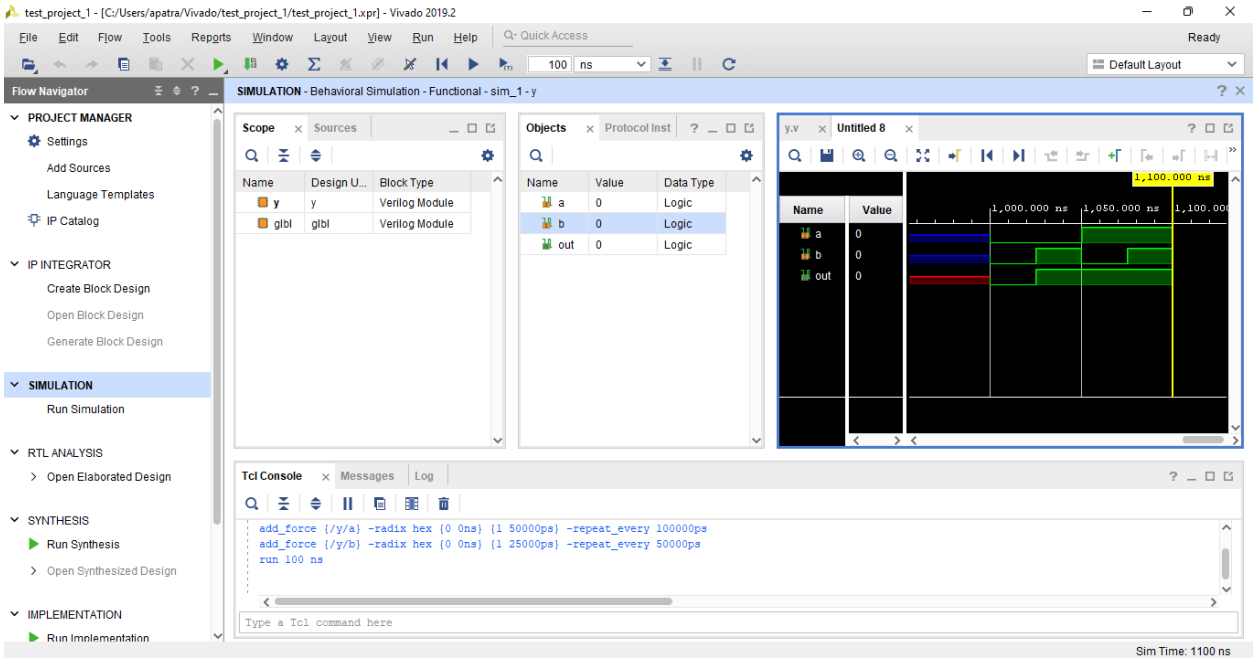
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Scope
Sources
Name Design U... Block Type
y y Verilog Module
glbl glbl Verilog Module
Objects
Protocol Inst
Name Value Data Type
a 0 Logic
b 0 Logic
out 0 Logic
y.v
Untitled 8
C:/Users/apatra/Vivado/test_project_1/test_project_1.srcs/sources_1/new/y.v
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
module y(
input a,b,
output out
);
or or1(out,a,b);
endmodule
Tcl Console
Messages
Log
add_force {/y/a} -radix hex {0 0ns} {1 50000ps} -repeat_every 100000ps
add_force {/y/b} -radix hex {0 0ns} {1 25000ps} -repeat_every 50000ps
run 100 ns
Type a Tcl command here
Sim Time: 1100 ns


test_project_1 - [C:/Users/apatra/Vivado/test_project_1/test_project_1.xpr] - Vivado 2019.2
File Edit Flow Tools Reports Window Layout View Run Help
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Open Block Design
Generate Block Design
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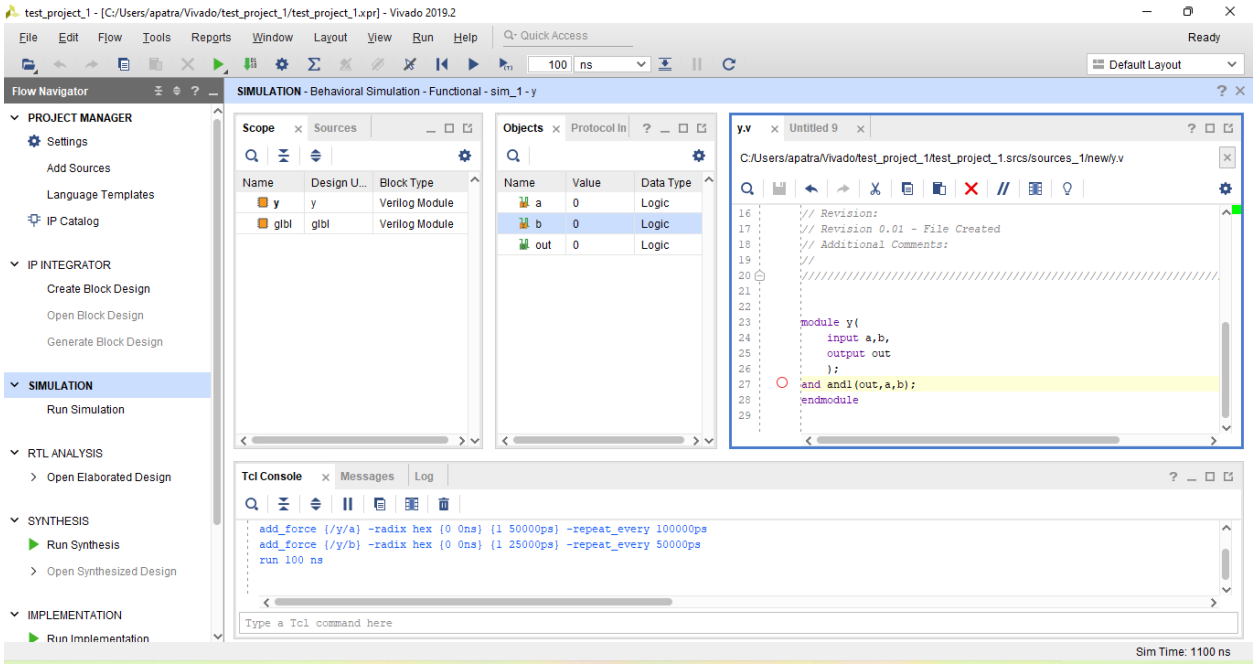
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Scope
Sources
Name Design U... Block Type
y y Verilog Module
glbl glbl Verilog Module
Objects
Protocol Inst
Name Value Data Type
a 0 Logic
b 0 Logic
out 0 Logic
y.v
Untitled 8
Name
Value
a 0
b 0
out 0
1,100.000 ns
1,000.000 ns
1,050.000 ns
Tcl Console
Messages
Log
add_force {/y/a} -radix hex {0 0ns} {1 50000ps} -repeat_every 100000ps
add_force {/y/b} -radix hex {0 0ns} {1 25000ps} -repeat_every 50000ps
run 100 ns
Type a Tcl command here
Sim Time: 1100 ns

2. AND Gate


test_project_1 - [C:/Users/apatra/Vivado/test_project_1/test_project_1.xpr] - Vivado 2019.2
File Edit Flow Tools Reports Window Layout View Run Help
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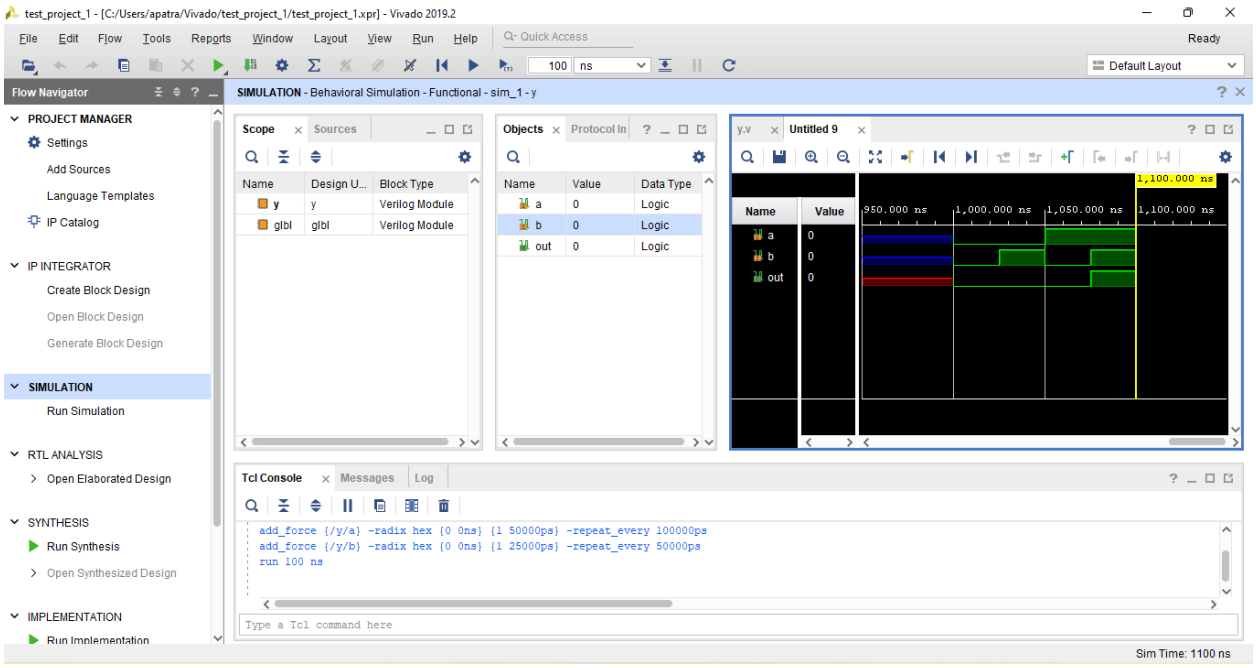
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Scope
Sources
Name Design U... Block Type
y y Verilog Module
glbl glbl Verilog Module
Objects
Protocol In
Name Value Data Type
a 0 Logic
b 0 Logic
out 0 Logic
y.v
Untitled 9
C:/Users/apatra/Vivado/test_project_1/test_project_1.srcs/sources_1/new/y.v
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
module y(
input a,b,
output out
);
and and1(out,a,b);
endmodule
Tcl Console
Messages
Log
add_force {/y/a} -radix hex {0 0ns} {1 50000ps} -repeat_every 100000ps
add_force {/y/b} -radix hex {0 0ns} {1 25000ps} -repeat_every 50000ps
run 100 ns
Type a Tcl command here
Sim Time: 1100 ns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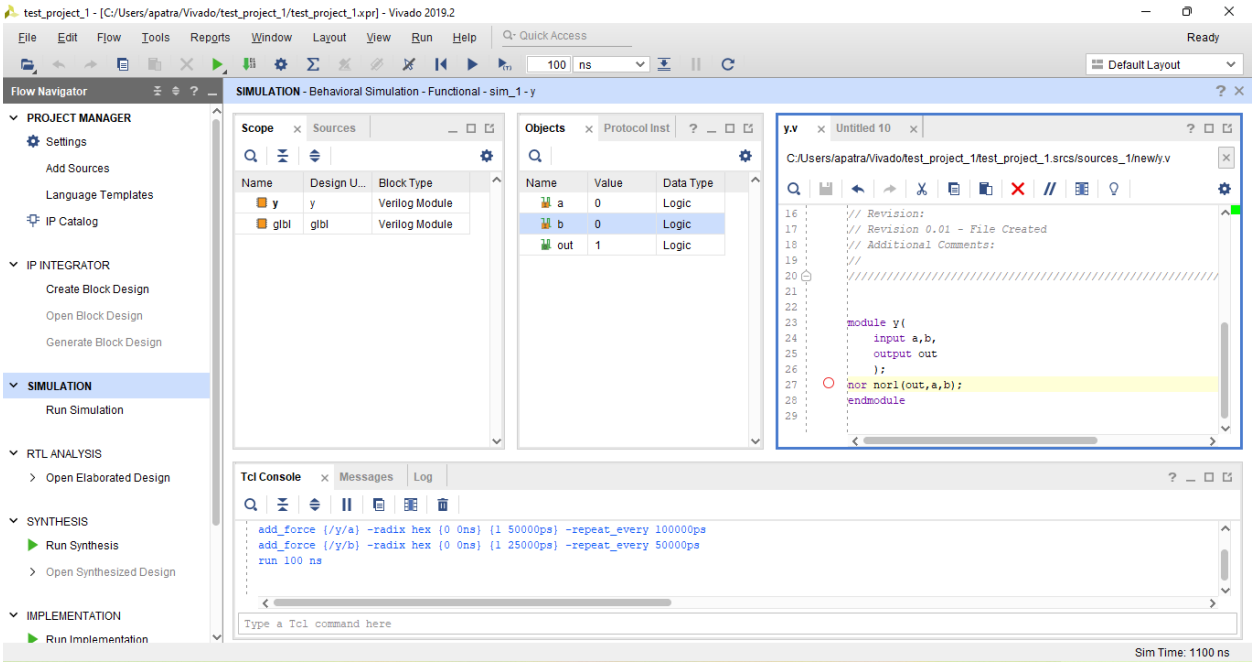
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Scope
Sources
Name Design U... Block Type
y y Verilog Module
glbl glbl Verilog Module
Objects
Protocol In
Name Value Data Type
a 0 Logic
b 0 Logic
out 0 Logic
y.v
Untitled 9
Name
Value
a
b
out
950.000 ns
1,000.000 ns
1,050.000 ns
1,100.000 ns
Tcl Console
Messages
Log
add_force {/y/a} -radix hex {0 0ns} {1 50000ps} -repeat_every 100000ps
add_force {/y/b} -radix hex {0 0ns} {1 25000ps} -repeat_every 50000ps
run 100 ns
Type a Tcl command here
Sim Time: 1100 ns

3. NOR Gate


test_project_1 - [C:/Users/apatra/Vivado/test_project_1/test_project_1.xpr] - Vivado 2019.2
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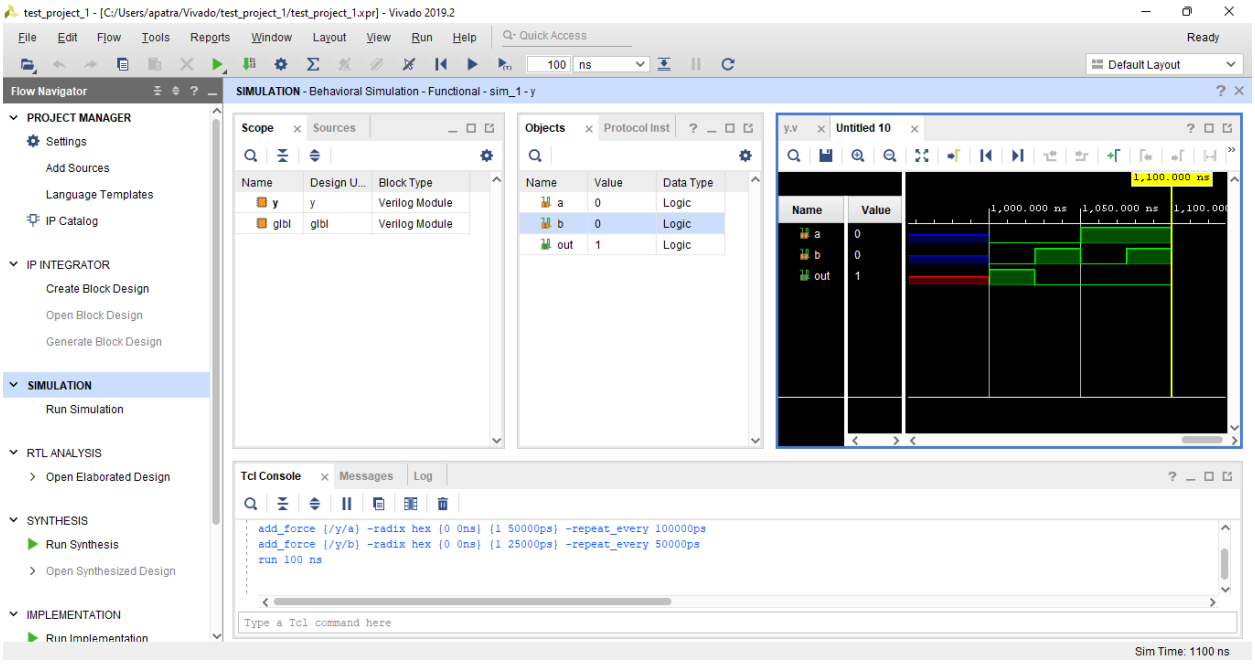
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Scope
Sources
Name Design U... Block Type
y y Verilog Module
glbl glbl Verilog Module
Objects
Protocol Inst
Name Value Data Type
a 0 Logic
b 0 Logic
out 1 Logic
y.v
Untitled 10
C:/Users/apatra/Vivado/test_project_1/test_project_1.srcs/sources_1/new/y.v
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
module y(
input a,b,
output out
);
nor nor1(out,a,b);
endmodule
Tcl Console
Messages
Log
add_force {/y/a} -radix hex {0 0ns} {1 50000ps} -repeat_every 100000ps
add_force {/y/b} -radix hex {0 0ns} {1 25000ps} -repeat_every 50000ps
run 100 ns
Type a Tcl command here
Sim Time: 1100 ns


test_project_1 - [C:/Users/apatra/Vivado/test_project_1/test_project_1.xpr] - Vivado 2019.2
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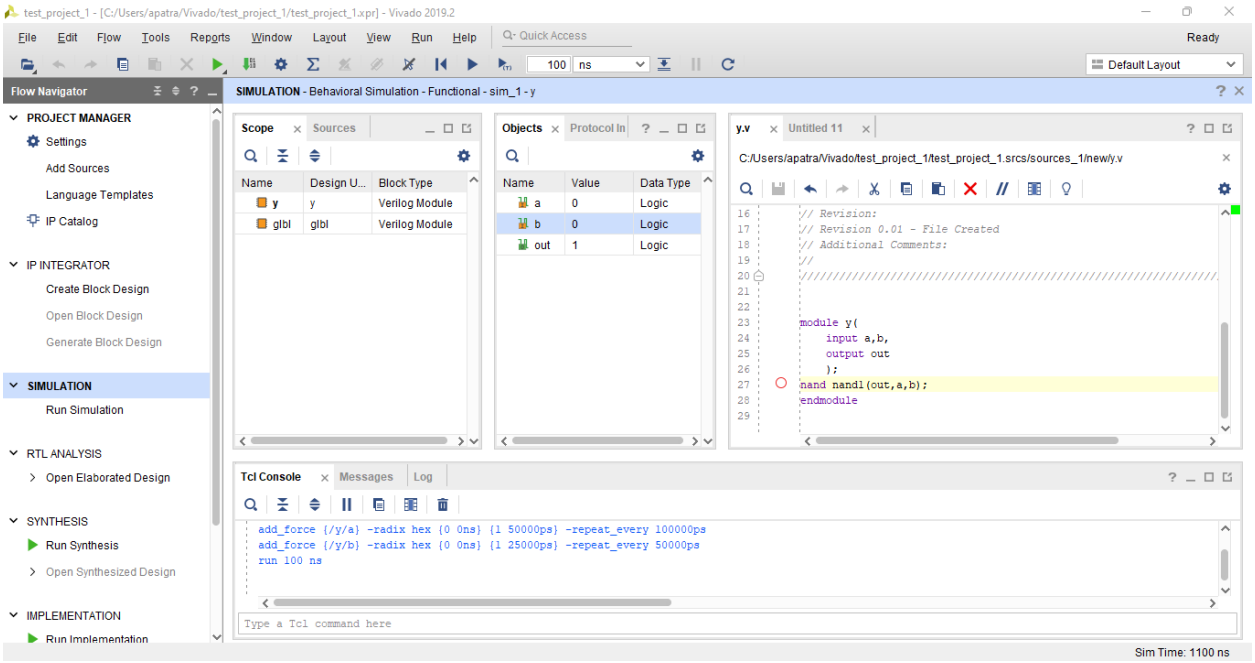
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Scope
Sources
Name Design U... Block Type
y y Verilog Module
glbl glbl Verilog Module
Objects
Protocol Inst
Name Value Data Type
a 0 Logic
b 0 Logic
out 1 Logic
y.v
Untitled 10
Name
Value
a 0
b 0
out 1
1,100.000 ns
1,000.000 ns
1,050.000 ns
Tcl Console
Messages
Log
add_force {/y/a} -radix hex {0 0ns} {1 50000ps} -repeat_every 100000ps
add_force {/y/b} -radix hex {0 0ns} {1 25000ps} -repeat_every 50000ps
run 100 ns
Type a Tcl command here
Sim Time: 1100 ns

4. NAND Gate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Generate Block Design
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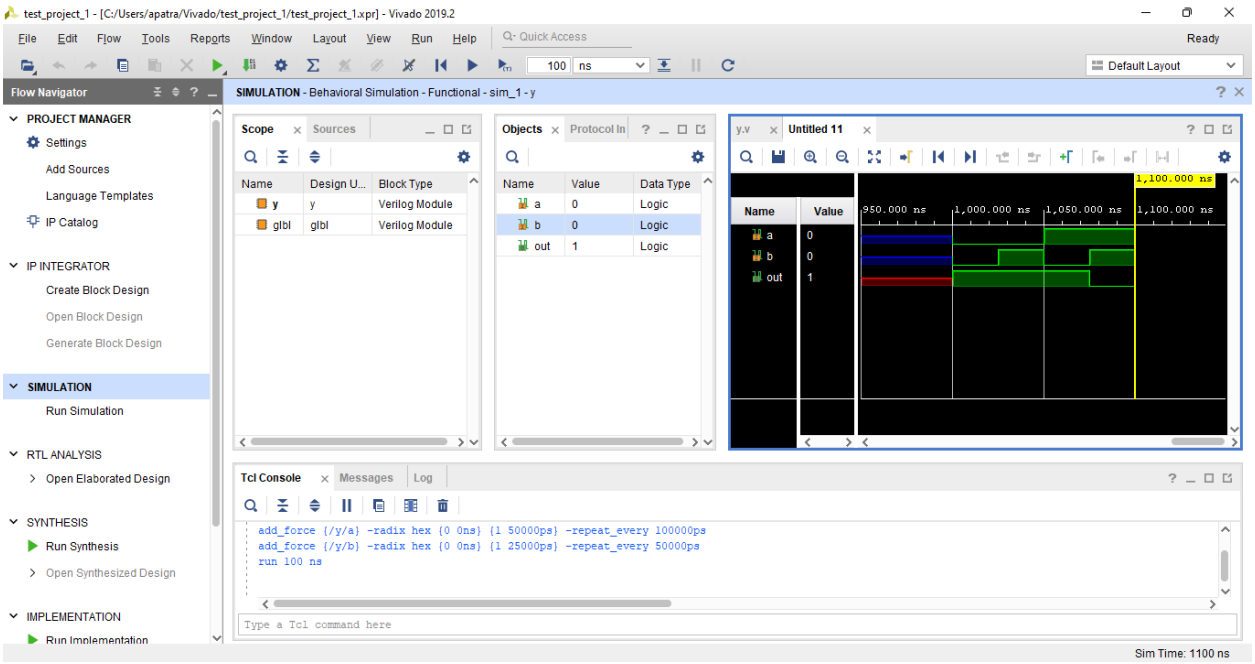
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Scope
Sources
Name Design U... Block Type
y y Verilog Module
glbl glbl Verilog Module
Objects
Protocol In
Name Value Data Type
a 0 Logic
b 0 Logic
out 1 Logic
y.v
Untitled 11
C:/Users/apatra/Vivado/test_project_1/test_project_1.srcs/sources_1/new/y.v
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
module y(
input a,b,
output out
);
nand nand1(out,a,b);
endmodule
Tcl Console
Messages
Log
add_force {/y/a} -radix hex {0 0ns} {1 50000ps} -repeat_every 100000ps
add_force {/y/b} -radix hex {0 0ns} {1 25000ps} -repeat_every 50000ps
run 100 ns
Type a Tcl command here
Sim Time: 1100 ns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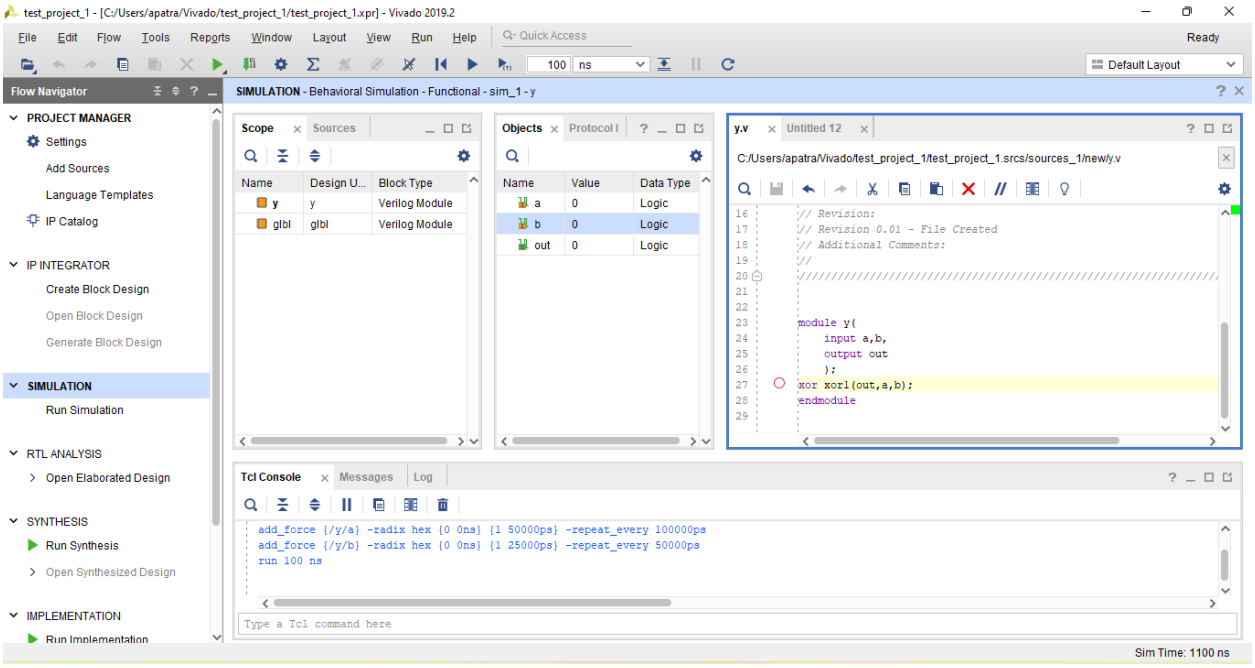
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Scope
Sources
Name Design U... Block Type
y y Verilog Module
glbl glbl Verilog Module
Objects
Protocol In
Name Value Data Type
a 0 Logic
b 0 Logic
out 1 Logic
y.v
Untitled 11
Name
Value
a
b
out
0
0
1
950.000 ns
1,000.000 ns
1,050.000 ns
1,100.000 ns
1,100.000 ns
Tcl Console
Messages
Log
add_force {/y/a} -radix hex {0 0ns} {1 50000ps} -repeat_every 100000ps
add_force {/y/b} -radix hex {0 0ns} {1 25000ps} -repeat_every 50000ps
run 100 ns
Type a Tcl command here
Sim Time: 1100 ns

5. XOR Gate


test_project_1 - [C:/Users/apatra/Vivado/test_project_1/test_project_1.xpr] - Vivado 2019.2
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Generate Block Design
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Run Simulation
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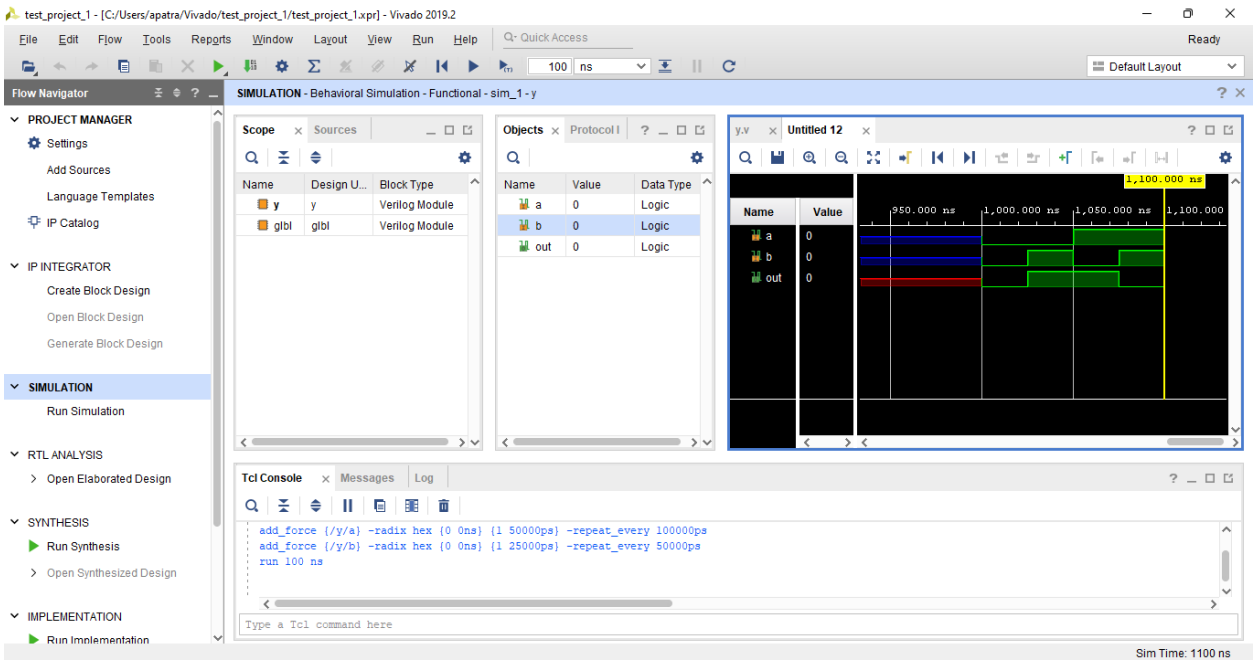
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Scope
Sources
Name
Design U...
Block Type
y
y
Verilog Module
glbl
glbl
Verilog Module
Objects
Protocol I
Name
Value
Data Type
a
0
Logic
b
0
Logic
out
0
Logic
y.v
Untitled 12
C:/Users/apatra/Vivado/test_project_1/test_project_1.srcs/sources_1/new/y.v
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
module y(
input a,b,
output out
);
xor xor1(out,a,b);
endmodule
Tcl Console
Messages
Log
add_force {/y/a} -radix hex {0 0ns} {1 50000ps} -repeat_every 100000ps
add_force {/y/b} -radix hex {0 0ns} {1 25000ps} -repeat_every 50000ps
run 100 ns
Type a Tcl command here
Sim Time: 1100 ns


test_project_1 - [C:/Users/apatra/Vivado/test_project_1/test_project_1.xpr] - Vivado 2019.2
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IP INTEGRATOR
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Generate Block Design
SIMULATION
Run Simulation
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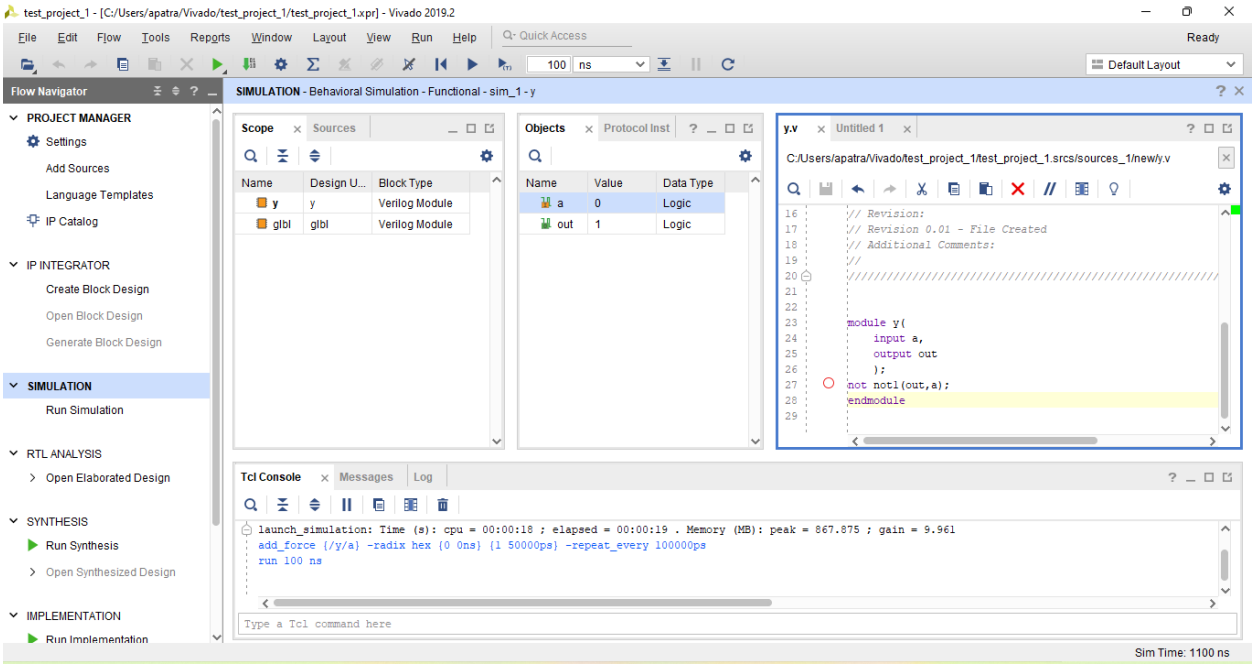
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Scope
Sources
Name
Design U...
Block Type
y
y
Verilog Module
glbl
glbl
Verilog Module
Objects
Protocol I
Name
Value
Data Type
a
0
Logic
b
0
Logic
out
0
Logic
y.v
Untitled 12
1,100.000 ns
950.000 ns
1,000.000 ns
1,050.000 ns
1,100.000
Name
Value
a
0
b
0
out
0
Tcl Console
Messages
Log
add_force {/y/a} -radix hex {0 0ns} {1 50000ps} -repeat_every 100000ps
add_force {/y/b} -radix hex {0 0ns} {1 25000ps} -repeat_every 50000ps
run 100 ns
Type a Tcl command here
Sim Time: 1100 ns

6. NOT Gate


test_project_1 - [C:/Users/apatra/Vivado/test_project_1/test_project_1.xpr] - Vivado 2019.2
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Generate Block Design
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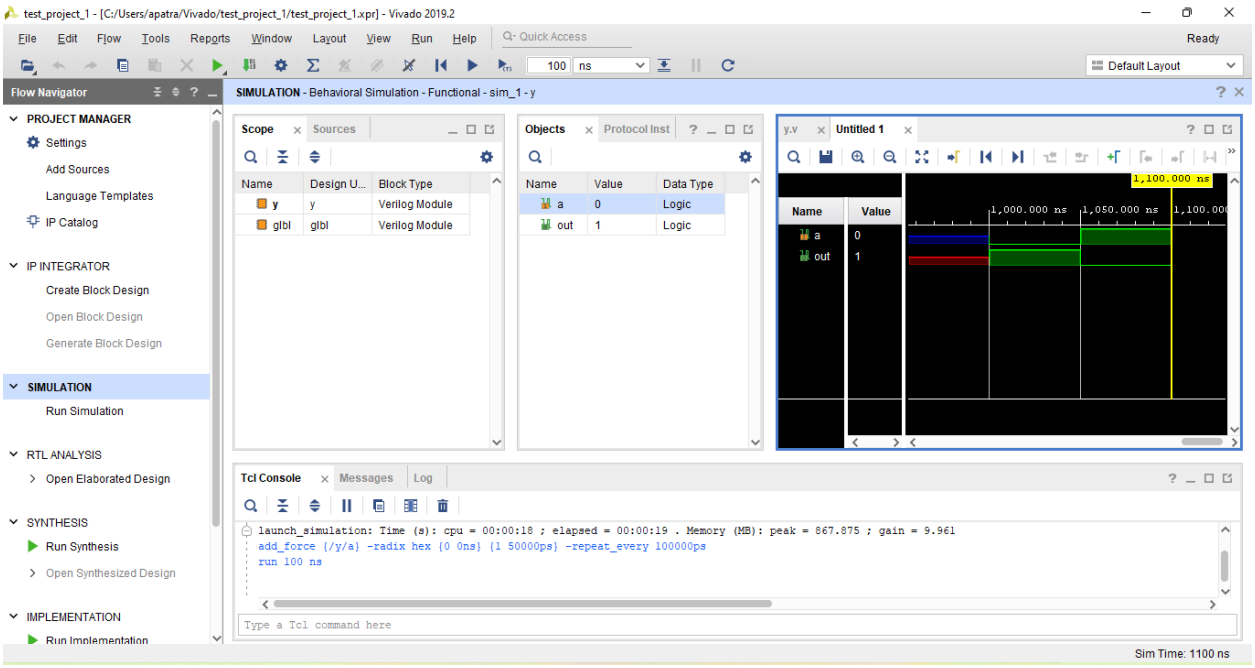
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Scope
Sources
Name Design U... Block Type
y y Verilog Module
glbl glbl Verilog Module
Objects
Protocol Inst
Name Value Data Type
a 0 Logic
out 1 Logic
y.v
Untitled 1
C:/Users/apatra/Vivado/test_project_1/test_project_1.srcs/sources_1/new/y.v
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
module y(
input a,
output out
);
not not1(out,a);
endmodule
Tcl Console
Messages
Log
launch_simulation: Time (s): cpu = 00:00:18 ; elapsed = 00:00:19 . Memory (MB): peak = 867.875 ; gain = 9.961
add_force {/y/a} -radix hex {0 0ns} {1 50000ps} -repeat_every 100000ps
run 100 ns
Type a Tcl command here
Sim Time: 1100 ns


test_project_1 - [C:/Users/apatra/Vivado/test_project_1/test_project_1.xpr] - Vivado 2019.2
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Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
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SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Scope
Sources
Name Design U... Block Type
y y Verilog Module
glbl glbl Verilog Module
Objects
Protocol Inst
Name Value Data Type
a 0 Logic
out 1 Logic
y.v
Untitled 1
Name
Value
a
out
0
1
1,100.000 ns
1,000.000 ns
1,050.000 ns
Tcl Console
Messages
Log
launch_simulation: Time (s): cpu = 00:00:18 ; elapsed = 00:00:19 . Memory (MB): peak = 867.875 ; gain = 9.961
add_force {/y/a} -radix hex {0 0ns} {1 50000ps} -repeat_every 100000ps
run 100 ns
Type a Tcl command here
Sim Time: 1100 ns