

## 1. OR Gate

test\_project\_1 - [C:/Users/apatra/Vivado/test\_project\_1/test\_project\_1.xpr] - Vivado 2019.2

File Edit Flow Tools Reports Window Layout View Run Help Q: Quick Access Ready

100 ns

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SIMULATION - Behavioral Simulation - Functional - sim\_1 - y

Scope x Sources

Name	Design U...	Block Type
y	y	Verilog Module
gbl	gbl	Verilog Module

Objects x Protocol Inst

Name	Value	Data Type
a	0	Logic
b	0	Logic
out	0	Logic

y.v x Untitled 8

```
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 //
22 //
23 module y(
24     input a,b,
25     output out
26 );
27     orl(out,a,b);
28 endmodule
29
```

Tcl Console x Messages Log

```
add_force [/y/a] -radix hex [0 0ns] [1 50000ps] -repeat_every 100000ps
add_force [/y/b] -radix hex [0 0ns] [1 25000ps] -repeat_every 50000ps
run 100 ns
```

Type a Tcl command here

Sim Time: 1100 ns

test\_project\_1 - [C:/Users/apatra/Vivado/test\_project\_1/test\_project\_1.xpr] - Vivado 2019.2

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100 ns

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SIMULATION - Behavioral Simulation - Functional - sim\_1 - y

Scope x Sources

Name	Design U...	Block Type
y	y	Verilog Module
gbl	gbl	Verilog Module

Objects x Protocol Inst

Name	Value	Data Type
a	0	Logic
b	0	Logic
out	0	Logic

y.v x Untitled 8

1,100,000 ns

Name	Value
a	0
b	0
out	0

Tcl Console x Messages Log

```
add_force [/y/a] -radix hex [0 0ns] [1 50000ps] -repeat_every 100000ps
add_force [/y/b] -radix hex [0 0ns] [1 25000ps] -repeat_every 50000ps
run 100 ns
```

Type a Tcl command here

Sim Time: 1100 ns

## 2. AND Gate

test\_project\_1 - [C:/Users/apatra/Vivado/test\_project\_1/test\_project\_1.xpr] - Vivado 2019.2

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Ready

100 ns

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IMPLEMENTATION

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SIMULATION - Behavioral Simulation - Functional - sim\_1 - y

Scope

Name	Design U...	Block Type
y	y	Verilog Module
gbl	gbl	Verilog Module

Objects

Name	Value	Data Type
a	0	Logic
b	0	Logic
out	0	Logic

y.v

```
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//
module y(
    input a,b,
    output out
);
    and and1(out,a,b);
endmodule
```

Tcl Console

```
add_force (/y/a) -radix hex [0 0ns] [1 50000ps] -repeat_every 10000ps
add_force (/y/b) -radix hex [0 0ns] [1 25000ps] -repeat_every 5000ps
run 100 ns
```

Sim Time: 1100 ns

test\_project\_1 - [C:/Users/apatra/Vivado/test\_project\_1/test\_project\_1.xpr] - Vivado 2019.2

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Ready

100 ns

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SIMULATION - Behavioral Simulation - Functional - sim\_1 - y

Scope

Name	Design U...	Block Type
y	y	Verilog Module
gbl	gbl	Verilog Module

Objects

Name	Value	Data Type
a	0	Logic
b	0	Logic
out	0	Logic

y.v

```
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//
module y(
    input a,b,
    output out
);
    and and1(out,a,b);
endmodule
```

Tcl Console

```
add_force (/y/a) -radix hex [0 0ns] [1 50000ps] -repeat_every 10000ps
add_force (/y/b) -radix hex [0 0ns] [1 25000ps] -repeat_every 5000ps
run 100 ns
```

Sim Time: 1100 ns

Timing Diagram

Name	Value	Time
a	0	0 ns
a	1	50000 ps
a	0	100000 ps
b	0	0 ns
b	1	25000 ps
b	0	50000 ps
out	0	0 ns
out	1	50000 ps
out	0	100000 ps

### 3. NOR Gate

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Scope

Name	Design U...	Block Type
y	y	Verilog Module
gbl	gbl	Verilog Module

Objects

Name	Value	Data Type
a	0	Logic
b	0	Logic
out	1	Logic

y.v

```
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//
module y(
    input a,b,
    output out
);
    or nor1(out,a,b);
endmodule
```

Tcl Console

```
add_force (/y/a) -radix hex (0 0ns) (1 50000ps) -repeat_every 10000ps
add_force (/y/b) -radix hex (0 0ns) (1 25000ps) -repeat_every 5000ps
run 100 ns
```

Sim Time: 1100 ns

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Flow Navigator SIMULATION - Behavioral Simulation - Functional - sim\_1 - y

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Scope

Name	Design U...	Block Type
y	y	Verilog Module
gbl	gbl	Verilog Module

Objects

Name	Value	Data Type
a	0	Logic
b	0	Logic
out	1	Logic

y.v

```
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//
module y(
    input a,b,
    output out
);
    or nor1(out,a,b);
endmodule
```

Tcl Console

```
add_force (/y/a) -radix hex (0 0ns) (1 50000ps) -repeat_every 10000ps
add_force (/y/b) -radix hex (0 0ns) (1 25000ps) -repeat_every 5000ps
run 100 ns
```

Sim Time: 1100 ns

## 4. NAND Gate

test\_project\_1 - [C:/Users/apatra/Vivado/test\_project\_1/test\_project\_1.xpr] - Vivado 2019.2

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100 ns

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IMPLEMENTATION

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SIMULATION - Behavioral Simulation - Functional - sim\_1 - y

Scope

Name	Design U...	Block Type
y	y	Verilog Module
gbl	gbl	Verilog Module

Objects

Name	Value	Data Type
a	0	Logic
b	0	Logic
out	1	Logic

y.v x Untitled 11 x

C:/Users/apatra/Vivado/test\_project\_1/test\_project\_1.srscs/sources\_1/newly.v

```
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18 // Additional Comments:
19 //
20 //
21 //
22 //
23 module y(
24     input a,b,
25     output out
26 );
27     nand nand1(out,a,b);
28 endmodule
29
```

Tcl Console

Messages Log

```
add_force (/y/a) -radix hex (0 0ns) (1 50000ps) -repeat_every 100000ps
add_force (/y/b) -radix hex (0 0ns) (1 25000ps) -repeat_every 50000ps
run 100 ns
```

Type a Tcl command here

Sim Time: 1100 ns

test\_project\_1 - [C:/Users/apatra/Vivado/test\_project\_1/test\_project\_1.xpr] - Vivado 2019.2

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Ready

100 ns

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SYNTHESIS

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IMPLEMENTATION

- Run Implementation

SIMULATION - Behavioral Simulation - Functional - sim\_1 - y

Scope

Name	Design U...	Block Type
y	y	Verilog Module
gbl	gbl	Verilog Module

Objects

Name	Value	Data Type
a	0	Logic
b	0	Logic
out	1	Logic

y.v x Untitled 11 x

C:/Users/apatra/Vivado/test\_project\_1/test\_project\_1.srscs/sources\_1/newly.v

Waveform

Name	Value	Time
a	0	0 ns
b	0	0 ns
out	1	0 ns

Tcl Console

Messages Log

```
add_force (/y/a) -radix hex (0 0ns) (1 50000ps) -repeat_every 100000ps
add_force (/y/b) -radix hex (0 0ns) (1 25000ps) -repeat_every 50000ps
run 100 ns
```

Type a Tcl command here

Sim Time: 1100 ns

## 5. XOR Gate

test\_project\_1 - [C:/Users/apatra/Vivado/test\_project\_1/test\_project\_1.xpr] - Vivado 2019.2

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Ready

100 ns

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IMPLEMENTATION

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SIMULATION - Behavioral Simulation - Functional - sim\_1 - y

Scope

Name	Design U...	Block Type
y	y	Verilog Module
gbl	gbl	Verilog Module

Objects

Name	Value	Data Type
a	0	Logic
b	0	Logic
out	0	Logic

y.v

```
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//
module y(
    input a,b,
    output out
);
    xor xorl(out,a,b);
endmodule
```

Tcl Console

```
add_force [/y/a] -radix hex [0 0ns] [1 50000ps] -repeat_every 100000ps
add_force [/y/b] -radix hex [0 0ns] [1 25000ps] -repeat_every 50000ps
run 100 ns
```

Sim Time: 1100 ns

test\_project\_1 - [C:/Users/apatra/Vivado/test\_project\_1/test\_project\_1.xpr] - Vivado 2019.2

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Ready

100 ns

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IMPLEMENTATION

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SIMULATION - Behavioral Simulation - Functional - sim\_1 - y

Scope

Name	Design U...	Block Type
y	y	Verilog Module
gbl	gbl	Verilog Module

Objects

Name	Value	Data Type
a	0	Logic
b	0	Logic
out	0	Logic

y.v

```
Name Value
a 0
b 0
out 0
```

Tcl Console

```
add_force [/y/a] -radix hex [0 0ns] [1 50000ps] -repeat_every 100000ps
add_force [/y/b] -radix hex [0 0ns] [1 25000ps] -repeat_every 50000ps
run 100 ns
```

Sim Time: 1100 ns

## 6. NOT Gate

test\_project\_1 - [C:/Users/apatra/Vivado/test\_project\_1/test\_project\_1.xpr] - Vivado 2019.2

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100 ns

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SIMULATION - Behavioral Simulation - Functional - sim\_1 - y

Scope x Sources

Name	Design U...	Block Type
y	y	Verilog Module
gblbl	gblbl	Verilog Module

Objects x Protocol Inst

Name	Value	Data Type
a	0	Logic
out	1	Logic

y.v x Untitled 1 x

C:/Users/apatra/Vivado/test\_project\_1/test\_project\_1.srcs/sources\_1/new/y.v

```
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 //
22 //
23 module y(
24     input a,
25     output out
26 );
27     out not1(out,a);
28 endmodule
29
```

Tcl Console x Messages Log

```
launch_simulation: Time (s): cpu = 00:00:18 ; elapsed = 00:00:19 . Memory (MB): peak = 867.875 ; gain = 9.961
add_force (/y/a) -radix hex (0 0ns) (1 50000ps) -repeat_every 100000ps
run 100 ns
```

Type a Tcl command here

Sim Time: 1100 ns

test\_project\_1 - [C:/Users/apatra/Vivado/test\_project\_1/test\_project\_1.xpr] - Vivado 2019.2

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100 ns

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SIMULATION - Behavioral Simulation - Functional - sim\_1 - y

Scope x Sources

Name	Design U...	Block Type
y	y	Verilog Module
gblbl	gblbl	Verilog Module

Objects x Protocol Inst

Name	Value	Data Type
a	0	Logic
out	1	Logic

y.v x Untitled 1 x

C:/Users/apatra/Vivado/test\_project\_1/test\_project\_1.srcs/sources\_1/new/y.v

Waveform visualization showing signals 'a' and 'out' over time. Signal 'a' is a square wave alternating between 0 and 1. Signal 'out' is a square wave alternating between 1 and 0, representing the NOT operation. The time scale is 1,000.000 ns.

Tcl Console x Messages Log

```
launch_simulation: Time (s): cpu = 00:00:18 ; elapsed = 00:00:19 . Memory (MB): peak = 867.875 ; gain = 9.961
add_force (/y/a) -radix hex (0 0ns) (1 50000ps) -repeat_every 100000ps
run 100 ns
```

Type a Tcl command here

Sim Time: 1100 ns