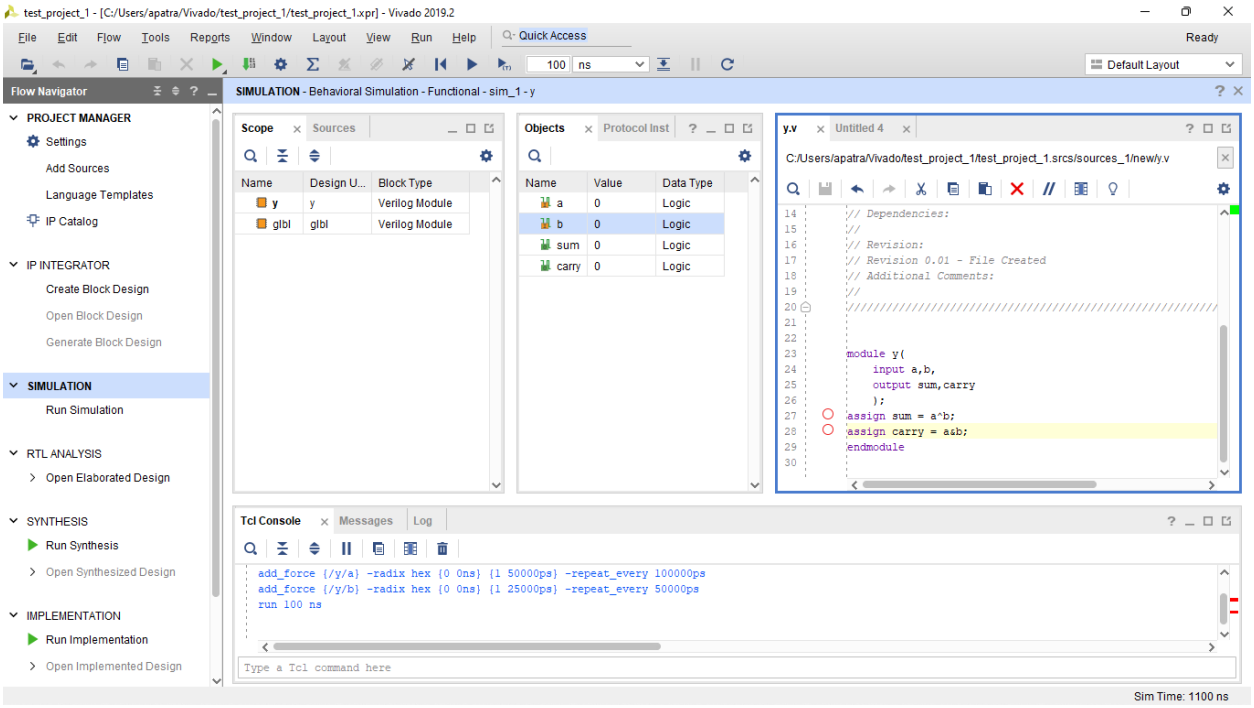
1. Half Adder


test_project_1 - [C:/Users/apatra/Vivado/test_project_1/test_project_1.xpr] - Vivado 2019.2
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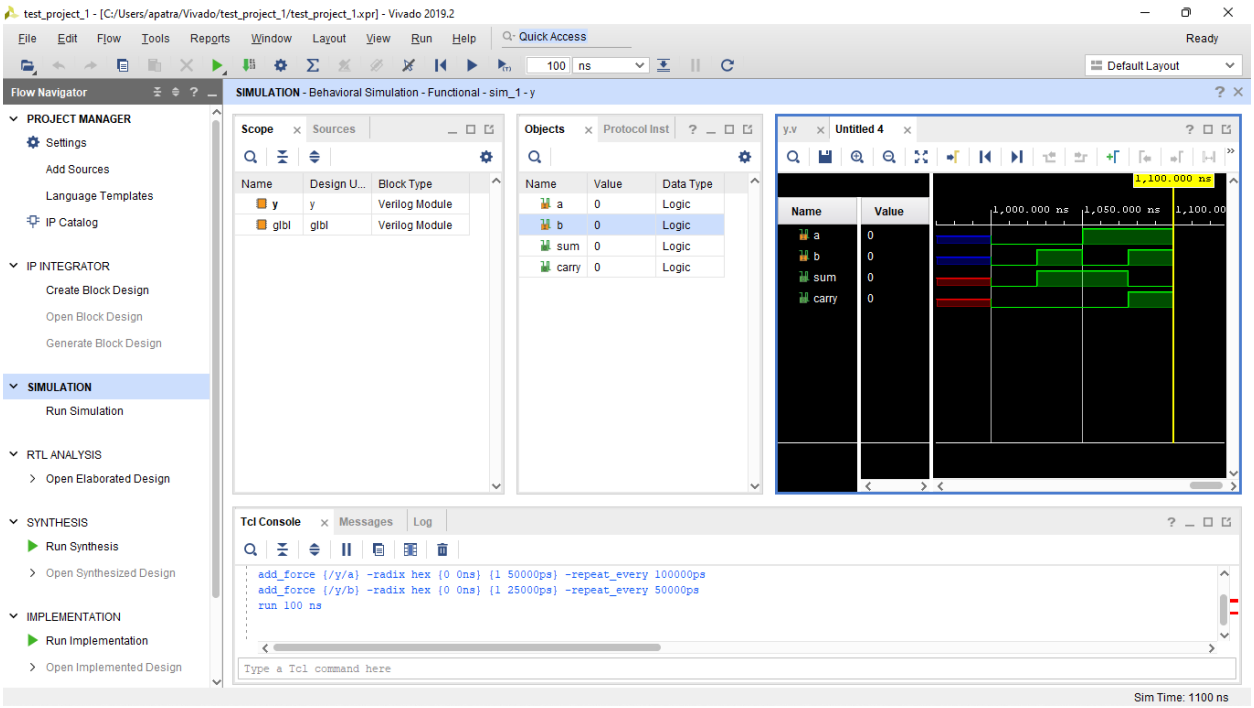
Name Design U... Block Type
y y Verilog Module
glbl glbl Verilog Module
Objects
Protocol Inst
Name Value Data Type
a 0 Logic
b 0 Logic
sum 0 Logic
carry 0 Logic
y.v
Untitled 4
C:/Users/apatra/Vivado/test_project_1/test_project_1.srcs/sources_1/new/y.v
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
module y(
input a,b,
output sum,carry
);
assign sum = a^b;
assign carry = a&b;
endmodule
Tcl Console
Messages
Log
add_force {/y/a} -radix hex {0 0ns} {1 50000ps} -repeat_every 100000ps
add_force {/y/b} -radix hex {0 0ns} {1 25000ps} -repeat_every 50000ps
run 100 ns
Type a Tcl command here
Sim Time: 1100 ns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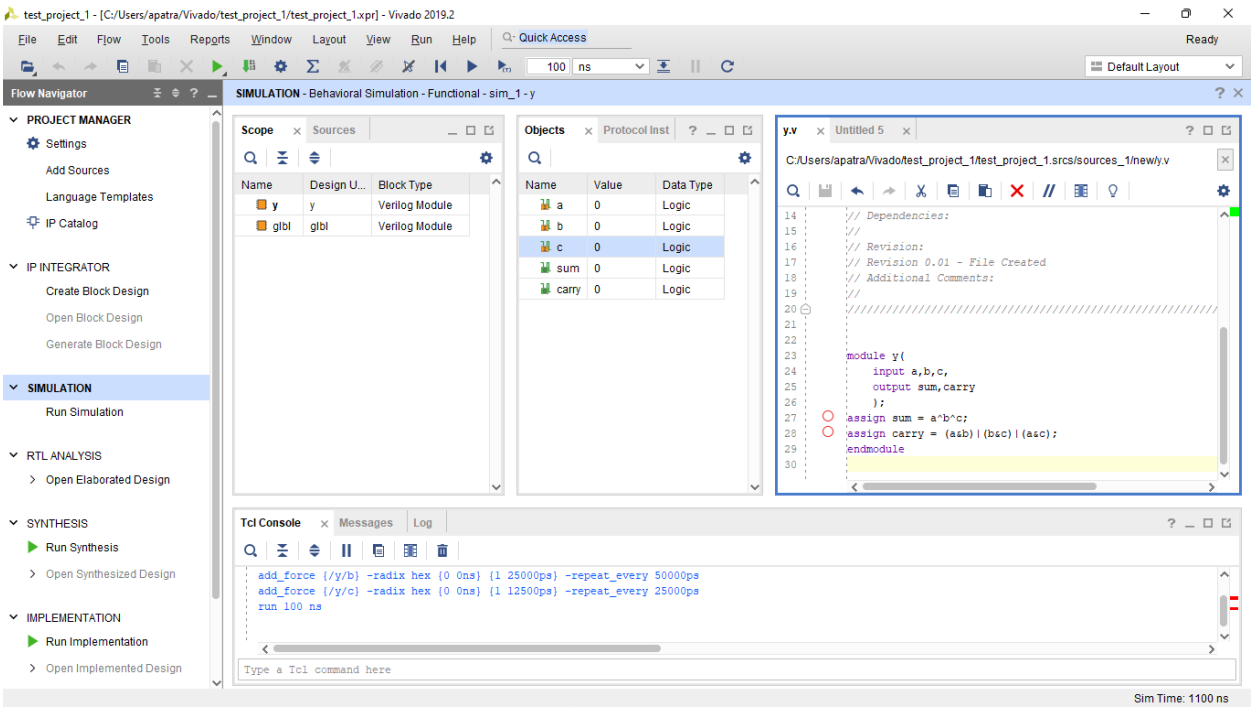
Name Design U... Block Type
y y Verilog Module
glbl glbl Verilog Module
Objects
Protocol Inst
Name Value Data Type
a 0 Logic
b 0 Logic
sum 0 Logic
carry 0 Logic
y.v
Untitled 4
Name
Value
a 0
b 0
sum 0
carry 0
1,100.000 ns
1,000.000 ns
1,050.000 ns
Tcl Console
Messages
Log
add_force {/y/a} -radix hex {0 0ns} {1 50000ps} -repeat_every 100000ps
add_force {/y/b} -radix hex {0 0ns} {1 25000ps} -repeat_every 50000ps
run 100 ns
Type a Tcl command here
Sim Time: 1100 ns

2. Full Adder


test_project_1 - [C:/Users/apatra/Vivado/test_project_1/test_project_1.xpr] - Vivado 2019.2
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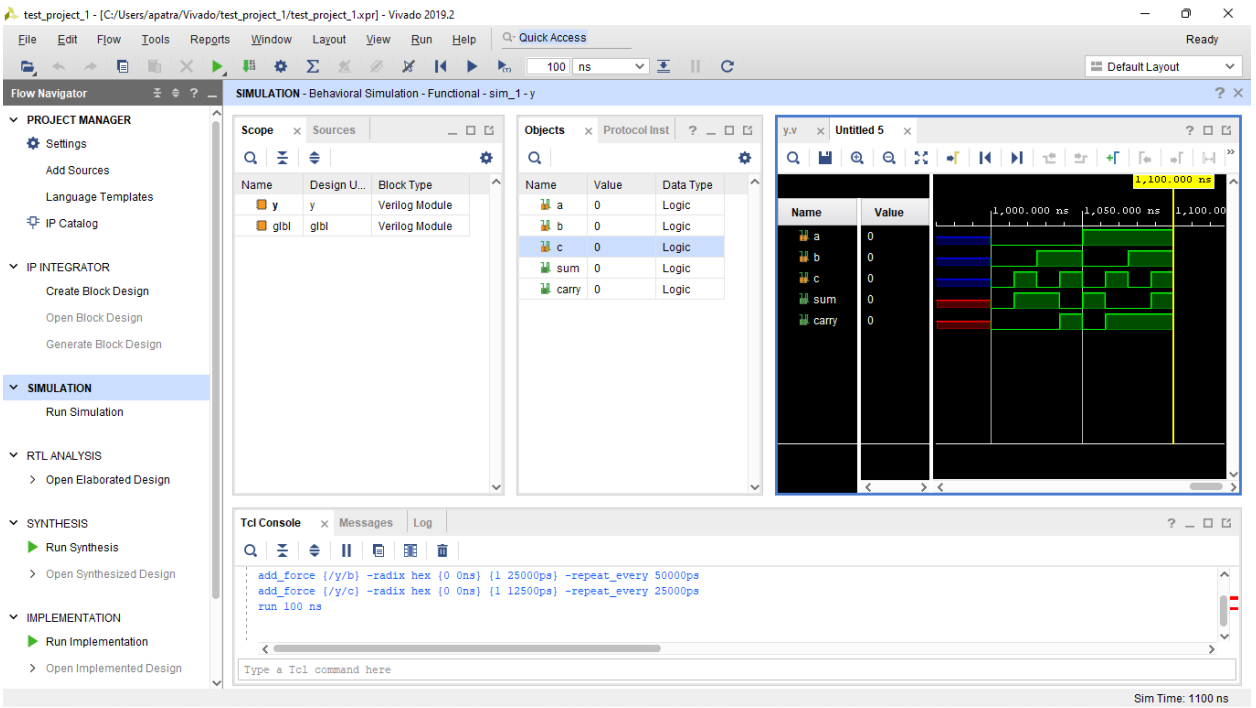
Scope
Sources
Name Design U... Block Type
y y Verilog Module
glbl glbl Verilog Module
Objects
Protocol Inst
Name Value Data Type
a 0 Logic
b 0 Logic
c 0 Logic
sum 0 Logic
carry 0 Logic
y.v
Untitled 5
C:/Users/apatra/Vivado/test_project_1/test_project_1.srcs/sources_1/new/y.v
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
module y(
input a,b,c,
output sum,carry
);
assign sum = a^b^c;
assign carry = (a&b)|(b&c)|(a&c);
endmodule
Tcl Console
Messages
Log
add_force {/y/b} -radix hex {0 0ns} {1 25000ps} -repeat_every 50000ps
add_force {/y/c} -radix hex {0 0ns} {1 12500ps} -repeat_every 25000ps
run 100 ns
Type a Tcl command here
Sim Time: 1100 ns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glbl glbl Verilog Module
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Protocol Inst
Name Value Data Type
a 0 Logic
b 0 Logic
c 0 Logic
sum 0 Logic
carry 0 Logic
y.v
Untitled 5
1,100.000 ns
1,000.000 ns
1,050.000 ns
1,100.00
Name
Value
a 0
b 0
c 0
sum 0
carry 0
Tcl Console
Messages
Log
add_force {/y/b} -radix hex {0 0ns} {1 25000ps} -repeat_every 50000ps
add_force {/y/c} -radix hex {0 0ns} {1 12500ps} -repeat_every 25000ps
run 100 ns
Type a Tcl command here
Sim Time: 1100 ns