Assignment No. 2
Computer Organisation - CS220

Note: On 27/01/2023, we will discuss how to calculate area and delay for a particular design. In the lab, we will just see the post-route simulation of the given adder designs. We will show some new constraints in the UCF file. You are NOT required to run them on FPGA. It is highly recommended that you attend the class on coming Friday. Otherwise, it will be very difficult for you to generate the report on area and delay during the lab session.

Group A

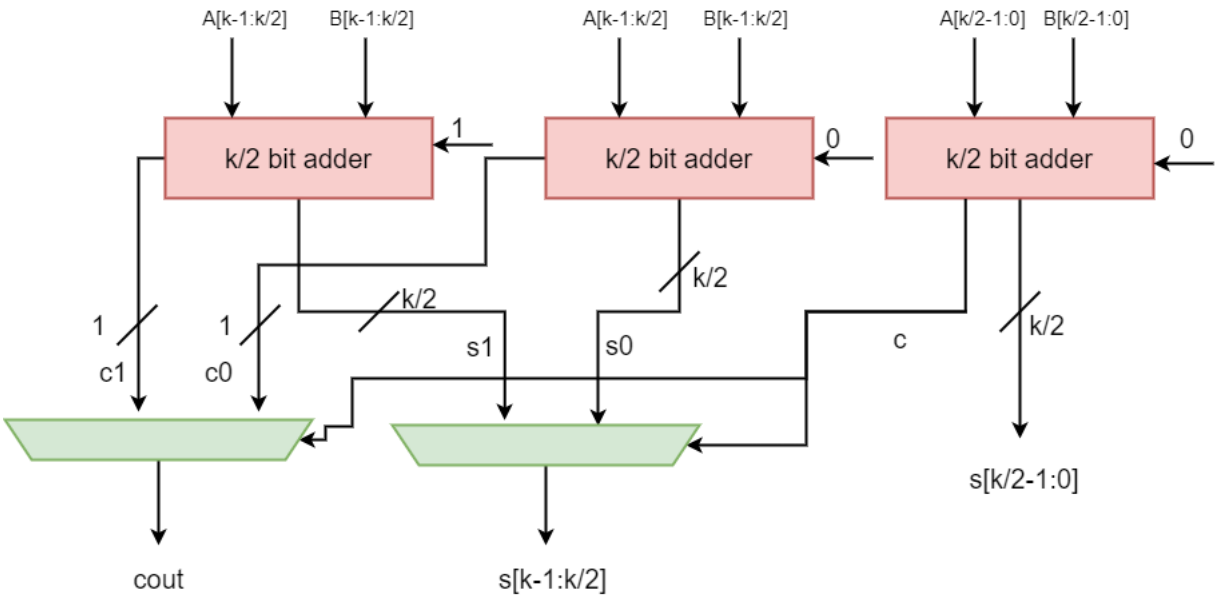


Figure 1: Architecture of "Mjolnir" Adder Circuit

1. Suppose we have a new adder circuit named "Mjolnir" as shown in Figure 2. Implement k-bit "Mjolnir" adder where $k = 16,\ 32,\ 64,\ 128$ using $k/2$-bit ripple carry adder. Use verilog parameters for k.

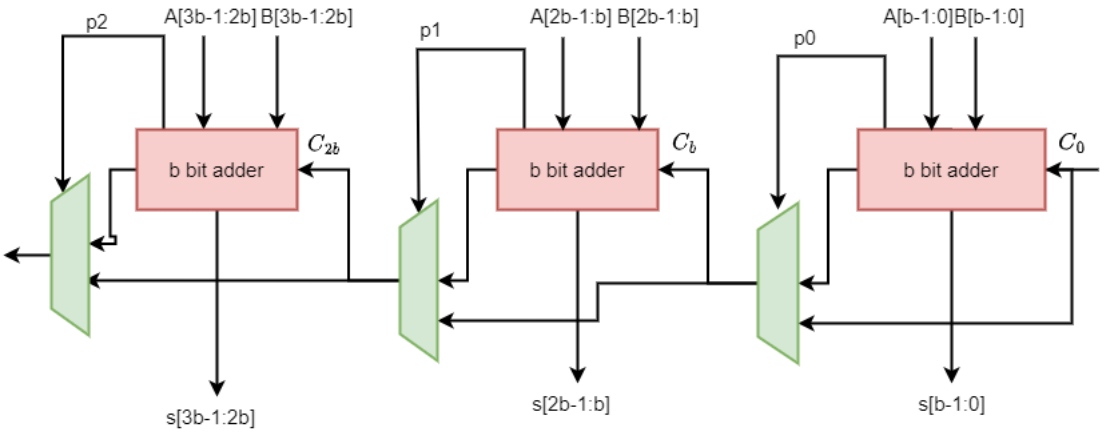
2. Compare the area requirement of the design with k-bit "Mjolnir" adder k-bit ripple carry adder where $k = 16,\ 32,\ 64,\ 128$.

3. Compare the delay of k-bit "Mjolnir" adder with k-bit ripple carry adder where $k =$

16, 32, 64, 128. Please note that both the inputs and the outputs are required to be registered.

4. Comment when k-bit "Mjolnir" will be more efficient than k-bit ripple carry adder.

Group B



$$p0 = (A[0] \oplus B[0])(A[1] \oplus B[1]) \cdots (A[b-1] \oplus B[-1])$$

Figure 2: Architecture of "Stormbreaker" Adder Circuit

1. Suppose we have a new adder circuit named "Stormbreaker" as shown in Figure.2. Implement 128-bit "Stormbreaker" adder using b-bit ripple carry adder where $b = 4,\ 8,\ 16,\ 32$. Use verilog parameters for b.

2. Compare the area requirement of 128-bit "Stormbreaker" adder where $b = 4,\ 8,\ 16,\ 32$ with a 128-bit ripple carry adder.

3. Compare the delay of the 128-bit "Stormbreaker" adder where $b = 4,\ 8,\ 16,\ 32$ with a 128-bit ripple carry adder. Please note that both the inputs and the outputs are required to be registered.

4. Comment when 128-bit "Stormbreaker" will be more efficient than 128-bit ripple carry adder.