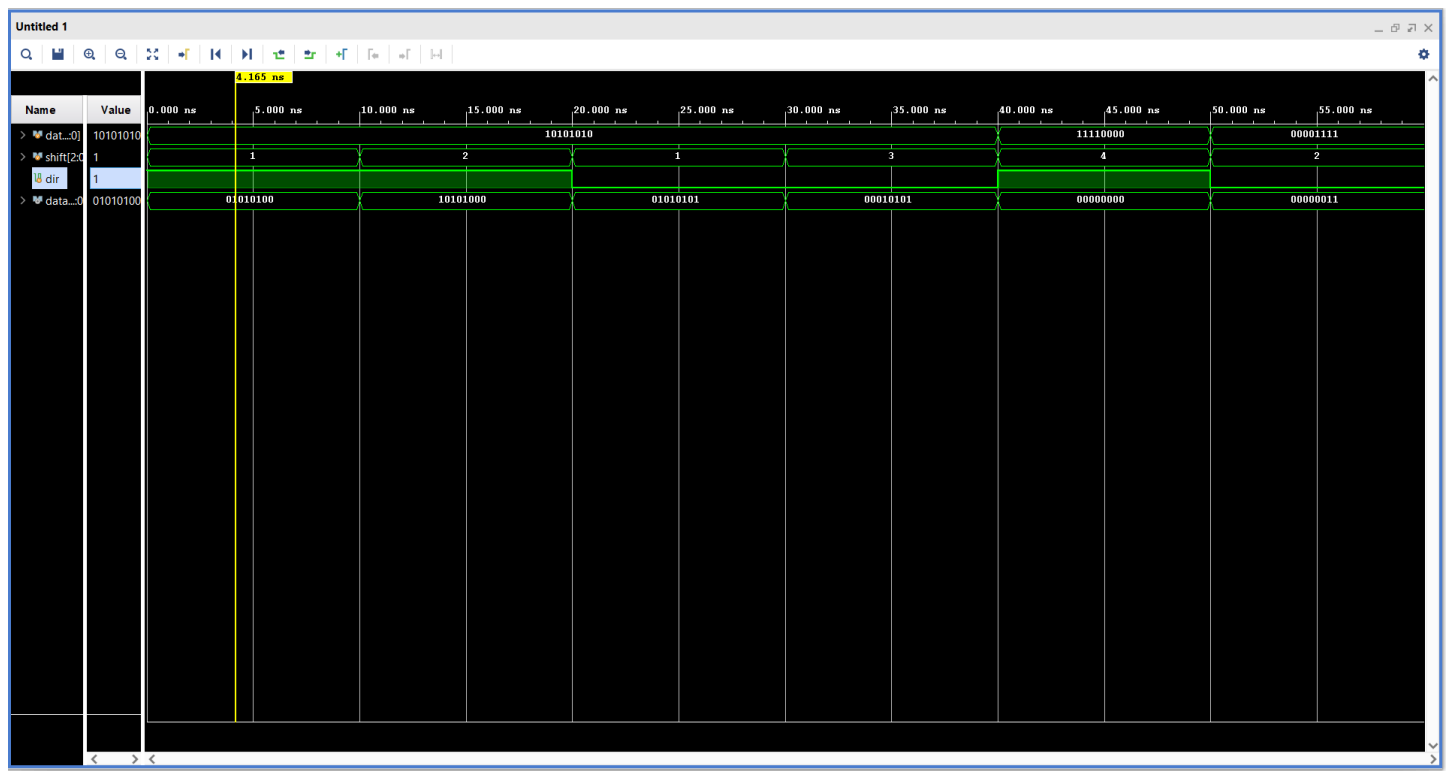


Design a 8-bit Logarithmic Barrel shifter, for performing Right and Left Shift (Logical) operation. Write a testbench and simulate the circuit

1. Using >> and << operator

Simulation Waveform using >> and << operator



Verilog Code:

```

module BarrelShifter (
    input [7:0] data_in, // Input data
    input [2:0] shift, // Shift amount (3 bits to represent 0 to 7)
    input dir, // Direction (0 for right, 1 for left)
    output [7:0] data_out // Shifted output
);
    // Perform shift based on direction
    assign data_out = (dir == 1'b1) ? (data_in << shift) : (data_in >> shift);
endmodule

```

Test Bench Code:

```

module TestBench;
    // Testbench signals

```

```
reg [7:0] data_in; // Input data
reg [2:0] shift; // Shift amount
reg dir; // Shift direction (0 for right, 1 for left)
wire [7:0] data_out; // Output data

// Instantiate the BarrelShifter module
BarrelShifter uut (
    .data_in(data_in),
    .shift(shift),
    .dir(dir),
    .data_out(data_out)
);

initial begin
    // Display header for the simulation results
    $display("Time | Data In | Shift | Dir | Data Out ");
    $display("-----");

    // Test cases
    data_in = 8'b10101010; shift = 3'b001; dir = 1'b1; #10; // Left shift by 1
    $display("%4d | %b | %d | %b | %b", $time, data_in, shift, dir, data_out);

    data_in = 8'b10101010; shift = 3'b010; dir = 1'b1; #10; // Left shift by 2
    $display("%4d | %b | %d | %b | %b", $time, data_in, shift, dir, data_out);

    data_in = 8'b10101010; shift = 3'b001; dir = 1'b0; #10; // Right shift by 1
    $display("%4d | %b | %d | %b | %b", $time, data_in, shift, dir, data_out);

    data_in = 8'b10101010; shift = 3'b011; dir = 1'b0; #10; // Right shift by 3
    $display("%4d | %b | %d | %b | %b", $time, data_in, shift, dir, data_out);
```

```
// Additional cases
```

```
data_in = 8'b11110000; shift = 3'b100; dir = 1'b1; #10; // Left shift by 4
```

```
$display("%4d | %b | %d | %b | %b", $time, data_in, shift, dir, data_out);
```

```
data_in = 8'b00001111; shift = 3'b010; dir = 1'b0; #10; // Right shift by 2
```

```
$display("%4d | %b | %d | %b | %b", $time, data_in, shift, dir, data_out);
```

```
// End simulation
```

```
$finish;
```

```
end
```

```
endmodule
```

Utilisation Report:

The screenshot shows the Vivado 2020.2 interface with the Utilization report for the BarrelShifter design. The report is circled in red, showing the following data:

Name	Slice LUTs (53200)	Slice (13300)	LUT as Logic (53200)	Bonded IOB (125)
BarrelShifter	18	6	18	20

The report also includes a hierarchy view on the left, showing the design structure. The top-level design is EE705_2_2_2, which contains the BarrelShifter component.

Utilization - Synth Design - synth_1					
C:/Users/Tarious/7EE705_2_2/7EE705_2_2.runs/synth_1/BarrelShifter_utilization_synth.rpt					
Read-only					
Copyright 1986-2020 Xilinx, Inc. All Rights Reserved.					

Tool Version : Vivado v.2020.2 (win64) Build 3064766 Wed Nov 18 09:12:45 MST 2020					
Date : Fri Jan 24 20:33:26 2025					
Host : LAPTOP-M216N101 running 64-bit major release (build 9200)					
Command : report_utilization -file BarrelShifter_utilization_synth.rpt -pb BarrelShifter_utilization_synth.pb					
Design : BarrelShifter					
Device : 7z020clg400-1					
Design State : Synthesized					

Utilization Design Information					
Table of Contents					

1. Slice Logic					
1.1 Summary of Registers by Type					
2. Memory					
3. DSP					
4. IO and GT Specific					
5. Clocking					
6. Specific Feature					
7. Primitives					
8. Block Boxes					
9. Instantiated Netlists					

1. Slice Logic					

+-----+-----+-----+-----+-----+					
Site Type Used Fixed Available Util%					
+-----+-----+-----+-----+-----+					
Slice LUTs* 18 0 53200 0.03					
LUT as Logic 18 0 53200 0.03					
LUT as Memory 0 0 17400 0.00					
Slice Registers 0 0 106400 0.00					
Register as Flip Flop 0 0 106400 0.00					
Register as Latch 0 0 106400 0.00					
F7 Muxes 0 0 26600 0.00					
F8 Muxes 0 0 13300 0.00					
+-----+-----+-----+-----+-----+					

Utilization - Synth Design - synth_1					
C:/Users/Tarious/7EE705_2_2/7EE705_2_2.runs/synth_1/BarrelShifter_utilization_synth.rpt					
Read-only					
* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.					

1.1 Summary of Registers by Type					

+-----+-----+-----+-----+-----+					
Total Clock Enable Synchronous Asynchronous					
+-----+-----+-----+-----+-----+					
0 - - -					
0 - - Set					
0 - - Reset					
0 - Set -					
0 - Reset -					
0 Yes - -					
0 Yes - Set					
0 Yes - Reset					
0 Yes Set -					
0 Yes Reset -					
+-----+-----+-----+-----+-----+					
2. Memory					

+-----+-----+-----+-----+-----+					
Site Type Used Fixed Available Util%					
+-----+-----+-----+-----+-----+					
Block RAM Tile 0 0 140 0.00					
RAMB36/FIFO* 0 0 140 0.00					
RAMB18 0 0 280 0.00					
+-----+-----+-----+-----+-----+					
* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accom					

3. DSP					

+-----+-----+-----+-----+-----+					
Site Type Used Fixed Available Util%					
+-----+-----+-----+-----+-----+					

Utilization - Synth Design - synth_1

C:/Users/Tarious/7EE705_2_2/7EE705_2_2_runs/synth_1/BarrelShifter_utilization_synth.rpt

Read-only

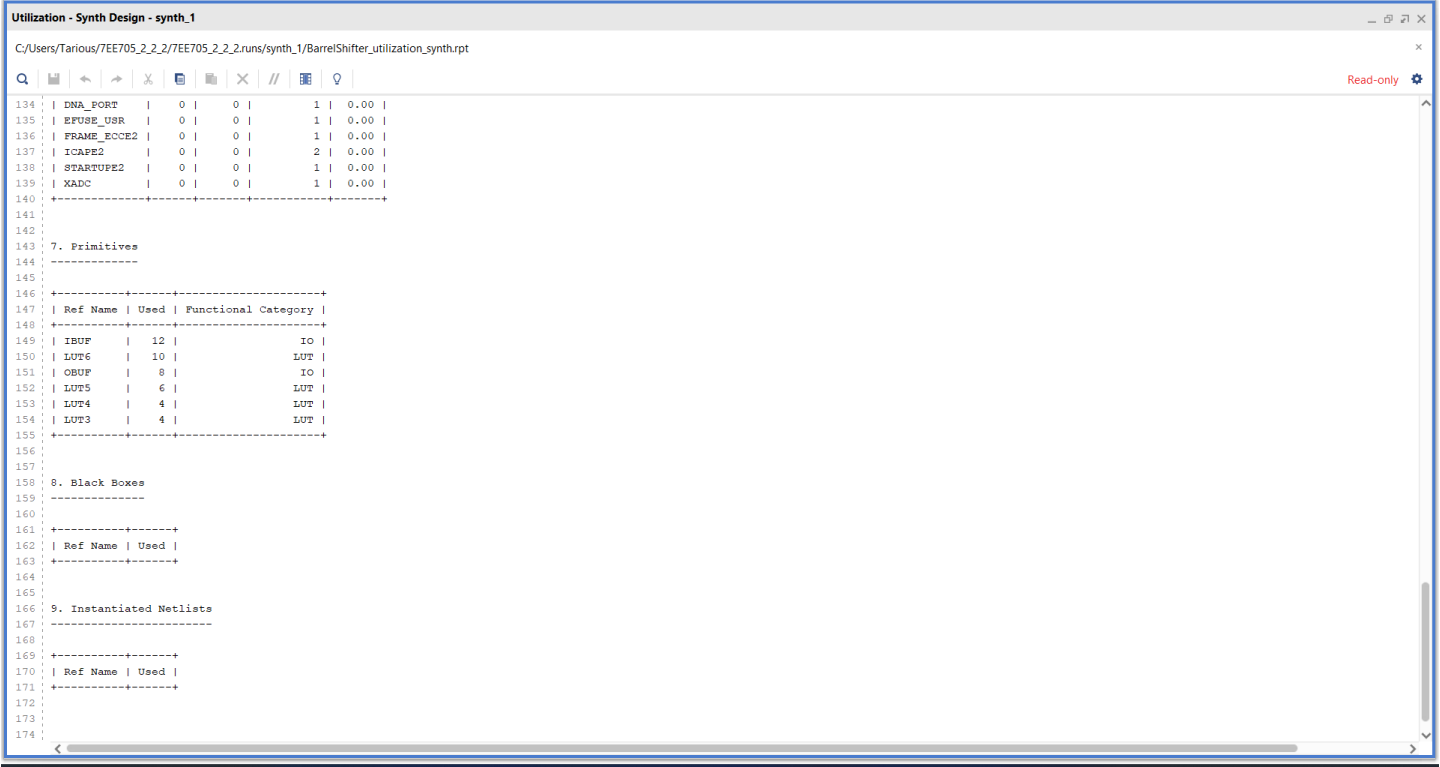
77	3. DSP					
78	-----					
79						
80	+-----+-----+-----+-----+-----+					
81	Site Type	Used	Fixed	Available	Util%	
82	+-----+-----+-----+-----+-----+					
83	DSPs	0	0	220	0.00	
84	+-----+-----+-----+-----+-----+					
85						
86	4. IO and GT Specific					
87	-----					
88						
89						
90	+-----+-----+-----+-----+-----+					
91	Site Type	Used	Fixed	Available	Util%	
92	+-----+-----+-----+-----+-----+					
93	Bonded IOB	20	0	125	16.00	
94	Bonded IPADs	0	0	2	0.00	
95	Bonded IOPADs	0	0	130	0.00	
96	PHY_CONTROL	0	0	4	0.00	
97	PHASER_REF	0	0	4	0.00	
98	OUT_FIFO	0	0	16	0.00	
99	IN_FIFO	0	0	16	0.00	
100	IDELAYCTRL	0	0	4	0.00	
101	IBUFDS	0	0	121	0.00	
102	PHASER_OUT/PHASER_OUT_PHY	0	0	16	0.00	
103	PHASER_IN/PHASER_IN_PHY	0	0	16	0.00	
104	IDELAY2/IDELAY2_FINEDELAY	0	0	200	0.00	
105	ILOGIC	0	0	125	0.00	
106	OLOGIC	0	0	125	0.00	
107	+-----+-----+-----+-----+-----+					
108						
109	5. Clocking					
110	-----					
111						
112						
113	+-----+-----+-----+-----+-----+					
114	Site Type	Used	Fixed	Available	Util%	
115	+-----+-----+-----+-----+-----+					
116	BUFGCTRL	0	0	32	0.00	
117	BUFIO	0	0	16	0.00	
118	+-----+-----+-----+-----+-----+					
119						
120						
121						
122						
123						
124						
125						
126	6. Specific Feature					
127	-----					
128						
129	+-----+-----+-----+-----+-----+					
130	Site Type	Used	Fixed	Available	Util%	
131	+-----+-----+-----+-----+-----+					
132	BSCAN2	0	0	4	0.00	
133	CAPTURE2	0	0	1	0.00	
134	DNA_PORT	0	0	1	0.00	
135	EFUSE_USR	0	0	1	0.00	
136	FRAME_ECCE2	0	0	1	0.00	
137	ICAPE2	0	0	2	0.00	
138	STARPUPE2	0	0	1	0.00	
139	XADC	0	0	1	0.00	
140	+-----+-----+-----+-----+-----+					
141						
142						
143	7. Primitives					
144	-----					
145						
146	+-----+-----+-----+-----+-----+					
147	Ref Name	Used	Functional Category			
148	+-----+-----+-----+-----+-----+					
149	IBUF	12	IO			
150	LUT6	10	LUT			

Utilization - Synth Design - synth_1

C:/Users/Tarious/7EE705_2_2/7EE705_2_2_runs/synth_1/BarrelShifter_utilization_synth.rpt

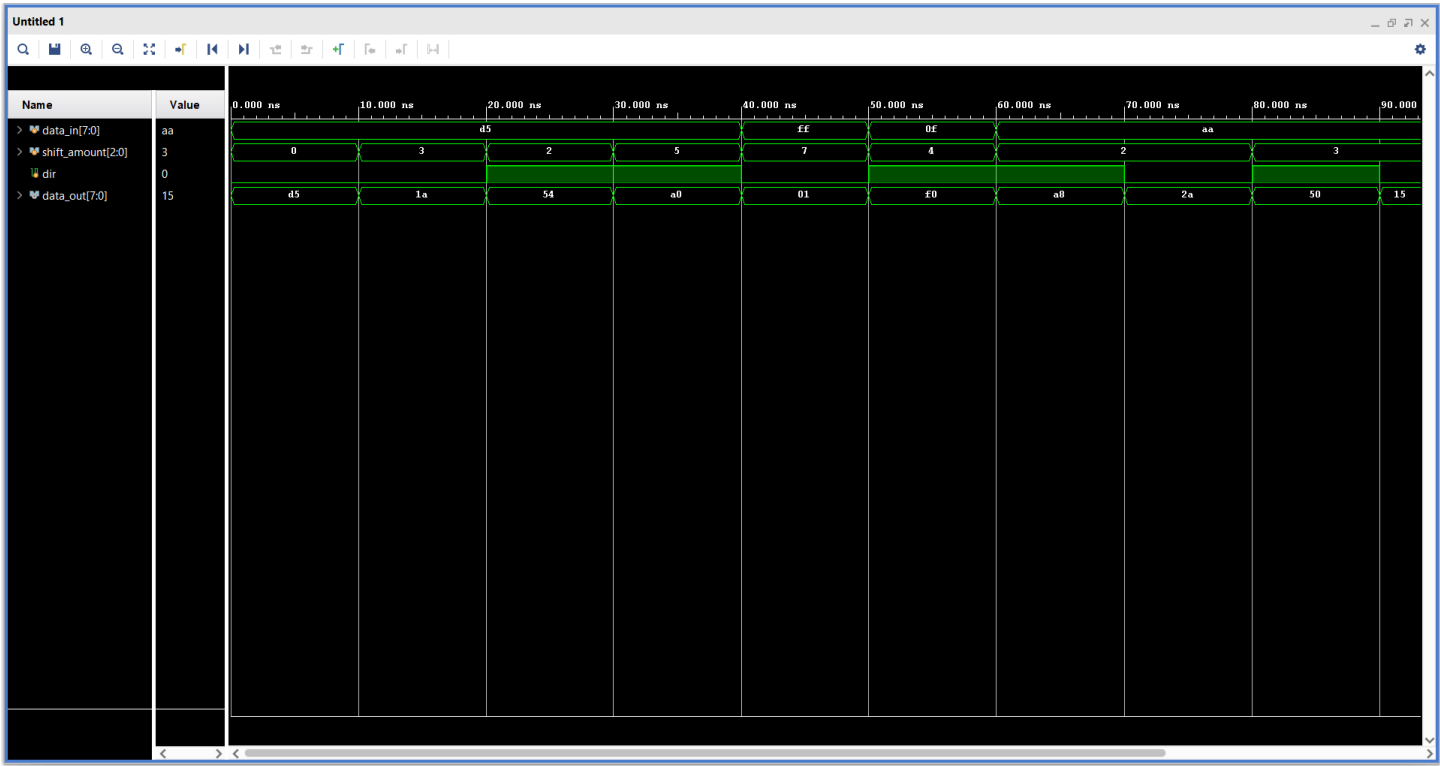
Read-only

110	5. Clocking					
111	-----					
112						
113	+-----+-----+-----+-----+-----+					
114	Site Type	Used	Fixed	Available	Util%	
115	+-----+-----+-----+-----+-----+					
116	BUFGCTRL	0	0	32	0.00	
117	BUFIO	0	0	16	0.00	
118	M4CM2_ADV	0	0	4	0.00	
119	FLLE2_ADV	0	0	4	0.00	
120	BUFMCE	0	0	8	0.00	
121	BUFHCE	0	0	72	0.00	
122	BUFR	0	0	16	0.00	
123	+-----+-----+-----+-----+-----+					
124						
125						
126	6. Specific Feature					
127	-----					
128						
129	+-----+-----+-----+-----+-----+					
130	Site Type	Used	Fixed	Available	Util%	
131	+-----+-----+-----+-----+-----+					
132	BSCAN2	0	0	4	0.00	
133	CAPTURE2	0	0	1	0.00	
134	DNA_PORT	0	0	1	0.00	
135	EFUSE_USR	0	0	1	0.00	
136	FRAME_ECCE2	0	0	1	0.00	
137	ICAPE2	0	0	2	0.00	
138	STARPUPE2	0	0	1	0.00	
139	XADC	0	0	1	0.00	
140	+-----+-----+-----+-----+-----+					
141						
142						
143	7. Primitives					
144	-----					
145						
146	+-----+-----+-----+-----+-----+					
147	Ref Name	Used	Functional Category			
148	+-----+-----+-----+-----+-----+					
149	IBUF	12	IO			
150	LUT6	10	LUT			



Using Logarithmic Barrel shifter

Simulation Waveform Using Logarithmic Barrel shifter



Verilog Code:

```
// 8-bit Logarithmic Barrel Shifter
```

```
module BarrelShifter (  
    input [7:0] data_in,    // Input data  
    input [2:0] shift_amount, // Shift amount (3 bits for up to 7 shifts)  
    input dir,              // Direction: 0 for logical right, 1 for logical left  
    output [7:0] data_out   // Shifted output  
);  
    wire [7:0] stage1, stage2, stage3;  
  
    // Stage 1: Shift by 1 position (if shift_amount[0] == 1)  
    assign stage1 = shift_amount[0] ? (dir ? {data_in[6:0], 1'b0} : {1'b0, data_in[7:1]}) : data_in;  
  
    // Stage 2: Shift by 2 positions (if shift_amount[1] == 1)  
    assign stage2 = shift_amount[1] ? (dir ? {stage1[5:0], 2'b00} : {2'b00, stage1[7:2]}) : stage1;  
  
    // Stage 3: Shift by 4 positions (if shift_amount[2] == 1)  
    assign stage3 = shift_amount[2] ? (dir ? {stage2[3:0], 4'b0000} : {4'b0000, stage2[7:4]}) :  
    stage2;  
  
    // Final output  
    assign data_out = stage3;  
endmodule
```

Test Bench Code:

```
module Testbench;  
    reg [7:0] data_in;  
    reg [2:0] shift_amount;  
    reg dir;  
    wire [7:0] data_out;  
  
    // Instantiate the BarrelShifter module
```

BarrelShifter uut (

.data_in(data_in),

.shift_amount(shift_amount),

.dir(dir),

.data_out(data_out)

);

initial begin

// Test cases

\$monitor("Time = %0t | data_in = %b | shift_amount = %d | dir = %b | data_out = %b",
\$time, data_in, shift_amount, dir, data_out);

// Test case 1: Logical right shift by 0

data_in = 8'b11010101; shift_amount = 3'b000; dir = 0; #10;

// Test case 2: Logical right shift by 3

data_in = 8'b11010101; shift_amount = 3'b011; dir = 0; #10;

// Test case 3: Logical left shift by 2

data_in = 8'b11010101; shift_amount = 3'b010; dir = 1; #10;

// Test case 4: Logical left shift by 5

data_in = 8'b11010101; shift_amount = 3'b101; dir = 1; #10;

// Test case 5: Logical right shift by 7

data_in = 8'b11111111; shift_amount = 3'b111; dir = 0; #10;

// Test case 6: Logical left shift by 4

data_in = 8'b00001111; shift_amount = 3'b100; dir = 1; #10;

// Test case 7: Logical left shift by 2

data_in = 8'b10101010; shift_amount = 3'b010; dir = 1; #10;


```
// Test case 8: Logical right shift by 2
```

```
data_in = 8'b10101010; shift_amount = 3'b010; dir = 0; #10;
```

```
// Test case 9: Logical left shift by 3
```

```
data_in = 8'b10101010; shift_amount = 3'b011; dir = 1; #10;
```

```
// Test case 10: Logical right shift by 3
```

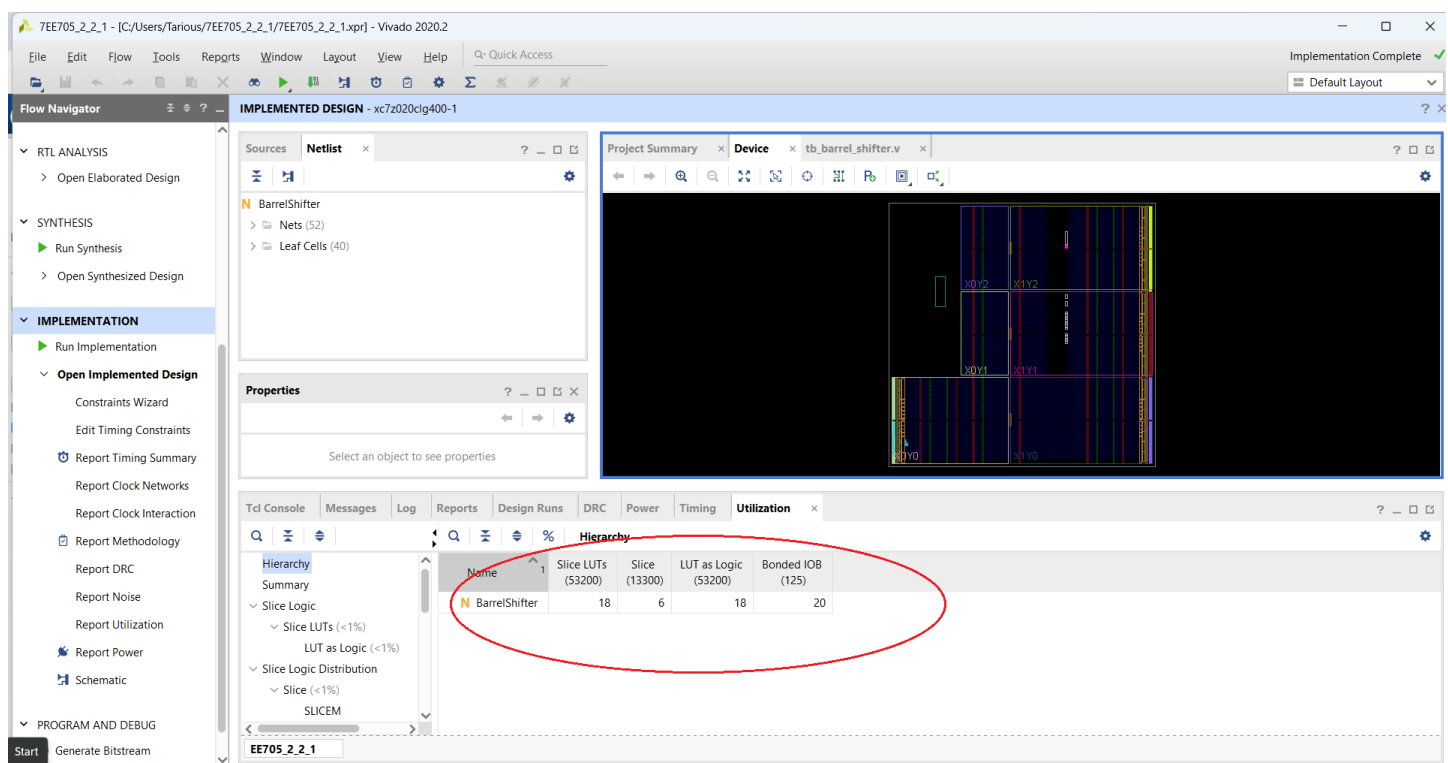
```
data_in = 8'b10101010; shift_amount = 3'b011; dir = 0; #10;
```

```
$finish;
```

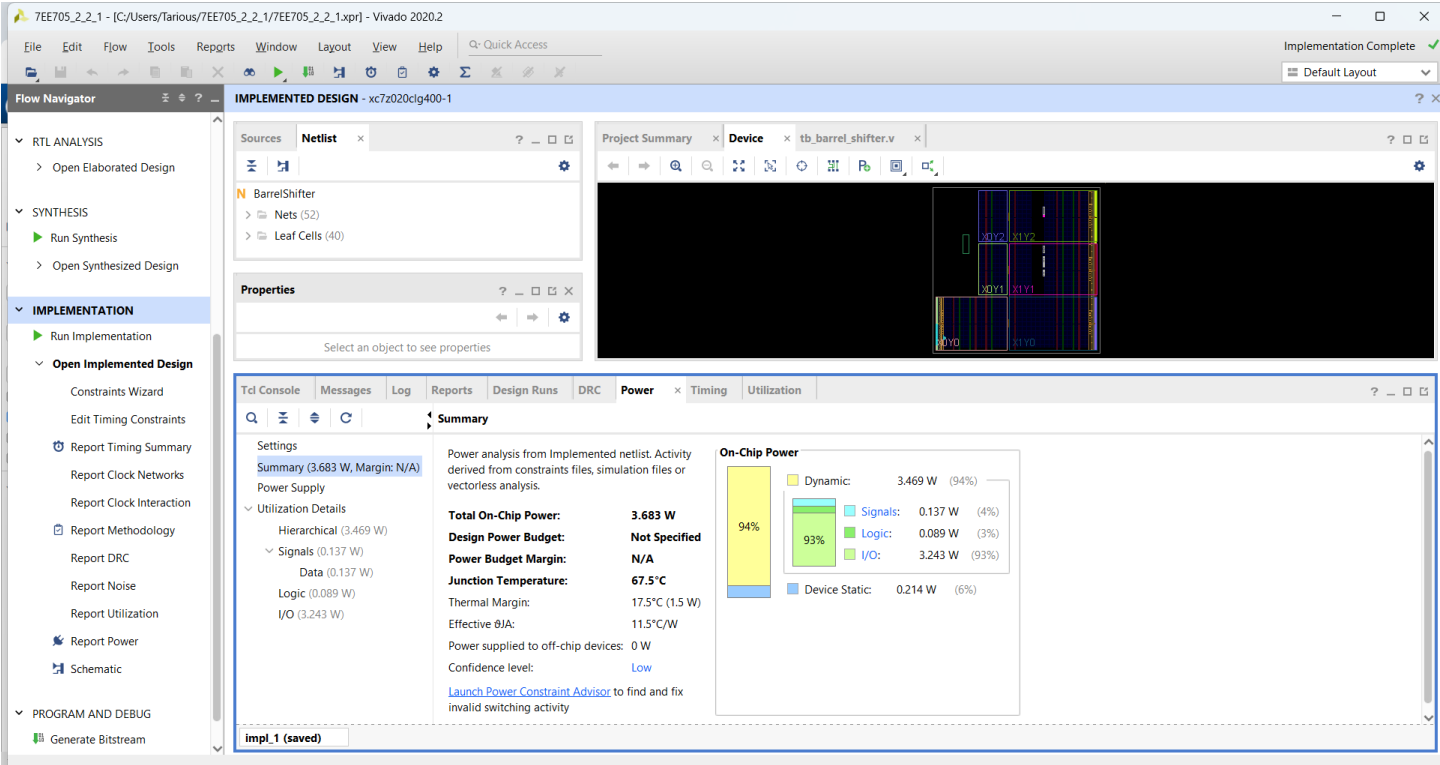
```
end
```

```
endmodule
```

Report Utilisation:



Power Consumption:



Resource Utilisation Report:

Utilization - Synth Design - synth_1

C:/Users/Tarious/7EE705_2_2_1/7EE705_2_2_1.runs/synth_1/BarrelShifter_utilization_synth.rpt

Copyright 1986-2020 Xilinx, Inc. All Rights Reserved.

Tool Version : Vivado v.2020.2 (win64) Build 3064766 Wed Nov 18 09:12:45 MST 2020

Date : Fri Jan 24 15:24:25 2025

Host : LAPTOP-M216N101 running 64-bit major release (build 9200)

Command : report_utilization -file BarrelShifter_utilization_synth.rpt -pb BarrelShifter_utilization_synth.pb

Design : BarrelShifter

Device : 7x020clg400-1

Design State : Synthesized

Utilization Design Information

Table of Contents

1. Slice Logic

1.1 Summary of Registers by Type

2. Memory

3. DSP

4. IO and GT Specific

5. Clocking

6. Specific Feature

7. Primitives

8. Black Boxes

9. Instantiated Netlists

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
1 Slice LUTs*	18	0	53200	0.03
1 LUT as Logic	18	0	53200	0.03
1 LUT as Memory	0	0	17400	0.00
1 Slice Registers	0	0	106400	0.00
1 Register as Flip Flop	0	0	106400	0.00
1 Register as Latch	0	0	106400	0.00
1 F7 Muxes	0	0	26600	0.00
1 F8 Muxes	0	0	13300	0.00

```
Utilization - Synth Design - synth_1
C:/Users/Tarios/T7EE705_2_2_1/T7EE705_2_2_1/runs/synth_1/BarrelShifter_utilization_synth.rpt

Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.

1.1 Summary of Registers by Type
-----
+-----+-----+-----+-----+
| Total | Clock Enable | Synchronous | Asynchronous |
+-----+-----+-----+-----+
| 0 | | - | - | - |
| 0 | | - | - | Set |
| 0 | | - | - | Reset |
| 0 | | - | Set | - |
| 0 | | - | Reset | - |
| 0 | | Yes | - | - |
| 0 | | Yes | - | Set |
| 0 | | Yes | - | Reset |
| 0 | | Yes | Set | - |
| 0 | | Yes | Reset | - |
+-----+-----+-----+-----+

2. Memory
-----
+-----+-----+-----+-----+
| Site Type | Used | Fixed | Available | Util% |
+-----+-----+-----+-----+
| Block RAM Tile | 0 | 0 | 140 | 0.00 |
| RAMB36/FIFO* | 0 | 0 | 140 | 0.00 |
| RAMB18 | 0 | 0 | 280 | 0.00 |
+-----+-----+-----+-----+

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accomm

3. DSP
-----
+-----+-----+-----+-----+
| Site Type | Used | Fixed | Available | Util% |
+-----+-----+-----+-----+
```

Utilization - Synth Design - synth_1

C:\Users\Tarious\7EE705_2_2_1\7EE705_2_2_1\runs\synth_1\BarrelShifter_utilization_synth.rpt

3. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	220	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	20	0	125	16.00
Bonded IOPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	4	0.00
PHASER_REF	0	0	4	0.00
OUT_FIFO	0	0	16	0.00
IN_FIFO	0	0	16	0.00
IDELAVCTRL	0	0	4	0.00
IBUFDS	0	0	121	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	16	0.00
PHASER_IN/PHASER_IN_PHY	0	0	16	0.00
IDELAVE2/IDELAVE2_FINEDELAY	0	0	200	0.00
ILOGIC	0	0	125	0.00
OLOGIC	0	0	125	0.00

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	0	0	32	0.00
BUFIO	0	0	16	0.00

Utilization - Synth Design - synth_1

C:/Users/Tarious/7EE705_2_2_1/7EE705_2_2_1.runs/synth_1/BarrelShifter_utilization_synth.rpt

Read-only

110	5. Clocking					
111	-----					
112	+-----+-----+-----+-----+-----+					
113	+-----+-----+-----+-----+-----+					
114	Site Type	Used	Fixed	Available	Util%	
115	+-----+-----+-----+-----+-----+					
116	BUFCTRL	0	0	32	0.00	
117	BUFIO	0	0	16	0.00	
118	MMCM2_ADV	0	0	4	0.00	
119	PLL2_ADV	0	0	4	0.00	
120	BUFMRCE	0	0	8	0.00	
121	BUFMRCE	0	0	72	0.00	
122	BUFR	0	0	16	0.00	
123	+-----+-----+-----+-----+-----+					
124						
125						
126	6. Specific Feature					
127	-----					
128						
129	+-----+-----+-----+-----+-----+					
130	Site Type	Used	Fixed	Available	Util%	
131	+-----+-----+-----+-----+-----+					
132	BSCAME2	0	0	4	0.00	
133	CAPTURE2	0	0	1	0.00	
134	DNA_PORT	0	0	1	0.00	
135	EFUSE_USR	0	0	1	0.00	
136	FRAME_ECCE2	0	0	1	0.00	
137	ICAPE2	0	0	2	0.00	
138	STARTUP2	0	0	1	0.00	
139	XADC	0	0	1	0.00	
140	+-----+-----+-----+-----+-----+					
141						
142						
143	7. Primitives					
144	-----					
145						
146	+-----+-----+-----+-----+-----+					
147	Ref Name	Used	Functional Category			
148	+-----+-----+-----+-----+-----+					
149	IBUF	12	IO			
150	LUT5	10	LUT			

Utilization - Synth Design - synth_1

C:/Users/Tarious/7EE705_2_2_1/7EE705_2_2_1.runs/synth_1/BarrelShifter_utilization_synth.rpt

Read-only

133	CAPTURE2	0	0	1	0.00	
134	DNA_PORT	0	0	1	0.00	
135	EFUSE_USR	0	0	1	0.00	
136	FRAME_ECCE2	0	0	1	0.00	
137	ICAPE2	0	0	2	0.00	
138	STARTUP2	0	0	1	0.00	
139	XADC	0	0	1	0.00	
140	+-----+-----+-----+-----+-----+					
141						
142						
143	7. Primitives					
144	-----					
145						
146	+-----+-----+-----+-----+-----+					
147	Ref Name	Used	Functional Category			
148	+-----+-----+-----+-----+-----+					
149	IBUF	12	IO			
150	LUT5	10	LUT			
151	OBUF	8	IO			
152	LUT6	6	LUT			
153	LUT4	4	LUT			
154	+-----+-----+-----+-----+-----+					
155						
156						
157	8. Black Boxes					
158	-----					
159						
160	+-----+-----+-----+-----+-----+					
161	Ref Name	Used				
162	+-----+-----+-----+-----+-----+					
163						
164						
165	9. Instantiated Netlists					
166	-----					
167						
168	+-----+-----+-----+-----+-----+					
169	Ref Name	Used				
170	+-----+-----+-----+-----+-----+					
171						
172						
173						