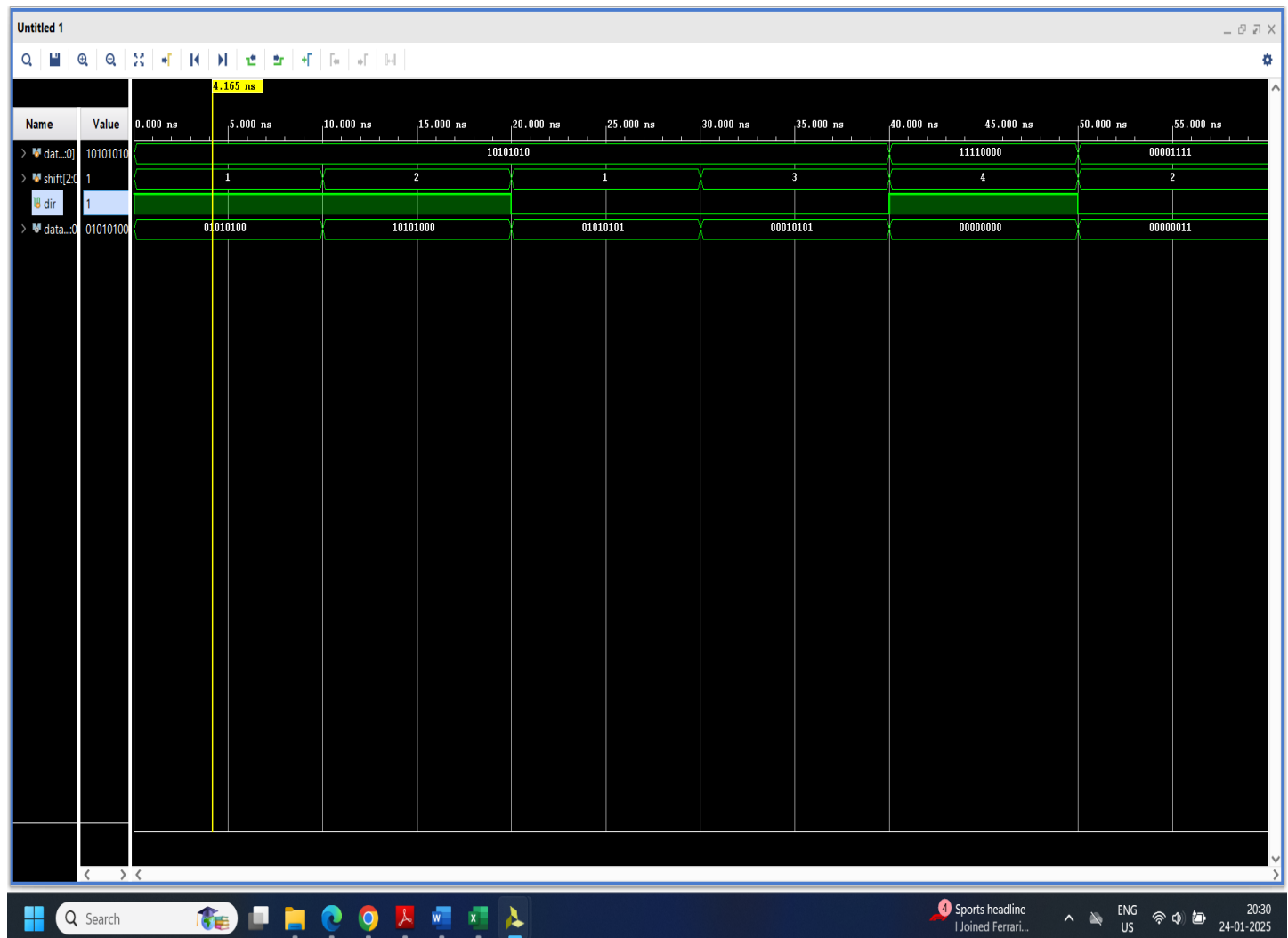


Design a 8-bit Logarithmic Barrel shifter, for performing Right and Left Shift (Logical) operation. Write a testbench and simulate the circuit

1. Using >> and << operator

Simulation Waveform using >> and << operator



Verilog Code:

```

module BarrelShifter (
    input [7:0] data_in, // Input data
    input [2:0] shift, // Shift amount (3 bits to represent 0 to 7)
    input dir, // Direction (0 for right, 1 for left)
    output [7:0] data_out // Shifted output
);

// Perform shift based on direction
assign data_out = (dir == 1'b1) ? (data_in << shift) : (data_in >> shift);

endmodule

```

Test Bench Code:

```
module TestBench;

    // Testbench signals

    reg [7:0] data_in; // Input data
    reg [2:0] shift;   // Shift amount
    reg dir;           // Shift direction (0 for right, 1 for left)
    wire [7:0] data_out; // Output data


    // Instantiate the BarrelShifter module
    BarrelShifter uut (
        .data_in(data_in),
        .shift(shift),
        .dir(dir),
        .data_out(data_out)
    );


    initial begin

        // Display header for the simulation results
        $display("Time | Data In | Shift | Dir | Data Out ");
        $display("-----");


        // Test cases

        data_in = 8'b10101010; shift = 3'b001; dir = 1'b1; #10; // Left shift by 1
        $display("%4d | %b | %d | %b | %b", $time, data_in, shift, dir, data_out);


        data_in = 8'b10101010; shift = 3'b010; dir = 1'b1; #10; // Left shift by 2
        $display("%4d | %b | %d | %b | %b", $time, data_in, shift, dir, data_out);


        data_in = 8'b10101010; shift = 3'b001; dir = 1'b0; #10; // Right shift by 1
        $display("%4d | %b | %d | %b | %b", $time, data_in, shift, dir, data_out);
```

```
data_in = 8'b10101010; shift = 3'b011; dir = 1'b0; #10; // Right shift by 3
$display("%4d | %b | %d | %b | %b", $time, data_in, shift, dir, data_out);
```

```
// Additional cases
```

```
data_in = 8'b11110000; shift = 3'b100; dir = 1'b1; #10; // Left shift by 4
$display("%4d | %b | %d | %b | %b", $time, data_in, shift, dir, data_out);
```

```
data_in = 8'b00001111; shift = 3'b010; dir = 1'b0; #10; // Right shift by 2
$display("%4d | %b | %d | %b | %b", $time, data_in, shift, dir, data_out);
```

```
// End simulation
```

```
$finish;
```

```
end
```

```
endmodule
```

Utilisation Report:

The screenshot shows the Vivado 2020.2 interface with the 'Utilization' report selected. The report is circled in red, showing the following data:

Name	Slice LUTs (53200)	Slice (13300)	LUT as Logic (53200)	Bonded IOB (125)
BarrelShifter	18	6	18	20

The report also shows the following hierarchy:

- Summary
 - Slice Logic
 - Slice LUTs (<1%)
 - LUT as Logic (<1%)
 - Slice Logic Distribution
 - Slice (<1%)
 - SliceM

Utilization - Synth Design - synth_1

C:/Users/Tarious/7EE705_2_2/7EE705_2_2.runs/synth_1/BarrelShifter_utilization_synth.rpt

Read-only

1 Copyright 1986-2020 Xilinx, Inc. All Rights Reserved.

2

3 | Tool Version : Vivado v.2020.2 (win64) Build 3064766 Wed Nov 18 09:12:45 MST 2020

4 | Date : Fri Jan 24 20:33:26 2025

5 | Host : LAPTOP-M216N101 running 64-bit major release (build 9200)

6 | Command : report_utilization -file BarrelShifter_utilization_synth.rpt -pb BarrelShifter_utilization_synth.pb

7 | Design : BarrelShifter

8 | Device : 7z020c1g400-1

9 | Design State : Synthesized

10

11

12 Utilization Design Information

13

14 Table of Contents

15 -----

16 1. Slice Logic

17 1.1 Summary of Registers by Type

18 2. Memory

19 3. DSP

20 4. IO and GT Specific

21 5. Clocking

22 6. Specific Feature

23 7. Primitives

24 8. Black Boxes

25 9. Instantiated Netlists

26

27 1. Slice Logic

28

29

30 +-----+-----+-----+-----+-----+

31 | Site Type | Used | Fixed | Available | Util% |

32 +-----+-----+-----+-----+-----+

33 | Slice LUTs* | 18 | 0 | 53200 | 0.03 |

34 | LUT as Logic | 18 | 0 | 53200 | 0.03 |

35 | LUT as Memory | 0 | 0 | 17400 | 0.00 |

36 | Slice Registers | 0 | 0 | 106400 | 0.00 |

37 | Register as Flip Flop | 0 | 0 | 106400 | 0.00 |

38 | Register as Latch | 0 | 0 | 106400 | 0.00 |

39 | F7 Muxes | 0 | 0 | 26600 | 0.00 |

40 | F8 Muxes | 0 | 0 | 13300 | 0.00 |

41 +-----+-----+-----+-----+-----+

27°C

Smoke

ENG

US

20:38

24-01-2025

Utilization - Synth Design - synth_1

C:/Users/Tarious/7EE705_2_2/7EE705_2_2.runs/synth_1/BarrelShifter_utilization_synth.rpt

Read-only

42 * Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.

43

44

45 1.1 Summary of Registers by Type

46 -----

47

48 +-----+-----+-----+-----+-----+

49 | Total | Clock Enable | Synchronous | Asynchronous |

50 +-----+-----+-----+-----+-----+

51 | 0 | - | - | - |

52 | 0 | - | - | Set |

53 | 0 | - | - | Reset |

54 | 0 | - | Set | - |

55 | 0 | - | Reset | - |

56 | 0 | Yes | - | - |

57 | 0 | Yes | - | Set |

58 | 0 | Yes | - | Reset |

59 | 0 | Yes | Set | - |

60 | 0 | Yes | Reset | - |

61 +-----+-----+-----+-----+-----+

62

63

64 2. Memory

65 -----

66

67 +-----+-----+-----+-----+-----+

68 | Site Type | Used | Fixed | Available | Util% |

69 +-----+-----+-----+-----+-----+

70 | Block RAM Tile | 0 | 0 | 140 | 0.00 |

71 | RAMB36/FIFO* | 0 | 0 | 140 | 0.00 |

72 | RAMB18 | 0 | 0 | 280 | 0.00 |

73 +-----+-----+-----+-----+-----+

74 * Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accom

75

76

77 3. DSP

78 -----

79

80 +-----+-----+-----+-----+-----+

81 | Site Type | Used | Fixed | Available | Util% |

82 +-----+-----+-----+-----+-----+

27°C

Smoke

ENG

US

20:38

24-01-2025

Utilization - Synth Design - synth_1

C:/Users/Tarios/7EE705_2_2/7EE705_2_2.runs/synth_1/BarrelShifter_utilization_synth.rpt

Read-only

77 3. DSP

78 -----

79

80 +-----+-----+-----+-----+-----+-----+

81 | Site Type | Used | Fixed | Available | Util% |

82 +-----+-----+-----+-----+-----+-----+

83 | DSPs | 0 | 0 | 220 | 0.00 |

84 +-----+-----+-----+-----+-----+-----+

85

86

87 4. IO and GT Specific

88 -----

89

90 +-----+-----+-----+-----+-----+-----+

91 | Site Type | Used | Fixed | Available | Util% |

92 +-----+-----+-----+-----+-----+-----+

93 | Bonded IOB | 20 | 0 | 125 | 16.00 |

94 | Bonded IPADs | 0 | 0 | 2 | 0.00 |

95 | Bonded IOPADs | 0 | 0 | 130 | 0.00 |

96 | PHY_CONTROL | 0 | 0 | 4 | 0.00 |

97 | PHASER_REF | 0 | 0 | 4 | 0.00 |

98 | OUT_FIFO | 0 | 0 | 16 | 0.00 |

99 | IN_FIFO | 0 | 0 | 16 | 0.00 |

100 | IDELAYCTRL | 0 | 0 | 4 | 0.00 |

101 | IBUFDS | 0 | 0 | 121 | 0.00 |

102 | PHASER_OUT/PHASER_OUT_PHY | 0 | 0 | 16 | 0.00 |

103 | PHASER_IN/PHASER_IN_PHY | 0 | 0 | 16 | 0.00 |

104 | IDELAYE2/IDELAYE2_FINEDELAY | 0 | 0 | 200 | 0.00 |

105 | ILOGIC | 0 | 0 | 125 | 0.00 |

106 | OLOGIC | 0 | 0 | 125 | 0.00 |

107 +-----+-----+-----+-----+-----+-----+

108

109

110 5. Clocking

111 -----

112

113 +-----+-----+-----+-----+-----+-----+

114 | Site Type | Used | Fixed | Available | Util% |

115 +-----+-----+-----+-----+-----+-----+

116 | BUFGCTRL | 0 | 0 | 32 | 0.00 |

117 | BUFIO | 0 | 0 | 16 | 0.00 |

27°C

Smoke

ENG

US

20:39

24-01-2025

Utilization - Synth Design - synth_1

C:/Users/Tarios/7EE705_2_2/7EE705_2_2.runs/synth_1/BarrelShifter_utilization_synth.rpt

Read-only

110 5. Clocking

111 -----

112

113 +-----+-----+-----+-----+-----+-----+

114 | Site Type | Used | Fixed | Available | Util% |

115 +-----+-----+-----+-----+-----+-----+

116 | BUFGCTRL | 0 | 0 | 32 | 0.00 |

117 | BUFIO | 0 | 0 | 16 | 0.00 |

118 | MMCME2_ADV | 0 | 0 | 4 | 0.00 |

119 | PLLE2_ADV | 0 | 0 | 4 | 0.00 |

120 | BUFMRCE | 0 | 0 | 8 | 0.00 |

121 | BUFHCE | 0 | 0 | 72 | 0.00 |

122 | BUFR | 0 | 0 | 16 | 0.00 |

123 +-----+-----+-----+-----+-----+-----+

124

125

126 6. Specific Feature

127 -----

128

129 +-----+-----+-----+-----+-----+-----+

130 | Site Type | Used | Fixed | Available | Util% |

131 +-----+-----+-----+-----+-----+-----+

132 | BSCANE2 | 0 | 0 | 4 | 0.00 |

133 | CAPTUREE2 | 0 | 0 | 1 | 0.00 |

134 | DNA_PORT | 0 | 0 | 1 | 0.00 |

135 | EFUSE_USR | 0 | 0 | 1 | 0.00 |

136 | FRAME_EOC2 | 0 | 0 | 1 | 0.00 |

137 | ICAPE2 | 0 | 0 | 2 | 0.00 |

138 | STARTUPE2 | 0 | 0 | 1 | 0.00 |

139 | XADC | 0 | 0 | 1 | 0.00 |

140 +-----+-----+-----+-----+-----+-----+

141

142

143 7. Primitives

144 -----

145

146 +-----+-----+-----+-----+-----+-----+

147 | Ref Name | Used | Functional Category |

148 +-----+-----+-----+-----+-----+-----+

149 | IBUF | 12 | IO |

150 | LUT6 | 10 | LUT |

27°C

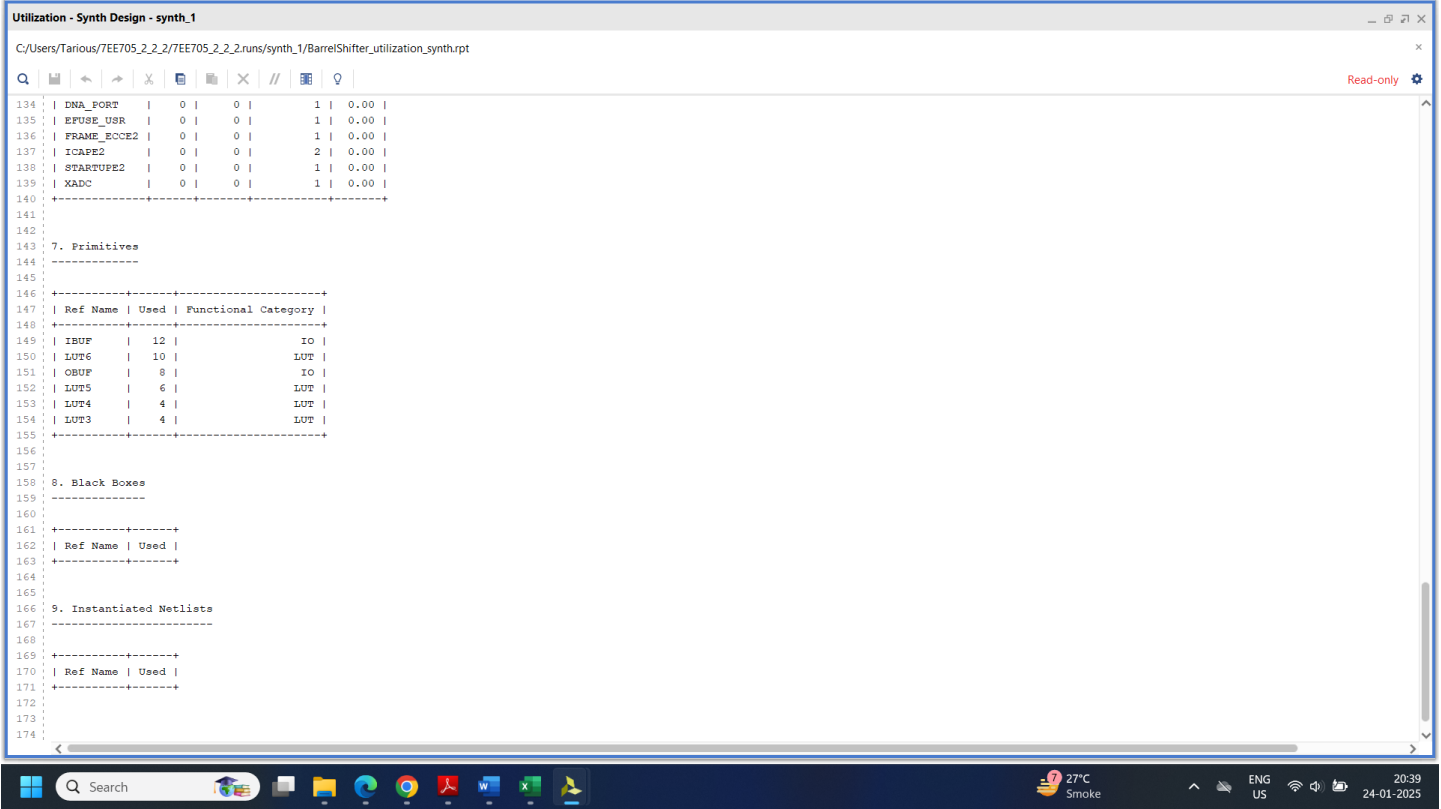
Smoke

ENG

US

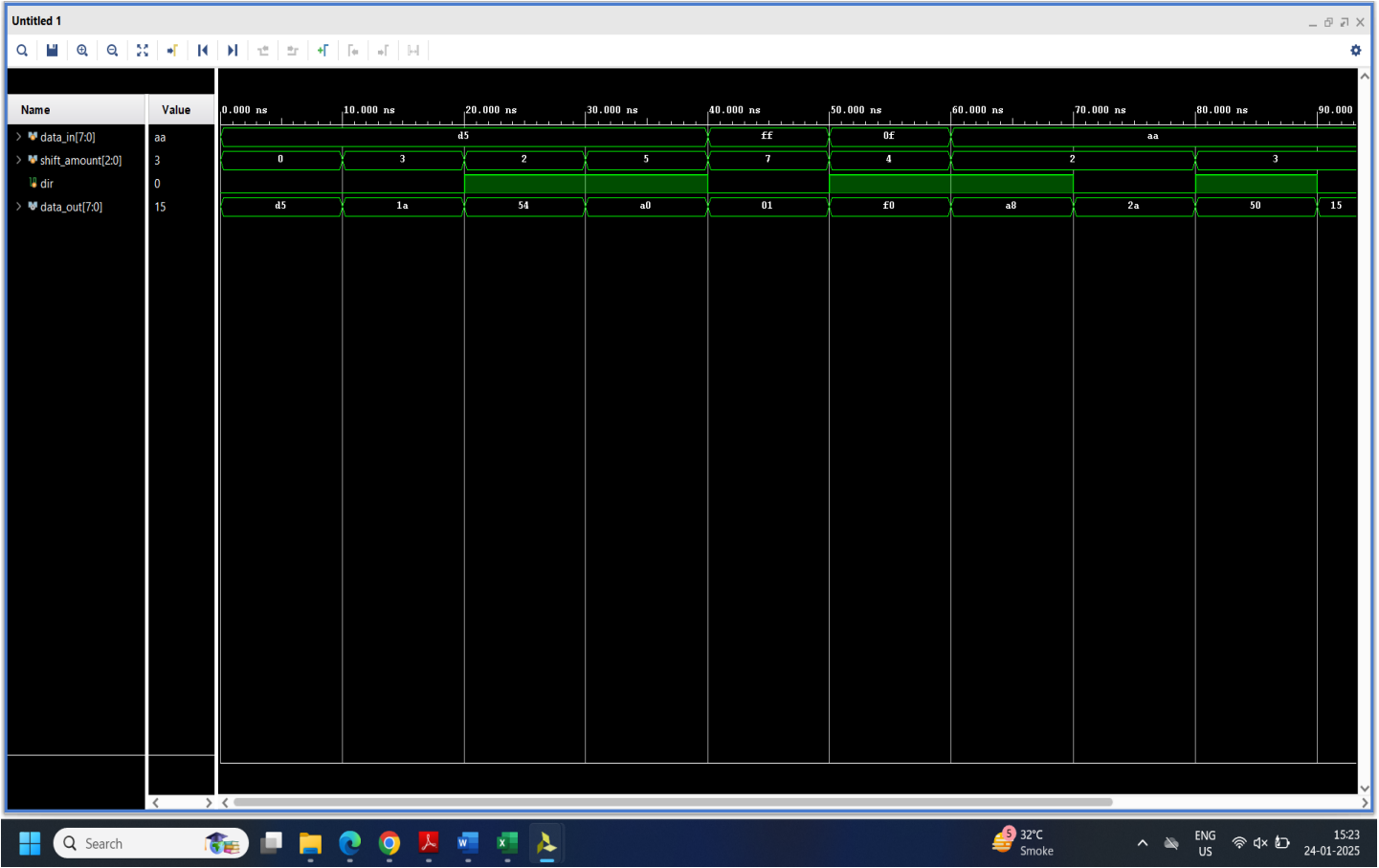
20:39

24-01-2025



Using Logarithmic Barrel shifter

Simulation Waveform Using Logarithmic Barrel shifter



Verilog Code:

```
// 8-bit Logarithmic Barrel Shifter
```

```
module BarrelShifter (  
    input [7:0] data_in,    // Input data  
    input [2:0] shift_amount, // Shift amount (3 bits for up to 7 shifts)  
    input dir,              // Direction: 0 for logical right, 1 for logical left  
    output [7:0] data_out   // Shifted output  
);  
    wire [7:0] stage1, stage2, stage3;  
  
    // Stage 1: Shift by 1 position (if shift_amount[0] == 1)  
    assign stage1 = shift_amount[0] ? (dir ? {data_in[6:0], 1'b0} : {1'b0, data_in[7:1]}) : data_in;  
  
    // Stage 2: Shift by 2 positions (if shift_amount[1] == 1)  
    assign stage2 = shift_amount[1] ? (dir ? {stage1[5:0], 2'b00} : {2'b00, stage1[7:2]}) : stage1;  
  
    // Stage 3: Shift by 4 positions (if shift_amount[2] == 1)  
    assign stage3 = shift_amount[2] ? (dir ? {stage2[3:0], 4'b0000} : {4'b0000, stage2[7:4]}) :  
    stage2;  
  
    // Final output  
    assign data_out = stage3;  
endmodule
```

Test Bench Code:

```
module Testbench;  
    reg [7:0] data_in;  
    reg [2:0] shift_amount;  
    reg dir;  
    wire [7:0] data_out;  
  
    // Instantiate the BarrelShifter module
```

```
BarrelShifter uut (  
    .data_in(data_in),  
    .shift_amount(shift_amount),  
    .dir(dir),  
    .data_out(data_out)  
);  
  
initial begin  
    // Test cases  
  
    $monitor("Time = %0t | data_in = %b | shift_amount = %d | dir = %b | data_out = %b",  
$time, data_in, shift_amount, dir, data_out);  
  
    // Test case 1: Logical right shift by 0  
    data_in = 8'b11010101; shift_amount = 3'b000; dir = 0; #10;  
  
    // Test case 2: Logical right shift by 3  
    data_in = 8'b11010101; shift_amount = 3'b011; dir = 0; #10;  
  
    // Test case 3: Logical left shift by 2  
    data_in = 8'b11010101; shift_amount = 3'b010; dir = 1; #10;  
  
    // Test case 4: Logical left shift by 5  
    data_in = 8'b11010101; shift_amount = 3'b101; dir = 1; #10;  
  
    // Test case 5: Logical right shift by 7  
    data_in = 8'b11111111; shift_amount = 3'b111; dir = 0; #10;  
  
    // Test case 6: Logical left shift by 4  
    data_in = 8'b00001111; shift_amount = 3'b100; dir = 1; #10;  
  
    // Test case 7: Logical left shift by 2  
    data_in = 8'b10101010; shift_amount = 3'b010; dir = 1; #10;
```



```
// Test case 8: Logical right shift by 2
```

```
data_in = 8'b10101010; shift_amount = 3'b010; dir = 0; #10;
```

```
// Test case 9: Logical left shift by 3
```

```
data_in = 8'b10101010; shift_amount = 3'b011; dir = 1; #10;
```

```
// Test case 10: Logical right shift by 3
```

```
data_in = 8'b10101010; shift_amount = 3'b011; dir = 0; #10;
```

```
$finish;
```

```
end
```

```
endmodule
```

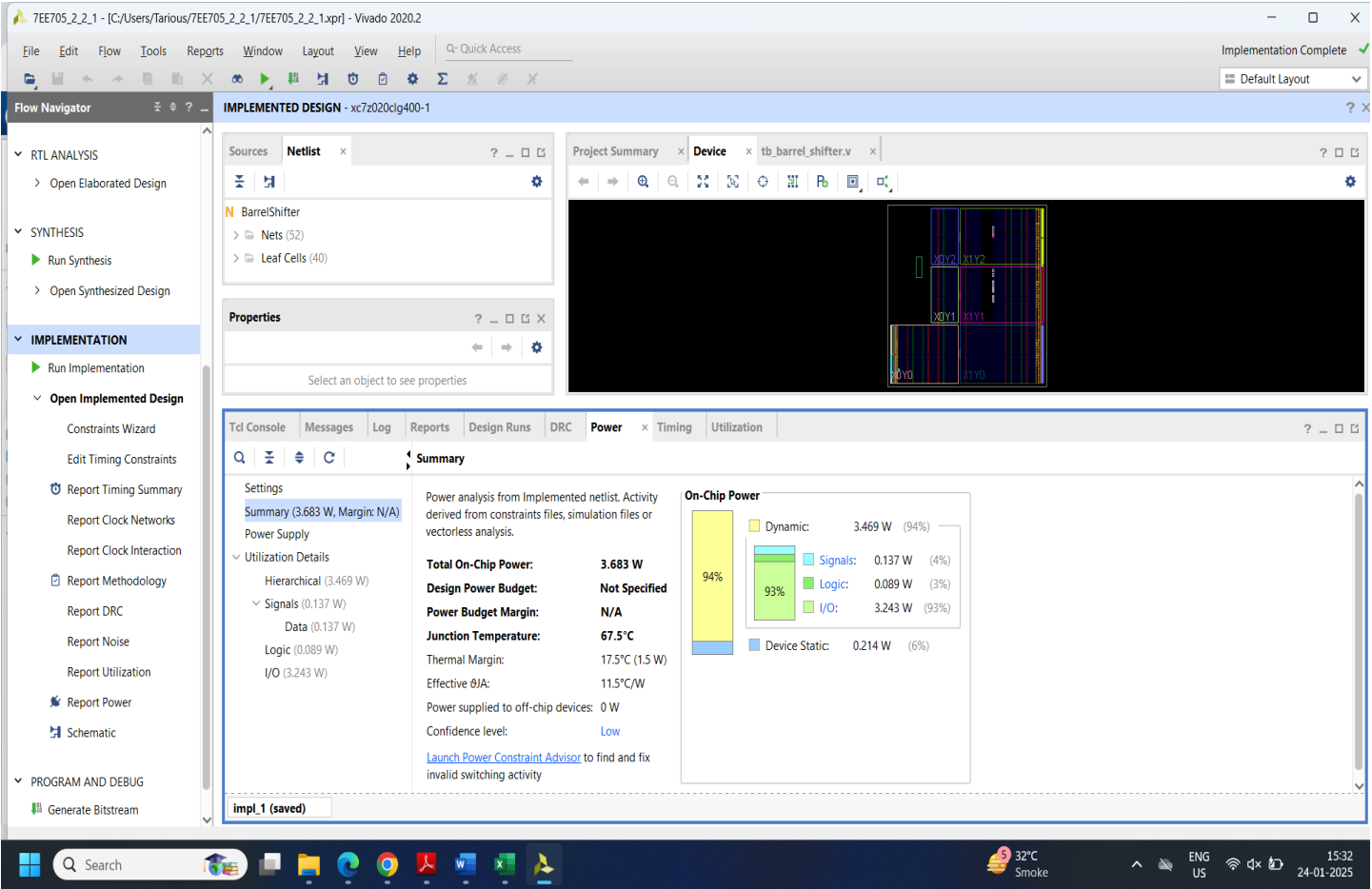
Report Utilisation:

The screenshot displays the Vivado 2020.2 interface with the 'IMPLEMENTED DESIGN' tab selected. The 'Utilization' report is open, showing the resource usage for the 'BarrelShifter' design. The report is circled in red, highlighting the following data:

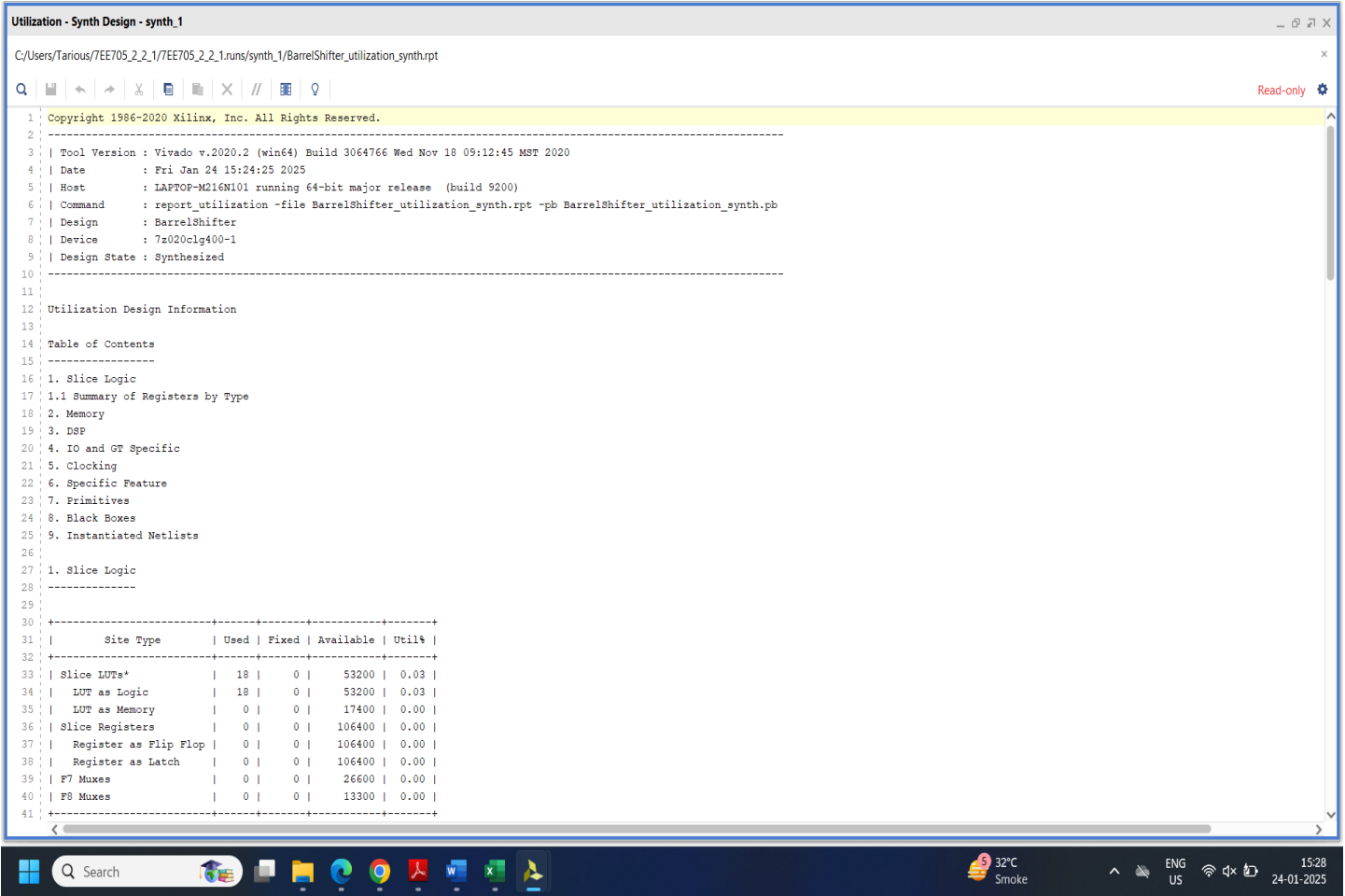
Name	Slice LUTs (53200)	Slice (13300)	LUT as Logic (53200)	Bonded IOB (125)
BarrelShifter	18	6	18	20

The 'Flow Navigator' on the left shows the project hierarchy, including 'RTL ANALYSIS', 'SYNTHESIS', and 'IMPLEMENTATION'. The 'IMPLEMENTATION' section is expanded, showing 'Run Implementation' and 'Open Implemented Design'. The 'Properties' panel on the right is empty, and the 'Tcl Console' at the bottom shows the command 'Generate Bitstream'.

Power Consumption:



Resource Utilisation Report:



Utilization - Synth Design - synth_1

C:/Users/Tarious/7EE705_2_2_1/7EE705_2_2_1.runs/synth_1/BarrelShifter_utilization_synth.rpt

Q

Read-only

42

* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.

43

44

45

1.1 Summary of Registers by Type

46

47

-----+-----+-----+-----+-----

48

| Total | Clock Enable | Synchronous | Asynchronous |

49

-----+-----+-----+-----+-----

50

| 0 | | | |

51

| 0 | | | |

52

| 0 | | | |

53

| 0 | | | |

54

| 0 | | | |

55

| 0 | | | |

56

| 0 | | | |

57

| 0 | | | |

58

| 0 | | | |

59

| 0 | | | |

60

| 0 | | | |

61

-----+-----+-----+-----+-----

62

63

64

2. Memory

65

66

-----+-----+-----+-----+-----

67

| Site Type | Used | Fixed | Available | Util% |

68

-----+-----+-----+-----+-----

69

| Block RAM Tile | 0 | 0 | 140 | 0.00 |

70

| RAMB36/FIFO* | 0 | 0 | 140 | 0.00 |

71

| RAMB18 | 0 | 0 | 280 | 0.00 |

72

-----+-----+-----+-----+-----

73

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accom

74

75

76

77

3. DSP

78

79

-----+-----+-----+-----+-----

80

| Site Type | Used | Fixed | Available | Util% |

81

-----+-----+-----+-----+-----

82

| DSPs | 0 | 0 | 220 | 0.00 |

83

-----+-----+-----+-----+-----

84

85

86

87

4. IO and GT Specific

88

89

-----+-----+-----+-----+-----

90

| Site Type | Used | Fixed | Available | Util% |

91

-----+-----+-----+-----+-----

92

| Bonded IOB | 20 | 0 | 125 | 16.00 |

93

| Bonded IPADs | 0 | 0 | 2 | 0.00 |

94

| Bonded IOPADs | 0 | 0 | 130 | 0.00 |

95

| PHY_CONTROL | 0 | 0 | 4 | 0.00 |

96

| PHASER_REF | 0 | 0 | 4 | 0.00 |

97

| OUT_FIFO | 0 | 0 | 16 | 0.00 |

98

| IN_FIFO | 0 | 0 | 16 | 0.00 |

99

| IDELAYCTRL | 0 | 0 | 4 | 0.00 |

100

| IBUFDS | 0 | 0 | 121 | 0.00 |

101

| PHASER_OUT/PHASER_OUT_PHY | 0 | 0 | 16 | 0.00 |

102

| PHASER_IN/PHASER_IN_PHY | 0 | 0 | 16 | 0.00 |

103

| IDELAY2/IDELAY2_FINEDELAY | 0 | 0 | 200 | 0.00 |

104

| ILOGIC | 0 | 0 | 125 | 0.00 |

105

| CLOGIC | 0 | 0 | 125 | 0.00 |

106

-----+-----+-----+-----+-----

107

108

109

110

5. Clocking

111

112

-----+-----+-----+-----+-----

113

| Site Type | Used | Fixed | Available | Util% |

114

-----+-----+-----+-----+-----

115

| BUFGCTRL | 0 | 0 | 32 | 0.00 |

116

| BUFGIO | 0 | 0 | 16 | 0.00 |

117

-----+-----+-----+-----+-----

Utilization - Synth Design - synth_1

C:/Users/Tarious/7EE705_2_2_1/7EE705_2_2_1.runs/synth_1/BarrelShifter_utilization_synth.rpt

Q

Read-only

77

3. DSP

78

79

-----+-----+-----+-----+-----

80

| Site Type | Used | Fixed | Available | Util% |

81

-----+-----+-----+-----+-----

82

| DSPs | 0 | 0 | 220 | 0.00 |

83

-----+-----+-----+-----+-----

84

85

86

87

4. IO and GT Specific

88

89

-----+-----+-----+-----+-----

90

| Site Type | Used | Fixed | Available | Util% |

91

-----+-----+-----+-----+-----

92

| Bonded IOB | 20 | 0 | 125 | 16.00 |

93

| Bonded IPADs | 0 | 0 | 2 | 0.00 |

94

| Bonded IOPADs | 0 | 0 | 130 | 0.00 |

95

| PHY_CONTROL | 0 | 0 | 4 | 0.00 |

96

| PHASER_REF | 0 | 0 | 4 | 0.00 |

97

| OUT_FIFO | 0 | 0 | 16 | 0.00 |

98

| IN_FIFO | 0 | 0 | 16 | 0.00 |

99

| IDELAYCTRL | 0 | 0 | 4 | 0.00 |

100

| IBUFDS | 0 | 0 | 121 | 0.00 |

101

| PHASER_OUT/PHASER_OUT_PHY | 0 | 0 | 16 | 0.00 |

102

| PHASER_IN/PHASER_IN_PHY | 0 | 0 | 16 | 0.00 |

103

| IDELAY2/IDELAY2_FINEDELAY | 0 | 0 | 200 | 0.00 |

104

| ILOGIC | 0 | 0 | 125 | 0.00 |

105

| CLOGIC | 0 | 0 | 125 | 0.00 |

106

-----+-----+-----+-----+-----

107

108

109

110

5. Clocking

111

112

-----+-----+-----+-----+-----

113

| Site Type | Used | Fixed | Available | Util% |

114

-----+-----+-----+-----+-----

115

| BUFGCTRL | 0 | 0 | 32 | 0.00 |

116

| BUFGIO | 0 | 0 | 16 | 0.00 |

117

-----+-----+-----+-----+-----

Utilization - Synth Design - synth_1

C:/Users/Tarios/7EE705_2_2_1/7EE705_2_2_1.runs/synth_1/BarrelShifter_utilization_synthrpt

Q

Read-only

110

5. Clocking

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126

6. Specific Feature

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142

143

7. Primitives

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150

	Site Type	Used	Fixed	Available	Util%
BUFGCTRL		0	0	32	0.00
BUFIO		0	0	16	0.00
MMCME2_ADV		0	0	4	0.00
PLL2_ADV		0	0	4	0.00
BUFMACE		0	0	8	0.00
BUFHCE		0	0	72	0.00
BUFR		0	0	16	0.00

	Site Type	Used	Fixed	Available	Util%
BSCANE2		0	0	4	0.00
CAPTUREE2		0	0	1	0.00
DNA_FORT		0	0	1	0.00
EFUSE_USR		0	0	1	0.00
FRAME_ECCE2		0	0	1	0.00
ICAPE2		0	0	2	0.00
STARTUPE2		0	0	1	0.00
XADC		0	0	1	0.00

Ref Name	Used	Functional Category
IBUF	12	IO
LUT5	10	LUT

Windows taskbar with search, icons, and system tray (32°C, Smoke, ENG US, 15:30, 24-01-2025)

Utilization - Synth Design - synth_1

C:/Users/Tarios/7EE705_2_2_1/7EE705_2_2_1.runs/synth_1/BarrelShifter_utilization_synthrpt

Q

Read-only

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7. Primitives

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8. Black Boxes

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165

9. Instantiated Netlists

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169

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172

173

Ref Name	Used	Functional Category
IBUF	12	IO
LUT5	10	LUT
OBUF	8	IO
LUT6	6	LUT
LUT4	4	LUT

Ref Name	Used
----------	------

Windows taskbar with search, icons, and system tray (32°C, Smoke, ENG US, 15:30, 24-01-2025)