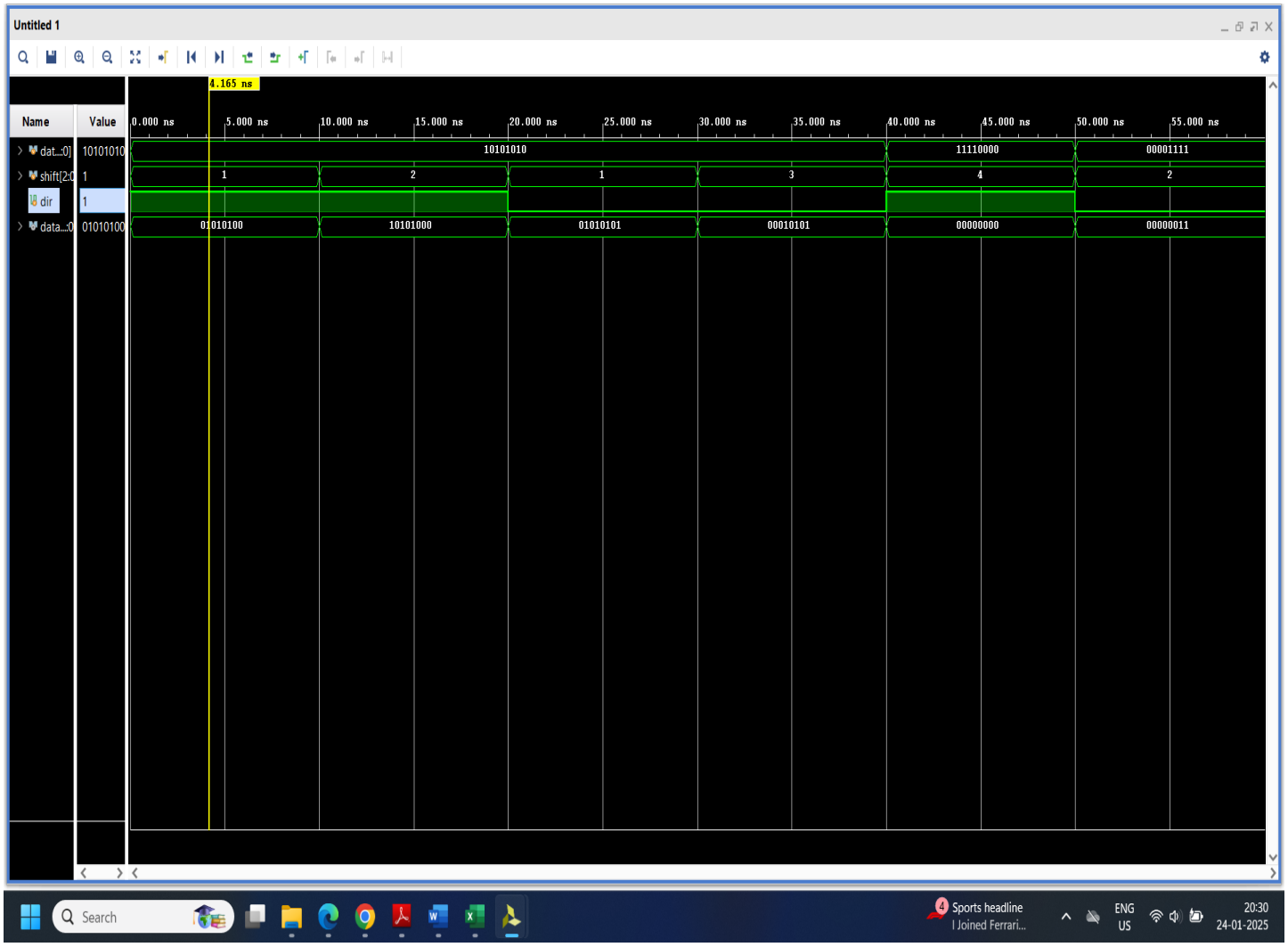
Design a 8-bit Logarithmic Barrel shifter, for performing Right and Left Shift (Logical) operation. Write a testbench and simulate the circuit

1.Using >> and << operator

Simulation Waveform using >> and << operator



Verilog Code:

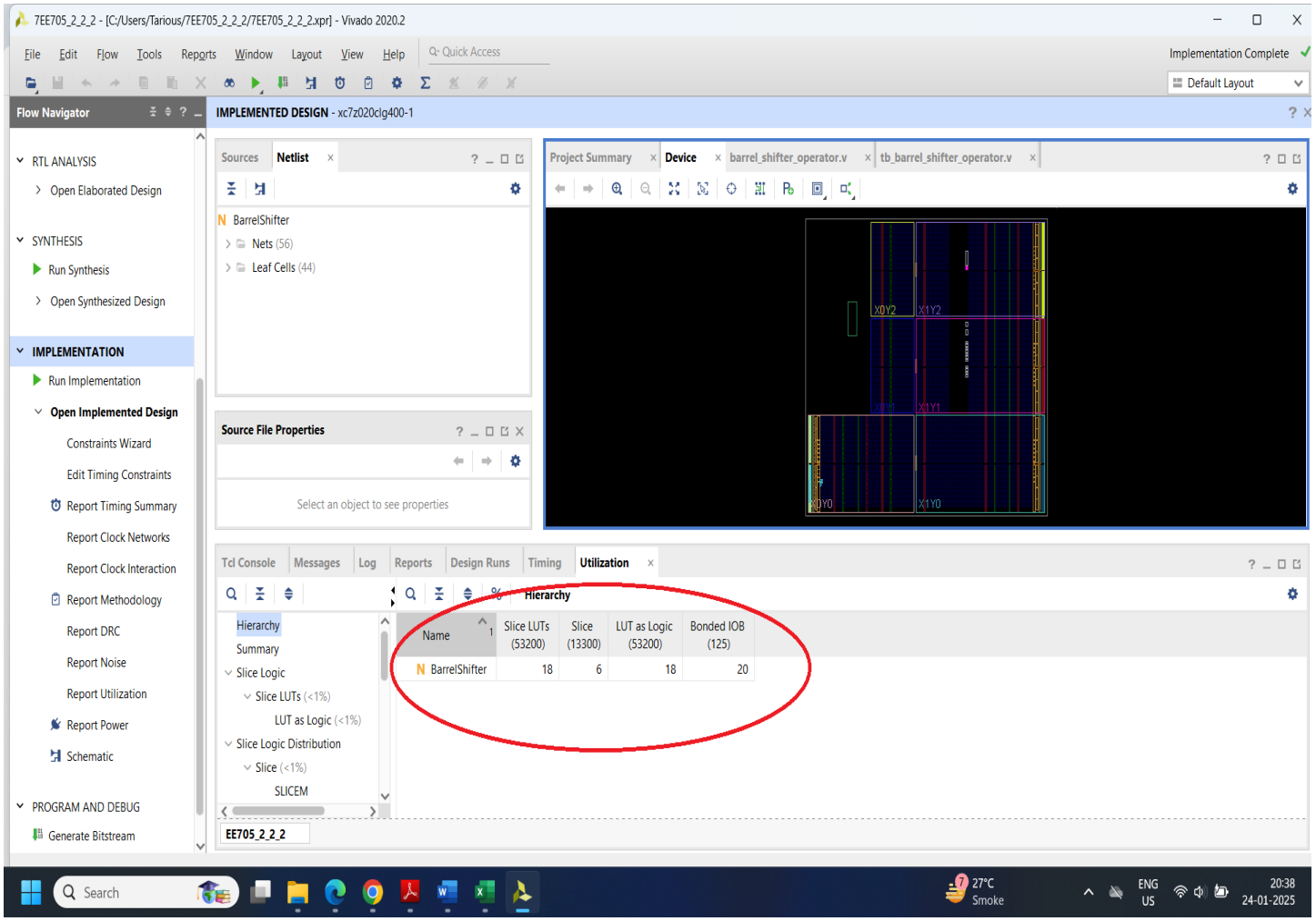
```
module BarrelShifter (
    input [7:0] data_in, // Input data
    input [2:0] shift,   // Shift amount (3 bits to represent 0 to 7)
    input dir,           // Direction (0 for right, 1 for left)
    output [7:0] data_out // Shifted output
);
    // Perform shift based on direction
    assign data_out = (dir == 1'b1) ? (data_in << shift) : (data_in >> shift);
endmodule
```

Test Bench Code:

```
module TestBench;
    // Testbench signals
    reg [7:0] data_in;  // Input data
    reg [2:0] shift;    // Shift amount
    reg dir;            // Shift direction (0 for right, 1 for left)
    wire [7:0] data_out; // Output data

    // Instantiate the BarrelShifter module
    BarrelShifter uut (
        .data_in(data_in),
        .shift(shift),
        .dir(dir),
        .data_out(data_out)
    );

    initial begin
        // Display header for the simulation results
        $display("Time | Data In   | Shift | Dir | Data Out ");
        $display("---------------------------------------");

        // Test cases
        data_in = 8'b10101010; shift = 3'b001; dir = 1'b1; #10; // Left shift by 1
        $display("%4d | %b |   %d   |  %b  | %b", $time, data_in, shift, dir, data_out);

        data_in = 8'b10101010; shift = 3'b010; dir = 1'b1; #10; // Left shift by 2
        $display("%4d | %b |   %d   |  %b  | %b", $time, data_in, shift, dir, data_out);

        data_in = 8'b10101010; shift = 3'b001; dir = 1'b0; #10; // Right shift by 1
        $display("%4d | %b |   %d   |  %b  | %b", $time, data_in, shift, dir, data_out);
```

```
        data_in = 8'b10101010; shift = 3'b011; dir = 1'b0; #10; // Right shift by 3
        $display("%4d | %b |   %d   | %b  | %b", $time, data_in, shift, dir, data_out);

        // Additional cases
        data_in = 8'b11110000; shift = 3'b100; dir = 1'b1; #10; // Left shift by 4
        $display("%4d | %b |   %d   | %b  | %b", $time, data_in, shift, dir, data_out);

        data_in = 8'b00001111; shift = 3'b010; dir = 1'b0; #10; // Right shift by 2
        $display("%4d | %b |   %d   | %b  | %b", $time, data_in, shift, dir, data_out);

        // End simulation
        $finish;
    end
endmodule
```

Utilisation Report:



Resource Utilisation Report:

Utilization - Synth Design - synth_1

C:/Users/Tarious/7EE705_2_2_2/7EE705_2_2_2.runs/synth_1/BarrelShifter_utilization_synth.rpt

Read-only

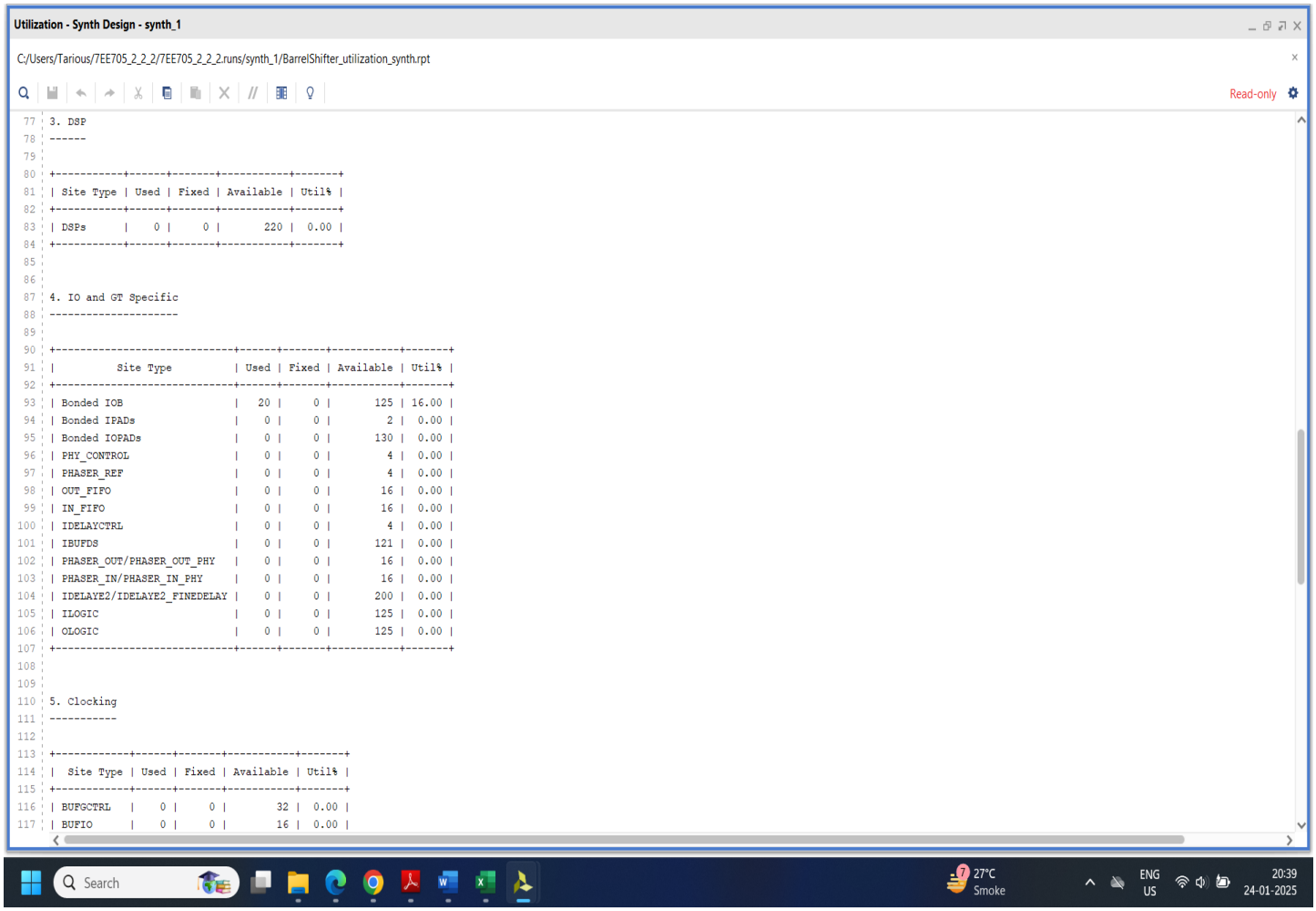
```
Copyright 1986-2020 Xilinx, Inc. All Rights Reserved.
----------------------------------------------------------------------------------------------------------------------------
| Tool Version : Vivado v.2020.2 (win64) Build 3064766 Wed Nov 18 09:12:45 MST 2020
| Date         : Fri Jan 24 20:33:26 2025
| Host         : LAPTOP-M216N101 running 64-bit major release  (build 9200)
| Command      : report_utilization -file BarrelShifter_utilization_synth.rpt -pb BarrelShifter_utilization_synth.pb
| Design       : BarrelShifter
| Device       : 7z020clg400-1
| Design State : Synthesized
----------------------------------------------------------------------------------------------------------------------------

Utilization Design Information

Table of Contents
-----------------
1. Slice Logic
1.1 Summary of Registers by Type
2. Memory
3. DSP
4. IO and GT Specific
5. Clocking
6. Specific Feature
7. Primitives
8. Black Boxes
9. Instantiated Netlists

1. Slice Logic
--------------

+-------------------------+------+-------+-----------+-------+
|        Site Type        | Used | Fixed | Available | Util% |
+-------------------------+------+-------+-----------+-------+
| Slice LUTs*             |   18 |     0 |     53200 |  0.03 |
|   LUT as Logic          |   18 |     0 |     53200 |  0.03 |
|   LUT as Memory         |    0 |     0 |     17400 |  0.00 |
| Slice Registers         |    0 |     0 |    106400 |  0.00 |
|   Register as Flip Flop |    0 |     0 |    106400 |  0.00 |
|   Register as Latch     |    0 |     0 |    106400 |  0.00 |
| F7 Muxes                |    0 |     0 |     26600 |  0.00 |
| F8 Muxes                |    0 |     0 |     13300 |  0.00 |
+-------------------------+------+-------+-----------+-------+
```

Utilization - Synth Design - synth_1

C:/Users/Tarious/7EE705_2_2_2/7EE705_2_2_2.runs/synth_1/BarrelShifter_utilization_synth.rpt

Read-only

```
* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.


1.1 Summary of Registers by Type
--------------------------------

+-------+--------------+-------------+--------------+
| Total | Clock Enable | Synchronous | Asynchronous |
+-------+--------------+-------------+--------------+
| 0     |            _ |           - |            - |
| 0     |            _ |           - |          Set |
| 0     |            _ |           - |        Reset |
| 0     |            _ |         Set |            - |
| 0     |            _ |       Reset |            - |
| 0     |          Yes |           - |            - |
| 0     |          Yes |           - |          Set |
| 0     |          Yes |           - |        Reset |
| 0     |          Yes |         Set |            - |
| 0     |          Yes |       Reset |            - |
+-------+--------------+-------------+--------------+


2. Memory
---------

+----------------+------+-------+-----------+-------+
|    Site Type   | Used | Fixed | Available | Util% |
+----------------+------+-------+-----------+-------+
| Block RAM Tile |    0 |     0 |       140 |  0.00 |
|   RAMB36/FIFO* |    0 |     0 |       140 |  0.00 |
|   RAMB18       |    0 |     0 |       280 |  0.00 |
+----------------+------+-------+-----------+-------+
* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accomm


3. DSP
------

+-----------+------+-------+-----------+-------+
| Site Type | Used | Fixed | Available | Util% |
+-----------+------+-------+-----------+-------+
```

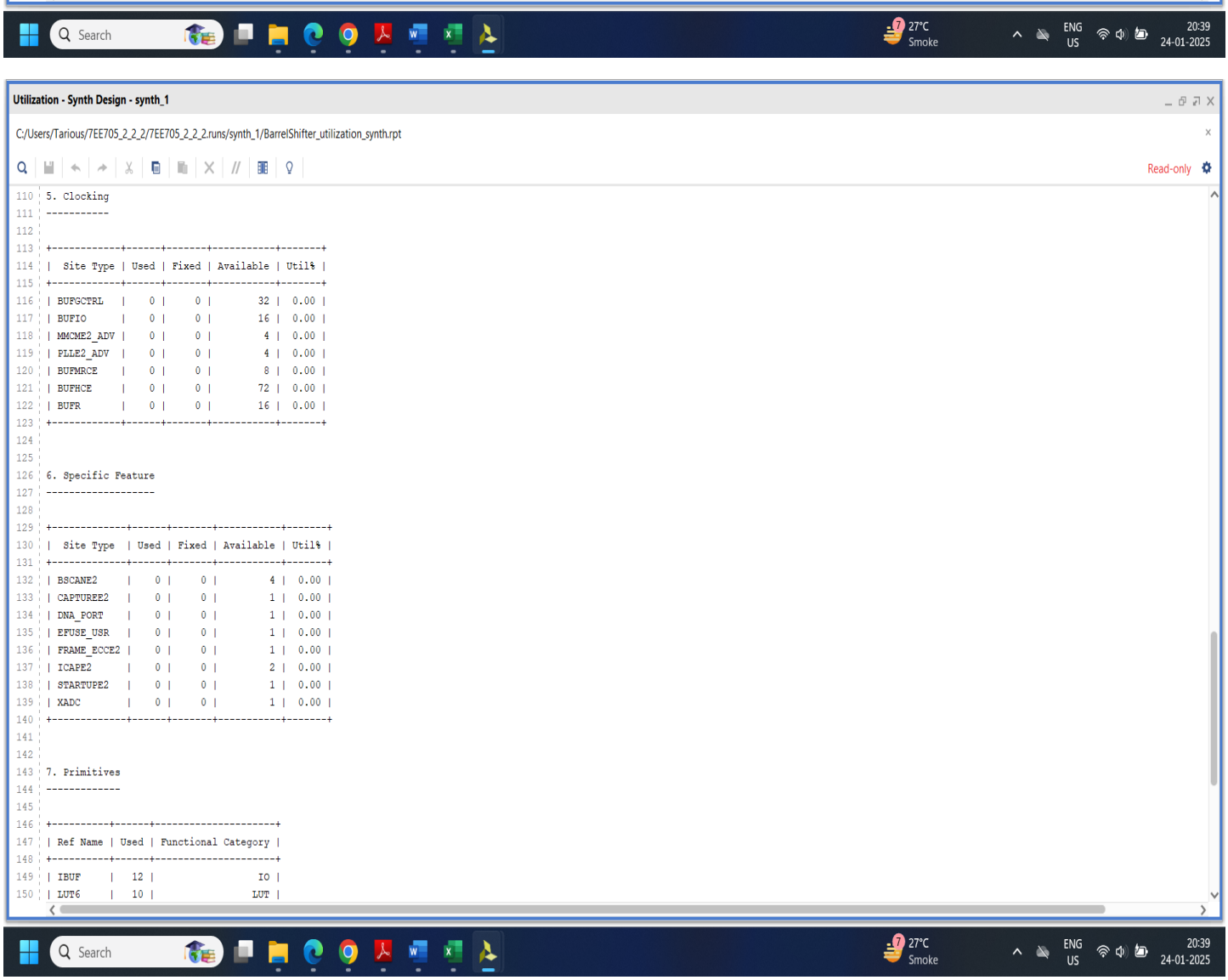


Utilization - Synth Design - synth_1

C:/Users/Tarious/7EE705_2_2_2/7EE705_2_2_2.runs/synth_1/BarrelShifter_utilization_synth.rpt

Read-only

```
3. DSP
------

+-----------+------+-------+-----------+-------+
| Site Type | Used | Fixed | Available | Util% |
+-----------+------+-------+-----------+-------+
| DSPs      |    0 |     0 |       220 |  0.00 |
+-----------+------+-------+-----------+-------+


4. IO and GT Specific
---------------------

+-----------------------------+------+-------+-----------+-------+
|          Site Type          | Used | Fixed | Available | Util% |
+-----------------------------+------+-------+-----------+-------+
| Bonded IOB                  |   20 |     0 |       125 | 16.00 |
| Bonded IPADs                |    0 |     0 |         2 |  0.00 |
| Bonded IOPADs               |    0 |     0 |       130 |  0.00 |
| PHY_CONTROL                 |    0 |     0 |         4 |  0.00 |
| PHASER_REF                  |    0 |     0 |         4 |  0.00 |
| OUT_FIFO                    |    0 |     0 |        16 |  0.00 |
| IN_FIFO                     |    0 |     0 |        16 |  0.00 |
| IDELAYCTRL                  |    0 |     0 |         4 |  0.00 |
| IBUFDS                      |    0 |     0 |       121 |  0.00 |
| PHASER_OUT/PHASER_OUT_PHY   |    0 |     0 |        16 |  0.00 |
| PHASER_IN/PHASER_IN_PHY     |    0 |     0 |        16 |  0.00 |
| IDELAYE2/IDELAYE2_FINEDELAY |    0 |     0 |       200 |  0.00 |
| ILOGIC                      |    0 |     0 |       125 |  0.00 |
| OLOGIC                      |    0 |     0 |       125 |  0.00 |
+-----------------------------+------+-------+-----------+-------+


5. Clocking
-----------

+------------+------+-------+-----------+-------+
|  Site Type | Used | Fixed | Available | Util% |
+------------+------+-------+-----------+-------+
| BUFGCTRL   |    0 |     0 |        32 |  0.00 |
| BUFIO      |    0 |     0 |        16 |  0.00 |
```

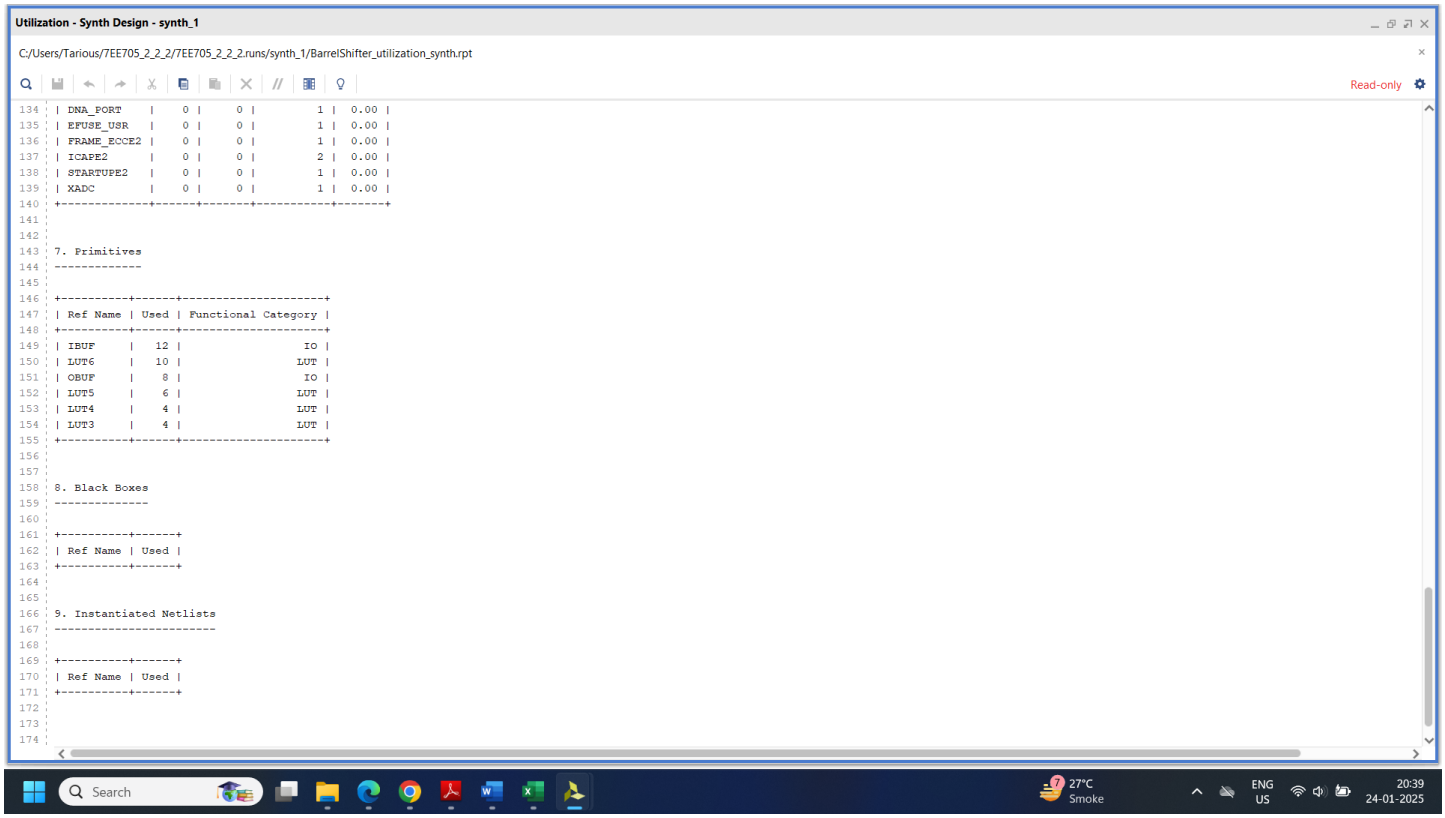


Utilization - Synth Design - synth_1

C:/Users/Tarious/7EE705_2_2_2/7EE705_2_2_2.runs/synth_1/BarrelShifter_utilization_synth.rpt

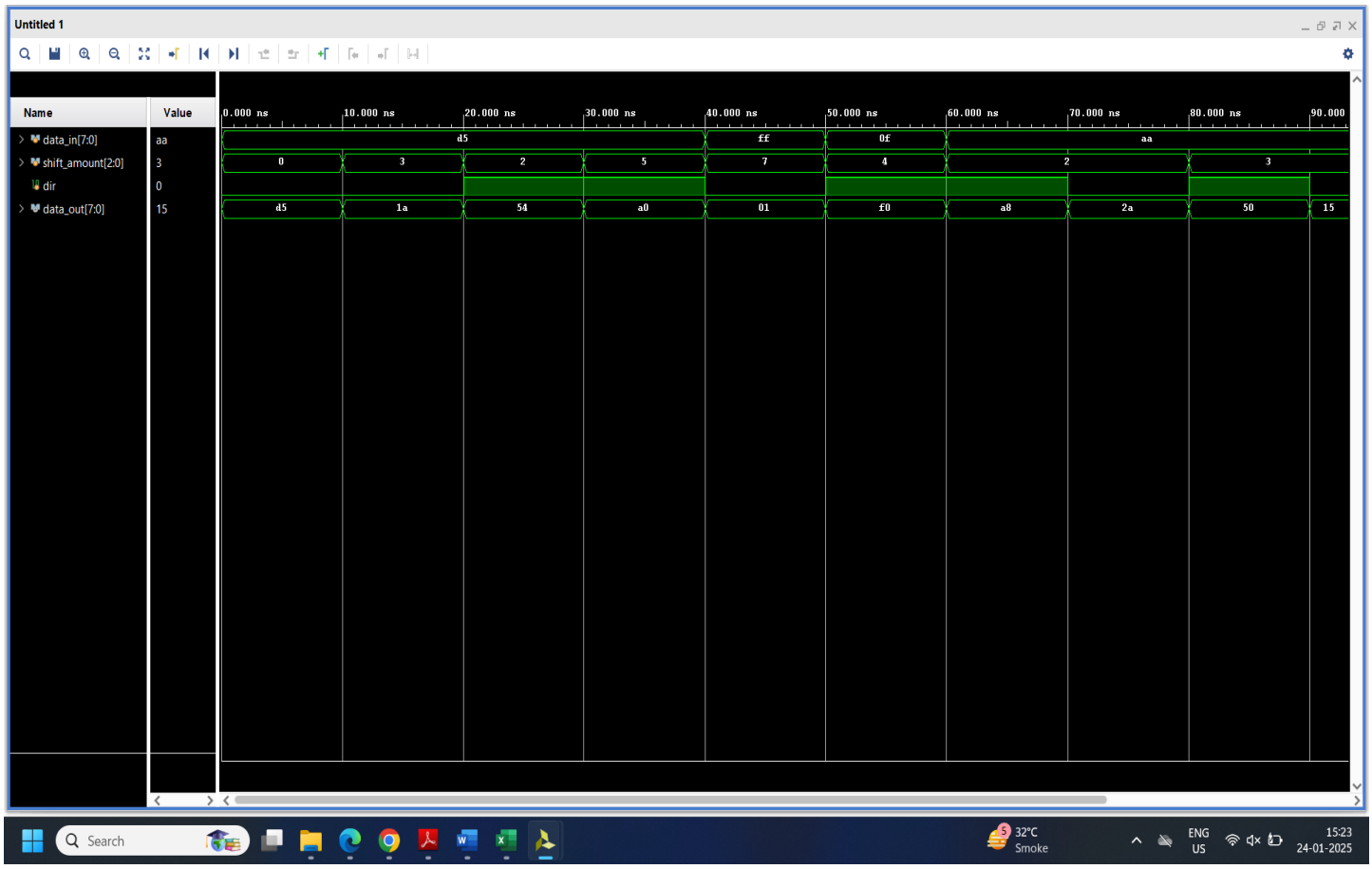
Read-only

```
5. Clocking
-----------

+------------+------+-------+-----------+-------+
|  Site Type | Used | Fixed | Available | Util% |
+------------+------+-------+-----------+-------+
| BUFGCTRL   |    0 |     0 |        32 |  0.00 |
| BUFIO      |    0 |     0 |        16 |  0.00 |
| MMCME2_ADV |    0 |     0 |         4 |  0.00 |
| PLLE2_ADV  |    0 |     0 |         4 |  0.00 |
| BUFMRCE    |    0 |     0 |         8 |  0.00 |
| BUFHCE     |    0 |     0 |        72 |  0.00 |
| BUFR       |    0 |     0 |        16 |  0.00 |
+------------+------+-------+-----------+-------+


6. Specific Feature
-------------------

+-------------+------+-------+-----------+-------+
|  Site Type  | Used | Fixed | Available | Util% |
+-------------+------+-------+-----------+-------+
| BSCANE2     |    0 |     0 |         4 |  0.00 |
| CAPTUREE2   |    0 |     0 |         1 |  0.00 |
| DNA_PORT    |    0 |     0 |         1 |  0.00 |
| EFUSE_USR   |    0 |     0 |         1 |  0.00 |
| FRAME_ECCE2 |    0 |     0 |         1 |  0.00 |
| ICAPE2      |    0 |     0 |         2 |  0.00 |
| STARTUPE2   |    0 |     0 |         1 |  0.00 |
| XADC        |    0 |     0 |         1 |  0.00 |
+-------------+------+-------+-----------+-------+


7. Primitives
-------------

+----------+------+---------------------+
| Ref Name | Used | Functional Category |
+----------+------+---------------------+
| IBUF     |   12 |                  IO |
| LUT6     |   10 |                 LUT |
```



Using Logarithmic Barrel shifter

Simulation Waveform Using Logarithmic Barrel shifter



Verilog Code:

```
// 8-bit Logarithmic Barrel Shifter
module BarrelShifter (
    input [7:0] data_in,       // Input data
    input [2:0] shift_amount,  // Shift amount (3 bits for up to 7 shifts)
    input dir,                 // Direction: 0 for logical right, 1 for logical left
    output [7:0] data_out      // Shifted output
);
    wire [7:0] stage1, stage2, stage3;

    // Stage 1: Shift by 1 position (if shift_amount[0] == 1)
    assign stage1 = shift_amount[0] ? (dir ? {data_in[6:0], 1'b0} : {1'b0, data_in[7:1]}) : data_in;

    // Stage 2: Shift by 2 positions (if shift_amount[1] == 1)
    assign stage2 = shift_amount[1] ? (dir ? {stage1[5:0], 2'b00} : {2'b00, stage1[7:2]}) : stage1;

    // Stage 3: Shift by 4 positions (if shift_amount[2] == 1)
    assign stage3 = shift_amount[2] ? (dir ? {stage2[3:0], 4'b0000} : {4'b0000, stage2[7:4]}) :
stage2;

    // Final output
    assign data_out = stage3;
endmodule
```

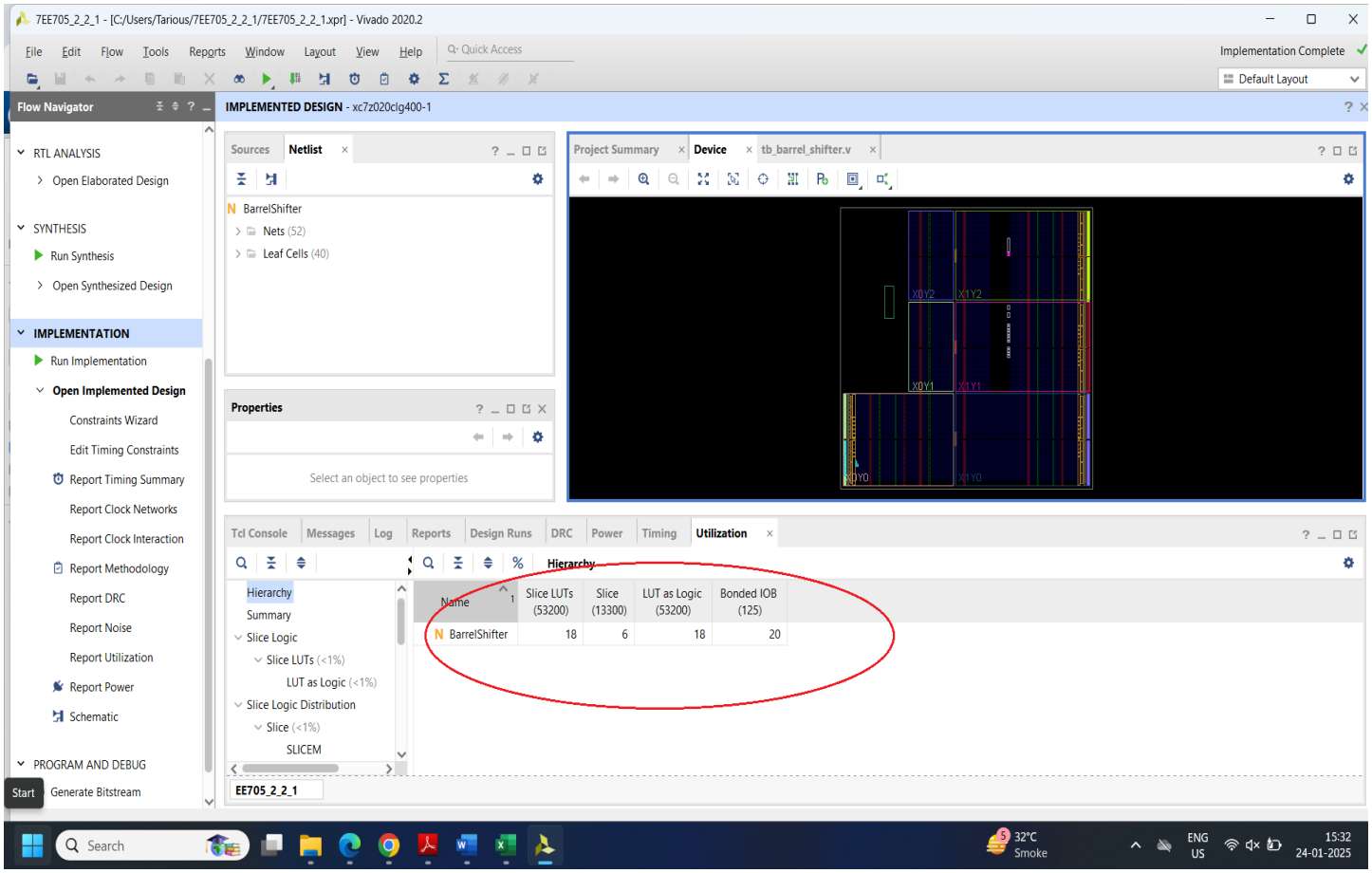
Test Bench Code:

```
module Testbench;
    reg [7:0] data_in;
    reg [2:0] shift_amount;
    reg dir;
    wire [7:0] data_out;

    // Instantiate the BarrelShifter module
```

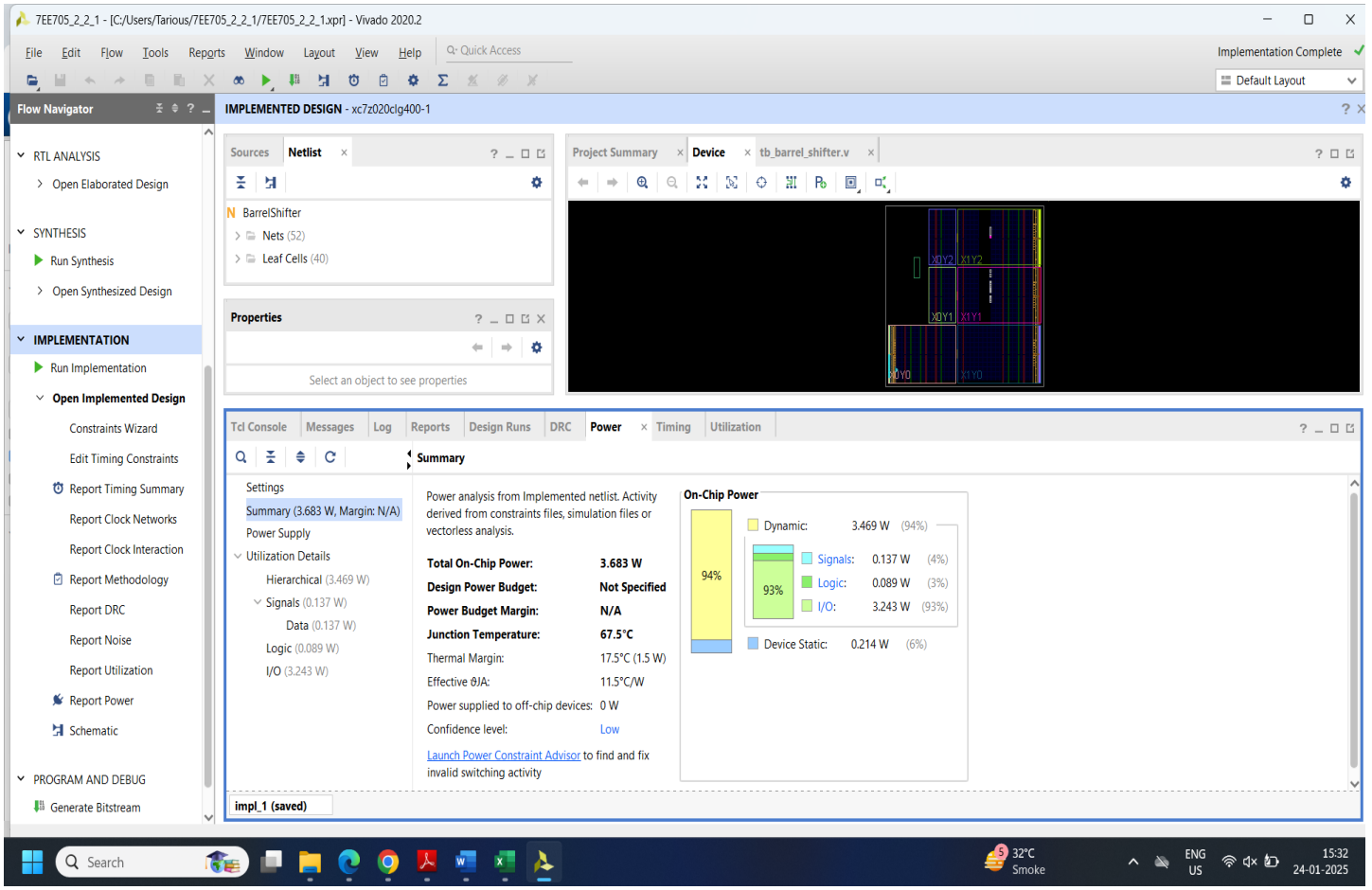
```
BarrelShifter uut (
    .data_in(data_in),
    .shift_amount(shift_amount),
    .dir(dir),
    .data_out(data_out)
);

initial begin
    // Test cases
    $monitor("Time = %0t | data_in = %b | shift_amount = %d | dir = %b | data_out = %b", $time, data_in, shift_amount, dir, data_out);

    // Test case 1: Logical right shift by 0
    data_in = 8'b11010101; shift_amount = 3'b000; dir = 0; #10;

    // Test case 2: Logical right shift by 3
    data_in = 8'b11010101; shift_amount = 3'b011; dir = 0; #10;

    // Test case 3: Logical left shift by 2
    data_in = 8'b11010101; shift_amount = 3'b010; dir = 1; #10;

    // Test case 4: Logical left shift by 5
    data_in = 8'b11010101; shift_amount = 3'b101; dir = 1; #10;

    // Test case 5: Logical right shift by 7
    data_in = 8'b11111111; shift_amount = 3'b111; dir = 0; #10;

    // Test case 6: Logical left shift by 4
    data_in = 8'b00001111; shift_amount = 3'b100; dir = 1; #10;

    // Test case 7: Logical left shift by 2
    data_in = 8'b10101010; shift_amount = 3'b010; dir = 1; #10;
```

```
        // Test case 8: Logical right shift by 2
        data_in = 8'b10101010; shift_amount = 3'b010; dir = 0; #10;

        // Test case 9: Logical left shift by 3
        data_in = 8'b10101010; shift_amount = 3'b011; dir = 1; #10;

        // Test case 10: Logical right shift by 3
        data_in = 8'b10101010; shift_amount = 3'b011; dir = 0; #10;

        $finish;
    end
endmodule
```

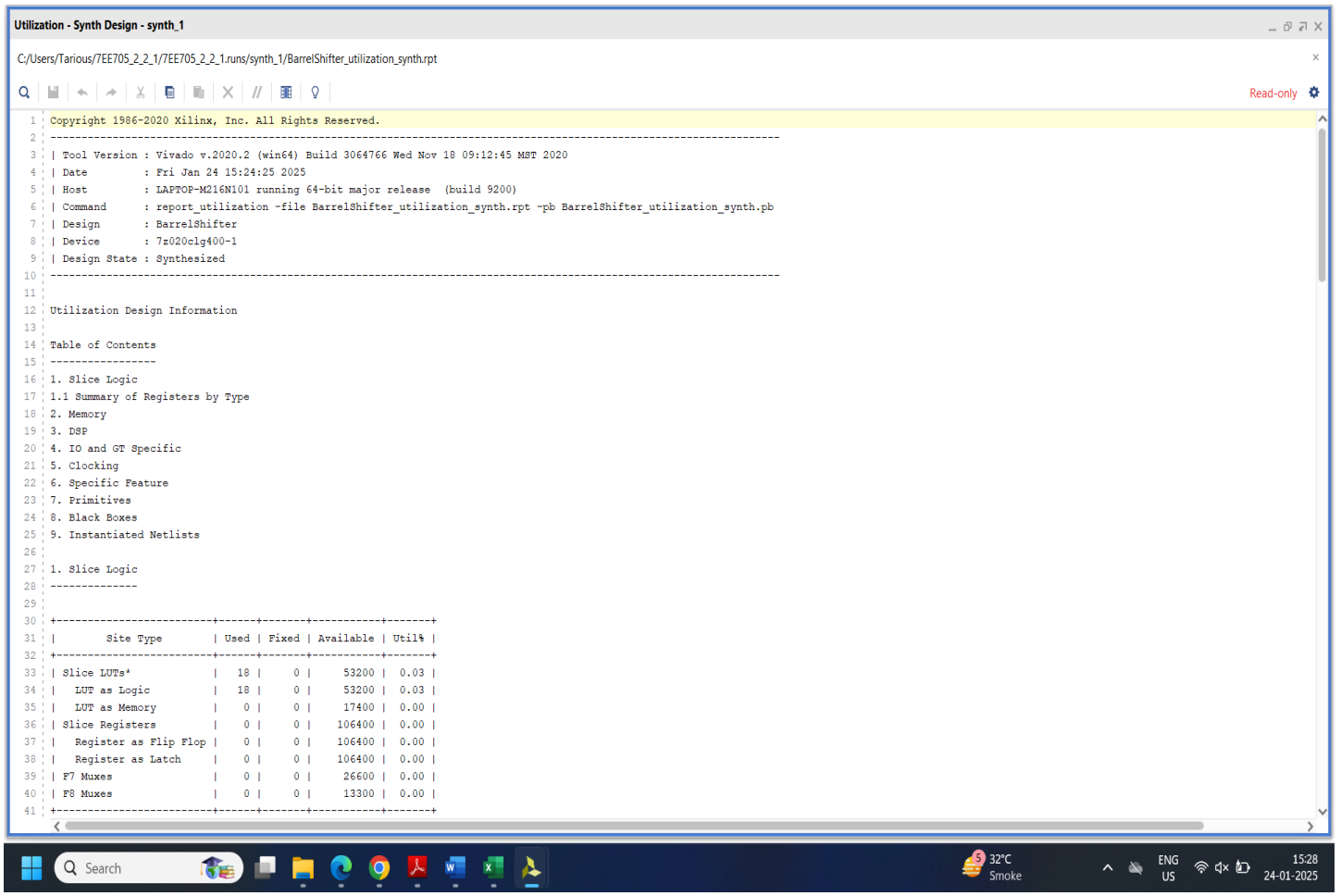
Report Utilisation:

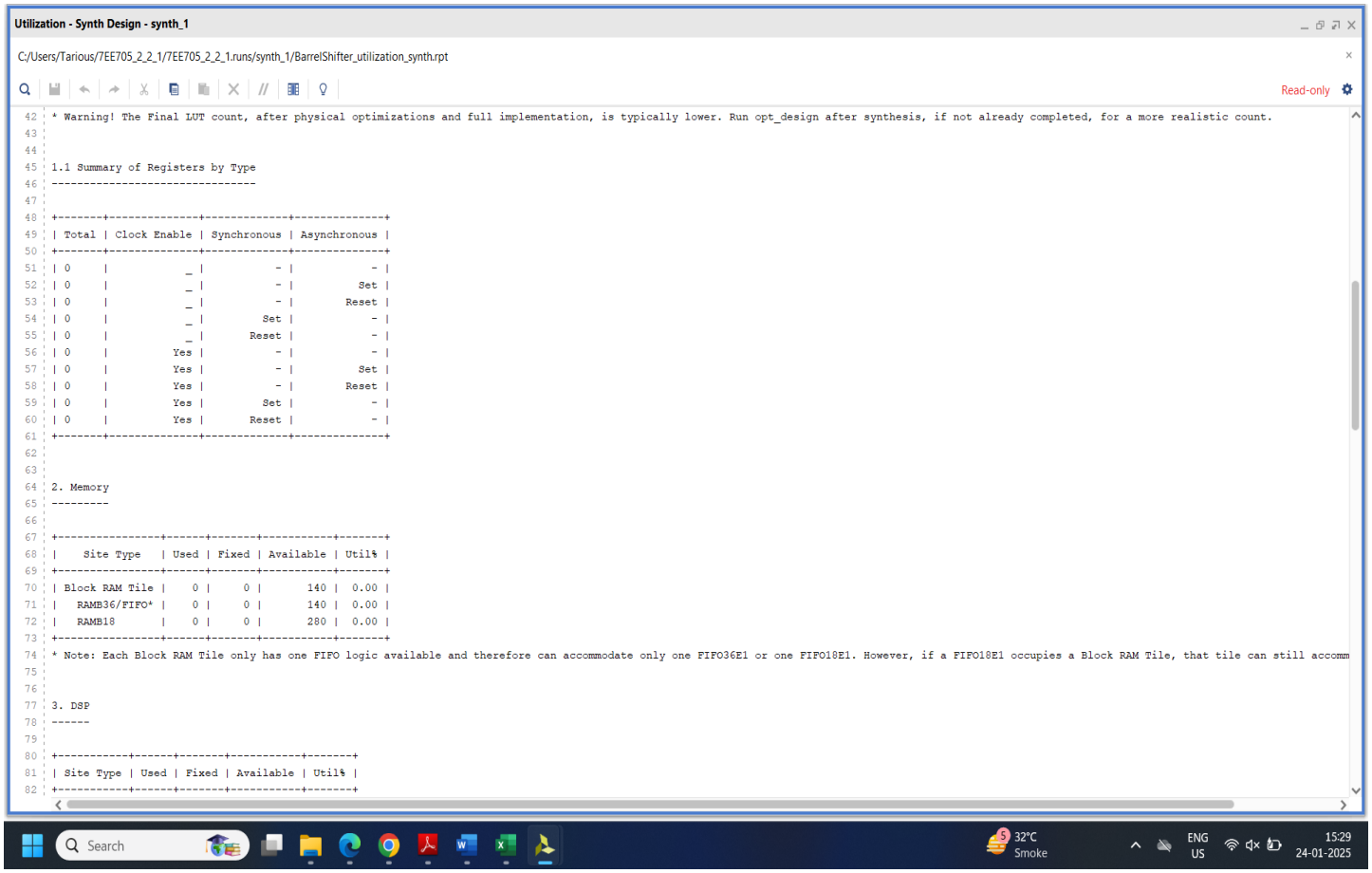


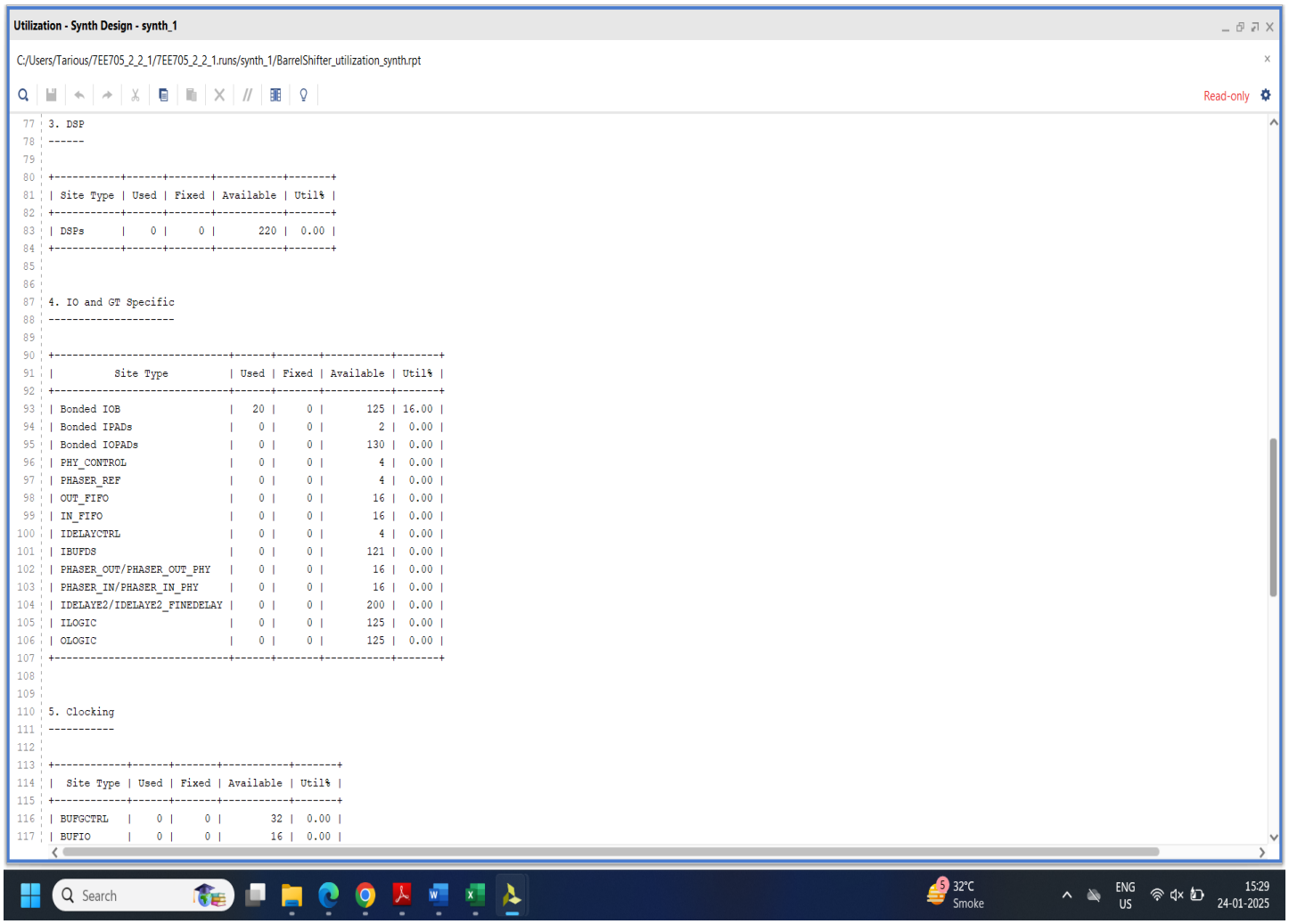
Power Consumption:

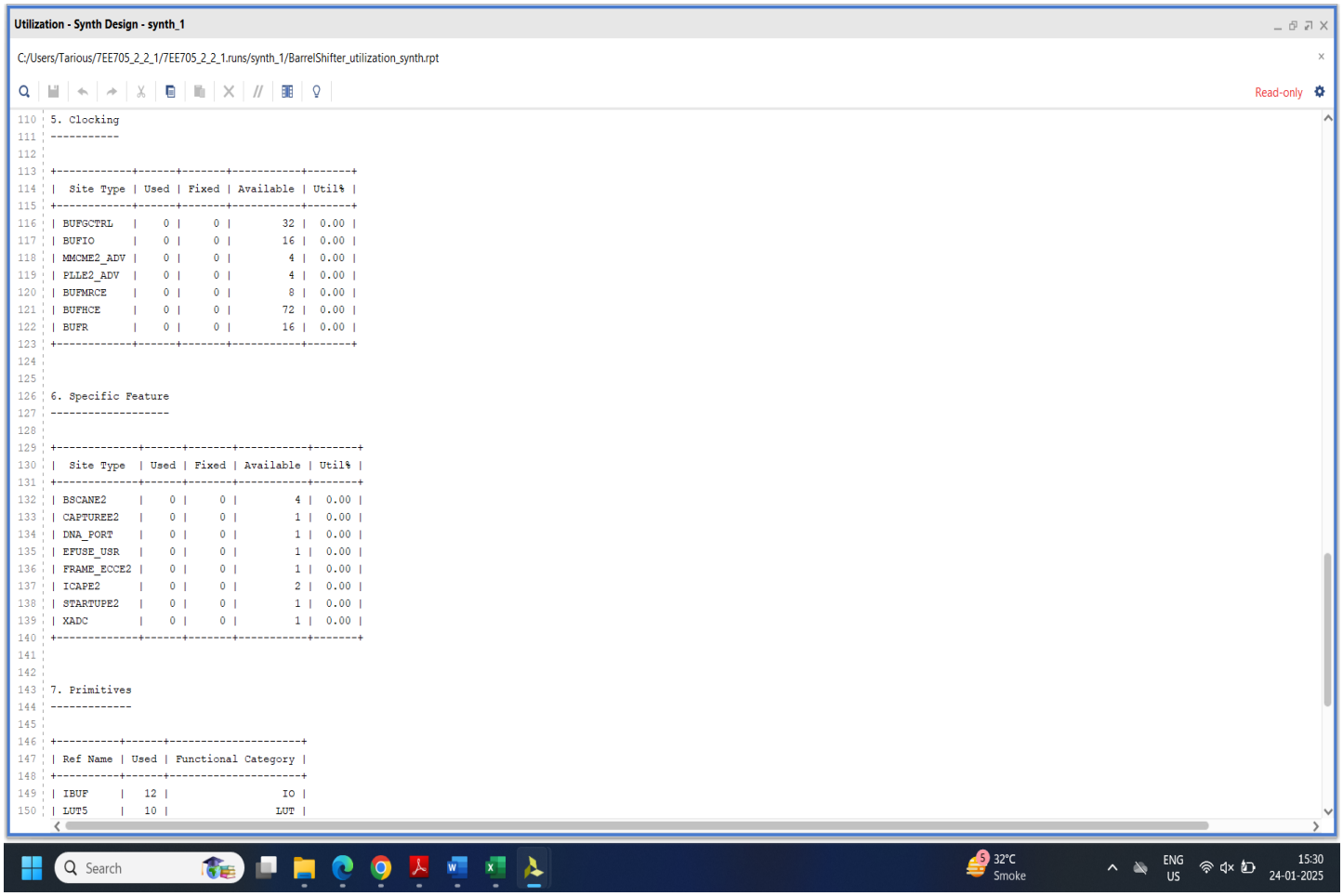


Resource Utilisation Report:

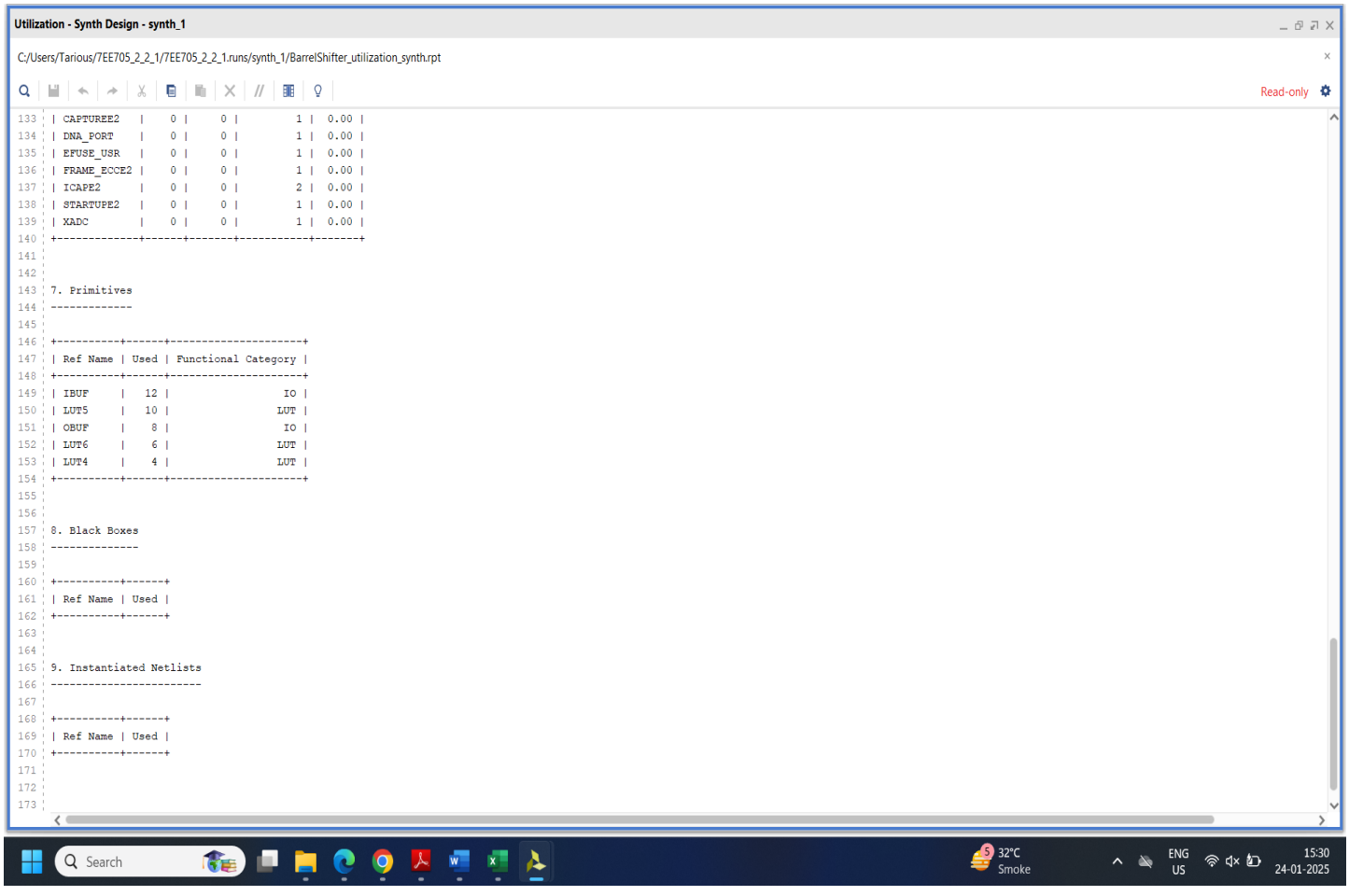



Utilization - Synth Design - synth_1
C:/Users/Tarious/7EE705_2_2_1/7EE705_2_2_1.runs/synth_1/BarrelShifter_utilization_synth.rpt
Read-only
* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.
1.1 Summary of Registers by Type
Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
0	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-
2. Memory
Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	140	0.00
RAMB36/FIFO*	0	0	140	0.00
RAMB18	0	0	280	0.00
* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accomm
3. DSP
| Site Type | Used | Fixed | Available | Util% |
Search
32°C Smoke
ENG US
15:29 24-01-2025


Utilization - Synth Design - synth_1
C:/Users/Tarious/7EE705_2_2_1/7EE705_2_2_1.runs/synth_1/BarrelShifter_utilization_synth.rpt
Read-only
3. DSP
| Site Type | Used | Fixed | Available | Util% |
| DSPs | 0 | 0 | 220 | 0.00 |
4. IO and GT Specific
Site Type	Used	Fixed	Available	Util%
Bonded IOB	20	0	125	16.00
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	4	0.00
PHASER_REF	0	0	4	0.00
OUT_FIFO	0	0	16	0.00
IN_FIFO	0	0	16	0.00
IDELAYCTRL	0	0	4	0.00
IBUFDS	0	0	121	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	16	0.00
PHASER_IN/PHASER_IN_PHY	0	0	16	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	200	0.00
ILOGIC	0	0	125	0.00
OLOGIC	0	0	125	0.00
5. Clocking
Site Type	Used	Fixed	Available	Util%
BUFGCTRL	0	0	32	0.00
BUFIO	0	0	16	0.00
Search
32°C Smoke
ENG US
15:29 24-01-2025




```
5. Clocking
-----------

+------------+------+-------+-----------+-------+
|  Site Type | Used | Fixed | Available | Util% |
+------------+------+-------+-----------+-------+
| BUFGCTRL   |    0 |     0 |        32 |  0.00 |
| BUFIO      |    0 |     0 |        16 |  0.00 |
| MMCME2_ADV |    0 |     0 |         4 |  0.00 |
| PLLE2_ADV  |    0 |     0 |         4 |  0.00 |
| BUFMRCE    |    0 |     0 |         8 |  0.00 |
| BUFHCE     |    0 |     0 |        72 |  0.00 |
| BUFR       |    0 |     0 |        16 |  0.00 |
+------------+------+-------+-----------+-------+


6. Specific Feature
-------------------

+-------------+------+-------+-----------+-------+
|  Site Type  | Used | Fixed | Available | Util% |
+-------------+------+-------+-----------+-------+
| BSCANE2     |    0 |     0 |         4 |  0.00 |
| CAPTUREE2   |    0 |     0 |         1 |  0.00 |
| DNA_PORT    |    0 |     0 |         1 |  0.00 |
| EFUSE_USR   |    0 |     0 |         1 |  0.00 |
| FRAME_ECCE2 |    0 |     0 |         1 |  0.00 |
| ICAPE2      |    0 |     0 |         2 |  0.00 |
| STARTUPE2   |    0 |     0 |         1 |  0.00 |
| XADC        |    0 |     0 |         1 |  0.00 |
+-------------+------+-------+-----------+-------+


7. Primitives
-------------

+----------+------+---------------------+
| Ref Name | Used | Functional Category |
+----------+------+---------------------+
| IBUF     |   12 |                  IO |
| LUT5     |   10 |                 LUT |
```


```
| CAPTUREE2   |    0 |     0 |         1 |  0.00 |
| DNA_PORT    |    0 |     0 |         1 |  0.00 |
| EFUSE_USR   |    0 |     0 |         1 |  0.00 |
| FRAME_ECCE2 |    0 |     0 |         1 |  0.00 |
| ICAPE2      |    0 |     0 |         2 |  0.00 |
| STARTUPE2   |    0 |     0 |         1 |  0.00 |
| XADC        |    0 |     0 |         1 |  0.00 |
+-------------+------+-------+-----------+-------+


7. Primitives
-------------

+----------+------+---------------------+
| Ref Name | Used | Functional Category |
+----------+------+---------------------+
| IBUF     |   12 |                  IO |
| LUT5     |   10 |                 LUT |
| OBUF     |    8 |                  IO |
| LUT6     |    6 |                 LUT |
| LUT4     |    4 |                 LUT |
+----------+------+---------------------+


8. Black Boxes
--------------

+----------+------+
| Ref Name | Used |
+----------+------+


9. Instantiated Netlists
------------------------

+----------+------+
| Ref Name | Used |
+----------+------+
```