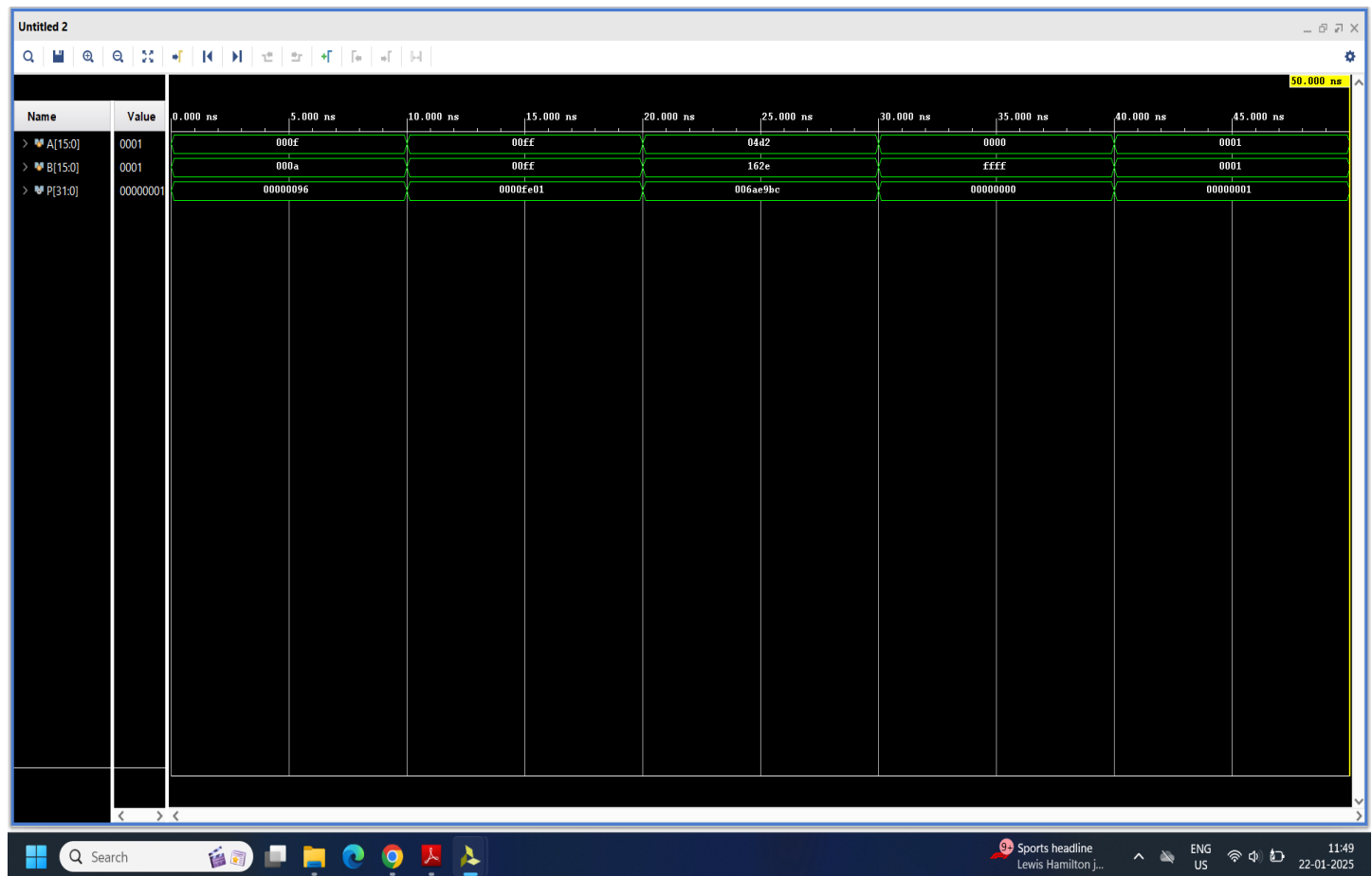


Design a 16-bit unsigned Dadda Multiplier using half adders and full adders, i.e. it takes two unsigned 16-bit numbers as input and the output should be unsigned 32-bit.

Using * operator only

Simulation Waveform using * operator



Verilog Code:

```
// 16-bit Dadda Multiplier using (*) operator
module DaddaMultiplier (
    input [15:0] A,    // First 16-bit input
    input [15:0] B,    // Second 16-bit input
    output [31:0] P     // 32-bit product output
);
    // Multiplication using (*) operator
    assign P = A * B;

endmodule
```

TestBench Code:

```
// Testbench

module tb_DaddaMultiplier;

    reg [15:0] A;
    reg [15:0] B;
    wire [31:0] P;

    // Instantiate the Dadda multiplier
    DaddaMultiplier uut (
        .A(A),
        .B(B),
        .P(P)
    );

    initial begin
        $monitor("A = %d, B = %d, Product = %d", A, B, P);

        // Test case 1
        A = 16'd15;
        B = 16'd10;
        #10;

        // Test case 2
        A = 16'd255;
        B = 16'd255;
        #10;

        // Test case 3
        A = 16'd1234;
        B = 16'd5678;
        #10;
```

```
// Test case 4
```

```
A = 16'd0;
```

```
B = 16'd65535;
```

```
#10;
```

```
// Test case 5
```

```
A = 16'd1;
```

```
B = 16'd1;
```

```
#10;
```

```
$finish;
```

```
end
```

```
endmodule
```

Utilisation Report:

The screenshot shows the Vivado 2020.2 interface with the 'Utilization' report open. The report is titled 'Hierarchy' and shows the resource utilization for the 'DaddaMultiplier' design. The 'DaddaMultiplier' block is highlighted with a red circle, showing 1 DSPs (220) and 64 Bonded IOB (125).

Name	DSPs (220)	Bonded IOB (125)
DaddaMultiplier	1	64

The report also shows the following utilization details:

- DSP:** 1 (1%)
- DSP48E1 only:** 1
- IO and GT Specific:** 1

The bottom status bar shows the system time as 01:24 on 23-01-2025, with network and power indicators.

Resource Utilisation Report:

Utilization - Synth Design - synth_1

C:/Users/Tariou5/SEE705/SEE705.runs/synth_1/DaddaMultiplier_utilization_synth.rpt

Q

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Read-only ⚙

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| Tool Version : Vivado v.2020.2 (win64) Build 3064766 Wed Nov 18 09:12:45 MST 2020

4

| Date : Wed Jan 22 12:09:05 2025

5

| Host : LAPTOP-M216N101 running 64-bit major release (build 9200)

6

| Command : report_utilization -file DaddaMultiplier_utilization_synth.rpt -pb DaddaMultiplier_utilization_synth.pb

7

| Design : DaddaMultiplier

8

| Device : 7z020clg400-1

9

| Design State : Synthesized

10

11

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1. Slice Logic

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Utilization - Synth Design - synth_1

C:/Users/Tarious/SEE705/SEE705.runs/synth_1/DaddaMultiplier_utilization_synthrpt

Read-only

```
77 3. DSP
78 -----
79
80 +-----+
81 | Site Type | Used | Fixed | Available | Util% |
82 +-----+
83 | DSPs      | 1   | 0   | 220  | 0.45 |
84 | DSP48E1 only | 1   |    |    |    |
85 +-----+
86
87
88 4. IO and GT Specific
89 -----
90
91 +-----+
92 | Site Type | Used | Fixed | Available | Util% |
93 +-----+
94 | Bonded IOB      | 64 | 0 | 125 | 51.20 |
95 | Bonded IPADs    | 0  | 0 | 2   | 0.00 |
96 | Bonded IOPADs   | 0  | 0 | 130 | 0.00 |
97 | PHY_CONTROL     | 0  | 0 | 4   | 0.00 |
98 | PHASER_REF      | 0  | 0 | 4   | 0.00 |
99 | OUT_FIFO        | 0  | 0 | 16  | 0.00 |
100 | IN_FIFO         | 0  | 0 | 16  | 0.00 |
101 | IDELAYCTRL      | 0  | 0 | 4   | 0.00 |
102 | IBUFDS          | 0  | 0 | 121 | 0.00 |
103 | PHASER_OUT/PHASER_OUT_PHY | 0  | 0 | 16  | 0.00 |
104 | PHASER_IN/PHASER_IN_PHY  | 0  | 0 | 16  | 0.00 |
105 | IDELAYE2/IDELAYE2_FINEDELAY | 0  | 0 | 200 | 0.00 |
106 | ILOGIC          | 0  | 0 | 125 | 0.00 |
107 | OLOGIC          | 0  | 0 | 125 | 0.00 |
108 +-----+
109
110
111 5. Clocking
112 -----
113
114 +-----+
115 | Site Type | Used | Fixed | Available | Util% |
116 +-----+
117 | BUFGCTRL   | 0  | 0 | 32  | 0.00 |
```

Windows taskbar: Search, Finance headline, Netflix adds 19..., ENG US, 12:12, 22-01-2025

Utilization - Synth Design - synth_1

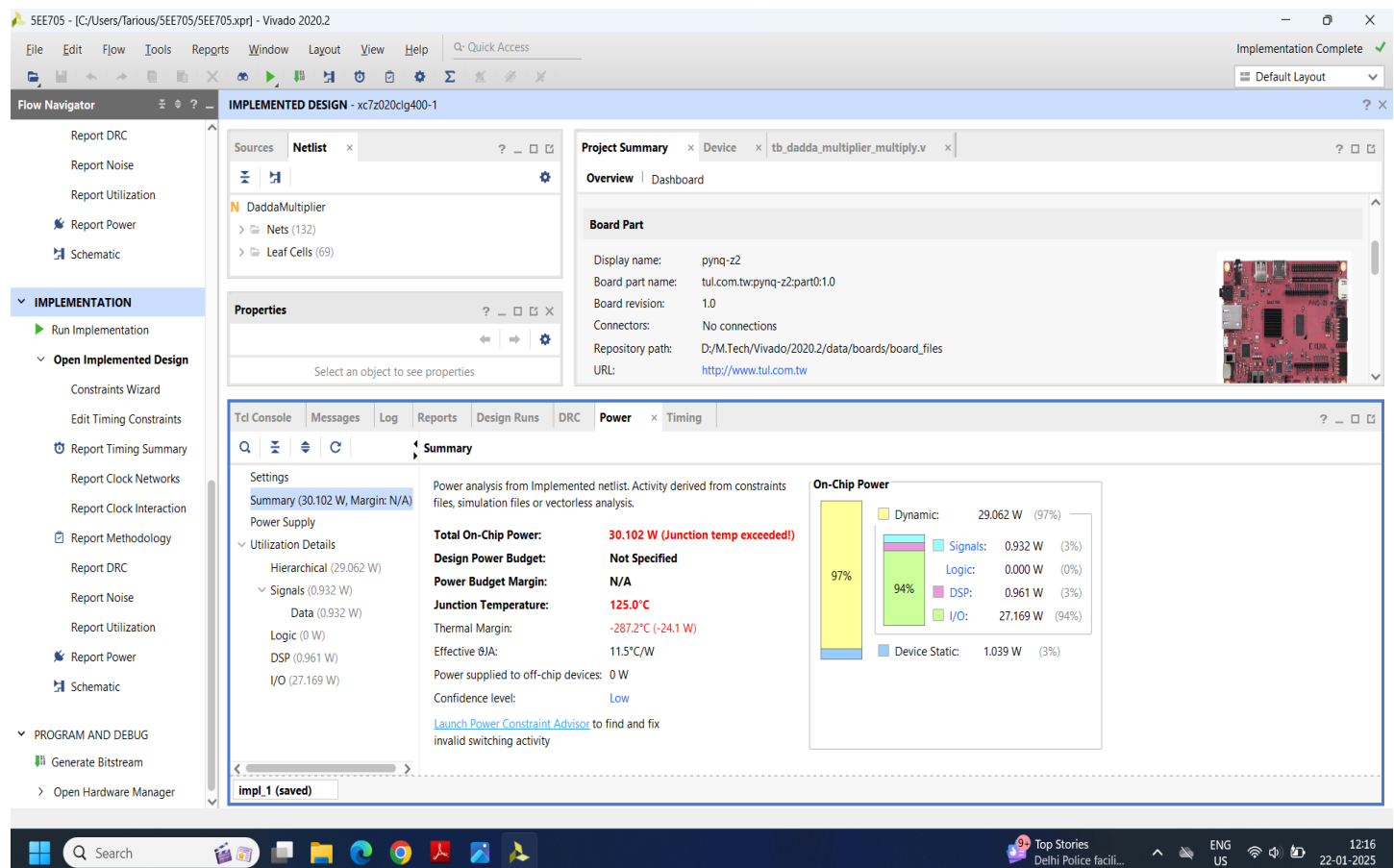
C:/Users/Tarious/SEE705/SEE705.runs/synth_1/DaddaMultiplier_utilization_synthrpt

Read-only

```
111 5. Clocking
112 -----
113
114 +-----+
115 | Site Type | Used | Fixed | Available | Util% |
116 +-----+
117 | BUFGCTRL   | 0  | 0 | 32  | 0.00 |
118 | BUFIO      | 0  | 0 | 16  | 0.00 |
119 | MMCME2_ADV | 0  | 0 | 4   | 0.00 |
120 | FLLE2_ADV  | 0  | 0 | 4   | 0.00 |
121 | BUFMRCE    | 0  | 0 | 8   | 0.00 |
122 | BUFHCE     | 0  | 0 | 72  | 0.00 |
123 | BUFR       | 0  | 0 | 16  | 0.00 |
124 +-----+
125
126
127 6. Specific Feature
128 -----
129
130 +-----+
131 | Site Type | Used | Fixed | Available | Util% |
132 +-----+
133 | BSCANE2   | 0  | 0 | 4   | 0.00 |
134 | CAPTUREE2 | 0  | 0 | 1   | 0.00 |
135 | DNA_FORT  | 0  | 0 | 1   | 0.00 |
136 | EFUSE_USR | 0  | 0 | 1   | 0.00 |
137 | FRAME_ECCE2 | 0  | 0 | 1   | 0.00 |
138 | ICAPE2    | 0  | 0 | 2   | 0.00 |
139 | STARTUPE2 | 0  | 0 | 1   | 0.00 |
140 | XADC      | 0  | 0 | 1   | 0.00 |
141 +-----+
142
143
144 7. Primitives
145 -----
146
147 +-----+
148 | Ref Name | Used | Functional Category |
149 +-----+
150 | OBUF     | 32  | IO |
151 | IBUF     | 32  | IO |
```

Windows taskbar: Search, Finance headline, Netflix adds 19..., ENG US, 12:13, 22-01-2025

Power:



Using Dadda Multiplier**Verilog Code:**

```
// Dadda Multiplier Implementation
```

```
module dadda_multiplier #(parameter WIDTH = 16)(
```

```
    input  [WIDTH-1:0] a, // Multiplier
```

```
    input  [WIDTH-1:0] b, // Multiplicand
```

```
    output [2*WIDTH-1:0] product // Product
```

```
);
```

```
    wire [WIDTH-1:0] partial_products[WIDTH-1:0];
```

```
    wire [2*WIDTH-1:0] sum[WIDTH-1:0];
```

```
    wire [2*WIDTH-1:0] carry[WIDTH-1:0];
```

```
    genvar i, j;
```

```
// Step 1: Generate Partial Products
```

```
generate
```

```
    for (i = 0; i < WIDTH; i = i + 1) begin
```

```
        for (j = 0; j < WIDTH; j = j + 1) begin
```

```
            assign partial_products[i][j] = a[i] & b[j];
```

```
        end
```

```
    end
```

```
endgenerate
```

```
// Step 2: Initialize First Stage
```

```
assign sum[0] = { {WIDTH{1'b0}}, partial_products[0] }; // Pad to match product size
```

```
assign carry[0] = 0;
```

```
// Step 3: Dadda Tree Reduction
```

```
generate
```

```
    for (i = 1; i < WIDTH; i = i + 1) begin
```

```
        dadda_reduce #(2*WIDTH) reduce_stage (
```

```
            .pp({ {(WIDTH+i){1'b0}}, partial_products[i], {i{1'b0}}} ), // Align PP properly
```

```
.prev_sum(sum[i-1]),
.prev_carry(carry[i-1]),
.sum_out(sum[i]),
.carry_out(carry[i])
);
end
endgenerate

// Step 4: Final Stage Addition
assign product = sum[WIDTH-1] + carry[WIDTH-1];

endmodule

// Dadda Reduction Stage
module dadda_reduce #(parameter WIDTH = 32)(
    input  [WIDTH-1:0] pp,      // Current Partial Product (Aligned)
    input  [WIDTH-1:0] prev_sum, // Sum from Previous Stage
    input  [WIDTH-1:0] prev_carry, // Carry from Previous Stage
    output [WIDTH-1:0] sum_out,  // Sum Output
    output [WIDTH-1:0] carry_out // Carry Output
);
    assign {carry_out, sum_out} = pp + prev_sum + prev_carry; // Full Addition
endmodule
```

Test Bench Code:

```
// Testbench for 16-bit Dadda Multiplier
module tb_dadda_multiplier;
    parameter WIDTH = 16;
    reg  [WIDTH-1:0] a, b;
    wire [2*WIDTH-1:0] product;
```



```
// Instantiate the multiplier
dadda_multiplier #(WIDTH) uut (
    .a(a),
    .b(b),
    .product(product)
);

initial begin
    $dumpfile("dadda_multiplier.vcd");
    $dumpvars(0, tb_dadda_multiplier);

    // Test cases
    a = 16'd3; b = 16'd5; #10;
    $display("A: %d, B: %d, Product: %d", a, b, product);

    a = 16'd15; b = 16'd10; #10;
    $display("A: %d, B: %d, Product: %d", a, b, product);

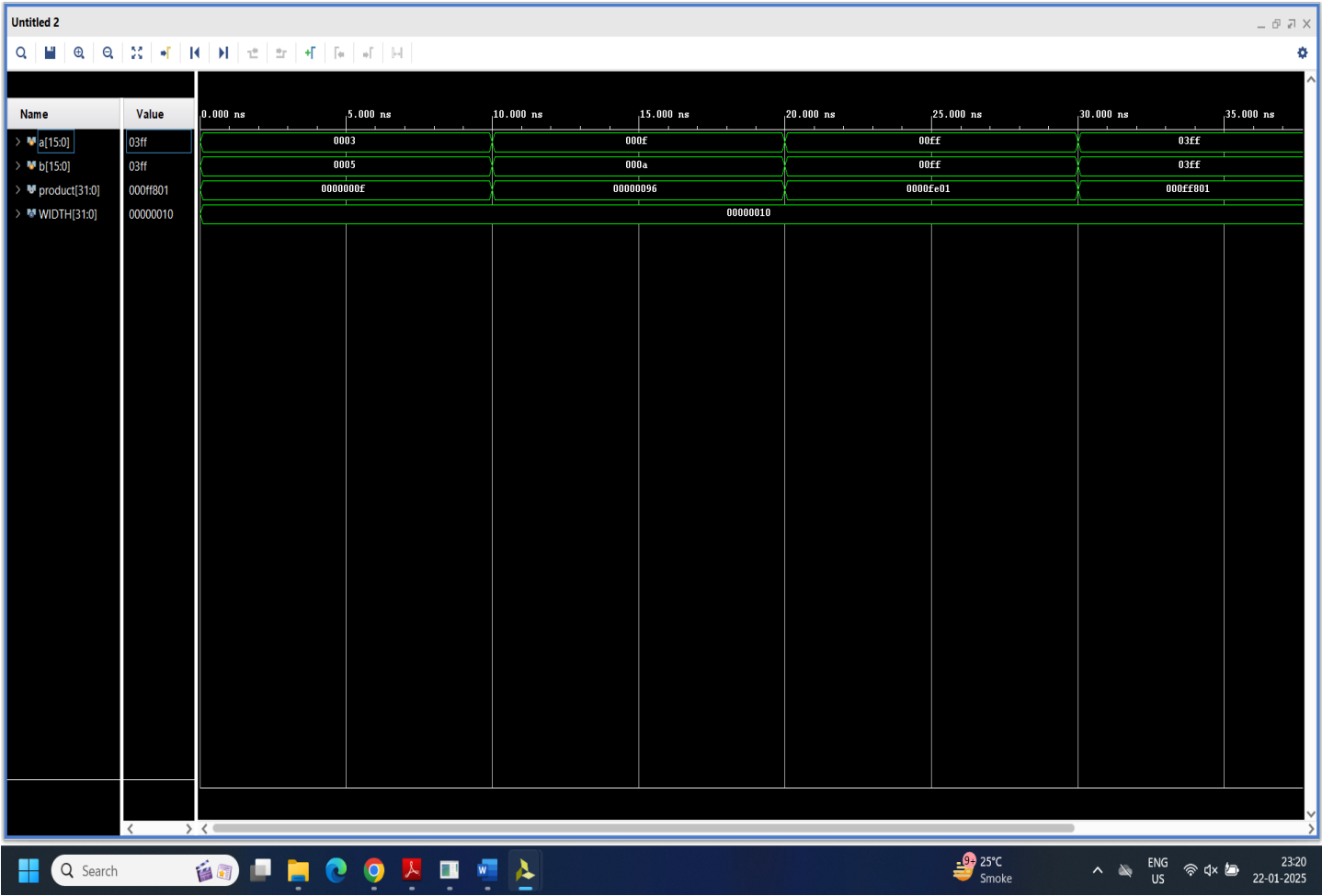
    a = 16'd255; b = 16'd255; #10;
    $display("A: %d, B: %d, Product: %d", a, b, product);

    a = 16'd1023; b = 16'd1023; #10;
    $display("A: %d, B: %d, Product: %d", a, b, product);

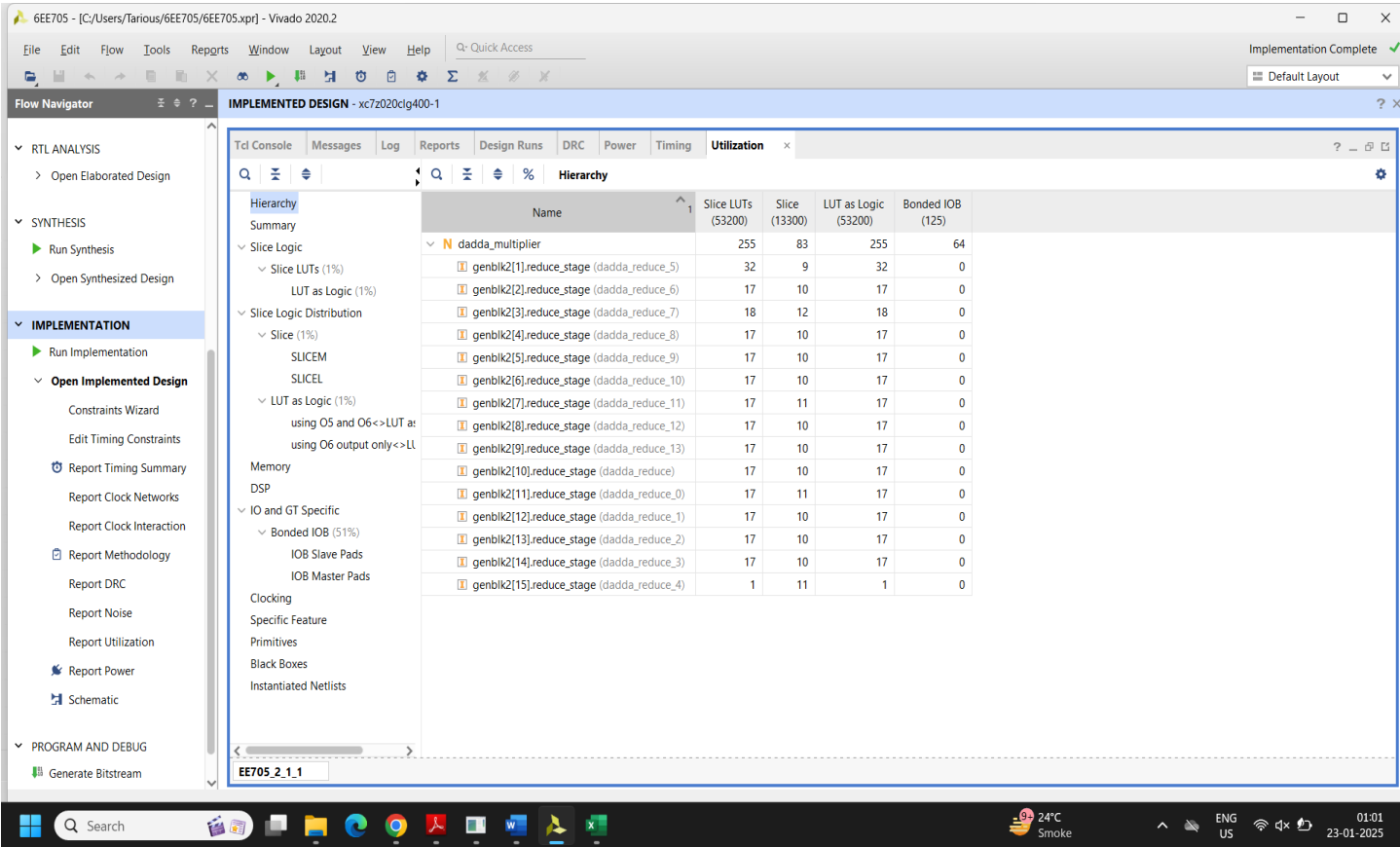
    a = 16'd65535; b = 16'd65534; #10;
    $display("A: %d, B: %d, Product: %d", a, b, product);

    $finish;
end
endmodule
```

Simulation Waveform Using Dadda Multiplier:



Utilisation Report:



Utilization - Synth Design - synth_1

C:\Users\Tarios\6EE705\6EE705.runs\synth_1\dadda_multiplier_utilization_synth.rpt

Q

Read-only

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Tool Version : Vivado v.2020.2 (win64) Build 3064766 Wed Nov 18 09:12:45 MST 2020

4

Date : Wed Jan 22 23:48:48 2025

5

Host : LAPTOP-M216N101 running 64-bit major release (build 9200)

6

Command : report_utilization -file dadda_multiplier_utilization_synth.rpt -pb dadda_multiplier_utilization_synth.pb

7

Design : dadda_multiplier

8

Device : 7z020c1g400-1

9

Design State : Synthesized

10

11

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24

9. Instantiated Netlists

25

26

1. Slice Logic

27

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31

| Site Type | Used | Fixed | Available | Util% |

32

33

| Slice LUTs* | 255 | 0 | 53200 | 0.48 |

34

| LUT as Logic | 255 | 0 | 53200 | 0.48 |

35

| LUT as Memory | 0 | 0 | 17400 | 0.00 |

36

| Slice Registers | 0 | 0 | 106400 | 0.00 |

37

| Register as Flip Flop | 0 | 0 | 106400 | 0.00 |

38

| Register as Latch | 0 | 0 | 106400 | 0.00 |

39

| F7 Muxes | 0 | 0 | 26600 | 0.00 |

40

| F8 Muxes | 0 | 0 | 13300 | 0.00 |

41

The screenshot displays a Synthesis Report window titled "Utilization - Synth Design - synth_1". The report path is "C:/Users/Tarious/6EE705/6EE705.runs/synth_1/dadda_multiplier_utilization_synthrpt". The report content includes a warning about the final LUT count, a summary of registers by type, and memory utilization statistics.

Warning: The Final LUT count, after physical optimizations and full implementation, is typically lower. Run `opt_design` after synthesis, if not already completed, for a more realistic count.

1.1 Summary of Registers by Type

	Total	Clock Enable	Synchronous	Asynchronous
0	-	-	-	-
0	-	-	-	Set
0	-	-	-	Reset
0	-	Set	-	-
0	-	Reset	-	-
0	Yes	-	-	-
0	Yes	-	-	Set
0	Yes	-	-	Reset
0	Yes	Set	-	-
0	Yes	Reset	-	-

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	140	0.00
RAMB36/FIFO*	0	0	140	0.00
RAMB18	0	0	280	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accomm

3. DSP

Site Type	Used	Fixed	Available	Util%
-----------	------	-------	-----------	-------

Utilization - Synth Design - synth_1

C:/Users/Tarios/6EE705/6EE705.runs/synth_1/dadda_multiplier_utilization_synth.rpt

Q

Read-only

77 3. DSP

78 -----

79

80 +-----+-----+-----+-----+-----+-----+

81 | Site Type | Used | Fixed | Available | Util% |

82 +-----+-----+-----+-----+-----+-----+

83 | DSPs | 0 | 0 | 220 | 0.00 |

84 +-----+-----+-----+-----+-----+-----+

85

86

87 4. IO and GT Specific

88 -----

89

90 +-----+-----+-----+-----+-----+-----+

91 | Site Type | Used | Fixed | Available | Util% |

92 +-----+-----+-----+-----+-----+-----+

93 | Bonded IOB | 64 | 0 | 125 | 51.20 |

94 | Bonded IPADs | 0 | 0 | 2 | 0.00 |

95 | Bonded IOPADs | 0 | 0 | 130 | 0.00 |

96 | PHY_CONTROL | 0 | 0 | 4 | 0.00 |

97 | PHASER_REF | 0 | 0 | 4 | 0.00 |

98 | OUT_FIFO | 0 | 0 | 16 | 0.00 |

99 | IN_FIFO | 0 | 0 | 16 | 0.00 |

100 | IDELAYCTRL | 0 | 0 | 4 | 0.00 |

101 | IBUFDS | 0 | 0 | 121 | 0.00 |

102 | PHASER_OUT/PHASER_OUT_PHY | 0 | 0 | 16 | 0.00 |

103 | PHASER_IN/PHASER_IN_PHY | 0 | 0 | 16 | 0.00 |

104 | IDELAYE2/IDELAYE2_FINEDELAY | 0 | 0 | 200 | 0.00 |

105 | ILOGIC | 0 | 0 | 125 | 0.00 |

106 | OLOGIC | 0 | 0 | 125 | 0.00 |

107 +-----+-----+-----+-----+-----+-----+

108

109

110 5. Clocking

111 -----

112

113 +-----+-----+-----+-----+-----+-----+

114 | Site Type | Used | Fixed | Available | Util% |

115 +-----+-----+-----+-----+-----+-----+

116 | BUFGCTRL | 0 | 0 | 32 | 0.00 |

117 | BUFIO | 0 | 0 | 16 | 0.00 |

118 +-----+-----+-----+-----+-----+-----+

Windows taskbar

24°C Smoke

ENG US

01:05 23-01-2025

Utilization - Synth Design - synth_1

C:/Users/Tarios/6EE705/6EE705.runs/synth_1/dadda_multiplier_utilization_synth.rpt

Q

Read-only

110 5. Clocking

111 -----

112

113 +-----+-----+-----+-----+-----+-----+

114 | Site Type | Used | Fixed | Available | Util% |

115 +-----+-----+-----+-----+-----+-----+

116 | BUFGCTRL | 0 | 0 | 32 | 0.00 |

117 | BUFIO | 0 | 0 | 16 | 0.00 |

118 | MMCME2_ADV | 0 | 0 | 4 | 0.00 |

119 | PLL2_ADV | 0 | 0 | 4 | 0.00 |

120 | BUFMRCE | 0 | 0 | 8 | 0.00 |

121 | BUFHCE | 0 | 0 | 72 | 0.00 |

122 | BUFR | 0 | 0 | 16 | 0.00 |

123 +-----+-----+-----+-----+-----+-----+

124

125

126 6. Specific Feature

127 -----

128

129 +-----+-----+-----+-----+-----+-----+

130 | Site Type | Used | Fixed | Available | Util% |

131 +-----+-----+-----+-----+-----+-----+

132 | BSCAN2 | 0 | 0 | 4 | 0.00 |

133 | CAPTURE2 | 0 | 0 | 1 | 0.00 |

134 | DNA_PORT | 0 | 0 | 1 | 0.00 |

135 | EFUSE_USR | 0 | 0 | 1 | 0.00 |

136 | FRAME_POCE2 | 0 | 0 | 1 | 0.00 |

137 | ICAPE2 | 0 | 0 | 2 | 0.00 |

138 | STARTUPE2 | 0 | 0 | 1 | 0.00 |

139 | XADC | 0 | 0 | 1 | 0.00 |

140 +-----+-----+-----+-----+-----+-----+

141

142

143 7. Primitives

144 -----

145

146 +-----+-----+-----+-----+-----+-----+

147 | Ref Name | Used | Functional Category |

148 +-----+-----+-----+-----+-----+-----+

149 | LUT3 | 227 | LUT |

150 | LUT5 | 224 | LUT |

151 +-----+-----+-----+-----+-----+-----+

Windows taskbar

24°C Smoke

ENG US

01:06 23-01-2025

Utilization - Synth Design - synth_1

C:/Users/Tarious/6EE705/6EE705.runs/synth_1/dadda_multiplier_utilization_synth.rpt

134	DNA_PORT	0	0	1	0.00
135	EFUSE_USR	0	0	1	0.00
136	FRAME_ECCE2	0	0	1	0.00
137	ICAPE2	0	0	2	0.00
138	STARTUPE2	0	0	1	0.00
139	XADC	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
LUT3	227	LUT
LUT5	224	LUT
CARRY4	83	CarryLogic
IOBUF	32	IO
IOBUF	32	IO
LUT4	30	LUT

8. Black Boxes

Ref Name	Used
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9. Instantiated Netlists

Ref Name	Used
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24°C Smoke

ENG US

01:06 23-01-2025

Power:

6EE705 - [C:/Users/Tarious/6EE705/6EE705.xpr] - Vivado 2020.2

File Edit Flow Tools Repgrts Window Layout View Help

Flow Navigator

- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Noise
 - Report Utilization
 - Report Power
 - Schematic
- PROGRAM AND DEBUG
 - Generate Bitstream

IMPLEMENTED DESIGN - xc7z020clg400-1

- Sources
 - Netlist
 - dadda_multiplier
 - Nets (607)
 - Leaf Cells (64)
- Source File Properties

Project Summary | Device | tb_dadda_multiplier.v | Utilization - Synth Design - synth_1

- C:/Users/Tarious/6EE705/6EE705.runs/synth_1/dadda_multiplier_utilization_synth.rpt

134	DNA_PORT	0	0	1	0.00
135	EFUSE_USR	0	0	1	0.00
136	FRAME_ECCE2	0	0	1	0.00
137	ICAPE2	0	0	2	0.00
138	STARTUPE2	0	0	1	0.00
139	XADC	0	0	1	0.00

Tcl Console | Messages | Log | Reports | Design Runs | DRC | Power | Timing | Utilization

- Summary
 - Settings
 - Summary (36.682 W, Margin: N/A)
 - Power Supply
 - Utilization Details
 - Hierarchical (35.643 W)
 - Signals (2.892 W)
 - Data (2.892 W)
 - Logic (3.672 W)
 - I/O (29.079 W)
 - Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
 - Total On-Chip Power: 36.682 W (Junction temp exceeded!)
 - Design Power Budget: Not Specified
 - Power Budget Margin: N/A
 - Junction Temperature: 125.0°C
 - Thermal Margin: -363.1°C (-30.7 W)
 - Effective θ JA: 11.5°C/W
 - Power supplied to off-chip devices: 0 W
 - Confidence level: Low
 - On-Chip Power
 - Dynamic: 35.643 W (97%)
 - Static: 1.039 W (3%)
 - Signals: 2.892 W (8%)
 - Logic: 3.672 W (10%)
 - I/O: 29.079 W (82%)
- impl_1 (saved)

24°C Smoke

ENG US

01:11 23-01-2025