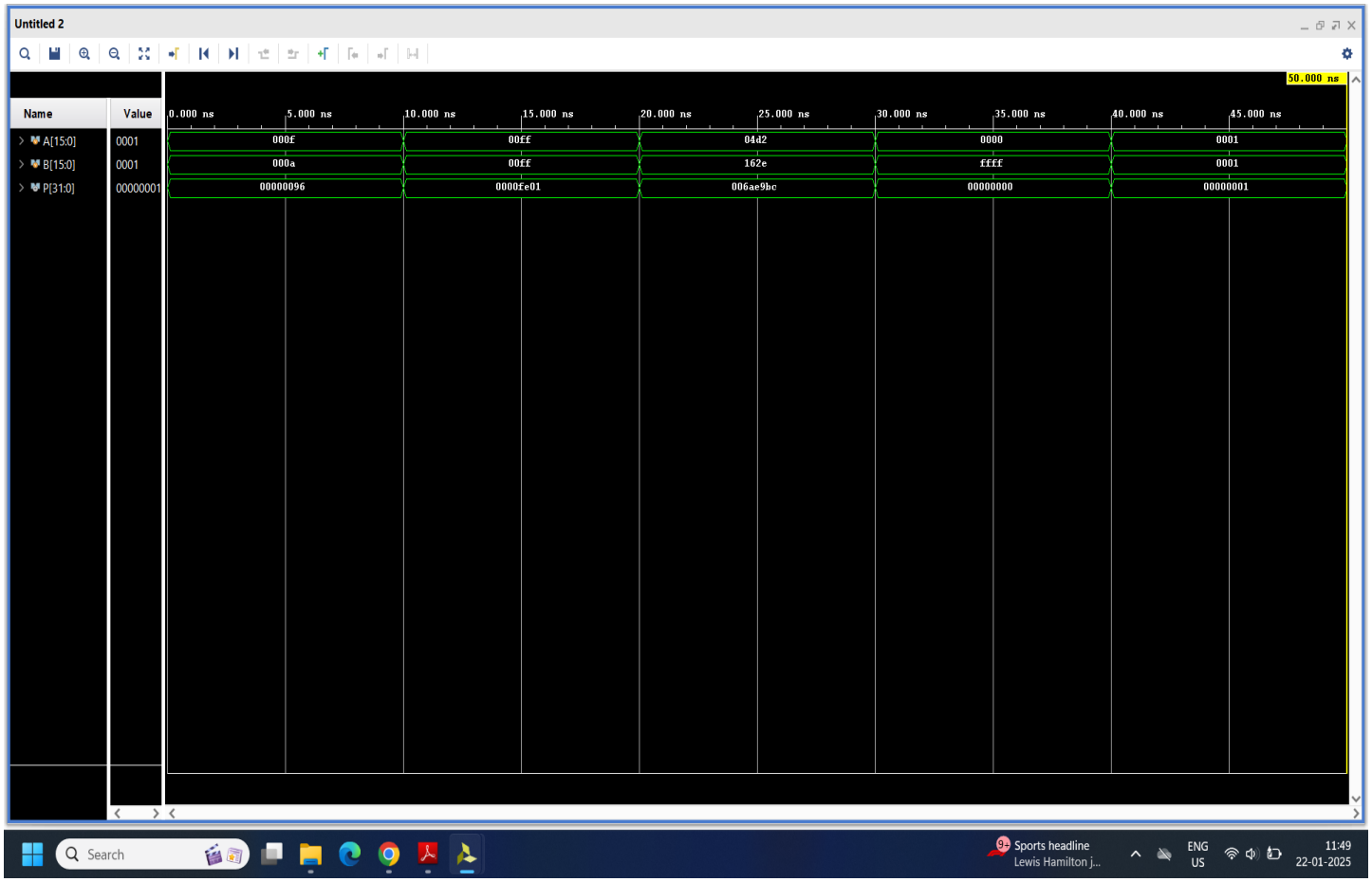
Design a 16-bit unsigned Dadda Multiplier using half adders and full adders, i.e. it takes two unsigned 16-bit numbers as input and the output should be unsigned 32-bit.

Using * operator only

Simulation Waveform using * operator



Verilog Code:

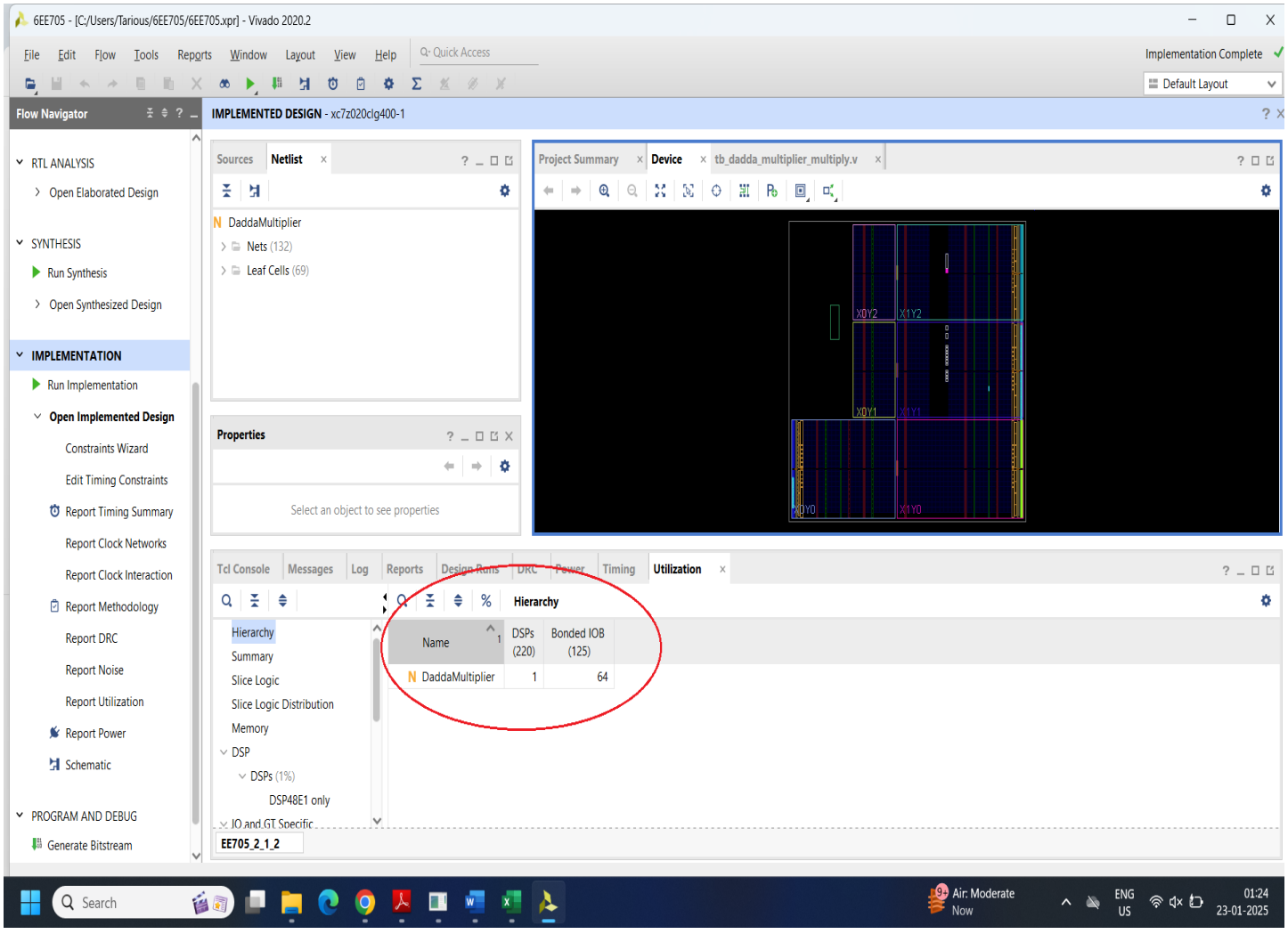
```
// 16-bit Dadda Multiplier using (*) operator
module DaddaMultiplier (
    input  [15:0] A,      // First 16-bit input
    input  [15:0] B,      // Second 16-bit input
    output [31:0] P       // 32-bit product output
);
    // Multiplication using (*) operator
    assign P = A * B;

endmodule
```

TestBench Code:

```
// Testbench
module tb_DaddaMultiplier;
    reg  [15:0] A;
    reg  [15:0] B;
    wire [31:0] P;

    // Instantiate the Dadda multiplier
    DaddaMultiplier uut (
        .A(A),
        .B(B),
        .P(P)
    );

    initial begin
        $monitor("A = %d, B = %d, Product = %d", A, B, P);

        // Test case 1
        A = 16'd15;
        B = 16'd10;
        #10;

        // Test case 2
        A = 16'd255;
        B = 16'd255;
        #10;

        // Test case 3
        A = 16'd1234;
        B = 16'd5678;
        #10;
```

```
        // Test case 4
        A = 16'd0;
        B = 16'd65535;
        #10;

        // Test case 5
        A = 16'd1;
        B = 16'd1;
        #10;

        $finish;
    end
endmodule
```

Utilisation Report:



Resource Utilisation Report:

Utilization - Synth Design - synth_1

C:/Users/Tarious/5EE705/5EE705.runs/synth_1/DaddaMultiplier_utilization_synth.rpt

Read-only

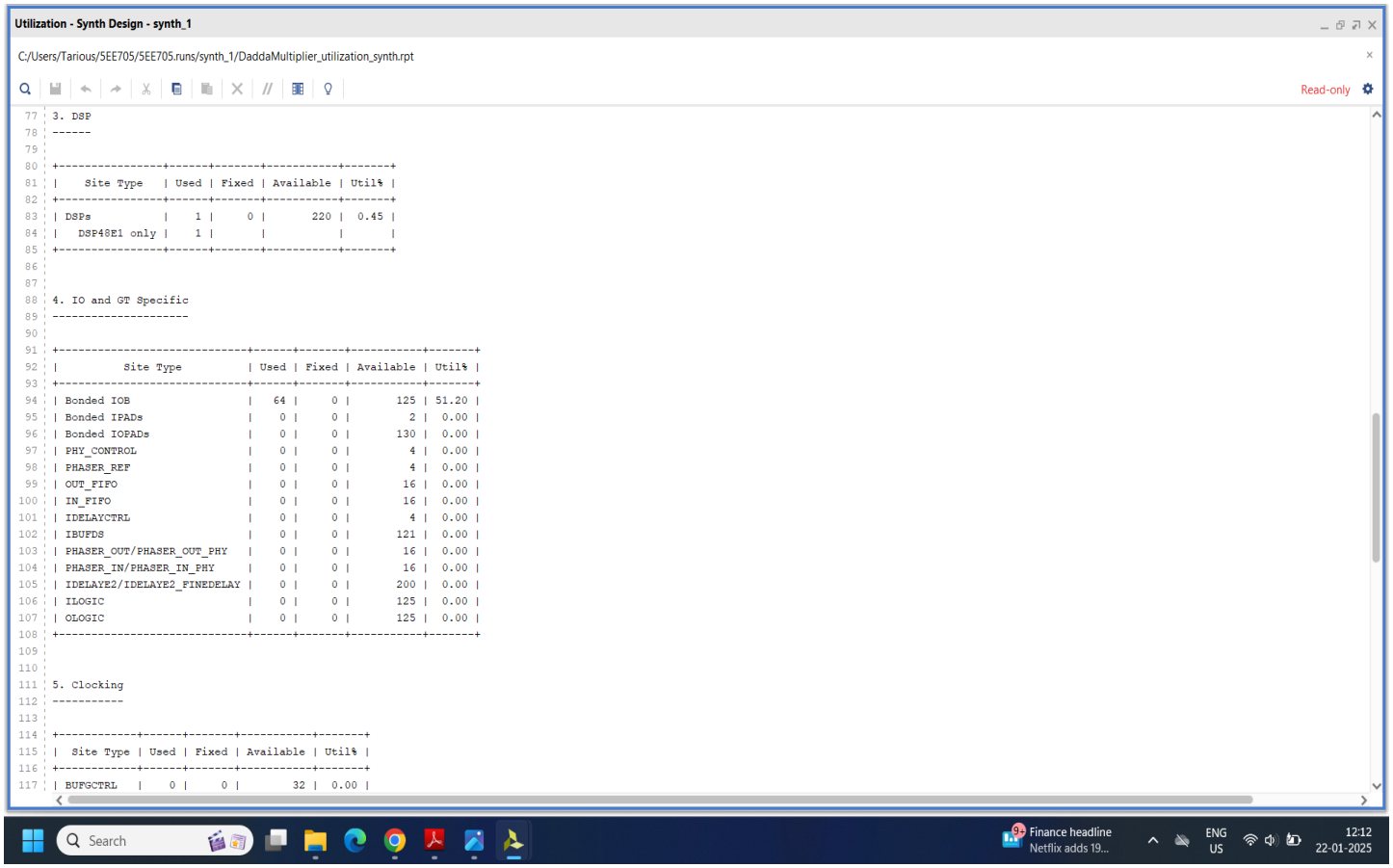
```
Copyright 1986-2020 Xilinx, Inc. All Rights Reserved.
----------------------------------------------------------------------------------------------------------------------------
| Tool Version : Vivado v.2020.2 (win64) Build 3064766 Wed Nov 18 09:12:45 MST 2020
| Date         : Wed Jan 22 12:09:05 2025
| Host         : LAPTOP-M216N101 running 64-bit major release  (build 9200)
| Command      : report_utilization -file DaddaMultiplier_utilization_synth.rpt -pb DaddaMultiplier_utilization_synth.pb
| Design       : DaddaMultiplier
| Device       : 7z020clg400-1
| Design State : Synthesized
----------------------------------------------------------------------------------------------------------------------------

Utilization Design Information

Table of Contents
-----------------
1. Slice Logic
1.1 Summary of Registers by Type
2. Memory
3. DSP
4. IO and GT Specific
5. Clocking
6. Specific Feature
7. Primitives
8. Black Boxes
9. Instantiated Netlists

1. Slice Logic
--------------

+-------------------------+------+-------+-----------+-------+
|        Site Type        | Used | Fixed | Available | Util% |
+-------------------------+------+-------+-----------+-------+
| Slice LUTs*             |    0 |     0 |     53200 |  0.00 |
|   LUT as Logic          |    0 |     0 |     53200 |  0.00 |
|   LUT as Memory         |    0 |     0 |     17400 |  0.00 |
| Slice Registers         |    0 |     0 |    106400 |  0.00 |
|   Register as Flip Flop |    0 |     0 |    106400 |  0.00 |
|   Register as Latch     |    0 |     0 |    106400 |  0.00 |
| F7 Muxes                |    0 |     0 |     26600 |  0.00 |
| F8 Muxes                |    0 |     0 |     13300 |  0.00 |
+-------------------------+------+-------+-----------+-------+
```

Utilization - Synth Design - synth_1

C:/Users/Tarious/5EE705/5EE705.runs/synth_1/DaddaMultiplier_utilization_synth.rpt

Read-only

```
* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.


1.1 Summary of Registers by Type
--------------------------------

+-------+--------------+-------------+--------------+
| Total | Clock Enable | Synchronous | Asynchronous |
+-------+--------------+-------------+--------------+
| 0     |            _ |           - |            - |
| 0     |            _ |           - |          Set |
| 0     |            _ |           - |        Reset |
| 0     |            _ |         Set |            - |
| 0     |            _ |       Reset |            - |
| 0     |          Yes |           - |            - |
| 0     |          Yes |           - |          Set |
| 0     |          Yes |           - |        Reset |
| 0     |          Yes |         Set |            - |
| 0     |          Yes |       Reset |            - |
+-------+--------------+-------------+--------------+


2. Memory
---------

+----------------+------+-------+-----------+-------+
|    Site Type   | Used | Fixed | Available | Util% |
+----------------+------+-------+-----------+-------+
| Block RAM Tile |    0 |     0 |       140 |  0.00 |
|   RAMB36/FIFO* |    0 |     0 |       140 |  0.00 |
|   RAMB18       |    0 |     0 |       280 |  0.00 |
+----------------+------+-------+-----------+-------+
* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accomm


3. DSP
------

+----------------+------+-------+-----------+-------+
|    Site Type   | Used | Fixed | Available | Util% |
+----------------+------+-------+-----------+-------+
```

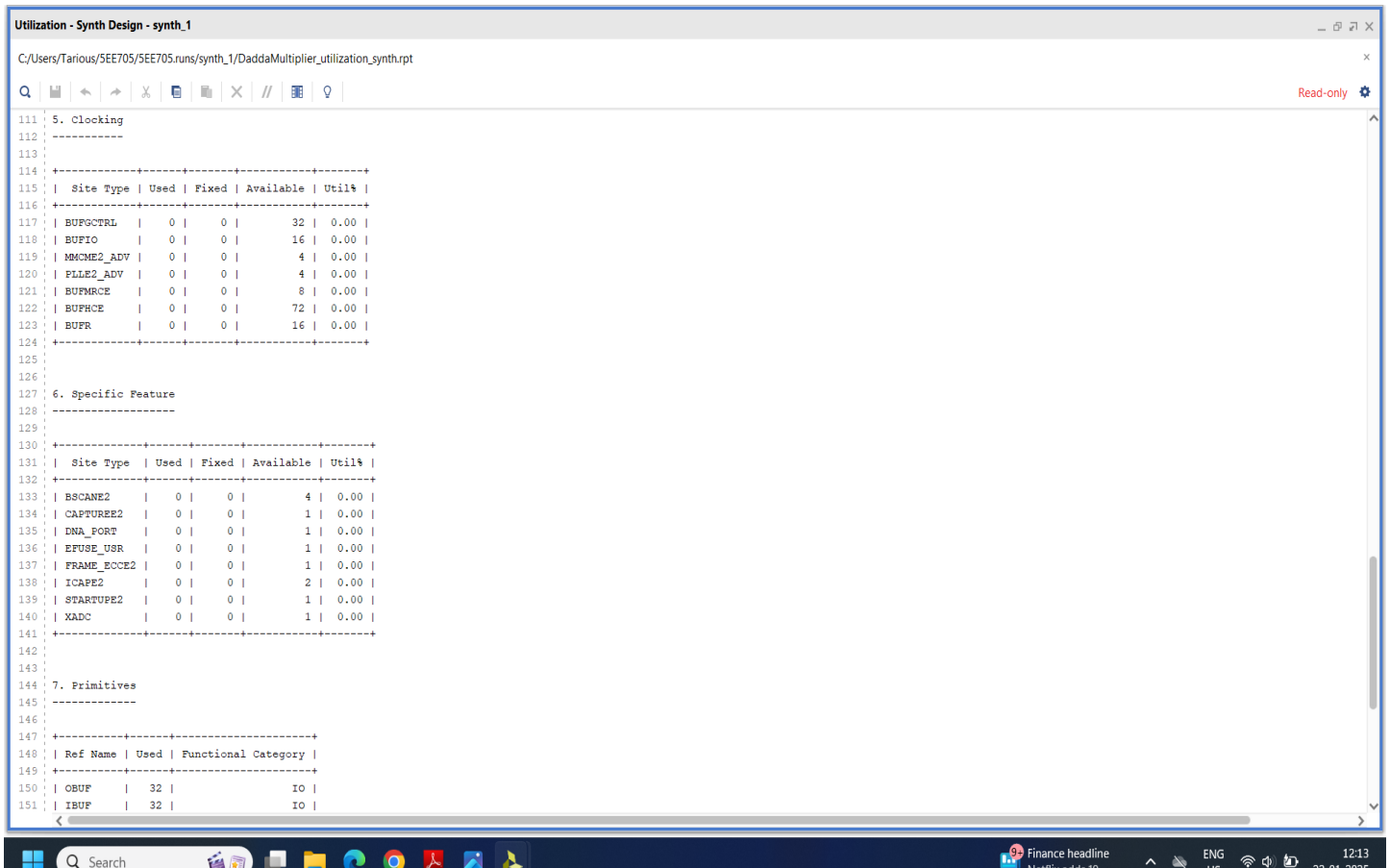


Utilization - Synth Design - synth_1

C:/Users/Tarious/5EE705/5EE705.runs/synth_1/DaddaMultiplier_utilization_synth.rpt

Read-only

```
3. DSP
------

+----------------+------+-------+-----------+-------+
|    Site Type   | Used | Fixed | Available | Util% |
+----------------+------+-------+-----------+-------+
| DSPs           |    1 |     0 |       220 |  0.45 |
|   DSP48E1 only |    1 |       |           |       |
+----------------+------+-------+-----------+-------+


4. IO and GT Specific
---------------------

+-----------------------------+------+-------+-----------+-------+
|          Site Type          | Used | Fixed | Available | Util% |
+-----------------------------+------+-------+-----------+-------+
| Bonded IOB                  |   64 |     0 |       125 | 51.20 |
| Bonded IPADs                |    0 |     0 |         2 |  0.00 |
| Bonded IOPADs               |    0 |     0 |       130 |  0.00 |
| PHY_CONTROL                 |    0 |     0 |         4 |  0.00 |
| PHASER_REF                  |    0 |     0 |         4 |  0.00 |
| OUT_FIFO                    |    0 |     0 |        16 |  0.00 |
| IN_FIFO                     |    0 |     0 |        16 |  0.00 |
| IDELAYCTRL                  |    0 |     0 |         4 |  0.00 |
| IBUFDS                      |    0 |     0 |       121 |  0.00 |
| PHASER_OUT/PHASER_OUT_PHY   |    0 |     0 |        16 |  0.00 |
| PHASER_IN/PHASER_IN_PHY     |    0 |     0 |        16 |  0.00 |
| IDELAYE2/IDELAYE2_FINEDELAY |    0 |     0 |       200 |  0.00 |
| ILOGIC                      |    0 |     0 |       125 |  0.00 |
| OLOGIC                      |    0 |     0 |       125 |  0.00 |
+-----------------------------+------+-------+-----------+-------+


5. Clocking
-----------

+------------+------+-------+-----------+-------+
|  Site Type | Used | Fixed | Available | Util% |
+------------+------+-------+-----------+-------+
| BUFGCTRL   |    0 |     0 |        32 |  0.00 |
```

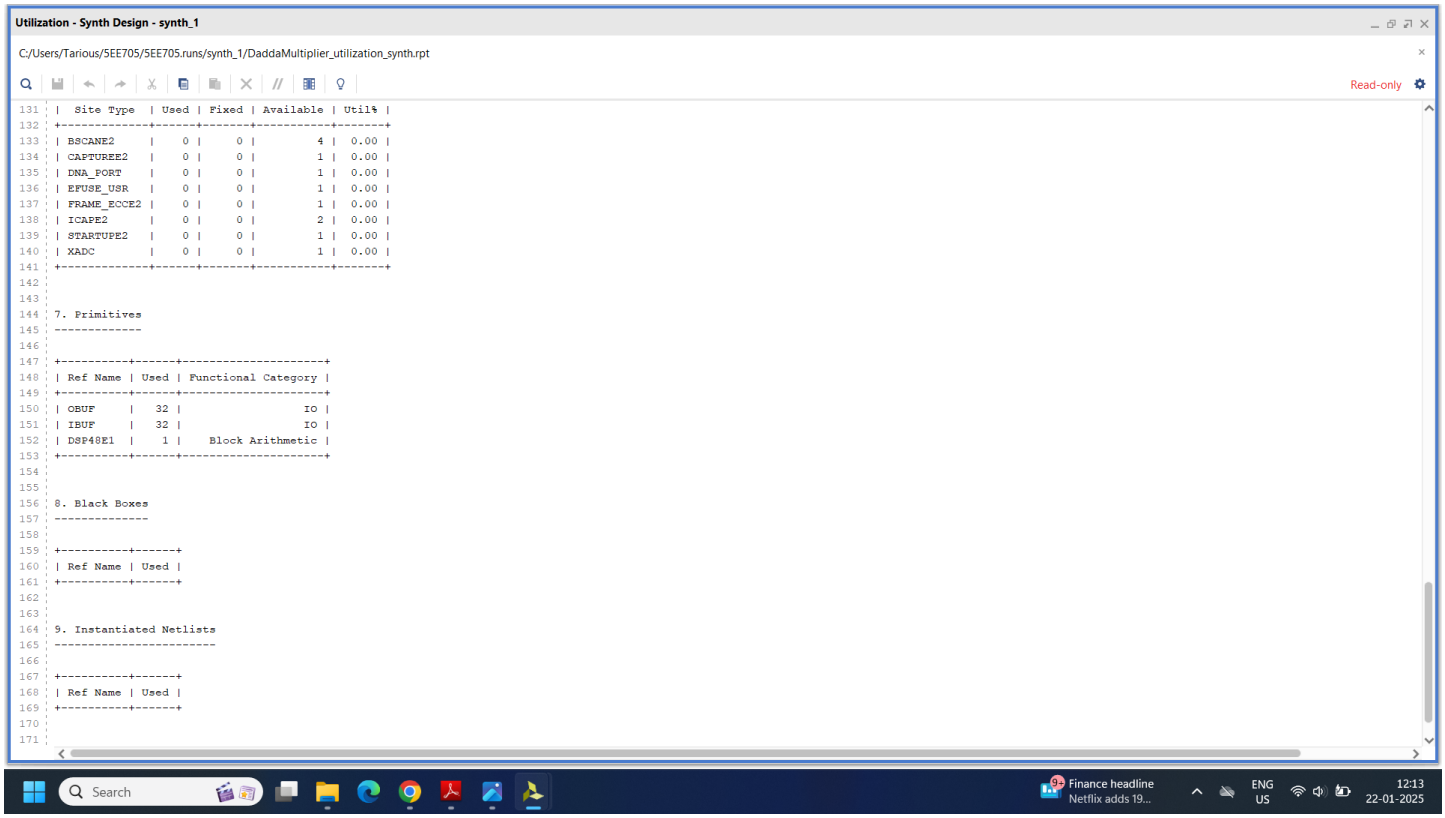



Utilization - Synth Design - synth_1

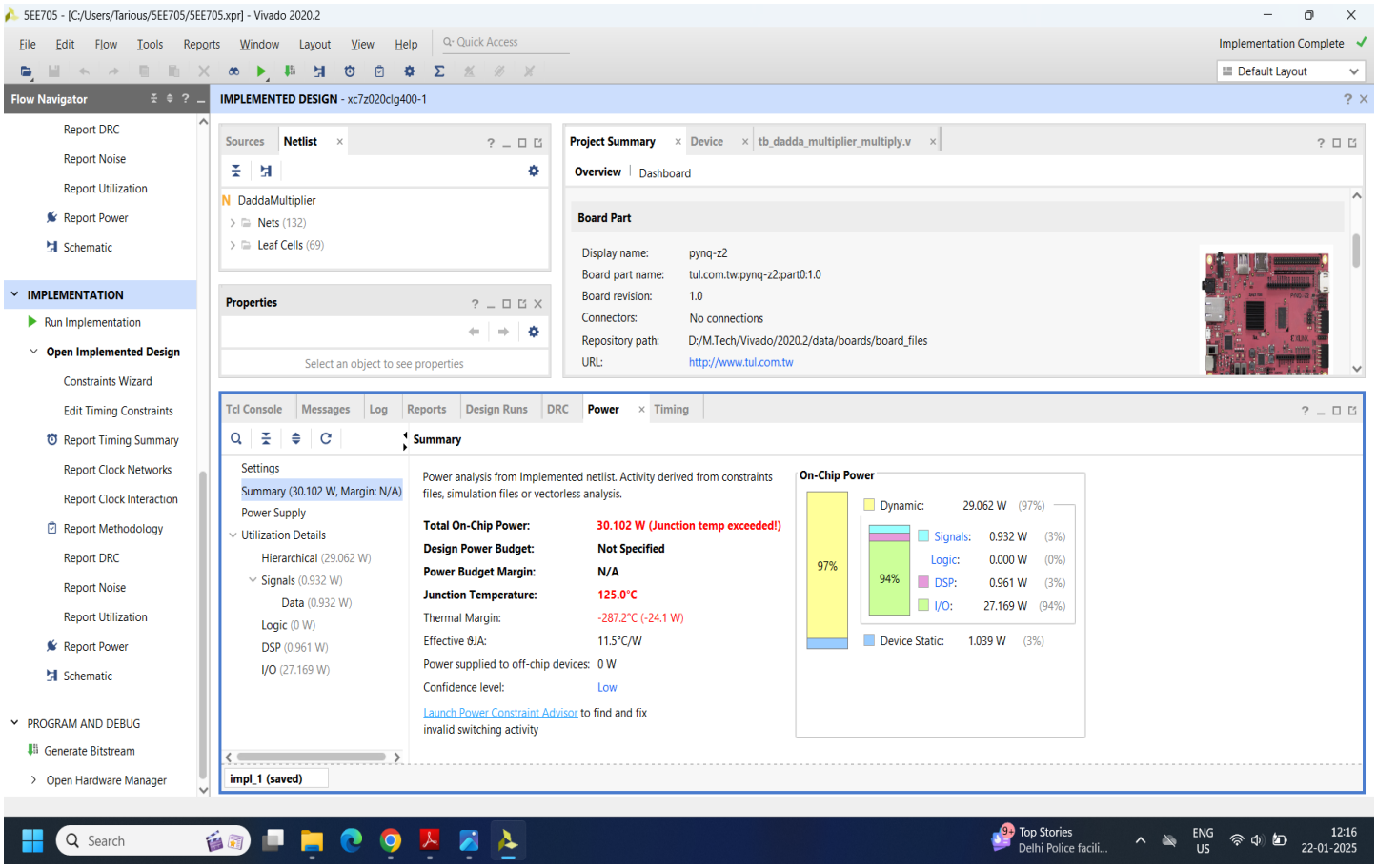
C:/Users/Tarious/5EE705/5EE705.runs/synth_1/DaddaMultiplier_utilization_synth.rpt

Read-only

```
5. Clocking
-----------

+------------+------+-------+-----------+-------+
|  Site Type | Used | Fixed | Available | Util% |
+------------+------+-------+-----------+-------+
| BUFGCTRL   |    0 |     0 |        32 |  0.00 |
| BUFIO      |    0 |     0 |        16 |  0.00 |
| MMCME2_ADV |    0 |     0 |         4 |  0.00 |
| PLLE2_ADV  |    0 |     0 |         4 |  0.00 |
| BUFMRCE    |    0 |     0 |         8 |  0.00 |
| BUFHCE     |    0 |     0 |        72 |  0.00 |
| BUFR       |    0 |     0 |        16 |  0.00 |
+------------+------+-------+-----------+-------+


6. Specific Feature
-------------------

+-------------+------+-------+-----------+-------+
|  Site Type  | Used | Fixed | Available | Util% |
+-------------+------+-------+-----------+-------+
| BSCANE2     |    0 |     0 |         4 |  0.00 |
| CAPTUREE2   |    0 |     0 |         1 |  0.00 |
| DNA_PORT    |    0 |     0 |         1 |  0.00 |
| EFUSE_USR   |    0 |     0 |         1 |  0.00 |
| FRAME_ECCE2 |    0 |     0 |         1 |  0.00 |
| ICAPE2      |    0 |     0 |         2 |  0.00 |
| STARTUPE2   |    0 |     0 |         1 |  0.00 |
| XADC        |    0 |     0 |         1 |  0.00 |
+-------------+------+-------+-----------+-------+


7. Primitives
-------------

+----------+------+---------------------+
| Ref Name | Used | Functional Category |
+----------+------+---------------------+
| OBUF     |   32 |                  IO |
| IBUF     |   32 |                  IO |
```


Utilization - Synth Design - synth_1
C:/Users/Tarious/5EE705/5EE705.runs/synth_1/DaddaMultiplier_utilization_synth.rpt
Read-only
Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00
7. Primitives
Ref Name	Used	Functional Category
OBUF	32	IO
IBUF	32	IO
DSP48E1	1	Block Arithmetic
8. Black Boxes
Ref Name	Used
9. Instantiated Netlists
Ref Name	Used
Search
Finance headline
Netflix adds 19...
ENG
US
12:13
22-01-2025

Power:


5EE705 - [C:/Users/Tarious/5EE705/5EE705.xpr] - Vivado 2020.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Implementation Complete
Default Layout
Flow Navigator
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
IMPLEMENTED DESIGN - xc7z020clg400-1
Sources
Netlist
DaddaMultiplier
Nets (132)
Leaf Cells (69)
Properties
Select an object to see properties
Project Summary
Device
tb_dadda_multiplier_multiply.v
Overview
Dashboard
Board Part
Display name: pynq-z2
Board part name: tul.com.tw:pynq-z2:part0:1.0
Board revision: 1.0
Connectors: No connections
Repository path: D:/M.Tech/Vivado/2020.2/data/boards/board_files
URL: http://www.tul.com.tw
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Summary
Settings
Summary (30.102 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (29.062 W)
Signals (0.932 W)
Data (0.932 W)
Logic (0 W)
DSP (0.961 W)
I/O (27.169 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 30.102 W (Junction temp exceeded!)
Design Power Budget: Not Specified
Power Budget Margin: N/A
Junction Temperature: 125.0°C
Thermal Margin: -287.2°C (-24.1 W)
Effective θJA: 11.5°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
97%
94%
Dynamic: 29.062 W (97%)
Signals: 0.932 W (3%)
Logic: 0.000 W (0%)
DSP: 0.961 W (3%)
I/O: 27.169 W (94%)
Device Static: 1.039 W (3%)
impl_1 (saved)
Search
Top Stories
Delhi Police facili...
ENG
US
12:16
22-01-2025

Using Dadda Multiplier

Verilog Code:

```
// Dadda Multiplier Implementation
module dadda_multiplier #(parameter WIDTH = 16)(
    input  [WIDTH-1:0] a, // Multiplier
    input  [WIDTH-1:0] b, // Multiplicand
    output [2*WIDTH-1:0] product // Product
);
    wire [WIDTH-1:0] partial_products[WIDTH-1:0];
    wire [2*WIDTH-1:0] sum[WIDTH-1:0];
    wire [2*WIDTH-1:0] carry[WIDTH-1:0];
    genvar i, j;

    // Step 1: Generate Partial Products
    generate
        for (i = 0; i < WIDTH; i = i + 1) begin
            for (j = 0; j < WIDTH; j = j + 1) begin
                assign partial_products[i][j] = a[i] & b[j];
            end
        end
    endgenerate

    // Step 2: Initialize First Stage
    assign sum[0] = {{WIDTH{1'b0}}, partial_products[0]}; // Pad to match product size
    assign carry[0] = 0;

    // Step 3: Dadda Tree Reduction
    generate
        for (i = 1; i < WIDTH; i = i + 1) begin
            dadda_reduce #(2*WIDTH) reduce_stage (
                .pp({{(WIDTH+i){1'b0}}, partial_products[i], {i{1'b0}}}), // Align PP properly
```

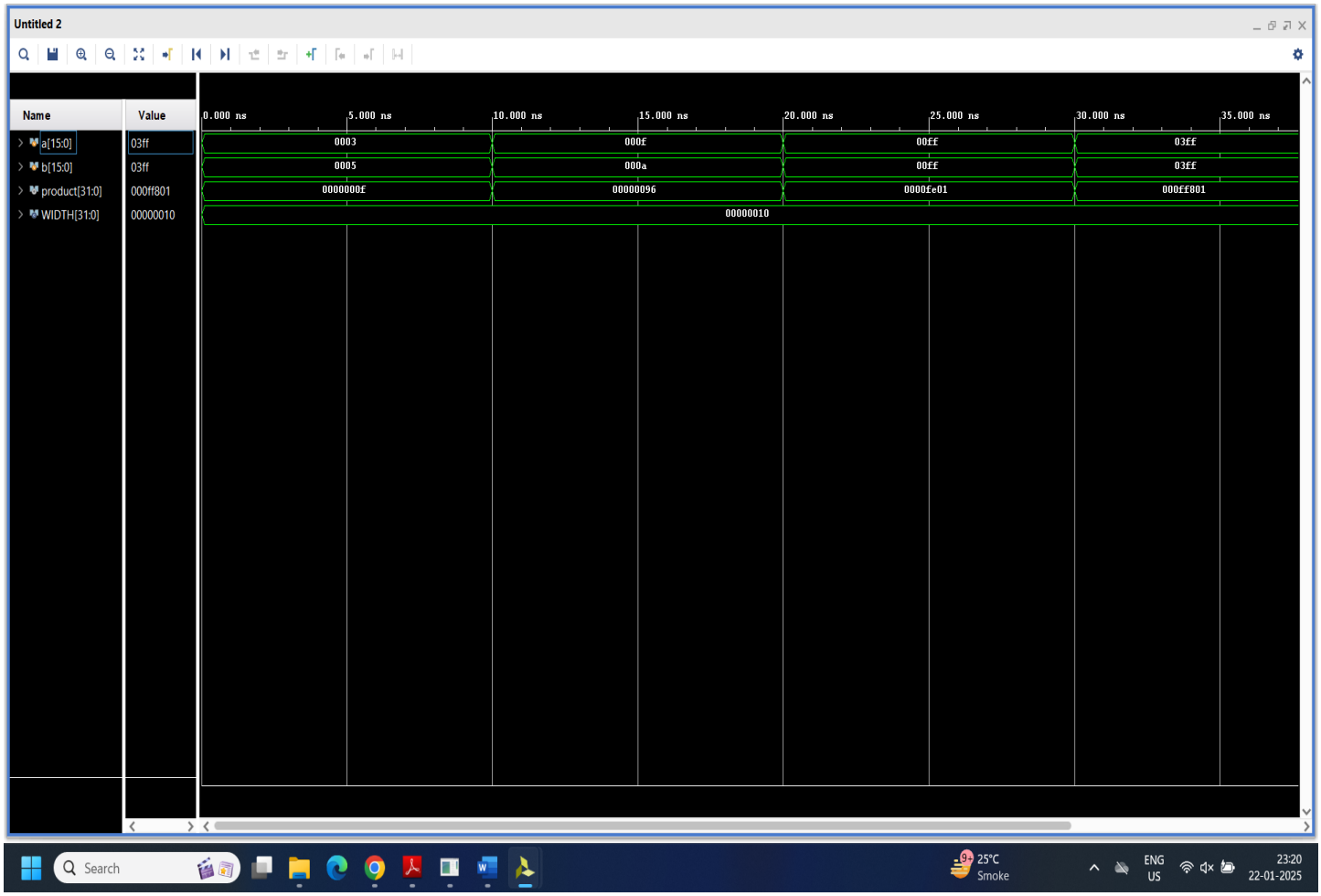
```
            .prev_sum(sum[i-1]),
            .prev_carry(carry[i-1]),
            .sum_out(sum[i]),
            .carry_out(carry[i])
        );
    end
endgenerate

// Step 4: Final Stage Addition
assign product = sum[WIDTH-1] + carry[WIDTH-1];

endmodule

// Dadda Reduction Stage
module dadda_reduce #(parameter WIDTH = 32)(
    input  [WIDTH-1:0] pp,         // Current Partial Product (Aligned)
    input  [WIDTH-1:0] prev_sum,   // Sum from Previous Stage
    input  [WIDTH-1:0] prev_carry, // Carry from Previous Stage
    output [WIDTH-1:0] sum_out,    // Sum Output
    output [WIDTH-1:0] carry_out   // Carry Output
);
    assign {carry_out, sum_out} = pp + prev_sum + prev_carry; // Full Addition
endmodule
```

Test Bench Code:

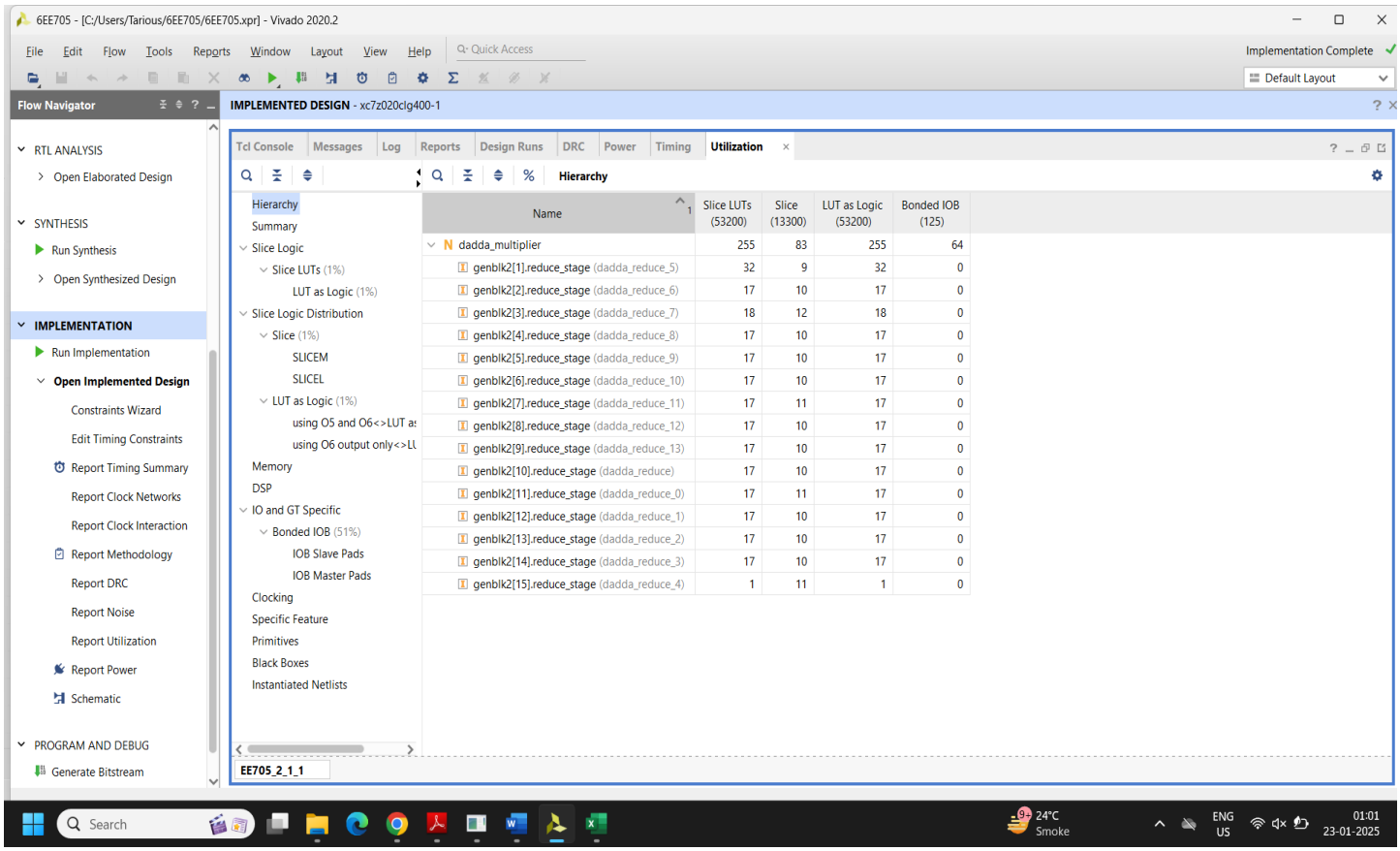
```
// Testbench for 16-bit Dadda Multiplier
module tb_dadda_multiplier;
    parameter WIDTH = 16;
    reg  [WIDTH-1:0] a, b;
    wire [2*WIDTH-1:0] product;
```

```
    // Instantiate the multiplier
    dadda_multiplier #(WIDTH) uut (
        .a(a),
        .b(b),
        .product(product)
    );

    initial begin
        $dumpfile("dadda_multiplier.vcd");
        $dumpvars(0, tb_dadda_multiplier);

        // Test cases
        a = 16'd3; b = 16'd5; #10;
        $display("A: %d, B: %d, Product: %d", a, b, product);

        a = 16'd15; b = 16'd10; #10;
        $display("A: %d, B: %d, Product: %d", a, b, product);

        a = 16'd255; b = 16'd255; #10;
        $display("A: %d, B: %d, Product: %d", a, b, product);

        a = 16'd1023; b = 16'd1023; #10;
        $display("A: %d, B: %d, Product: %d", a, b, product);

         a = 16'd65535; b = 16'd65534; #10;
        $display("A: %d, B: %d, Product: %d", a, b, product);

        $finish;
    end
endmodule
```

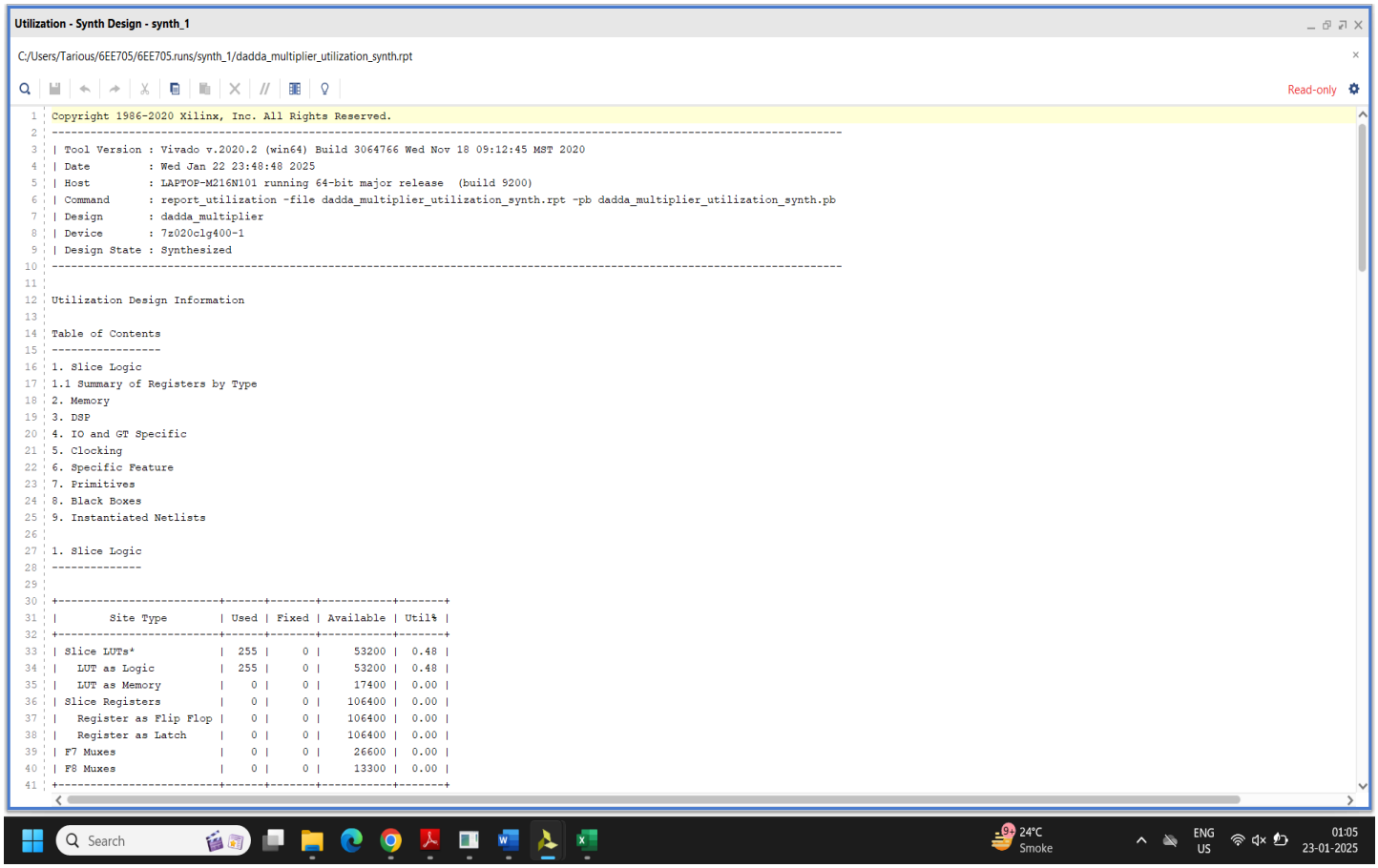
Simulation Waveform Using Dadda Multiplier:



Utilisation Report:



Resource Utilisation Report:

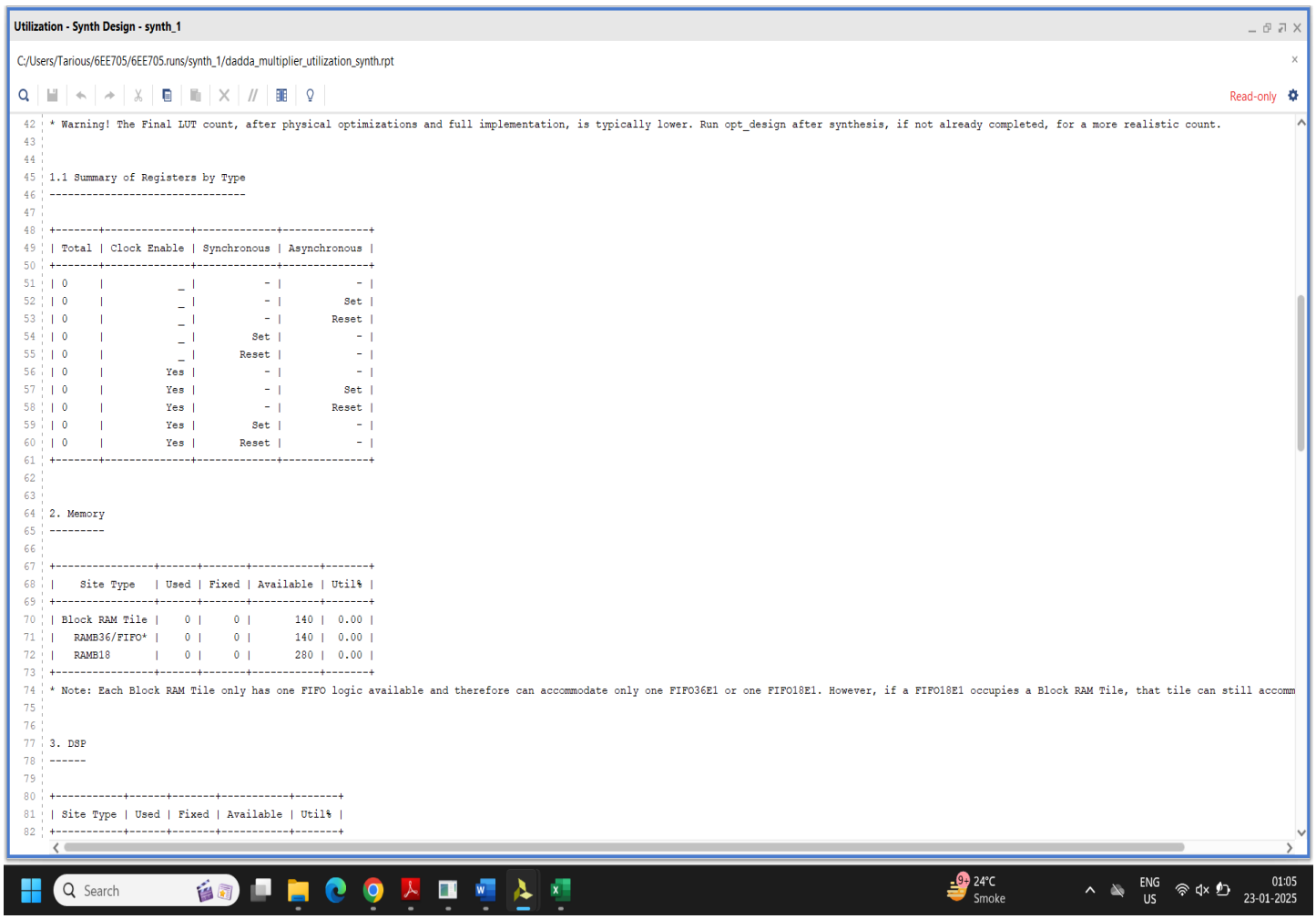


Utilization - Synth Design - synth_1

C:/Users/Tarious/6EE705/6EE705.runs/synth_1/dadda_multiplier_utilization_synth.rpt

Read-only

```
Copyright 1986-2020 Xilinx, Inc. All Rights Reserved.
------------------------------------------------------------------------------------------------------------------------
| Tool Version : Vivado v.2020.2 (win64) Build 3064766 Wed Nov 18 09:12:45 MST 2020
| Date         : Wed Jan 22 23:48:48 2025
| Host         : LAPTOP-M216N101 running 64-bit major release  (build 9200)
| Command      : report_utilization -file dadda_multiplier_utilization_synth.rpt -pb dadda_multiplier_utilization_synth.pb
| Design       : dadda_multiplier
| Device       : 7z020clg400-1
| Design State : Synthesized
------------------------------------------------------------------------------------------------------------------------

Utilization Design Information

Table of Contents
-----------------
1. Slice Logic
1.1 Summary of Registers by Type
2. Memory
3. DSP
4. IO and GT Specific
5. Clocking
6. Specific Feature
7. Primitives
8. Black Boxes
9. Instantiated Netlists

1. Slice Logic
--------------

+-------------------------+------+-------+-----------+-------+
|        Site Type        | Used | Fixed | Available | Util% |
+-------------------------+------+-------+-----------+-------+
| Slice LUTs*             |  255 |     0 |     53200 |  0.48 |
|   LUT as Logic          |  255 |     0 |     53200 |  0.48 |
|   LUT as Memory         |    0 |     0 |     17400 |  0.00 |
| Slice Registers         |    0 |     0 |    106400 |  0.00 |
|   Register as Flip Flop |    0 |     0 |    106400 |  0.00 |
|   Register as Latch     |    0 |     0 |    106400 |  0.00 |
| F7 Muxes                |    0 |     0 |     26600 |  0.00 |
| F8 Muxes                |    0 |     0 |     13300 |  0.00 |
+-------------------------+------+-------+-----------+-------+
```

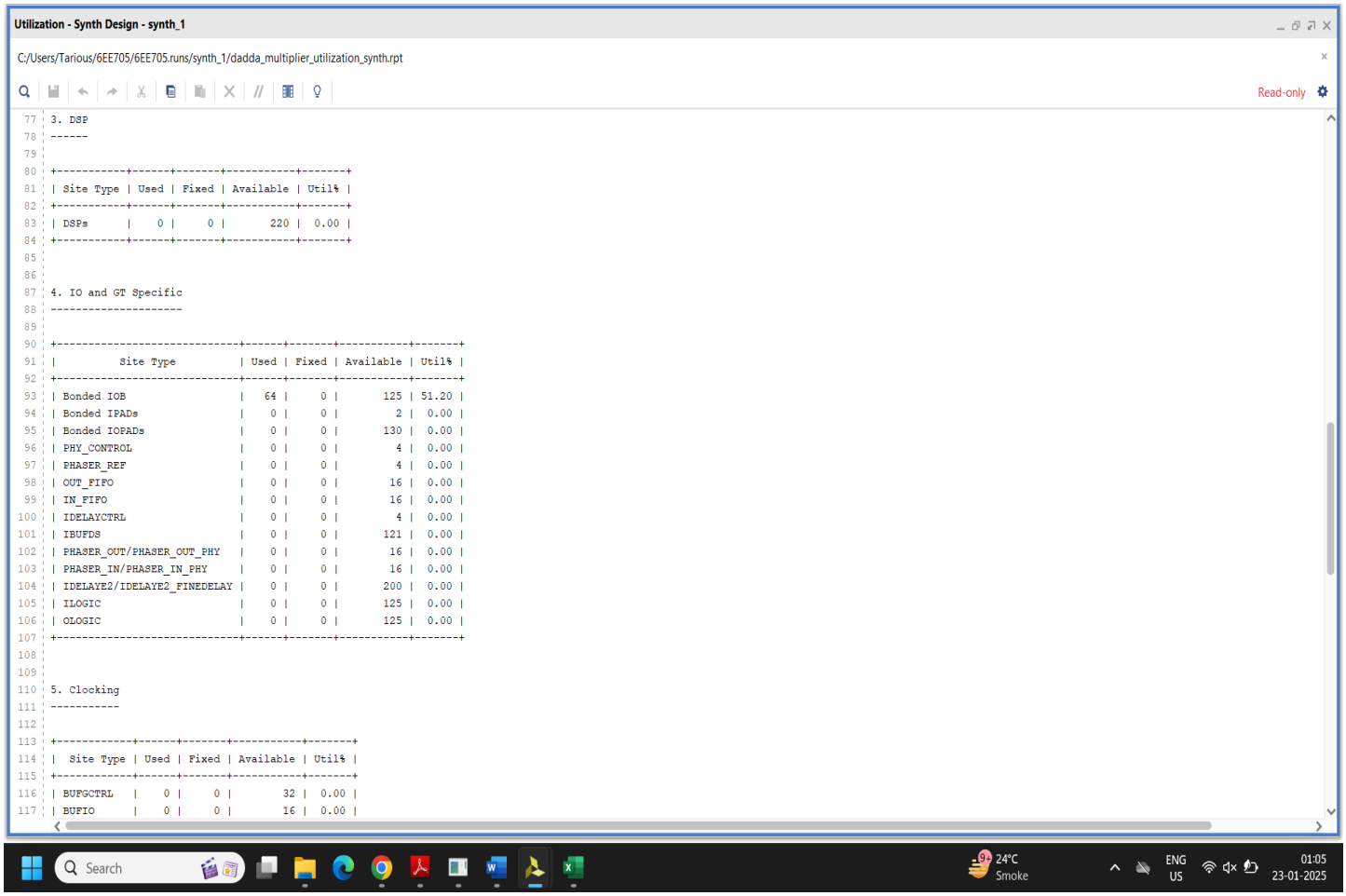



Utilization - Synth Design - synth_1

C:/Users/Tarious/6EE705/6EE705.runs/synth_1/dadda_multiplier_utilization_synth.rpt

Read-only

```
* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.


1.1 Summary of Registers by Type
--------------------------------

+-------+--------------+-------------+--------------+
| Total | Clock Enable | Synchronous | Asynchronous |
+-------+--------------+-------------+--------------+
| 0     |            _ |           - |            - |
| 0     |            _ |           - |          Set |
| 0     |            _ |           - |        Reset |
| 0     |            _ |         Set |            - |
| 0     |            _ |       Reset |            - |
| 0     |          Yes |           - |            - |
| 0     |          Yes |           - |          Set |
| 0     |          Yes |           - |        Reset |
| 0     |          Yes |         Set |            - |
| 0     |          Yes |       Reset |            - |
+-------+--------------+-------------+--------------+


2. Memory
---------

+----------------+------+-------+-----------+-------+
|    Site Type   | Used | Fixed | Available | Util% |
+----------------+------+-------+-----------+-------+
| Block RAM Tile |    0 |     0 |       140 |  0.00 |
|   RAMB36/FIFO* |    0 |     0 |       140 |  0.00 |
|   RAMB18       |    0 |     0 |       280 |  0.00 |
+----------------+------+-------+-----------+-------+
* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accomm


3. DSP
------

+-----------+------+-------+-----------+-------+
| Site Type | Used | Fixed | Available | Util% |
+-----------+------+-------+-----------+-------+
```



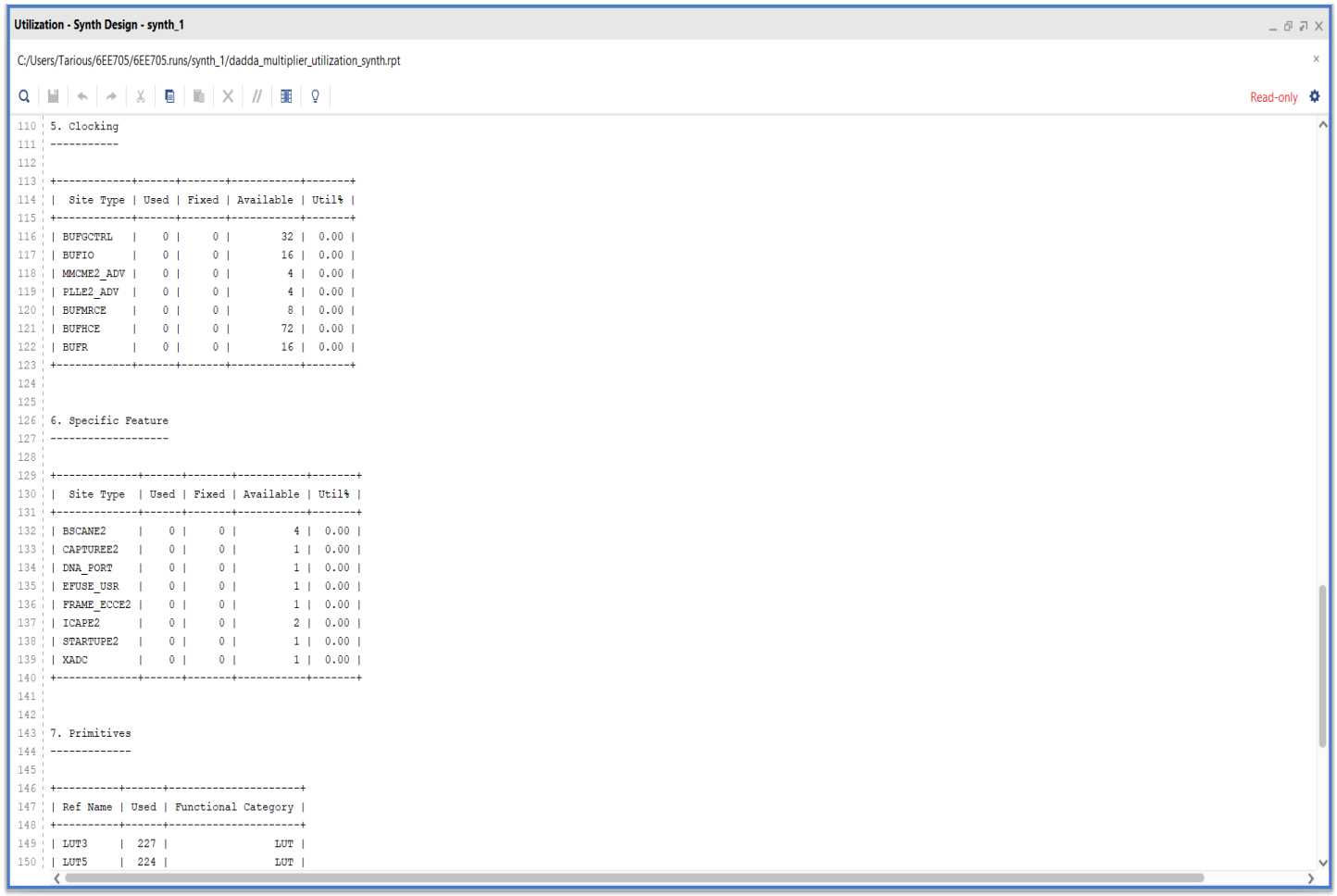
Utilization - Synth Design - synth_1

C:/Users/Tarious/6EE705/6EE705.runs/synth_1/dadda_multiplier_utilization_synth.rpt

Read-only

```
3. DSP
------

+-----------+------+-------+-----------+-------+
| Site Type | Used | Fixed | Available | Util% |
+-----------+------+-------+-----------+-------+
| DSPs      |    0 |     0 |       220 |  0.00 |
+-----------+------+-------+-----------+-------+


4. IO and GT Specific
---------------------

+-----------------------------+------+-------+-----------+-------+
|          Site Type          | Used | Fixed | Available | Util% |
+-----------------------------+------+-------+-----------+-------+
| Bonded IOB                  |   64 |     0 |       125 | 51.20 |
| Bonded IPADs                |    0 |     0 |         2 |  0.00 |
| Bonded IOPADs               |    0 |     0 |       130 |  0.00 |
| PHY_CONTROL                 |    0 |     0 |         4 |  0.00 |
| PHASER_REF                  |    0 |     0 |         4 |  0.00 |
| OUT_FIFO                    |    0 |     0 |        16 |  0.00 |
| IN_FIFO                     |    0 |     0 |        16 |  0.00 |
| IDELAYCTRL                  |    0 |     0 |         4 |  0.00 |
| IBUFDS                      |    0 |     0 |       121 |  0.00 |
| PHASER_OUT/PHASER_OUT_PHY   |    0 |     0 |        16 |  0.00 |
| PHASER_IN/PHASER_IN_PHY     |    0 |     0 |        16 |  0.00 |
| IDELAYE2/IDELAYE2_FINEDELAY |    0 |     0 |       200 |  0.00 |
| ILOGIC                      |    0 |     0 |       125 |  0.00 |
| OLOGIC                      |    0 |     0 |       125 |  0.00 |
+-----------------------------+------+-------+-----------+-------+


5. Clocking
-----------

+------------+------+-------+-----------+-------+
|  Site Type | Used | Fixed | Available | Util% |
+------------+------+-------+-----------+-------+
| BUFGCTRL   |    0 |     0 |        32 |  0.00 |
| BUFIO      |    0 |     0 |        16 |  0.00 |
```


Search 24°C Smoke ENG US 01:05 23-01-2025

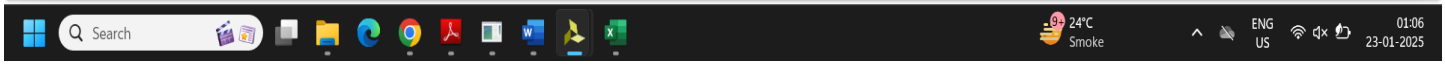


Utilization - Synth Design - synth_1

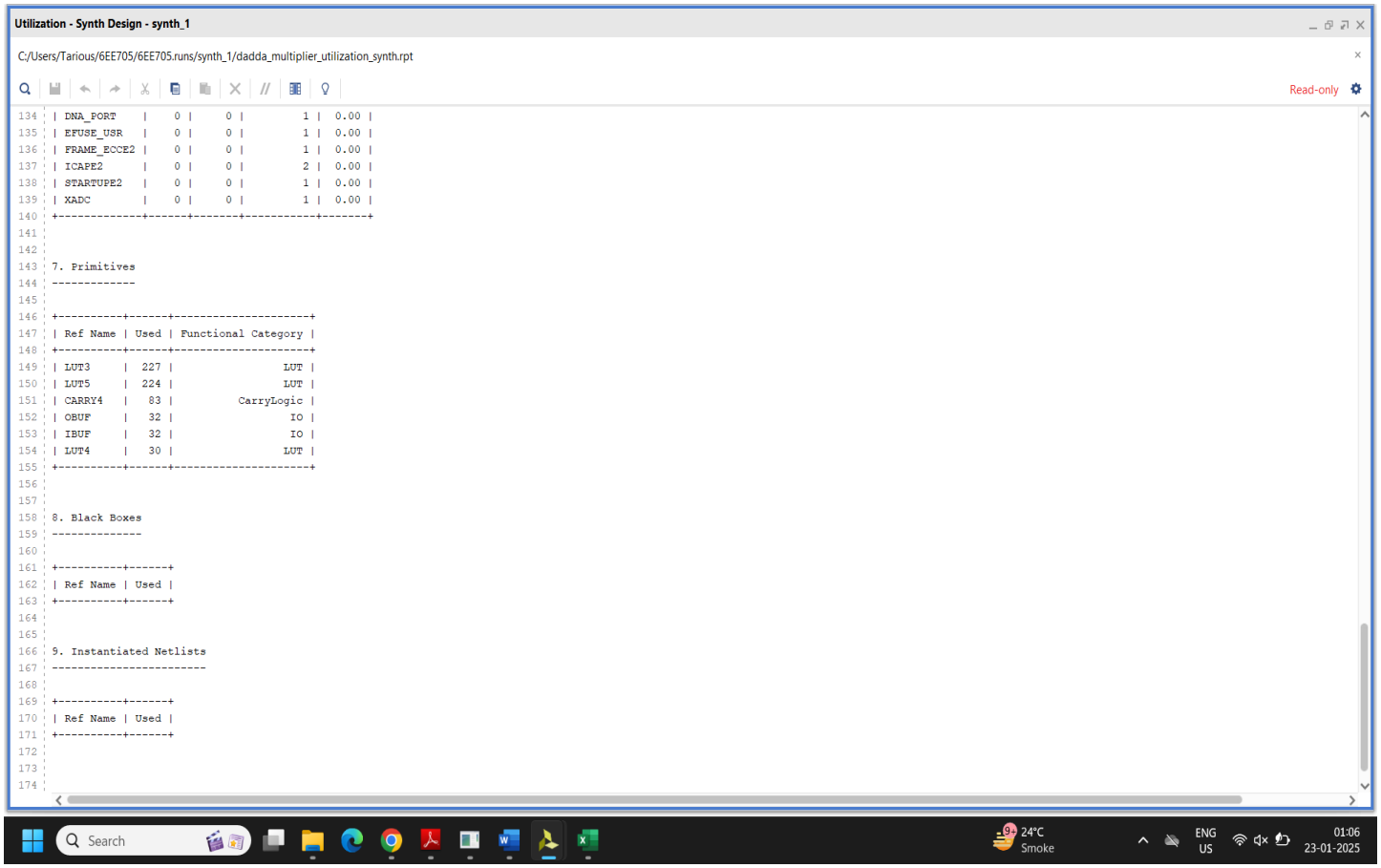
C:/Users/Tarious/6EE705/6EE705.runs/synth_1/dadda_multiplier_utilization_synth.rpt

Read-only

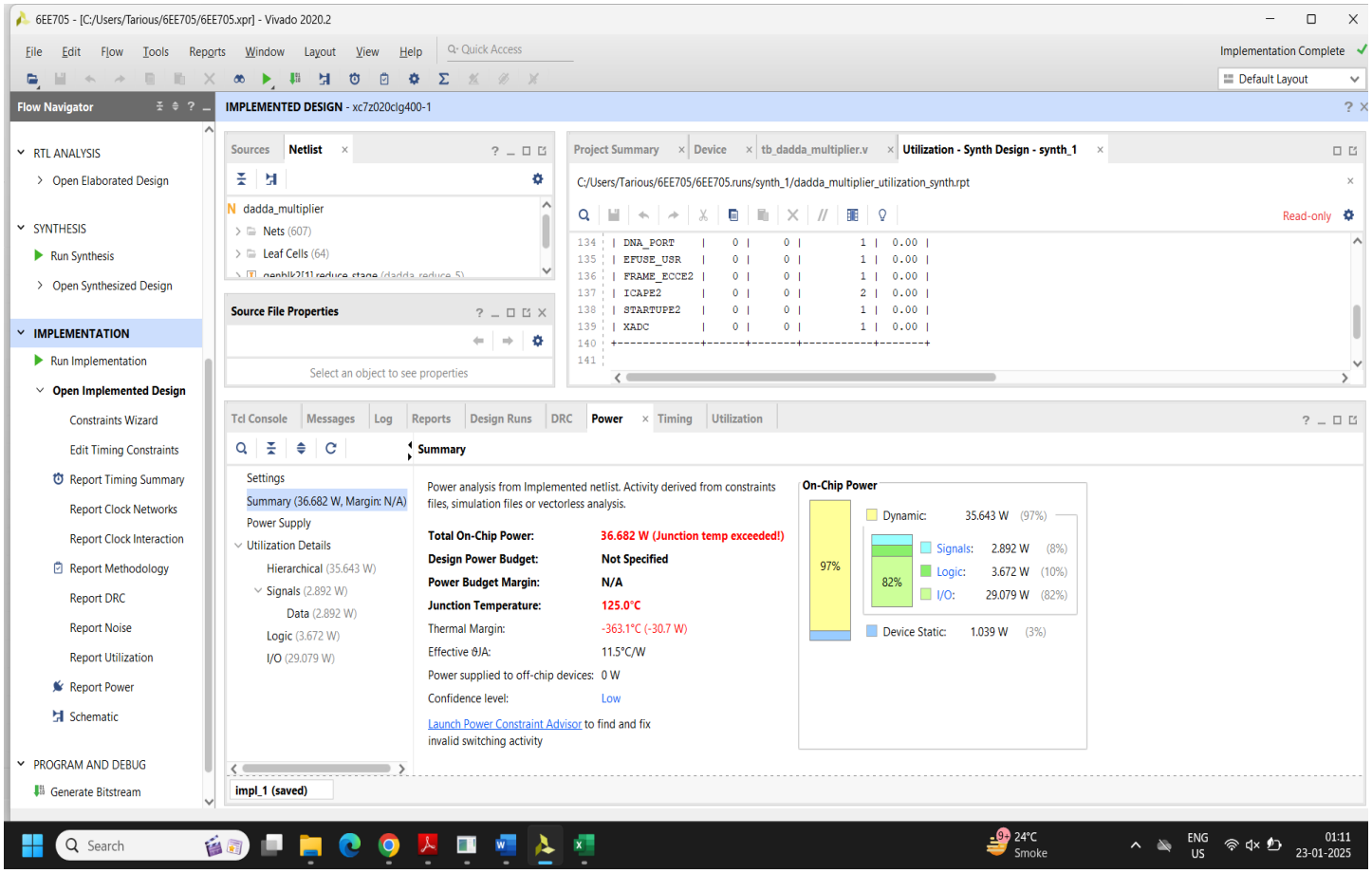
```
5. Clocking
-----------

+------------+------+-------+-----------+-------+
|  Site Type | Used | Fixed | Available | Util% |
+------------+------+-------+-----------+-------+
| BUFGCTRL   |    0 |     0 |        32 |  0.00 |
| BUFIO      |    0 |     0 |        16 |  0.00 |
| MMCME2_ADV |    0 |     0 |         4 |  0.00 |
| PLLE2_ADV  |    0 |     0 |         4 |  0.00 |
| BUFMRCE    |    0 |     0 |         8 |  0.00 |
| BUFHCE     |    0 |     0 |        72 |  0.00 |
| BUFR       |    0 |     0 |        16 |  0.00 |
+------------+------+-------+-----------+-------+


6. Specific Feature
-------------------

+-------------+------+-------+-----------+-------+
|  Site Type  | Used | Fixed | Available | Util% |
+-------------+------+-------+-----------+-------+
| BSCANE2     |    0 |     0 |         4 |  0.00 |
| CAPTUREE2   |    0 |     0 |         1 |  0.00 |
| DNA_PORT    |    0 |     0 |         1 |  0.00 |
| EFUSE_USR   |    0 |     0 |         1 |  0.00 |
| FRAME_ECCE2 |    0 |     0 |         1 |  0.00 |
| ICAPE2      |    0 |     0 |         2 |  0.00 |
| STARTUPE2   |    0 |     0 |         1 |  0.00 |
| XADC        |    0 |     0 |         1 |  0.00 |
+-------------+------+-------+-----------+-------+


7. Primitives
-------------

+----------+------+---------------------+
| Ref Name | Used | Functional Category |
+----------+------+---------------------+
| LUT3     |  227 |                 LUT |
| LUT5     |  224 |                 LUT |
```



Search 24°C Smoke ENG US 01:06 23-01-2025


Utilization - Synth Design - synth_1
C:/Users/Tarious/6EE705/6EE705.runs/synth_1/dadda_multiplier_utilization_synth.rpt
Read-only
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00
7. Primitives
Ref Name	Used	Functional Category
LUT3	227	LUT
LUT5	224	LUT
CARRY4	83	CarryLogic
OBUF	32	IO
IBUF	32	IO
LUT4	30	LUT
8. Black Boxes
Ref Name	Used
9. Instantiated Netlists
Ref Name	Used
Search
24°C Smoke
ENG US
01:06 23-01-2025

Power:


6EE705 - [C:/Users/Tarious/6EE705/6EE705.xpr] - Vivado 2020.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Implementation Complete
Default Layout
Flow Navigator
IMPLEMENTED DESIGN - xc7z020clg400-1
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
Generate Bitstream
Sources
Netlist
dadda_multiplier
Nets (607)
Leaf Cells (64)
Source File Properties
Select an object to see properties
Project Summary
Device
tb_dadda_multiplier.v
Utilization - Synth Design - synth_1
C:/Users/Tarious/6EE705/6EE705.runs/synth_1/dadda_multiplier_utilization_synth.rpt
Read-only
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Utilization
Summary
Settings
Summary (36.682 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (35.643 W)
Signals (2.892 W)
Data (2.892 W)
Logic (3.672 W)
I/O (29.079 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 36.682 W (Junction temp exceeded!)
Design Power Budget: Not Specified
Power Budget Margin: N/A
Junction Temperature: 125.0°C
Thermal Margin: -363.1°C (-30.7 W)
Effective θJA: 11.5°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
97%
82%
Dynamic: 35.643 W (97%)
Signals: 2.892 W (8%)
Logic: 3.672 W (10%)
I/O: 29.079 W (82%)
Device Static: 1.039 W (3%)
impl_1 (saved)
Search
24°C Smoke
ENG US
01:11 23-01-2025