Chapter 1
Analog-to-Digital Converter (ATD10B8CV2) Block Description

1.1 Introduction

The ATD10B8C is an 8-channel, 10-bit, multiplexed input successive approximation analog-to-digital converter. Refer to device electrical specifications for ATD accuracy.

The block is designed to be upwards compatible with the 68HC11 standard 8-bit A/D converter. In addition, there are new operating modes that are unique to the HC12 design.

1.1.1 Features

- 8/10-bit resolution.
- 7 µsec, 10-bit single conversion time.
- Sample buffer amplifier.
- Programmable sample time.
- Left/right justified, signed/unsigned result data.
- External trigger control.
- Conversion completion interrupt generation.
- Analog input multiplexer for eight analog input channels.
- Analog/digital input pin multiplexing.
- 1-to-8 conversion sequence lengths.
- Continuous conversion mode.
- Multiple channel scans.

1.1.2 Modes of Operation

1.1.2.1 Conversion Modes

There is software programmable selection between performing **single** or **continuous conversion** on a **single channel** or **multiple channels**.

1.1.2.2 MCU Operating Modes

- **Stop Mode**

  Entering stop mode causes all clocks to halt and thus the system is placed in a minimum power standby mode. This aborts any conversion sequence in progress. During recovery from stop mode, there must be a minimum delay for the stop recovery time, t_{SR}, before initiating a new ATD conversion sequence.

- **Wait Mode**

  Entering wait mode the ATD conversion either continues or aborts for low power depending on the logical value of the AWAIT bit.

- **Freeze Mode**

  In freeze mode the ATD10B8C will behave according to the logical values of the FRZ1 and FRZ0 bits. This is useful for debugging and emulation.

## 1.1.3 Block Diagram

Figure 1-1 is a block diagram of the ATD.
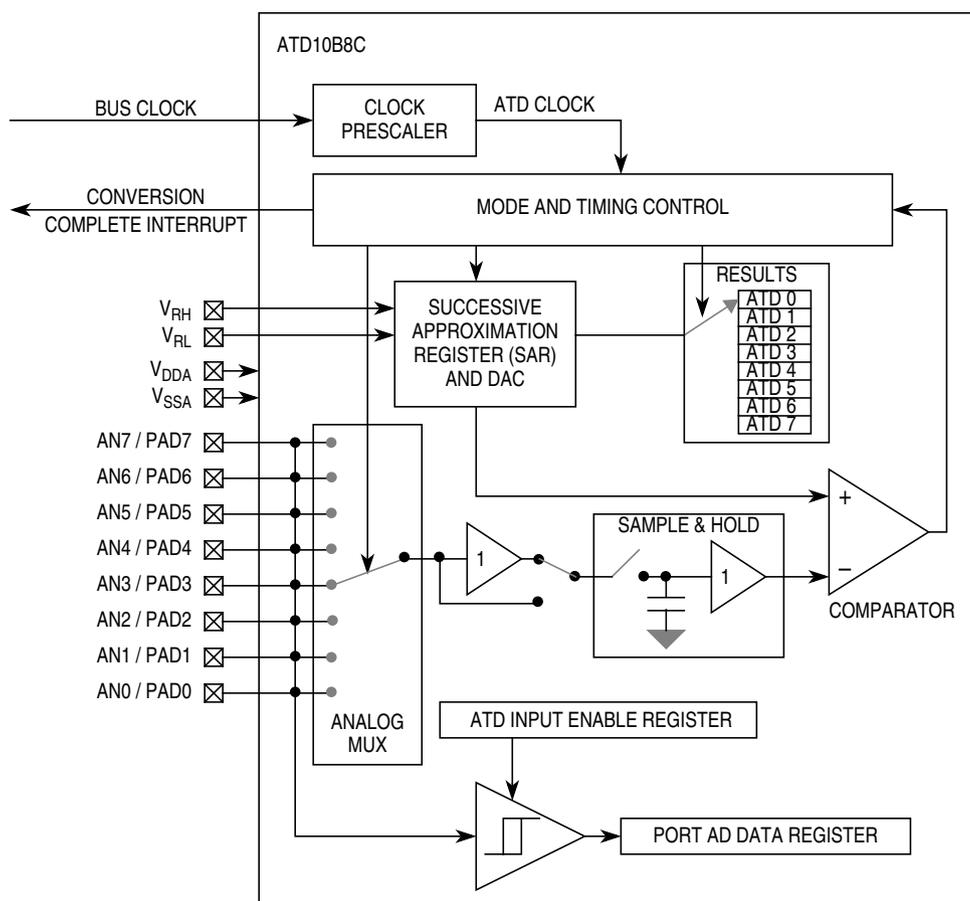
Figure 1-1. ATD10B8C Block Diagram

1.2 Signal Description

The ATD10B8C has a total of 12 external pins.

1.2.1 AN7 / ETRIG / PAD7

This pin serves as the analog input channel 7. It can be configured to provide an external trigger for the ATD conversion. It can be configured as general-purpose digital I/O.

1.2.2 AN6 / PAD6

This pin serves as the analog input channel 6. It can be configured as general-purpose digital I/O.

1.2.3 AN5 / PAD5

This pin serves as the analog input channel 5. It can be configured as general-purpose digital I/O.

1.2.4 AN4 / PAD4

This pin serves as the analog input channel 4. It can be configured as general-purpose digital I/O.

1.2.5 AN3 / PAD3

This pin serves as the analog input channel 3. It can be configured as general-purpose digital I/O.

1.2.6 AN2 / PAD2

This pin serves as the analog input channel 2. It can be configured as general-purpose digital I/O.

1.2.7 AN1 / PAD1

This pin serves as the analog input channel 1. It can be configured as general-purpose digital I/O.

1.2.8 AN0 / PAD0

This pin serves as the analog input channel 0. It can be configured as general-purpose digital I/O.

1.2.9 V_{RH}, V_{RL}

V_{RH} is the high reference voltage and V_{RL} is the low reference voltage for ATD conversion.

1.2.10 V_{DDA}, V_{SSA}

These pins are the power supplies for the analog circuitry of the ATD10B8C block.

1.3 Memory Map and Registers

This section provides a detailed description of all registers accessible in the ATD10B8C.

1.3.1 Module Memory Map

Figure 1-2 gives an overview on all ATD10B8C registers.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	ATDCTL0	R	0	0	0	0	0	0	0	0
		W								
0x0001	ATDCTL1	R	0	0	0	0	0	0	0	0
		W								
0x0002	ATDCTL2	R	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ASCIF
		W								
0x0003	ATDCTL3	R	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		W								
0x0004	ATDCTL4	R	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		W								
0x0005	ATDCTL5	R	DJM	DSGN	SCAN	MULT	0	CC	CB	CA
		W								
0x0006	ATDSTAT0	R	SCF	0	ETORF	FIFOR	0	CC2	CC1	CC0
		W								
0x0007	Unimplemented	R	0	0	0	0	0	0	0	0
		W								
0x0008	ATDTEST0	R	U	U	U	U	U	U	U	U
		W								
0x0009	ATDTEST1	R	U	U	U	U	U	U	U	SC
		W								
0x000A	Unimplemented	R	0	0	0	0	0	0	0	0
		W								
0x000B	ATDSTAT1	R	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
		W								
0x000C	Unimplemented	R	0	0	0	0	0	0	0	0
		W								
0x000D	ATDDIEN	R	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
		W								
0x000E	Unimplemented	R	0	0	0	0	0	0	0	0
		W								
0x000F	PORTAD	R	PTAD7	PTAD6	PTAD5	PTAD4	PTAD3	PTAD2	PTAD1	PTAD0
		W								

[ ] = Unimplemented or Reserved

Figure 1-2. ATD Register Summary (Sheet 1 of 4)

Left Justified Result Data

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0010	ATDDR0H	R	BIT 9 MSB / BIT 7 MSB	BIT 8 / BIT 6	BIT 7 / BIT 5	BIT 6 / BIT 4	BIT 5 / BIT 3	BIT 4 / BIT 2	BIT 3 / BIT 1	BIT 2 / BIT 0
		W								
0x0011	ATDDR0L	R	BIT 1 / u	BIT 0 / u	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0
		W								
0x0012	ATDDR1H	R	BIT 9 MSB / BIT 7 MSB	BIT 8 / BIT 6	BIT 7 / BIT 5	BIT 6 / BIT 4	BIT 5 / BIT 3	BIT 4 / BIT 2	BIT 3 / BIT 1	BIT 2 / BIT 0
		W								
0x0013	ATDDR1L	R	BIT 1 / u	BIT 0 / u	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0
		W								
0x0014	ATDDR2H	R	BIT 9 MSB / BIT 7 MSB	BIT 8 / BIT 6	BIT 7 / BIT 5	BIT 6 / BIT 4	BIT 5 / BIT 3	BIT 4 / BIT 2	BIT 3 / BIT 1	BIT 2 / BIT 0
		W								
0x0015	ATDDR2L	R	BIT 1 / u	BIT 0 / u	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0
		W								
0x0016	ATDDR3H	R	BIT 9 MSB / BIT 7 MSB	BIT 8 / BIT 6	BIT 7 / BIT 5	BIT 6 / BIT 4	BIT 5 / BIT 3	BIT 4 / BIT 2	BIT 3 / BIT 1	BIT 2 / BIT 0
		W								
0x0017	ATDDR3L	R	BIT 1 / u	BIT 0 / u	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0
		W								
0x0018	ATDDR4H	R	BIT 9 MSB / BIT 7 MSB	BIT 8 / BIT 6	BIT 7 / BIT 5	BIT 6 / BIT 4	BIT 5 / BIT 3	BIT 4 / BIT 2	BIT 3 / BIT 1	BIT 2 / BIT 0
		W								
0x0019	ATDDR4L	R	BIT 1 / u	BIT 0 / u	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0
		W								
0x001A	ATDDR5H	R	BIT 9 MSB / BIT 7 MSB	BIT 8 / BIT 6	BIT 7 / BIT 5	BIT 6 / BIT 4	BIT 5 / BIT 3	BIT 4 / BIT 2	BIT 3 / BIT 1	BIT 2 / BIT 0
		W								
0x001B	ATDDR5L	R	BIT 1 / u	BIT 0 / u	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0
		W								
0x001C	ATDDR6H	R	BIT 9 MSB / BIT 7 MSB	BIT 8 / BIT 6	BIT 7 / BIT 5	BIT 6 / BIT 4	BIT 5 / BIT 3	BIT 4 / BIT 2	BIT 3 / BIT 1	BIT 2 / BIT 0
		W								
0x001D	ATDDR6L	R	BIT 1 / u	BIT 0 / u	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0
		W								

= Unimplemented or Reserved

Figure 1-2. ATD Register Summary (Sheet 2 of 4)

Analog-To-Digital Converter Block Description, Rev. 2

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x001E	ATDDR7H	R	BIT 9 MSB / BIT 7 MSB	BIT 8 / BIT 6	BIT 7 / BIT 5	BIT 6 / BIT 4	BIT 5 / BIT 3	BIT 4 / BIT 2	BIT 3 / BIT 1	BIT 2 / BIT 0
		W								
0x001F	ATDDR7L	R	BIT 1 / u	BIT 0 / u	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0
		W								

Right Justified Result Data

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0010	ATDDR0H	R	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	BIT 9 MSB / 0	BIT 8 / 0
		W								
0x0011	ATDDR0L	R	BIT 7 / BIT 7 MSB	BIT 6 / BIT 6	BIT 5 / BIT 5	BIT 4 / BIT 4	BIT 3 / BIT 3	BIT 2 / BIT 2	BIT 1 / BIT 1	BIT 0 / BIT 0
		W								
0x0012	ATDDR1H	R	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	BIT 9 MSB / 0	BIT 8 / 0
		W								
0x0013	ATDDR1L	R	BIT 7 / BIT 7 MSB	BIT 6 / BIT 6	BIT 5 / BIT 5	BIT 4 / BIT 4	BIT 3 / BIT 3	BIT 2 / BIT 2	BIT 1 / BIT 1	BIT 0 / BIT 0
		W								
0x0014	ATDDR2H	R	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	BIT 9 MSB / 0	BIT 8 / 0
		W								
0x0015	ATDDR2L	R	BIT 7 / BIT 7 MSB	BIT 6 / BIT 6	BIT 5 / BIT 5	BIT 4 / BIT 4	BIT 3 / BIT 3	BIT 2 / BIT 2	BIT 1 / BIT 1	BIT 0 / BIT 0
		W								
0x0016	ATDDR3H	R	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	BIT 9 MSB / 0	BIT 8 / 0
		W								
0x0017	ATDDR3L	R	BIT 7 / BIT 7 MSB	BIT 6 / BIT 6	BIT 5 / BIT 5	BIT 4 / BIT 4	BIT 3 / BIT 3	BIT 2 / BIT 2	BIT 1 / BIT 1	BIT 0 / BIT 0
		W								
0x0018	ATDDR4H	R	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	BIT 9 MSB / 0	BIT 8 / 0
		W								
0x0019	ATDDR4L	R	BIT 7 / BIT 7 MSB	BIT 6 / BIT 6	BIT 5 / BIT 5	BIT 4 / BIT 4	BIT 3 / BIT 3	BIT 2 / BIT 2	BIT 1 / BIT 1	BIT 0 / BIT 0
		W								
0x001A	ATDDR5H	R	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	BIT 9 MSB / 0	BIT 8 / 0
		W								
0x001B	ATDDR5L	R	BIT 7 / BIT 7 MSB	BIT 6 / BIT 6	BIT 5 / BIT 5	BIT 4 / BIT 4	BIT 3 / BIT 3	BIT 2 / BIT 2	BIT 1 / BIT 1	BIT 0 / BIT 0
		W								

= Unimplemented or Reserved

Figure 1-2. ATD Register Summary (Sheet 3 of 4)

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x001C	ATDDR6H	R	0 0	0 0	0 0	0 0	0 0	0 0	BIT 9 MSB 0	BIT 8 0
		W								
0x001D	ATDDR6L	R	BIT 7 BIT 7 MSB	BIT 6 BIT 6	BIT 5 BIT 5	BIT 4 BIT 4	BIT 3 BIT 3	BIT 2 BIT 2	BIT 1 BIT 1	BIT 0 BIT 0
		W								
0x001E	ATDDR7H	R	0 0	0 0	0 0	0 0	0 0	0 0	BIT 9 MSB 0	BIT 8 0
		W								
0x001F	ATDDR7L	R	BIT 7 BIT 7 MSB	BIT 6 BIT 6	BIT 5 BIT 5	BIT 4 BIT 4	BIT 3 BIT 3	BIT 2 BIT 2	BIT 1 BIT 1	BIT 0 BIT 0
		W								

☐ = Unimplemented or Reserved

Figure 1-2. ATD Register Summary (Sheet 4 of 4)

NOTE

Register Address = Module Base Address + Address Offset, where the Module Base Address is defined at the MCU level and the Address Offset is defined at the module level.

1.3.2   Register Descriptions

This section describes in address order all the ATD10B8C registers and their individual bits.

1.3.2.1   Reserved Register (ATDCTL0)

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

☐ = Unimplemented or Reserved
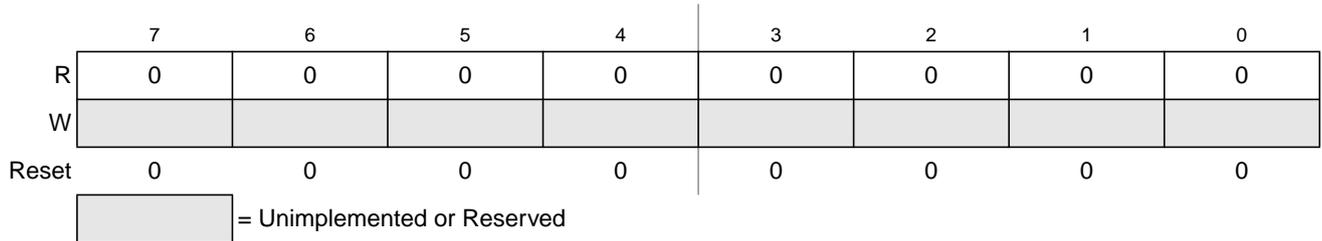
Figure 1-3. Reserved Register (ATDCTL0)

Read: Always read $00 in normal modes

Write: Unimplemented in normal modes

1.3.2.2   Reserved Register (ATDCTL1)

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

☐ = Unimplemented or Reserved
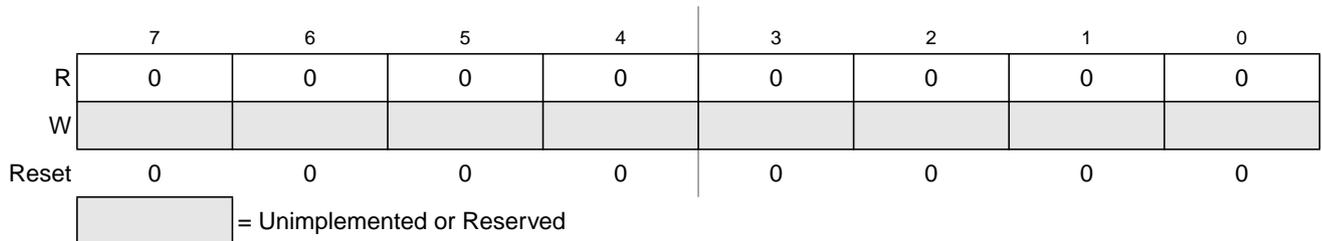
Figure 1-4. Reserved Register (ATDCTL1)

Read: Always read $00 in normal modes

Write: Unimplemented in normal modes

NOTE

Writing to this registers when in special modes can alter functionality.

1.3.2.3   ATD Control Register 2 (ATDCTL2)

This register controls power down, interrupt, and external trigger. Writes to this register will abort current conversion sequence but will not start a new sequence.

Module Base + 0x0002

|	7	6	5	4	3	2	1	0
R	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ASCIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved
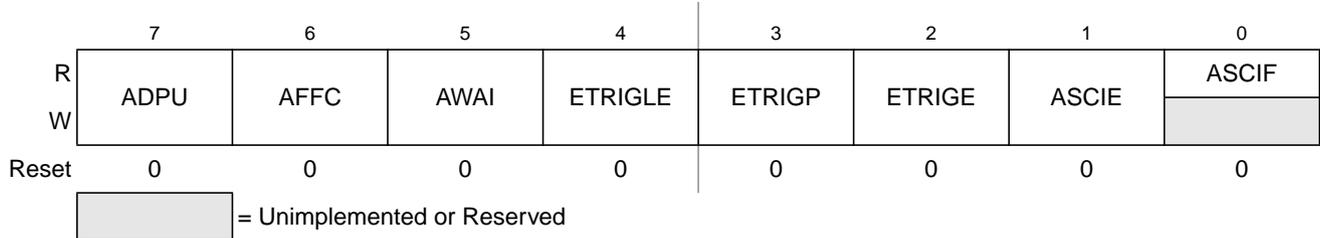
Figure 1-5. ATD Control Register 2 (ATDCTL2)

Read: Anytime

Write: Anytime

Table 1-1. ATDCTL2 Field Descriptions

Field	Description
7 ADPU	**ATD Power Down** — This bit provides on/off control over the ATD10B8C block allowing reduced MCU power consumption. Because analog electronic is turned off when powered down, the ATD requires a recovery time period after ADPU bit is enabled. 0 Power down ATD 1 Normal ATD functionality
6 AFFC	**ATD Fast Flag Clear All** 0 ATD flag clearing operates normally (read the status register ATDSTAT1 before reading the result register to clear the associate CCF flag). 1 Changes all ATD conversion complete flags to a fast clear sequence. Any access to a result register will cause the associate CCF flag to clear automatically.
5 AWAI	**ATD Power Down in Wait Mode** — When entering Wait Mode this bit provides on/off control over the ATD10B8C block allowing reduced MCU power. Because analog electronic is turned off when powered down, the ATD requires a recovery time period after exit from Wait mode. 0 ATD continues to run in Wait mode 1 Halt conversion and power down ATD during Wait mode After exiting Wait mode with an interrupt conversion will resume. But due to the recovery time the result of this conversion should be ignored.
4 ETRIGLE	**External Trigger Level/Edge Control** — This bit controls the sensitivity of the external trigger signal. See Table 1-2 for details.
3 ETRIGP	**External Trigger Polarity** — This bit controls the polarity of the external trigger signal. See Table 1-2 for details.
2 ETRIGE	**External Trigger Mode Enable** — This bit enables the external trigger on ATD channel 7. The external trigger allows to synchronize sample and ATD conversions processes with external events. 0 Disable external trigger 1 Enable external trigger **Note:** The conversion results for the external trigger ATD channel 7 have no meaning while external trigger mode is enabled.

Table 1-1. ATDCTL2 Field Descriptions (continued)

Field	Description
1 ASCIE	**ATD Sequence Complete Interrupt Enable** 0 ATD Sequence Complete interrupt requests are disabled. 1 ATD Interrupt will be requested whenever ASCIF = 1 is set.
0 ASCIF	**ATD Sequence Complete Interrupt Flag** — If ASCIE = 1 the ASCIF flag equals the SCF flag (see Section 1.3.2.7, "ATD Status Register 0 (ATDSTAT0)"), else ASCIF reads zero. Writes have no effect. 0 No ATD interrupt occurred 1 ATD sequence complete interrupt pending

Table 1-2. External Trigger Configurations

ETRIGLE	ETRIGP	External Trigger Sensitivity
0	0	Falling edge
0	1	Rising edge
1	0	Low level
1	1	High level

1.3.2.4   ATD Control Register 3 (ATDCTL3)

This register controls the conversion sequence length, FIFO for results registers and behavior in Freeze Mode. Writes to this register will abort current conversion sequence but will not start a new sequence.

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
W								
Reset	0	0	1	0	0	0	0	0

= Unimplemented or Reserved
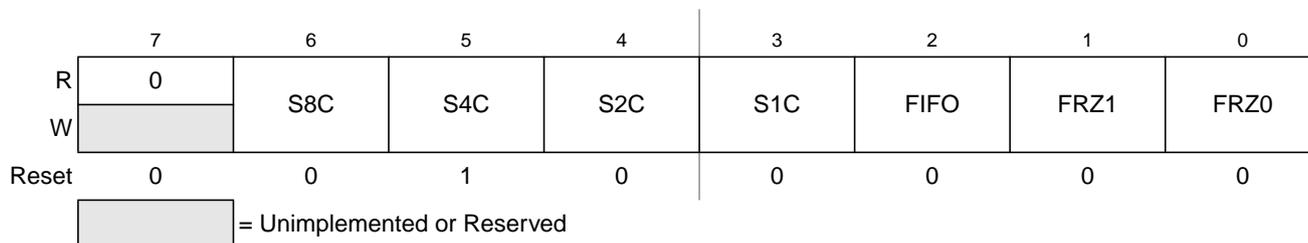
Figure 1-6. ATD Control Register 3 (ATDCTL3)

Read: Anytime

Write: Anytime

Table 1-3. ATDCTL3 Field Descriptions

Field	Description
6–3 S8C, S4C, S2C, S1C	**Conversion Sequence Length** — These bits control the number of conversions per sequence. Table 1-4 shows all combinations. At reset, S4C is set to 1 (sequence length is 4). This is to maintain software continuity to HC12 Family.

Table 1-3. ATDCTL3 Field Descriptions (continued)

Field	Description
2 FIFO	**Result Register FIFO Mode** — If this bit is zero (non-FIFO mode), the A/D conversion results map into the result registers based on the conversion sequence; the result of the first conversion appears in the first result register, the second result in the second result register, and so on. If this bit is one (FIFO mode) the conversion counter is not reset at the beginning or ending of a conversion sequence; sequential conversion results are placed in consecutive result registers. In a continuously scanning conversion sequence, the result register counter will wrap around when it reaches the end of the result register file. The conversion counter value (CC2-0 in ATDSTAT0) can be used to determine where in the result register file, the current conversion result will be placed. Aborting a conversion or starting a new conversion by write to an ATDCTL register (ATDCTL5-0) clears the conversion counter even if FIFO=1. So the first result of a new conversion sequence, started by writing to ATDCTL5, will always be place in the first result register (ATDDDR0). Intended usage of FIFO mode is continuos conversion (SCAN=1) or triggered conversion (ETRIG=1). Which result registers hold valid data can be tracked using the conversion complete flags. Fast flag clear mode may or may not be useful in a particular application to track valid data. 0 Conversion results are placed in the corresponding result register up to the selected sequence length. 1 Conversion results are placed in consecutive result registers (wrap around at end).
1–0 FRIZ[1:0]	**Background Debug Freeze Enable** — When debugging an application, it is useful in many cases to have the ATD pause when a breakpoint (Freeze Mode) is encountered. These 2 bits determine how the ATD will respond to a breakpoint as shown in Table 1-5. Leakage onto the storage node and comparator reference capacitors may compromise the accuracy of an immediately frozen conversion depending on the length of the freeze period.

Table 1-4. Conversion Sequence Length Coding

S8C	S4C	S2C	S1C	Number of Conversions per Sequence
0	0	0	0	8
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	8

Table 1-5. ATD Behavior in Freeze Mode (Breakpoint)

FRZ1	FRZ0	Behavior in Freeze Mode
0	0	Continue conversion
0	1	Reserved
1	0	Finish current conversion, then freeze
1	1	Freeze Immediately

1.3.2.5   ATD Control Register 4 (ATDCTL4)

This register selects the conversion clock frequency, the length of the second phase of the sample time and the resolution of the A/D conversion (i.e.: 8-bits or 10-bits). Writes to this register will abort current conversion sequence but will not start a new sequence.

Module Base + 0x0004

	7	6	5	4	3	2	1	0
R	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
W								
Reset	0	0	0	0	0	1	0	1
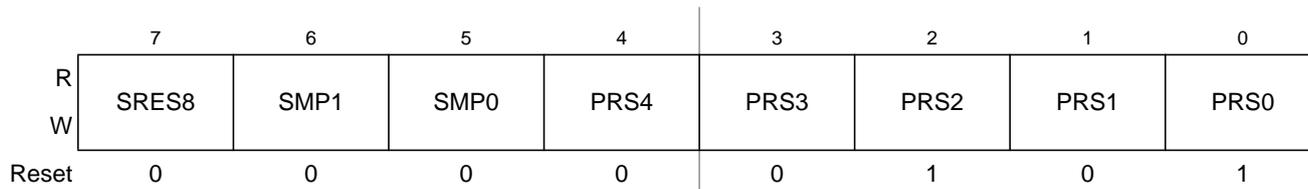
Figure 1-7. ATD Control Register 4 (ATDCTL4)

Read: Anytime

Write: Anytime

Table 1-6. ATDCTL4 Field Descriptions

Field	Description
7 SRES8	**A/D Resolution Select** — This bit selects the resolution of A/D conversion results as either 8 or 10 bits. The A/D converter has an accuracy of 10 bits; however, if low resolution is required, the conversion can be speeded up by selecting 8-bit resolution. 0 10-bit resolution 1 8-bit resolution
6–5 SMP[1:0]	**Sample Time Select** — These two bits select the length of the second phase of the sample time in units of ATD conversion clock cycles. Note that the ATD conversion clock period is itself a function of the prescaler value (bits PRS4-0). The sample time consists of two phases. The first phase is two ATD conversion clock cycles long and transfers the sample quickly (via the buffer amplifier) onto the A/D machine's storage node. The second phase attaches the external analog signal directly to the storage node for final charging and high accuracy. Table 1-7 lists the lengths available for the second sample phase.
4–0 PRS[4:0}	**ATD Clock Prescaler** — These 5 bits are the binary value prescaler value PRS. The ATD conversion clock frequency is calculated as follows: $$\text{ATDclock} = \frac{[\text{BusClock}]}{[\text{PRS}+1]} \times 0.5$$ **Note:** The maximum ATD conversion clock frequency is half the Bus Clock. The default (after reset) prescaler value is 5 which results in a default ATD conversion clock frequency that is Bus Clock divided by 12. Table 1-8 illustrates the divide-by operation and the appropriate range of the Bus Clock.

Table 1-7. Sample Time Select

SMP1	SMP0	Length of 2nd Phase of Sample Time
0	0	2 A/D conversion clock periods
0	1	4 A/D conversion clock periods
1	0	8 A/D conversion clock periods
1	1	16 A/D conversion clock periods

Table 1-8. Clock Prescaler Values

| Prescale Value	Total Divisor Value	Maximum Bus Clock[1]	Minimum Bus Clock[2]
00000	Divide by 2	4 MHz	1 MHz
00001	Divide by 4	8 MHz	2 MHz
00010	Divide by 6	12 MHz	3 MHz
00011	Divide by 8	16 MHz	4 MHz
00100	Divide by 10	20 MHz	5 MHz
00101	Divide by 12	24 MHz	6 MHz
00110	Divide by 14	28 MHz	7 MHz
00111	Divide by 16	32 MHz	8 MHz
01000	Divide by 18	36 MHz	9 MHz
01001	Divide by 20	40 MHz	10 MHz
01010	Divide by 22	44 MHz	11 MHz
01011	Divide by 24	48 MHz	12 MHz
01100	Divide by 26	52 MHz	13 MHz
01101	Divide by 28	56 MHz	14 MHz
01110	Divide by 30	60 MHz	15 MHz
01111	Divide by 32	64 MHz	16 MHz
10000	Divide by 34	68 MHz	17 MHz
10001	Divide by 36	72 MHz	18 MHz
10010	Divide by 38	76 MHz	19 MHz
10011	Divide by 40	80 MHz	20 MHz
10100	Divide by 42	84 MHz	21 MHz
10101	Divide by 44	88 MHz	22 MHz
10110	Divide by 46	92 MHz	23 MHz
10111	Divide by 48	96 MHz	24 MHz
11000	Divide by 50	100 MHz	25 MHz
11001	Divide by 52	104 MHz	26 MHz
11010	Divide by 54	108 MHz	27 MHz
11011	Divide by 56	112 MHz	28 MHz
11100	Divide by 58	116 MHz	29 MHz
11101	Divide by 60	120 MHz	30 MHz
11110	Divide by 62	124 MHz	31 MHz
11111	Divide by 64	128 MHz	32 MHz

[1] Maximum ATD conversion clock frequency is 2 MHz. The maximum allowed bus clock frequency is shown in this column.

[2] Minimum ATD conversion clock frequency is 500 kHz. The minimum allowed bus clock frequency is shown in this column.

1.3.2.6   ATD Control Register 5 (ATDCTL5)

This register selects the type of conversion sequence and the analog input channels sampled. Writes to this register will abort current conversion sequence and start a new conversion sequence.

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	DJM	DSGN	SCAN	MULT	0	CC	CB	CA
W								
Reset	0	0	0	0	0	0	0	0

  = Unimplemented or Reserved
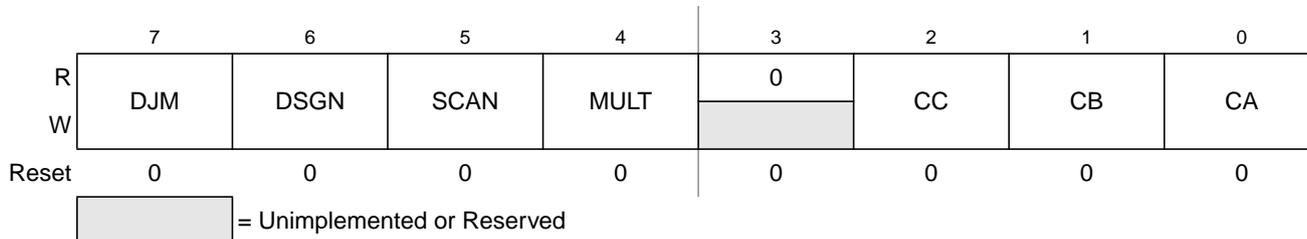
Figure 1-8. ATD Control Register 5 (ATDCTL5)

Read: Anytime

Write: Anytime

Table 1-9. ATDCTL5 Field Descriptions

Field	Description
7 DJM	**Result Register Data Justification** — This bit controls justification of conversion data in the result registers. See Section 1.3.2.13, "ATD Conversion Result Registers (ATDDRHx/ATDDRLx)" for details. 0 Left justified data in the result registers 1 Right justified data in the result registers
6 DSGN	Result Register Data Signed or Unsigned Representation — This bit selects between signed and unsigned conversion data representation in the result registers. Signed data is represented as 2's complement. Signed data is not available in right justification. See Section 1.3.2.13, "ATD Conversion Result Registers (ATDDRHx/ATDDRLx)" for details. 0 Unsigned data representation in the result registers 1 Signed data representation in the result registers Table 1-10 summarizes the result data formats available and how they are set up using the control bits. Table 1-11 illustrates the difference between the signed and unsigned, left justified output codes for an input signal range between 0 and 5.12 Volts.
5 SCAN	**Continuous Conversion Sequence Mode** — This bit selects whether conversion sequences are performed continuously or only once. 0 Single conversion sequence 1 Continuous conversion sequences (scan mode)
4 MULT	**Multi-Channel Sample Mode** — When MULT is 0, the ATD sequence controller samples only from the specified analog input channel for an entire conversion sequence. The analog channel is selected by channel selection code (control bits CC/CB/CA located in ATDCTL5). When MULT is 1, the ATD sequence controller samples across channels. The number of channels sampled is determined by the sequence length value (S8C, S4C, S2C, S1C). The first analog channel examined is determined by channel selection code (CC, CB, CA control bits); subsequent channels sampled in the sequence are determined by incrementing the channel selection code. 0 Sample only one channel 1 Sample across several channels
2–1 CC, CB, CA	**Analog Input Channel Select Code** — These bits select the analog input channel(s) whose signals are sampled and converted to digital codes. Table 1-12 lists the coding used to select the various analog input channels. In the case of single channel scans (MULT = 0), this selection code specified the channel examined. In the case of multi-channel scans (MULT = 1), this selection code represents the first channel to be examined in the conversion sequence. Subsequent channels are determined by incrementing channel selection code; selection codes that reach the maximum value wrap around to the minimum value.

Table 1-10. Available Result Data Formats

SRES8	DJM	DSGN	Result Data Formats Description and Bus Bit Mapping
1	0	0	8-bit / left justified / unsigned — bits 8–15
1	0	1	8-bit / left justified / signed — bits 8–15
1	1	X	8-bit / right justified / unsigned — bits 0–7
0	0	0	10-bit / left justified / unsigned — bits 6–15
0	0	1	10-bit / left justified / signed — bits 6–15
0	1	X	10-bit / right justified / unsigned — bits 0–9

Table 1-11. Left Justified, Signed, and Unsigned ATD Output Codes.

Input Signal V_{RL} = 0 Volts V_{RH} = 5.12 Volts	Signed 8-Bit Codes	Unsigned 8-Bit Codes	Signed 10-Bit Codes	Unsigned 10-Bit Codes
5.120 Volts	7F	FF	7FC0	FFC0
5.100	7F	FF	7F00	FF00
5.080	7E	FE	7E00	FE00
2.580	01	81	0100	8100
2.560	00	80	0000	8000
2.540	FF	7F	FF00	7F00
0.020	81	01	8100	0100
0.000	80	00	8000	0000

Table 1-12. Analog Input Channel Select Coding

CC	CB	CA	Analog Input Channel
0	0	0	AN0
0	0	1	AN1
0	1	0	AN2
0	1	1	AN3
1	0	0	AN4
1	0	1	AN5
1	1	0	AN6
1	1	1	AN7

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1.3.2.7   ATD Status Register 0 (ATDSTAT0)

This read-only register contains the sequence complete flag, overrun flags for external trigger and FIFO mode, and the conversion counter.

Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	SCF	0	ETORF	FIFOR	0	CC2	CC1	CC0
W								
Reset	0	0	0	0	0	0	0	0

☐ = Unimplemented or Reserved

Figure 1-9. ATD Status Register 0 (ATDSTAT0)

Read: Anytime

Write: Anytime (no effect on (CC2, CC1, CC0))

Table 1-13. ATDSTAT0 Field Descriptions

Field	Description
7 SCF	**Sequence Complete Flag** — This flag is set upon completion of a conversion sequence. If conversion sequences are continuously performed (SCAN = 1), the flag is set after each one is completed. This flag is cleared when one of the following occurs: 　　A) Write "1" to SCF 　　B) Write to ATDCTL5 (a new conversion sequence is started) 　　C) If AFFC=1 and read of a result register 0　Conversion sequence not completed 1　Conversion sequence has completed
5 ETORF	**External Trigger Overrun Flag** — While in edge trigger mode (ETRIGLE = 0), if additional active edges are detected while a conversion sequence is in process the overrun flag is set. This flag is cleared when one of the following occurs: 　　A) Write "1" to ETORF 　　B) Write to ATDCTL2, ATDCTL3 or ATDCTL4 (a conversion sequence is aborted) 　　C) Write to ATDCTL5 (a new conversion sequence is started) 0　No External trigger over run error has occurred 1　External trigger over run error has occurred

Table 1-13. ATDSTAT0 Field Descriptions (continued)

Field	Description
4 FIFOR	**FIFO Over Run Flag** — This bit indicates that a result register has been written to before its associated conversion complete flag (CCF) has been cleared. This flag is most useful when using the FIFO mode because the flag potentially indicates that result registers are out of sync with the input channels. However, it is also practical for non-FIFO modes, and indicates that a result register has been over written before it has been read (i.e. the old data has been lost). This flag is cleared when one of the following occurs: 　　A) Write "1" to FIFOR 　　B) Start a new conversion sequence (write to ATDCTL5 or external trigger) 0　No over run has occurred 1　An over run condition exists
2–0 CC[2:0]	**Conversion Counter** — These 3 read-only bits are the binary value of the conversion counter. The conversion counter points to the result register that will receive the result of the current conversion. For example, CC2 = 1, CC1 = 1, CC0 = 0 indicates that the result of the current conversion will be in ATD Result Register 6. If in non-FIFO mode (FIFO = 0) the conversion counter is initialized to zero at the begin and end of the conversion sequence. If in FIFO mode (FIFO = 1) the register counter is not initialized. The conversion counters wraps around when its maximum value is reached. Aborting a conversion or starting a new conversion by write to an ATDCTL register (ATDCTL5-2) clears the conversion counter even if FIFO=1.

1.3.2.8　Reserved Register (ATDTEST0)

Module Base + 0x0008

	7	6	5	4	3	2	1	0
R	U	U	U	U	U	U	U	U
W								
Reset	1	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 1-10. Reserved Register (ATDTEST0)

Read: Anytime, returns unpredictable values

Write: Anytime in special modes, unimplemented in normal modes

NOTE

Writing to this registers when in special modes can alter functionality.

1.3.2.9 ATD Test Register 1 (ATDTEST1)

This register contains the SC bit used to enable special channel conversions.

Module Base + 0x0009

	7	6	5	4	3	2	1	0
R	U	U	U	U	U	U	U	SC
W								
Reset	0	0	0	0	0	0	0	0

☐ = Unimplemented or Reserved
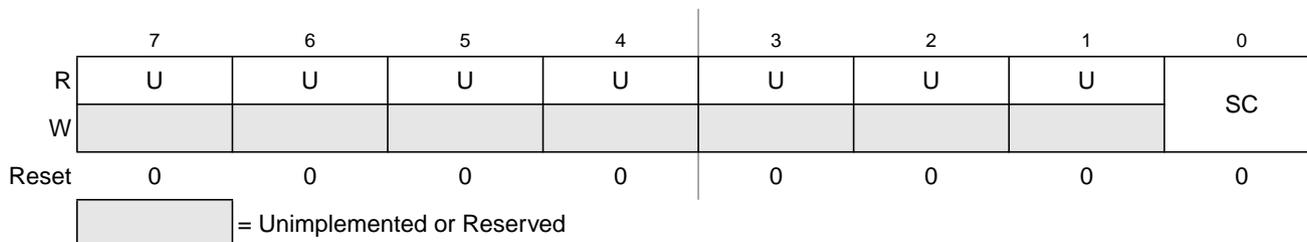
Figure 1-11. ATD Test Register 1 (ATDTEST1)

Read: Anytime, returns unpredictable values for Bit 7 and Bit 6

Write: Anytime

Table 1-14. ATDTEST1 Field Descriptions

Field	Description
0 SC	**Special Channel Conversion Bit** — If this bit is set, then special channel conversion can be selected using CC, CB, and CA of ATDCTL5. Table 1-15 lists the coding. 0 Special channel conversions disabled 1 Special channel conversions enabled **Note:** Always write remaining bits of ATDTEST1 (Bit7 to Bit1) zero when writing SC bit. Not doing so might result in unpredictable ATD behavior.

**Table 1-15. Special Channel Select Coding**

SC	CC	CB	CA	Analog Input Channel
1	0	X	X	Reserved
1	1	0	0	V_{RH}
1	1	0	1	V_{RL}
1	1	1	0	$(V_{RH}+V_{RL}) / 2$
1	1	1	1	Reserved

1.3.2.10 ATD Status Register 1 (ATDSTAT1)

This read-only register contains the Conversion Complete Flags.

Module Base + 0x000B

	7	6	5	4	3	2	1	0
R	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved
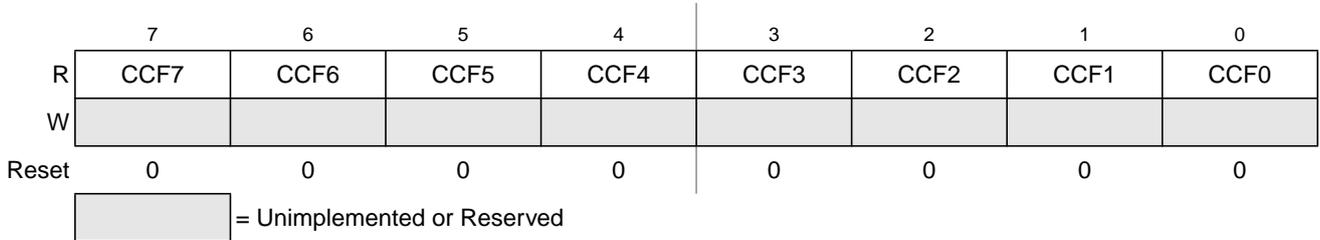
Figure 1-12. ATD Status Register 1 (ATDSTAT1)

Read: Anytime

Write: Anytime, no effect

Table 1-16. ATDSTAT1 Field Descriptions

Field	Description
7–0 CCF[7:0]	**Conversion Complete Flag x (x = 7, 6, 5, 4, 3, 2, 1, 0)** — A conversion complete flag is set at the end of each conversion in a conversion sequence. The flags are associated with the conversion position in a sequence (and also the result register number). Therefore, CCF0 is set when the first conversion in a sequence is complete and the result is available in result register ATDDR0; CCF1 is set when the second conversion in a sequence is complete and the result is available in ATDDR1, and so forth. A flag CCFx (x = 7, 6, 5, 4, 3, 2, 1, 0) is cleared when one of the following occurs: A) Write to ATDCTL5 (a new conversion sequence is started) B) If AFFC = 0 and read of ATDSTAT1 followed by read of result register ATDDRx C) If AFFC = 1 and read of result register ATDDRx 0 Conversion number x not completed 1 Conversion number x has completed, result ready in ATDDRx

1.3.2.11 ATD Input Enable Register (ATDDIEN)

Module Base + 0x000D

	7	6	5	4	3	2	1	0
R	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
W								
Reset	0	0	0	0	0	0	0	0
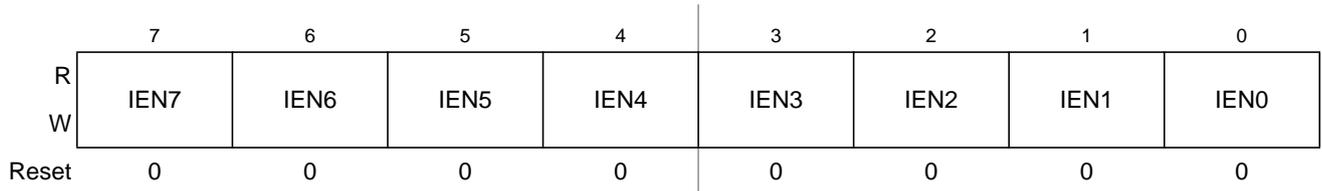
Figure 1-13. ATD Input Enable Register (ATDDIEN)

Read: Anytime

Write: Anytime

Table 1-17. ATDDIEN Field Descriptions

Field	Description
7–0 IEN[7:0]	**ATD Digital Input Enable on channel x (x = 7, 6, 5, 4, 3, 2, 1, 0)** — This bit controls the digital input buffer from the analog input pin (ANx) to PTADx data register. 0 Disable digital input buffer to PTADx 1 Enable digital input buffer to PTADx. **Note:** Setting this bit will enable the corresponding digital input buffer continuously. If this bit is set while simultaneously using it as an analog port, there is potentially increased power consumption because the digital input buffer maybe in the linear region.

1.3.2.12   Port Data Register (PORTAD)

The data port associated with the ATD is general purpose I/O. The port pins are shared with the analog A/D inputs AN7–AN0.

Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	PTAD7	PTAD6	PTAD5	PTAD4	PTAD3	PTAD2	PTAD1	PTAD0
W								
Reset	1	1	1	1	1	1	1	1
Pin Function	AN7	AN6	AN5	AN4	AN3'	AN2	AN1	AN0
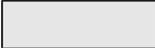
 = Unimplemented or Reserved

Figure 1-14. Port Data Register (PORTAD)

Read: Anytime

Write: Anytime, no effect

The A/D input channels may be used for general-purpose digital I/0.

Table 1-18. PORTAD Field Descriptions

Field	Description
7 PTAD[7:0]	**A/D Channel x (ANx) Digital Input (x = 7, 6, 5, 4, 3, 2, 1, 0)** — If the digital input buffer on the ANx pin is enabled (IENx = 1) read returns the logic level on ANx pin (signal potentials not meeting V_{IL} or V_{IH} specifications will have an indeterminate value)).
	If the digital input buffers are disabled (IENx = 0), read returns a "1".
	Reset sets all PORTAD bits to "1".

1.3.2.13   ATD Conversion Result Registers (ATDDRHx/ATDDRLx)

The A/D conversion results are stored in 8 read-only result registers ATDDRHx/ATDDRLx. The result data is formatted in the result registers based on two criteria. First there is left and right justification; this selection is made using the DJM control bit in ATDCTL5. Second there is signed and unsigned data; this selection is made using the DSGN control bit in ATDCTL5. Signed data is stored in 2's complement format and only exists in left justified format. Signed data selected for right justified format is ignored.

Read: Anytime

Write: Anytime, no effect in normal modes

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1.3.2.13.1 Left Justified Result Data

Module Base + 0x0010 = ATDDR0H, 0x0012 = ATDDR1H, 0x0014 = ATDDR2H, 0x0016 = ATDDR3H
0x0018 = ATDDR4H, 0x001A = ATDDR5H, 0x001C = ATDDR6H, 0x001E = ATDDR7H

	7	6	5	4	3	2	1	0	
R	BIT 9 MSB	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	10-bit data
W	BIT 7 MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	8-bit data
Reset	0	0	0	0	0	0	0	0	

Figure 1-15. Left Justified, ATD Conversion Result Register, High Byte (ATDDRxH)

Module Base + 0x0011 = ATDDR0L, 0x0013 = ATDDR1L, 0x0015 = ATDDR2L, 0x0017 = ATDDR3L
0x0019 = ATDDR4L, 0x001B = ATDDR5L, 0x001D = ATDDR6L, 0x001F = ATDDR7L

	7	6	5	4	3	2	1	0	
R	BIT 1	BIT 0	0	0	0	0	0	0	10-bit data
W	U	U	0	0	0	0	0	0	8-bit data
Reset	0	0	0	0	0	0	0	0	

Figure 1-16. Left Justified, ATD Conversion Result Register, Low Byte (ATDDRxL)

1.3.2.13.2 Right Justified Result Data

Module Base + 0x0010 = ATDDR0H, 0x0012 = ATDDR1H, 0x0014 = ATDDR2H, 0x0016 = ATDDR3H
0x0018 = ATDDR4H, 0x001A = ATDDR5H, 0x001C = ATDDR6H, 0x001E = ATDDR7H

	7	6	5	4	3	2	1	0	
R	0	0	0	0	0	0	BIT 9 MSB	BIT 8	10-bit data
W	0	0	0	0	0	0	0	0	8-bit data
Reset	0	0	0	0	0	0	0	0	

Figure 1-17. Right Justified, ATD Conversion Result Register, High Byte (ATDDRxH)

Module Base + 0x0011 = ATDDR0L, 0x0013 = ATDDR1L, 0x0015 = ATDDR2L, 0x0017 = ATDDR3L
0x0019 = ATDDR4L, 0x001B = ATDDR5L, 0x001D = ATDDR6L, 0x001F = ATDDR7L

	7	6	5	4	3	2	1	0	
R	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	10-bit data
W	BIT 7 MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	8-bit data
Reset	0	0	0	0	0	0	0	0	

Figure 1-18. Right Justified, ATD Conversion Result Register, Low Byte (ATDDRxL)

1.4 Functional Description

The ATD10B8C is structured in an analog and a digital sub-block.

1.4.1 Analog Sub-block

The analog sub-block contains all analog electronics required to perform a single conversion. Separate power supplies V_{DDA} and V_{SSA} allow to isolate noise of other MCU circuitry from the analog sub-block.

1.4.1.1 Sample and Hold Machine

The sample and hold (S/H) machine accepts analog signals from the external surroundings and stores them as capacitor charge on a storage node.

The sample process uses a two stage approach. During the first stage, the sample amplifier is used to quickly charge the storage node.The second stage connects the input directly to the storage node to complete the sample for high accuracy.

When not sampling, the sample and hold machine disables its own clocks. The analog electronics still draw their quiescent current. The power down (ADPU) bit must be set to disable both the digital clocks and the analog power consumption.

The input analog signals are unipolar and must fall within the potential range of V_{SSA} to V_{DDA}.

1.4.1.2 Analog Input Multiplexer

The analog input multiplexer connects one of the 8 external analog input channels to the sample and hold machine.

1.4.1.3 Sample Buffer Amplifier

The sample amplifier is used to buffer the input analog signal so that the storage node can be quickly charged to the sample potential.

1.4.1.4 Analog-to-Digital (A/D) Machine

The A/D machine performs analog-to-digital conversions. The resolution is program selectable at either 8 or 10 bits. The A/D machine uses a successive approximation architecture. It functions by comparing the stored analog sample potential with a series of digitally generated analog potentials. By following a binary search algorithm, the A/D machine locates the approximating potential that is nearest to the sampled potential.

When not converting the A/D machine disables its own clocks. The analog electronics still draws quiescent current. The power down (ADPU) bit must be set to disable both the digital clocks and the analog power consumption.

Only analog input signals within the potential range of V_{RL} to V_{RH} (A/D reference potentials) will result in a non-railed digital output codes.

1.4.2   Digital Sub-block

This subsection explains some of the digital features in more detail. See 7 for all details.

1.4.2.1   External Trigger Input (ETRIG)

The external trigger feature allows the user to synchronize ATD conversions to the external environment events rather than relying on software to signal the ATD module when ATD conversions are to take place. The input signal (ATD channel 7) is programmable to be edge or level sensitive with polarity control. Table 1-19 gives a brief description of the different combinations of control bits and their affect on the external trigger function

Table 1-19. External Trigger Control Bits

ETRIGLE	ETRIGP	ETRIGE	SCAN	Description
X	X	0	0	Ignores external trigger. Performs one conversion sequence and stops.
X	X	0	1	Ignores external trigger. Performs continuous conversion sequences.
0	0	1	X	Falling edge triggered. Performs one conversion sequence per trigger.
0	1	1	X	Rising edge triggered. Performs one conversion sequence per trigger.
1	0	1	X	Trigger active low. Performs continuous conversions while trigger is active.
1	1	1	X	Trigger active high. Performs continuous conversions while trigger is active.

During a conversion, if additional active edges are detected the overrun error flag ETORF is set.

In either level or edge triggered modes, the first conversion begins when the trigger is received. In both cases, the maximum latency time is one Bus Clock cycle plus any skew or delay introduced by the trigger circuitry.

NOTE

The conversion results for the external trigger ATD channel 7 have no meaning while external trigger mode is enabled.

Once ETRIGE is enabled, conversions cannot be started by a write to ATDCTL5, but rather must be triggered externally.

If the level mode is active and the external trigger both de-asserts and re-asserts itself during a conversion sequence, this does not constitute an overrun; therefore, the flag is not set. If the trigger is left asserted in level mode while a sequence is completing, another sequence will be triggered immediately.

1.4.2.2 General-Purpose Digital Port Operation

The channel pins can be multiplexed between analog and digital data. As analog inputs, they are multiplexed and sampled to supply signals to the A/D converter. Alternatively they can be configured as digital I/O signals with the port I/O data being held in PORTAD.

The analog/digital multiplex operation is performed in the pads. The pad is always connected to the analog inputs of the ATD10B8C. The pad signal is buffered to the digital port registers. This buffer can be turned on or off with the ATDDIEN register. This is important so that the buffer does not draw excess current when analog potentials are presented at its input.

1.4.2.3 Low-Power Modes

The ATD10B8C can be configured for lower MCU power consumption in three different ways:

1. Stop Mode: This halts A/D conversion. Exit from Stop mode will resume A/D conversion, But due to the recovery time the result of this conversion should be ignored.

2. Wait Mode with AWAI = 1: This halts A/D conversion. Exit from Wait mode will resume A/D conversion, but due to the recovery time the result of this conversion should be ignored.

3. Writing ADPU = 0 (Note that all ATD registers remain accessible.): This aborts any A/D conversion in progress.

NOTE

The reset value for the ADPU bit is zero. Therefore, when this module is reset, it is reset into the power down state.

1.5 Initialization/Application Information

1.5.1 Setting up and starting an A/D conversion

The following describes a typical setup procedure for starting A/D conversions. It is highly recommended to follow this procedure to avoid common mistakes.

Each step of the procedure will have a general remark and a typical example

1.5.1.1 Step 1

Power up the ATD and concurrently define other settings in ATDCTL2
Example: Write to ATDCTL2: ADPU=1 -> powers up the ATD, ASCIE=1 enable interrupt on finish of a conversion sequence.

1.5.1.2 Step 2

Wait for the ATD Recovery Time t_{REC} before you proceed with Step 3.

Example: Use the CPU in a branch loop to wait for a defined number of bus clocks.

1.5.1.3 Step 3

Configure how many conversions you want to perform in one sequence and define other settings in ATDCTL3.

Example: Write S4C=1 to do 4 conversions per sequence.

1.5.1.4 Step 4

Configure resolution, sampling time and ATD clock speed in ATDCTL4.

Example: Use default for resolution and sampling time by leaving SRES8, SMP1 and SMP0 clear. For a bus clock of 40MHz write 9 to PR4-0, this gives an ATD clock of 0.5*40MHz/(9+1) = 2MHz which is within the allowed range for f_{ATDCLK}.

1.5.1.5 Step 5

Configure starting channel, single/multiple channel, continuous or single sequence and result data format in ATDCTL5. Writing ATDCTL5 will start the conversion, so make sure your write ATDCTL5 in the last step.

Example: Leave CC,CB,CA clear to start on channel AN0. Write MULT=1 to convert channel AN0 to AN3 in a sequence (4 conversion per sequence selected in ATDCTL3).

1.5.2 Aborting an A/D conversion

1.5.2.1 Step 1

Disable the ATD Interrupt by writing ASCIE=0 in ATDCTL2. This will also abort any ongoing conversion sequence.

It is important to clear the interrupt enable at this point, prior to step 3, as depending on the device clock gating it may not always be possible to clear it or the SCF flag once the module is disabled (ADPU=0).

1.5.2.2 Step 2

Clear the SCF flag by writing a 1 in ATDSTAT0.

(Remaining flags will be cleared with the next start of a conversions, but SCF flag should be cleared to avoid SCF interrupt.)

1.5.2.3 Step 3

Power down ATD by writing ADPU=0 in ATDCTL2.

1.6 Resets

At reset the ATD10B8C is in a power down state. The reset state of each individual bit is listed within Section 1.3.2, "Register Descriptions" which details the registers and their bit-field.

1.7   Interrupts

The interrupt requested by the ATD10B8C is listed in Table 1-20. Refer to MCU specification for related vector address and priority.

Table 1-20. ATD10B8C Interrupt Vectors

Interrupt Source	CCR Mask	Local Enable
Sequence complete interrupt	I bit	ASCIE in ATDCTL2

See Section 1.3.2, "Register Descriptions" for further details.