VLSI Design Internship
AHB2APB BRIDGE DESIGN

1.Protocol:

The Advanced Microcontroller Bus Architecture(AMBA) specification defines an on-chip communications standard for designing high-performance embedded microcontrollers. Three distinct buses are defined within the AMBA specification:

- Advanced High -performance Bus (AHB)
- Advanced System Bus(ASB)
- Advanced Peripheral Bus(APB)

Advanced High -performance Bus(AHB) :

The AMBA AHB is for high-performance, high clock frequency system modules. AHB supports the efficient connection of processors, on-chip memories and off-chip external memory interfaces with low-power peripheral microcell functions.

Advanced Peripheral Bus(APB):

The AMBA APB is for low -power peripherals. AMBA APB is optimized for minimal power consumption and reduced interface complexity to support peripheral functions.

Basic Terminology

Bus cycle:

For AMBA AHB or APB protocol Bus cycle is defined from rising-edge to rising-edge transitions.

Bus transfer:

An AMBA AHB bus transfer is a read or write operation of a data object, which may take one or more bus cycles.

Burst operation:

A burst operation is defined as one or more data transactions, initiated by a bus master,which have a consistent width of transaction to an incremental region of address space.

Types of Bursts:

Hburst[2:0]	Type	Description
000	Single	Single Transfer
001	INCR	Incrementing length of unspecified length

010	WRAP4	4-beat Wrapping burst
011	INCR4	4-beat Incrementing burst
100	WRAP8	8-beat Wrapping burst
101	INCR 8	8-beat Incrementing burst
110	WRAP 16	16-beat Wrapping burst
111	INCR 16	16-beat Incrementing burst

Types of transfers:

Htrans[1:0]	Type	Description
2'b00	IDLE	Indicates that no data transfer is required
2'b01	BUSY	Master is busy in continuing with a bursts of transfers and can't take the next transfer immediately
2'b10	NON-SEQ	Indicates the first transfer of a burst or a single transfer. Address and control signals are unrelated to the previous transfer.
2'b11	SEQ	Remaining transfer in a burst are sequential. Address is related to the previous transfer.

Address Calculation for Burst transfer:

Hsize	Hburst	Haddr
8 bits	WRAP 4	{Haddr[31:2],Haddr[1:0]+1'b1}
	WRAP 8	{Haddr[31:3],Haddr[2:0]+1'b1}
	WRAP 16	{Haddr[31:4],Haddr[3:0]+1'b1}
	INCR 4	Haddr + 1'b1
	INCR 8	Haddr +1'b1
	INCR 16	Haddr +1'b1
16 bits	WRAP 4	{Haddr[31:3],Haddr[2:1]+1'b1,Haddr[0]}
	WRAP 8	{Haddr[31:4],Haddr[3:1]+1'b1,Haddr[0]}
	WRAP 16	{Haddr[31:5],Haddr[4:1]+1'b1,Haddr[0]}
	INCR 4	Haddr + 2'd2
	INCR 8	Haddr +2'd2
	INCR 16	Haddr +2'd2
32 bits	WRAP 4	{Haddr[31:4],Haddr[3:2]+1'b1,Haddr[1:0]}
	WRAP 8	{Haddr[31:5],Haddr[4:2]+1'b1,Haddr[1:0]}
	WRAP 16	{Haddr[31:6],Haddr[5:2]+1'b1,Haddr[1:0]}
	INCR 4	Haddr + 3'd4
	INCR 8	Haddr +3'd4
	INCR 16	Haddr +3'd4

AMBA SIGNALS

AMBA AHB Signals:

Name	Source	Description
HCLK	Clock source	This clock times all bus transfers. All signal timings are related to the rising edge of HCLK.
HRESETn	Reset controller	The bus reset signal is active LOW and is used to reset the system and the bus.This is the only active LOW signal.
HADDR[31:0]	Master	The 32-bit system address bus.
HTRANS[1:0]	Master	Indicates the type of the current transfer, which can be NONSEQUENTIAL, SEQUENTIAL, IDLE or BUSY.
HWRITE	Master	When HIGH this signal indicates a write transfer and when LOW a read transfer.
HSIZE[2:0]	Master	Indicates the size of the transfer, which is typically byte (8-bit), halfword (16-bit) or word (32-bit). The protocol allows for larger transfer sizes up to a maximum of 1024 bits.
HBURST[2:0]	Master	Indicates if the transfer forms part of a burst. Four, eight and sixteen beat bursts are supported and the burst may be either incrementing or wrapping.
HWDATA[31:0]	Master	The write data bus is used to transfer data from the master to the bus slaves during write operations. A minimum data bus width of 32 bits is recommended.
HRDATA[31:0]	Slave	The read data bus is used to transfer data from bus slaves to the bus master during read operations. A minimum data bus width of 32 bits is recommended.
HREADY	Slave	When HIGH the HREADY signal indicates that a transfer has finished on the bus. This signal may be driven LOW to extend a transfer. **Note: Slaves on the bus require HREADY as both an input and an output signal.**
HRESP[1:0]	Slave	The transfer response provides additional information on the status of a transfer. Four different responses are provided, OKAY, ERROR, RETRY and SPLIT.

AMBA APB Signals:

Name	Source	Description
PADDR[31:0]	Master	This is the APB address bus, which may be up to 32-bits wide and is driven by the peripheral bus bridge unit.
PSELx[2:0]	Decoder	A signal from the secondary decoder, within the peripheral bus bridge unit, to each peripheral bus slave x. This signal indicates that the slave device is selected and a data transfer is required. There is a PSELx signal for each bus slave.
PENABLE	Master	This strobe signal is used to time all accesses on the peripheral bus. The enable signal is used to indicate the second cycle of an APB transfer. The rising edge of PENABLE occurs in the middle of the APB transfer.

PWRITE	Master	When HIGH this signal indicates an APB write access and when LOW a read access.
PRDATA[31:0]	Slave	The read data bus is driven by the selected slave during read cycles (when PWRITE is LOW). The read data bus can be up to 32-bits wide.
PWDATA[31:0]	Master	The write data bus is driven by the peripheral bus bridge unit during write cycles (when PWRITE is HIGH). The write data bus can be up to 32-bits wide.

Design Modules

AHB Slave Interface:

An AHB bus slave responds to transfers initiated by bus masters within the system. The signals required for transfer such as the address and control information, will be generated by the bus master.

APB Controller:

The AHB to APB bridge comprises a state machine, which is used to control the generation of the APB and aHB output signals, and the address decoding logic which is used to generate the APB peripheral select lines.

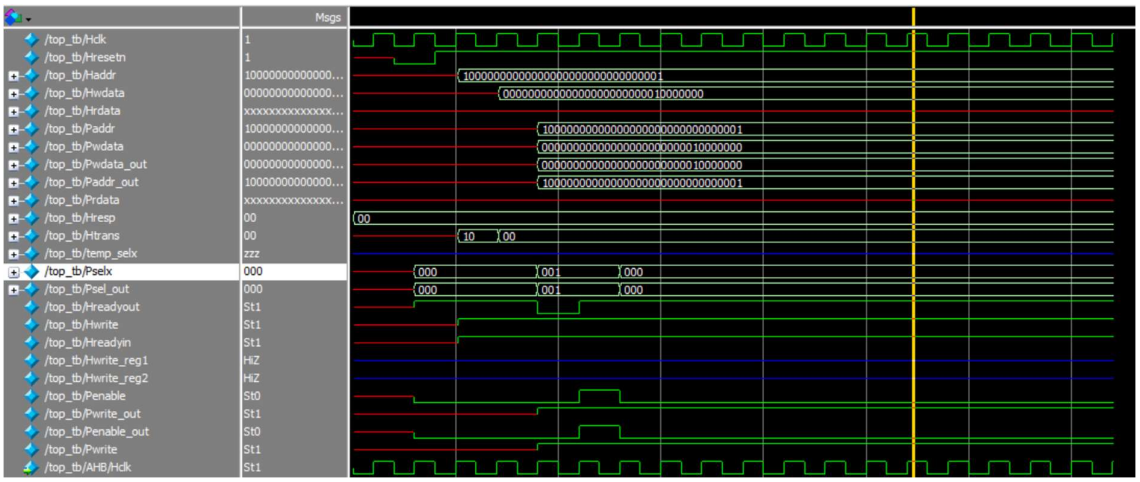
Peripheral memory map:

Indicates the address needed for selecting APB Peripheral

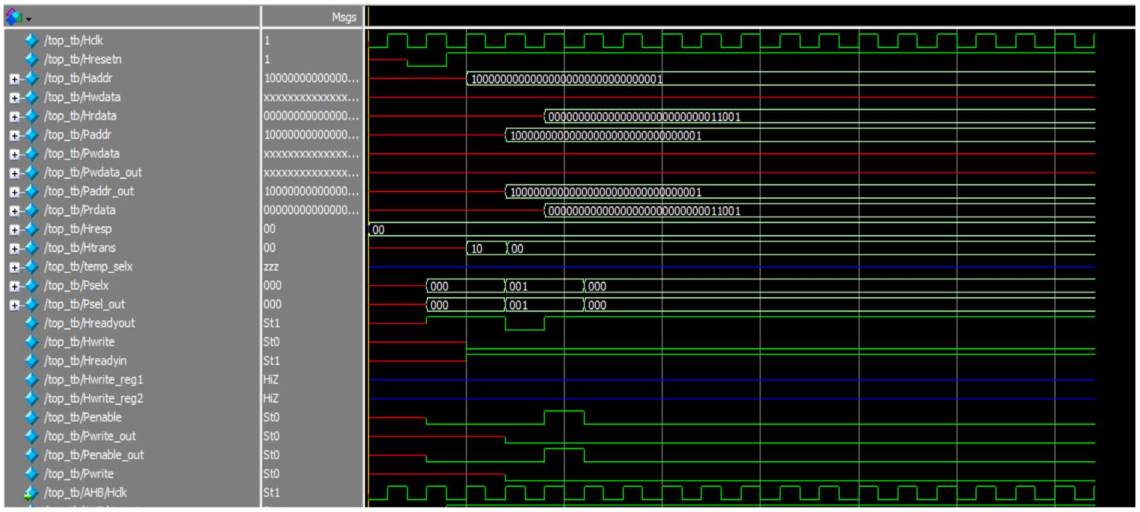
Address	**Peripheral**
0xBFFFFFFF 0x8C000000	undefined
  0x88000000	Remap & Pause
  0x84000000	Counters timers
  0x80000000	Interrupt controller

2.Simulation Waveforms for the output:

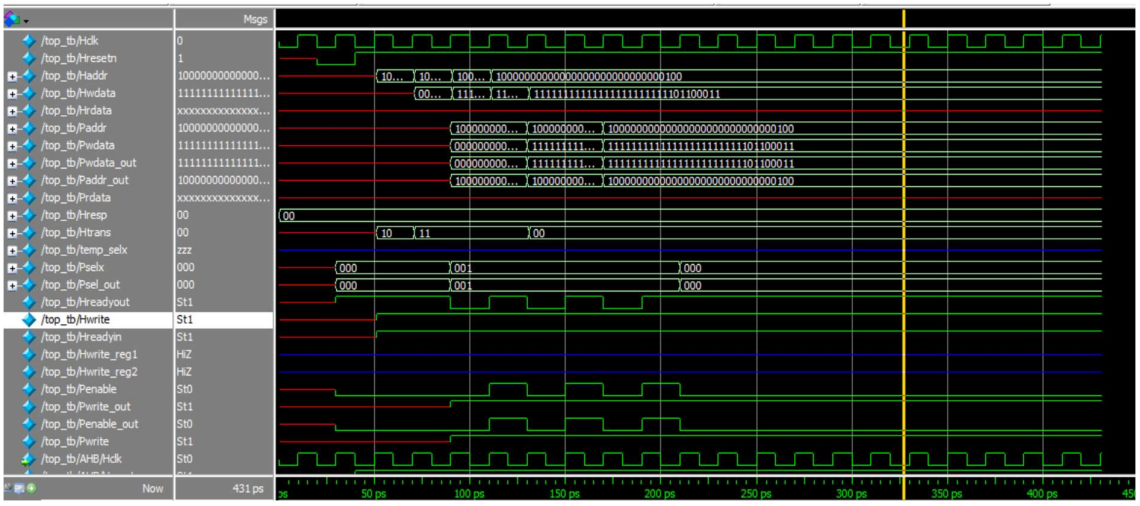
Single write:



Single read:

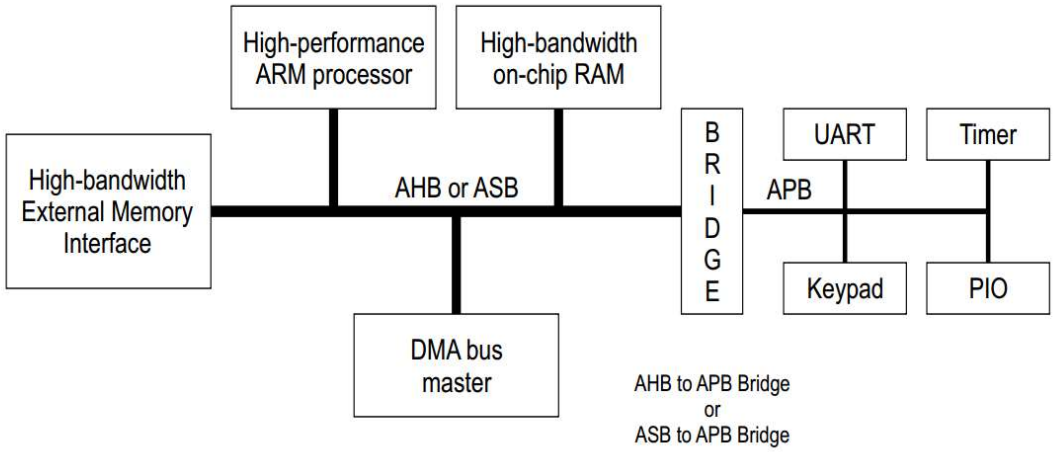


Burst write:

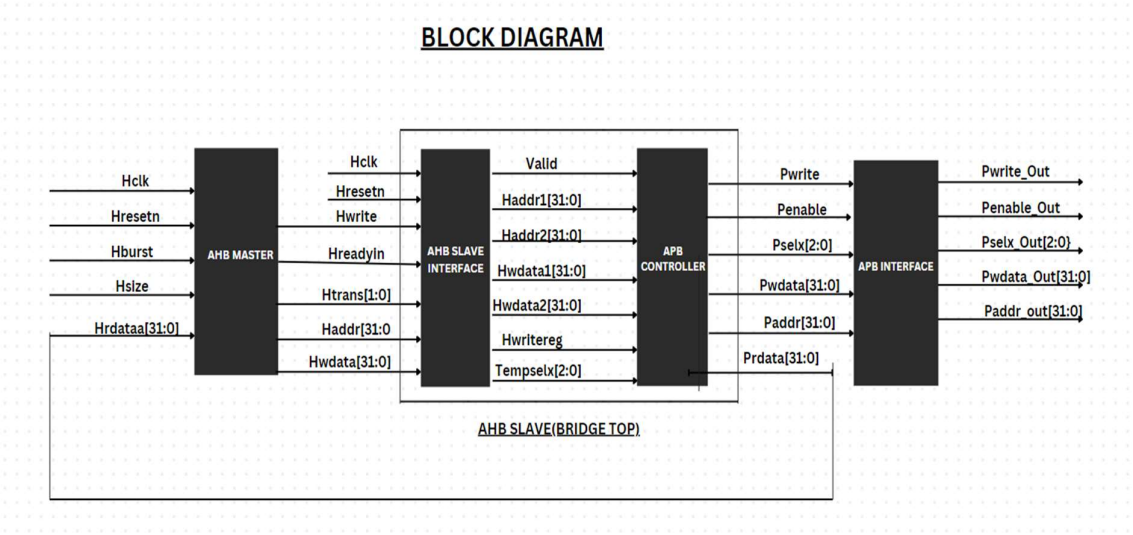


3. Block Diagram and Architecture:

Architecture:



BLOCK DIAGRAM:



4.Synthesis Part: