Embedded Systems Lab

Experiment 10: GP Series in ARM

Date: 5th April 2022

Platform: ARMSim 2.1

Objective: Write ARM assembly code to generate a GP consisting of 6 terms. The first term is to be stored in register R1, the common ratio in register R2, and the GP itself is to be stored in registers R3 to R8.

Algorithm:

1. Store the first term and the common ratio in registers R1 and R2 respectively using the MOV instruction
2. Copy the first term to register R3 using MOV instruction
3. Generate the rest of the terms of the GP by using the MUL instruction

Code:

```
@ Arm assembly code to generate a GP sequence with first term 2 and common
ratio 3, and store it in registers R3 to R8 (ie, total 6 terms)

MOV R1, #2    @ First term is stored in reg R1
MOV R2, #3    @ Common ratio is stored in reg R2

@ Generating six terms using first term and c.d.
@ The first term is stored in register R3, second in R4, ... , sixth in R8

MOV R3, R1
MUL R4, R3, R2
MUL R5, R4, R2
MUL R6, R5, R2
MUL R7, R6, R2
MUL R8, R7, R2
```

anuragbaundwal-1901038-embedded-systems-lab-exp10-.txt - Notepad

File Edit Format View Help

```
@ Arm assembly code to generate a GP sequence with first term 2 and common ratio 3, and store it in registers R3 to R8 (ie, total 6 terms)

MOV R1, #2      @ First term is stored in reg R1
MOV R2, #3      @ Common ratio is stored in reg R2

@ Generating six terms using first term and c.d.
@ The first term is stored in register R3, second in R4, ... , sixth in R8

MOV R3, R1
MUL R4, R3, R2
MUL R5, R4, R2
MUL R6, R5, R2
MUL R7, R6, R2
MUL R8, R7, R2
```

Ln 13, Col 15 | 100% | Windows (CRLF) | UTF-8

Output:

ARMSim# - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose | Floating Point

Hexadecimal | Unsigned Decimal | Signed Decimal

```
R0      :0
R1      :2
R2      :3
R3      :2
R4      :6
R5      :18
R6      :54
R7      :162
R8      :486
R9      :0
R10(sl):0
R11(fp):0
R12(ip):0
R13(sp):70656
R14(lr):0
R15(pc):70656
------------------
CPSR Register
Negative(N):0
Zero(Z)    :0
Carry(C)   :0
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)   :0
CPU Mode   :System
------------------
0x000000df
```

CodeView

anuragbaundwal-1901038-embedded-systems-lab-exp10-.o

```
                    @ Arm assembly code to generate a GP sequence with first term 2 and common ratio 3, and store it in
00001000:E3A01002   MOV R1, #2      @ First term is stored in reg R1
00001004:E3A02003   MOV R2, #3      @ Common ratio is stored in reg R2

                    @ Generating six terms using first term and c.d.
                    @ The first term is stored in register R3, second in R4, ... , sixth in R8

00001008:E1A03001   MOV R3, R1
0000100C:E0040293   MUL R4, R3, R2
00001010:E0050294   MUL R5, R4, R2
00001014:E0060295   MUL R6, R5, R2
00001018:E0070296   MUL R7, R6, R2
0000101C:E0080297   MUL R8, R7, R2
```

OutputView | WatchView

Console | stdin/stdout/stderr

Result and Conclusions:

It is observed that registers R3 to R8 contain the terms 2, 6, 18, 54, 162, and 486 of the GP. Hence, the code is working as expected and the experiment was performed successfully.

Experiment Performed By;

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