

# Embedded Systems Lab

## Experiment 9: AP Series in ARM

**Date:** 29th March 2022

**Platform:** ARMSim 2.1

**Objective:** Write ARM assembly code to generate an AP consisting of 6 terms. The first term is to be stored in register R1, the common difference in register R2, and the AP itself is to be stored in registers R3 to R8.

### Algorithm:

1. Store the first term and the common difference in registers R1 and R2 respectively using the MOV instruction
2. Copy the first term to register R3 using MOV instruction
3. Generate the rest of the terms of the AP by using the ADD instruction

### Code:

```
@ Arm assembly code to generate an AP with first term 18 and common
difference 10

MOV R1, #18 @ First term 18 is stored in reg R1
MOV R2, #10 @ Common difference 10 is stored in reg R2

@ Generating six terms using first term and c.d.
@ The first term is stored in register R3, second in R4, ... , sixth in R8

MOV R3, R1
ADD R4, R3, R2
ADD R5, R4, R2
ADD R6, R5, R2
ADD R7, R6, R2
ADD R8, R7, R2
```

```
anuragbaundwal-1901038-embedded-systems-lab-exp9.txt - Notepad
File Edit Format View Help
@ Arm assembly code to generate an AP with first term 18 and common difference 10

MOV R1, #18    @ First term 18 is stored in reg R1
MOV R2, #10    @ Common difference 10 is stored in reg R2
|
@ Generating six terms using first term and c.d.
@ The first term is stored in register R3, second in R4, ... , sixth in R8

MOV R3, R1
ADD R4, R3, R2
ADD R5, R4, R2
ADD R6, R5, R2
ADD R7, R6, R2
ADD R8, R7, R2
```

## Output:

ARMSim# - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView Floating Point

General Purpose	Floating Point
Hexadecimal	
Unsigned Decimal	
Signed Decimal	

R0 : 0  
R1 : 18  
R2 : 10  
R3 : 18  
R4 : 28  
R5 : 38  
R6 : 48  
R7 : 58  
R8 : 68  
R9 : 0  
R10 (s1) : 0  
R11 (fp) : 0  
R12 (ip) : 0  
R13 (sp) : 70656  
R14 (lr) : 0  
R15 (pc) : 70656

-----  
CPSR Register  
Negative (N) : 0  
Zero (Z) : 0  
Carry (C) : 0  
Overflow (V) : 0  
IRQ Disable : 1  
FIQ Disable : 1  
Thumb (T) : 0  
CPU Mode : System  
-----  
0x000000df

CodeView

anuragbaundwal-1901038-embedded-systems-lab-exp9.o

```
@ Arm assembly code to generate an AP with first term 18 and common difference 10

00001000:E3A01012 MOV R1, #18    @ First term 18 is stored in reg R1
00001004:E3A0200A MOV R2, #10    @ Common difference 10 is stored in reg R2

    @ Generating six terms using first term and c.d.
    @ The first term is stored in register R3, second in R4, ... , sixth in R8

00001008:E1A03001 MOV R3, R1
0000100C:E0834002 ADD R4, R3, R2
00001010:E0845002 ADD R5, R4, R2
00001014:E0856002 ADD R6, R5, R2
00001018:E0867002 ADD R7, R6, R2
0000101C:E0878002 ADD R8, R7, R2
```

OutputView WatchView

Console stdin/stdout/stderr

## Result and Conclusions:

It is observed that registers R3 to R8 contain the terms 18, 28, 38, 48, 58, and 68 of the AP. Hence, the code is working as expected and the experiment was performed successfully.

Experiment Performed By;  
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