The Analyzes of Network-on-Chip Architectures Based on NOXIM Simulator

Van-Nam Dinh[1(✉)], Mau-Viet Ho[1], Van-Cuong Nguyen[1], Tung-Son Ngo[2], and Effiong Charles[3]

[1] Electronic and Communication Faculty, Information and Communication Technology University, Thai Nguyen University, Thai Nguyen, Vietnam
{dvnam,hmviet,nvcuong}@ictu.edu.vn
[2] Computer Fundamental Department, FPT University, Ha Noi, Vietnam
sonnt5@fpt.edu.vn
[3] LIRMM, 161, Rue ADA, 34095 Montpellier Cedex 5, France
talkwithcharles@gmail.com

Abstract. Network-on-Chip (NoC), an interesting paradigm, is one of the newest technologies for VLSI design. In this research, we approach the architecture, algorithms and the performance analyses of a NoC system. The highlight point of this research is implementing additional features to the embedded codes and evaluating special applications in a NoC system based on NOXIM simulator. The results indicated that in certain cases, we should know which is appropriate algorithm for implementing tasks. The evaluating a NoC's performance is an important research trend, hence this study provides one new method for doing that.

Keywords: NoC architectures · NOXIM network-on-chip

1 Introduction

The emergence of Network-On-Chip (NoC) paradigm in recent years has changed the viewing of the world in IP cores design and on-chip communication mechanism. In NoCs, routing determines how information will be transferred among Intellectual Property (IP) cores. Routing algorithms play a vital role in the overall performance and resource utilization of the network, hence the focus of this research work would implement the new method assisting in performance of NoC's platform such some previous researches [8–10].

In this study, we aim to propose a new methodology of analyzing a NoC system based on three main goals. First, we consider the impacts of several NOXIM parameters, then we implement some basic routing algorithm and explore their impact on performance metrics such as delay (cycles), the bandwidth via throughput (flits/IP/cycle) and the power energy (J).

2 Methods

In this section, we detail the main tasks of this study, which includes implementing routing algorithms, techniques, tools and data analysis.

M. Akagi et al. (eds.), *Advances in Information and Communication Technology*,
Advances in Intelligent Systems and Computing 538, DOI 10.1007/978-3-319-49073-1_64

2.1 Routing Algorithms

Routing determines the path a packet takes from its IP (Source IP core) to the destination IP core. There are two main processes in a routing algorithm: routing function and selection function [3]

Figure 1 presents a 2D-mesh (4×4) topology of Network-on-Chip with all necessary components of a system. A link is used to connect routers together and creates a path for data flow in the network. The links shown in the figure represent both input and output links.

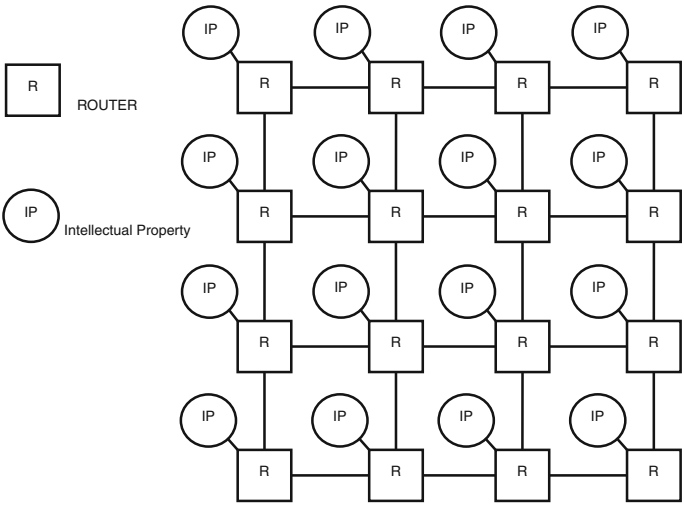

Fig. 1. 2D-mesh topology(4×4)

In this work, we focus our attention solely on the routing algorithm. As mentioned early, the routing algorithm impacts the overall performance of the system in terms of latency and power.

Deterministic Algorithms: Figure 2 depicts the mechanism of a deterministic algorithm in NoC system. In this situation, the selection block is not presented because the routing function returns only one fix path that have already created before transmitting process.

Adaptive Algorithms: In this mechanism, the network status information such as link utilization and buffer's status are cared by selection function block. Figure 3 shows the mechanism of this algorithm. In adaptive routing, several paths from source IP core to destination IP cores are available. So, it leads to some disadvantages such as needing large memory and implementation complexity [7]

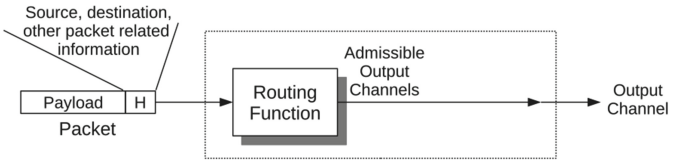

Fig. 2. The deterministic algorithm mechanism [3]

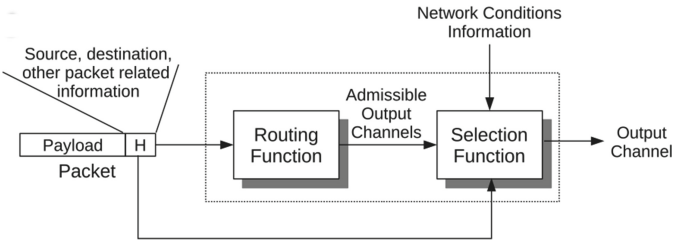

Fig. 3. The mechanism of adaptive algorithms [3]

In this study, we exploited deterministic algorithm because of it's advantages such as suitable with an uniform or regular traffic patterns. The other reason is suitable with a real technology system such as 2D-mesh topology, This leads to available in implementing on a real system.

2.2 A Methodology for Data Analyzing

Figure 4 shows the data flow of our methodology. Each of the process will be discussed in some detail in the following subsection.

In the methodology of implementing, at first, we choose applications [7] for inputs parameters configuring. Then, system will be configured with these basic information before creating proposal scenarios to implement based on noxim platform support [2] for embedded codes [6].

Te evaluate the system performance via Noxim, we implement this method with some specific applications that will be used for configuration the system's parameters. Specially, for updating the information to route packet during communicating processes between source to destination IP cores.

System's Inputs: We use the applications shown in Fig. 5 as our test cases. They are DVOPD, MPEG-4 and MWD applications [4].

System's Configuration: This research includes some scripts that are very useful because it allows the designers can integrate new tools such as ShellScript and Gnuplot for performance evaluation simulations [6].

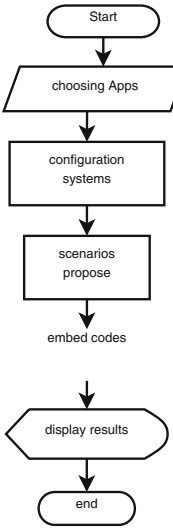

Fig. 4. The data flow of methodology.

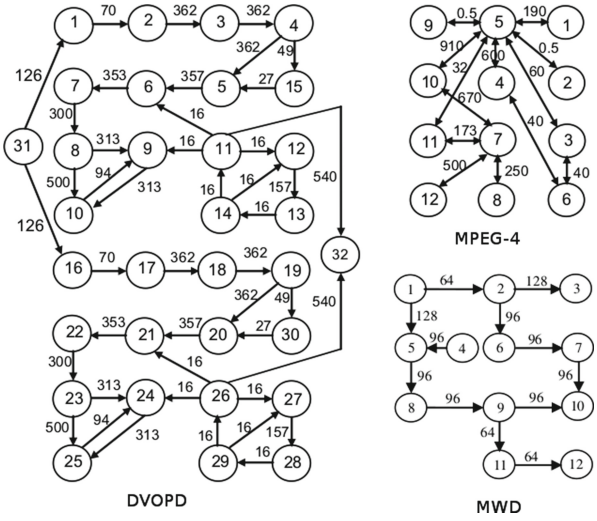

Fig. 5. The system's input applications [4].

In this study, we contributed one new method using NOXIM to map application into system, then with each routing algorithm in Network-on-Chip system (see on Fig. 6)

Futures	Description
Network configuration	
Topology	8x8 MESH 2D
Control Flow	Credit Based Mechanism
Routing algorithm	Deterministic XY algorithm
Switch technique	Wormhole (WH) switching
Communication pattern	
Traffic pattern	Complement, uniform
Packet size	2, 4, ... 512,1024 flits
Simulation environment	
HDL	SystemC 2.3.1
Operating system	Linux (Ubuntu 15.10)

Fig. 6. The system configuration

Proposed Evaluation Scenarios: This section will be used for simulating and collecting the final results that aim at exploring how different simulation parameters affects the system performance.

The main idea is that for each routing algorithm, we evaluate the impact of different packet injection rates for the applications.

In each scenario, the inputs consist of the core application graph (.cg), the reconfiguration file (.yaml); and the outputs include latency (cycles), throughput (flits/IP/cycle) and the power energy (J).

We considered DVOPD, MPEG-4 and MWD applications for scenario 1, 2 and 3 respectively.

We can convert from Fig. 5 into the core graph as Fig. 7 to make the simulation.

Embedded Codes: For this work, we integrated GNUplot tool (the information in Fig. 8) and techniques for system simulation such as ShellScript (open source from link [6]) into NOXIM.

2.3 System's Performance

As mentioned before, we used the data transferring latency (cycles), bandwidth of channels between IP cores, and power/energy (J) are main parameters for estimating the NoC system's performance.

```
% Communication graph of DVOPD
%       Source  targe
        1       2
        2       3
        3       4
        4       5
        4       15
        5       6
        6       7
        7       8
        8       9
        8       10
        9       10
        10      9
        11      9
        11      6
        11      12
        11      32
        12      13
        13      14
        14      11
        14      12
        15      5
        16      17
        17      18
        18      19
        19      20
% Communication graph of MPEG-4 application
%       Source  targe
        1       5
        5       1
        2       5
        5       2
        5       9
        9       5
        10      5
        5       10
        4       5
        5       4
        3       5
% Communication graph of MWD
%       Source  targe
        1       2
        2       3
        2       6
        1       5
        4       5
        6       7
        7       10
        5       8
        8       9
        9       10
        9       11
        11      12
```

Fig. 7. Communication graphs data inputs.

```
G N U P L O T
Version 4.6 patchlevel 6    last modified September 2014
Build System: Linux i686

Copyright (C) 1986-1993, 1998, 2004, 2007-2014
Thomas Williams, Colin Kelley and many others
```

Fig. 8. GNUplot tool.

Latency is one of the most important parameter to estimate the performance of system. It is the time difference (in clock cycles) between when a packet gets delivered to its destination IP and when it was sent.

The latency of the system can be follow the formula (B.1) [7]

$$L_{avg} = \frac{1}{1} \sum \frac{1}{N_i} \sum L_{ij} \tag{B.1}$$

Throughput is the parameter that was used for evaluating the bandwidth of data transfer between IP cores. It can be used to estimate the quality of service the network can achieve.

The throughput of the system can be follow the formula (B.2) [7]

$$T_{avg} = \frac{1}{N(T_{sim} - T_{warm})} \sum N_i \tag{B.2}$$

Power/Energy Consumption: is also a vital parameter that needs to be taken into consideration especially in the area of developing an integrated circuits.

3 Results

For estimating of the final results in this study, we will focus on the system performances such as latency, which is the time between the emission of data and reception of this data at the destination (cycles); throughput, which defines the quality of data transmitted from source to destination per a time unit (flits/IP/cycle) [5] and Power Energy (J).

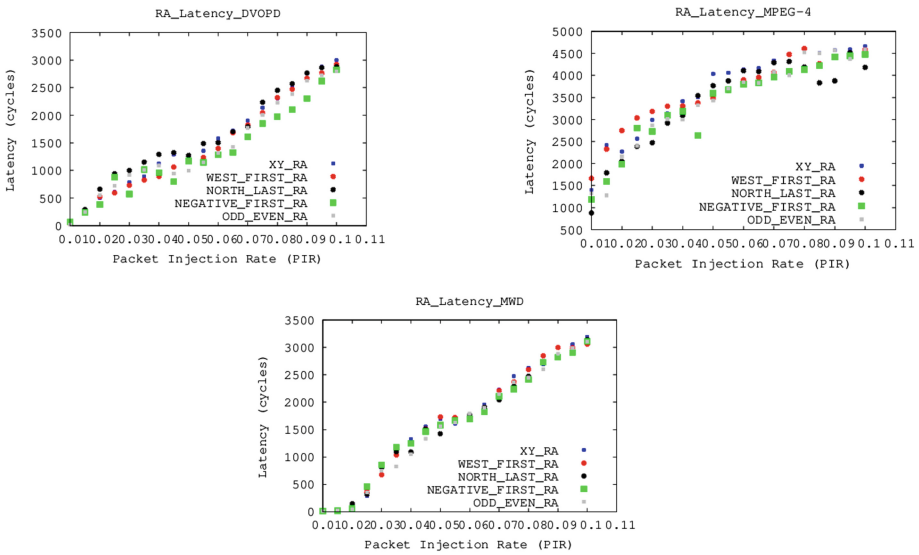

Fig. 9. The latency (cycles) of the system.

Figures 9 to 11 depict the outputs in terms of latency, throughput and power/energy corresponding to each application. First, the applications were mapped onto the NoC and NOXIM was used to run simulations with low to high packet injection rate (PIR).

The presented results provides designers with key insight into how different mappings and routing impacts NoC performance for a given application.

This will enable designers choose suitable routing algorithms for applications to be mapped on NoC. Our results show that the choice of suitable routing algorithm depends on the application requirements. If the system has real time constraint, as in Fig. 9, The NEGATIVE_FIRST algorithm is suitable. This is the case for DVOPD application. However, for MPEG-4 application, with bandwidth as highest priority factor, Fig. 10 suggest that the NORTH_LAST algorithm is most suitable.

The results obtained in this work is based on reconfiguring of the NOXIM platform [1], and we believe that similar evaluation will be obtained on a fabricated NoC system given our constraints.

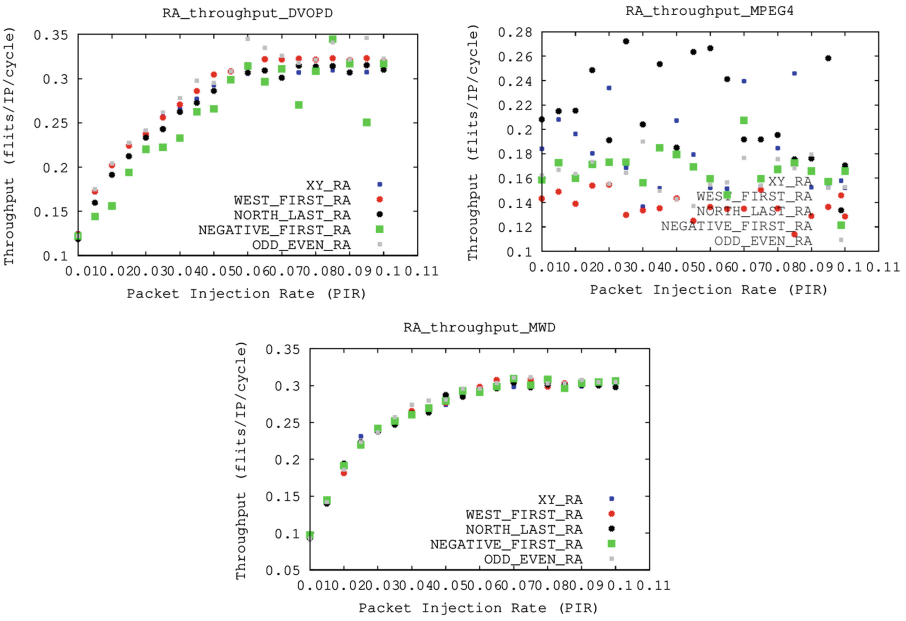

Fig. 10. The throughput (Flits/cycle/IP) of the system.

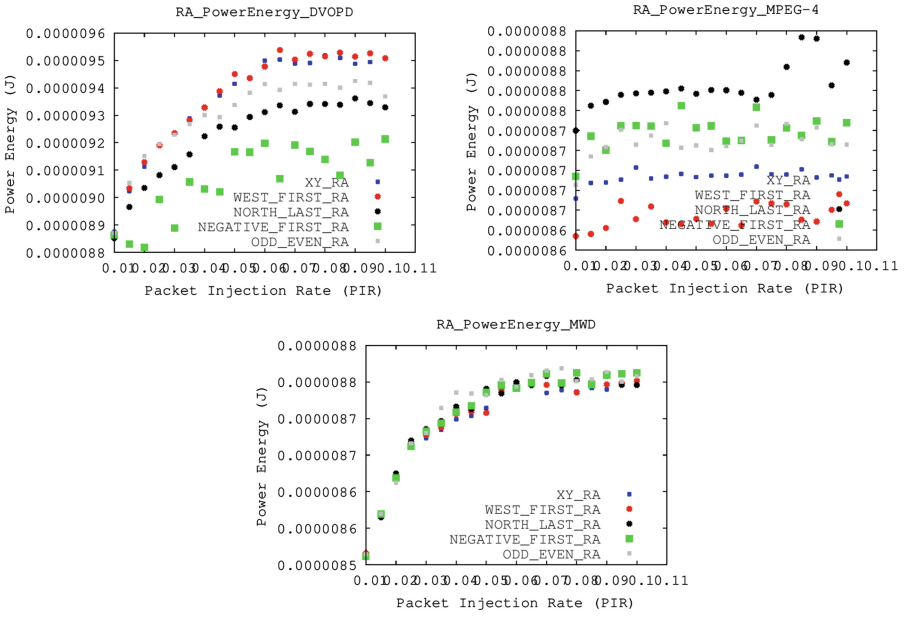

Fig. 11. The Power energy (J) of the system.

Acknowledgment. The authors would like to thank to the research group of University of Catana (Italy), especially Professor Maurizio Palesi, who helped and gave us a lot guides during we have doing this study.

We also would like to thank to Professor Xuan-Tu TRAN, who gave many useful advice for discussing section and also helping us can complete this paper with the best ability in his revising.

References

1. Catania, V., Mineo, A., Monteleone, S., Palesi, M., Patti, D.: (Italy) Noxim: an open, extensible and cycle-accurate network-on-chip simulator. In: 2015 IEEE International Conference on Application-Specific System, Architectures and Processors, pp. 27–29, Toronto, Canada, July 2015
2. NOXIM: Open Source. https://github.com/davidepatti/noxim
3. Palesi, M., Daneshtalab, M.: Routing Algorithms in Network-On-Chip. Springer Science + Business Media, New York (2014)
4. Chattopadhyay, S.: A survey on application mapping strategies for network-on-chip design. J. Syst. Archit. **59**, 60–75 (2013)
5. Xuan-Tu, T., et al.: Emerging Aspects in Electronic and Communication Engineering, pp. 91–92. Vietnam National University Publisher, Hanoi (2013)
6. ICTA2016: Open source. https://github.com/vnd2586/ICTA2016
7. Singh, J.K., et al: Performance evaluation of different routing algorithms in network on chip. In: 2013 IEEE Asian Pacific Conference on Postgraduate Research in Microelectronics and Electronics (2013)
8. Le Van, T.V., Tran, X.T.: Simulation and performance evaluation of a network-on-chip architecture based on systemC. In: Proceedings of the 5th International Conference on Advanced Technologies for Communication (ATC2012), pp. 170–175, Hanoi, October 2012
9. Dang, N.K., Le Van, T.V., Tran, X.T.: FPGA implementation of a low latency and high throughput network-on-chip router architecture. In: Proceedings of the 2011 International Conference on Integrated Circuits and Devices in Vietnam (ICDV 2011), Hanoi, August 2011
10. Le Van, T.V., Ngo, D.T., Tran, X.T.: A SystemC based simulation platform for network-on-chip architecture. In: Proceedings of the 2012 IEICE International Conference on Integrated Circuits and Devices in Vietnam (ICDV 2012), pp. 132–136, Danang, August 2012