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Section :	**3-1 L**

AIM : In How many ways one bit of information can be stored in computers. Design and verify at least three different methods using sequential logic circuits.

APPARATUS : RS, JK, T and D flip-flops,NAND & NOR gates ICs, LED, Board

Theory :

1) **RS flip flop :**

The RS Flip Flop is considered as one of the most basic sequential logic circuits. The Flip Flop is a one-bit memory bi-stable device. It has two inputs, one is called “SET” which will set the device (output = 1) and is labelled S and another is known as “RESET” which will reset the device (output = 0) labelled as R. The RS stands for SET/RESET.

Truth table below :

R	S	Output	State
0	0	No change	Previous
0	1	0	Reset
1	0	1	Set
1	1	-	Forbidden

2) **D flip flop :**

The **D**-type **flip**-**flop** is a modified Set-Reset **flip**-**flop** with the addition of an inverter to prevent the S and R inputs from being at the same logic level. One of the main disadvantages of the basic SR NAND Gate Bistable circuit is that the indeterminate input condition of SET = “0” and RESET = “0” is forbidden.These input conditions can be avoided by making them complement of each other.

Truth table given below :

D	reset	clock	Q	Q’
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	0	1

3) JK flip flop :

The **J-K flip-flop** is the most versatile of the basic **flip-flops**. It has the input- following character of the clocked D **flip-flop** but has two inputs,traditionally labeled J and K. If J and K are different then the output Q takes the value of J at the next clock edge.The RS flip flop circuit may be re-joined if both inputs are 1 than also the outputs are complement of each other as shown in **characteristics table below.**

clock	j	k	Q	Q’
1	0	0	Latch	Latch
1	0	1	0	1
1	1	0	1	0
1	1	1	Toggle	Toggle
0	0	0	Latch	Latch

0	0	1	Latch	Latch
0	1	0	Latch	Latch
0	1	1	Latch	Latch

4) T flip flop :

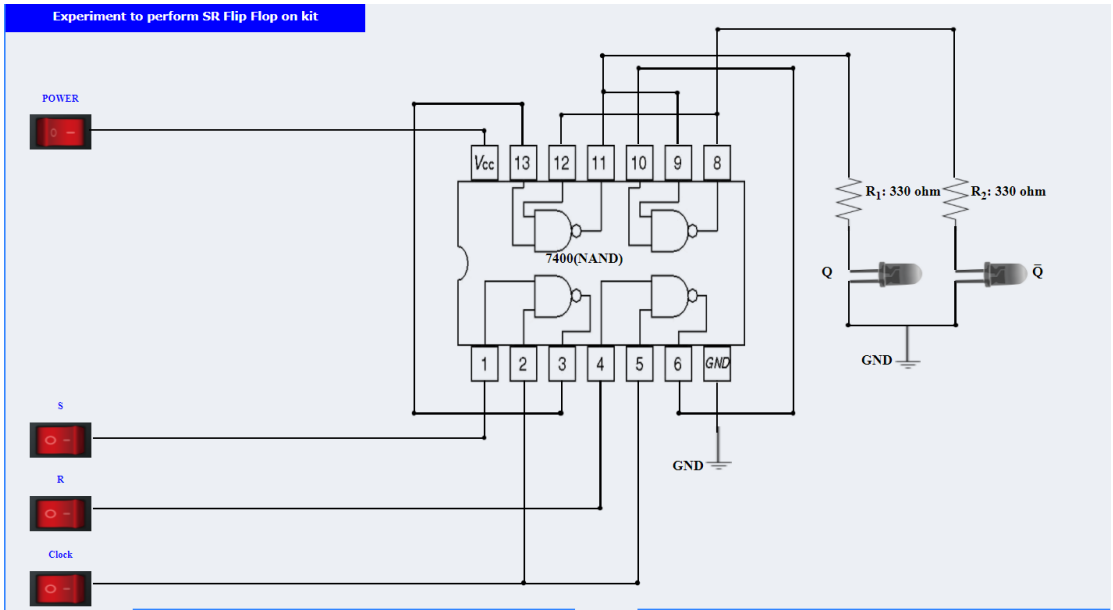
T flip – flop is also known as “Toggle Flip – flop”. To avoid the occurrence of intermediate state in SR flip – flop, we should provide only one input to the flip – flop called Trigger input or Toggle input (T). Then the flip – flop acts as a Toggle switch. Toggling means ‘Changing the next state output to complement of the present state output’.
We can design the T flip – flop by making simple modifications to the JK flip – flop. The T flip – flop is a single input device and hence by connecting J and K inputs together and giving them with single input called T we can convert a JK flip – flop into T flip – flop. So a T flip – flop is sometimes called as single input JK flip – flop.

Both the JK inputs of the JK flip – flop are held at logic 1 and the clock signal continuous to change as **shown in table below.**

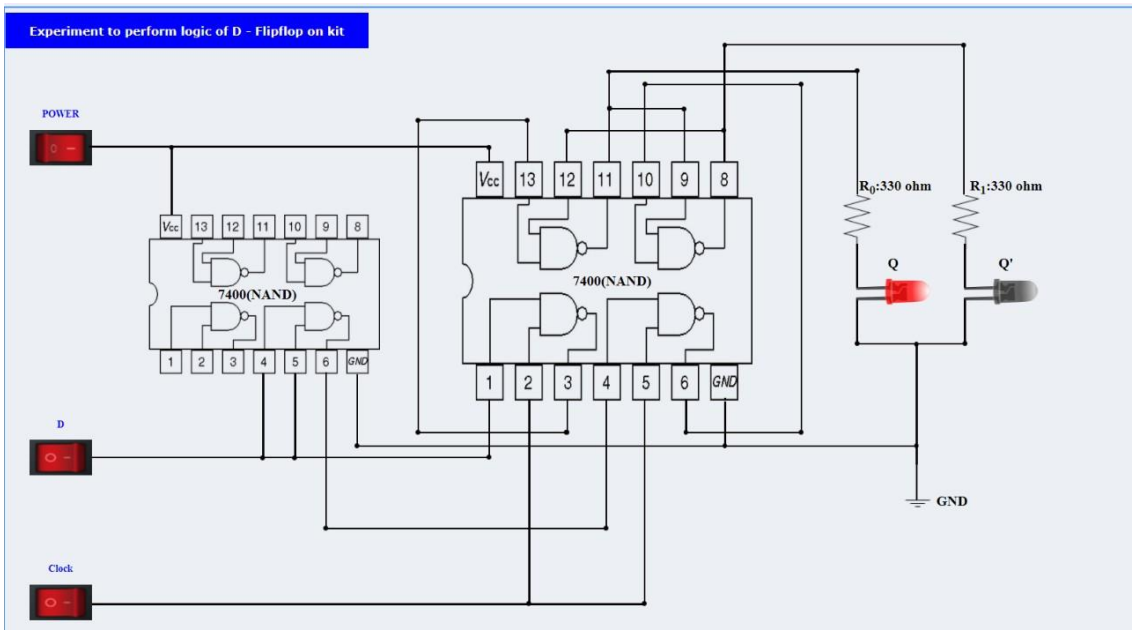
T	Q	Q’
0	0	0
1	0	1
0	1	0
1	1	0

Circuit Diagrams:

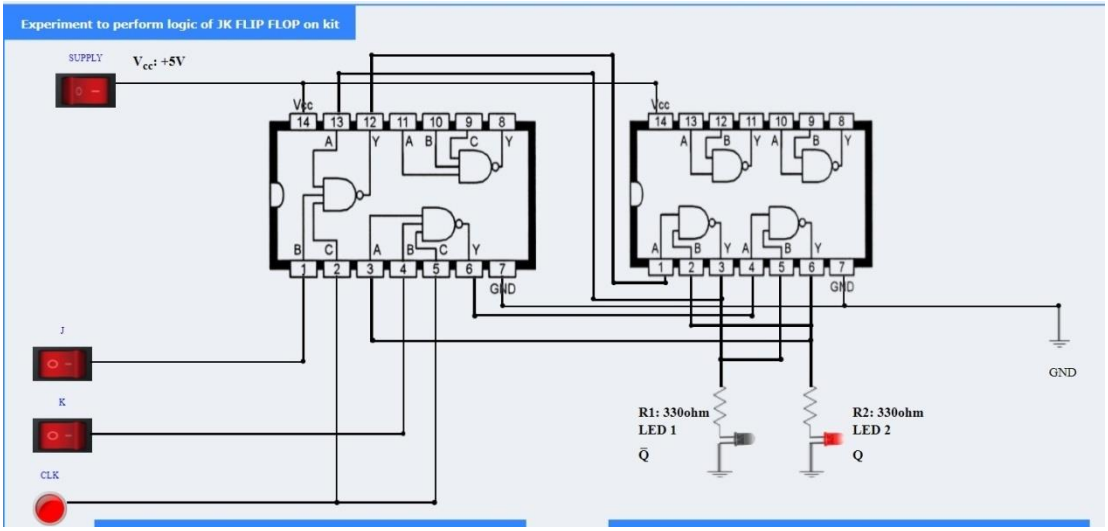
1) RS flip flop:



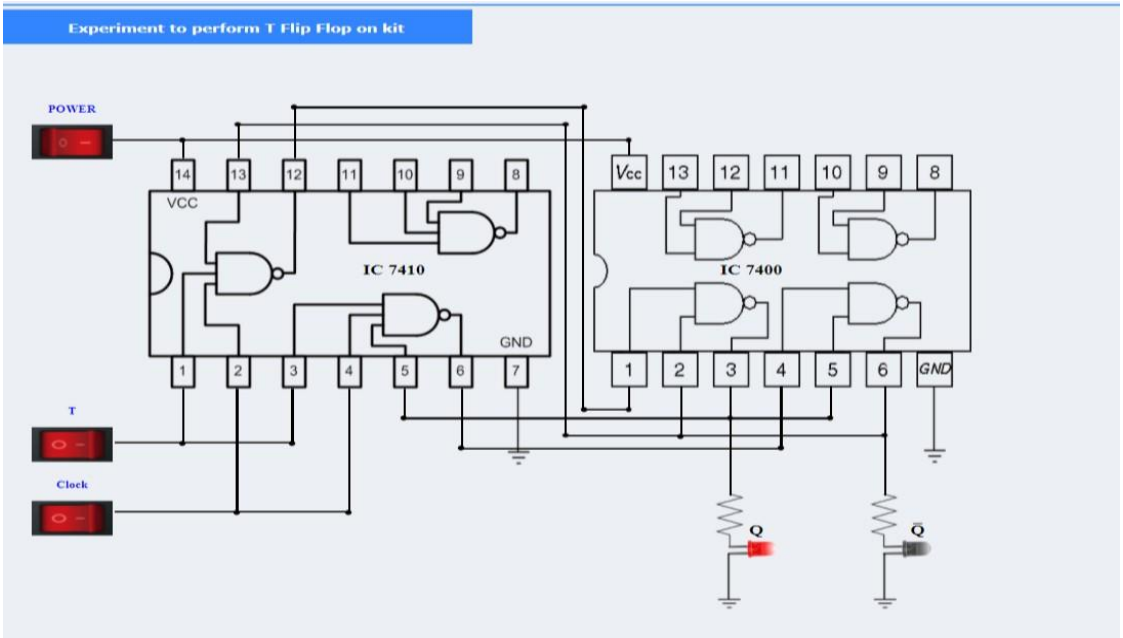
2) D flip flop :



3) JK flip flop :

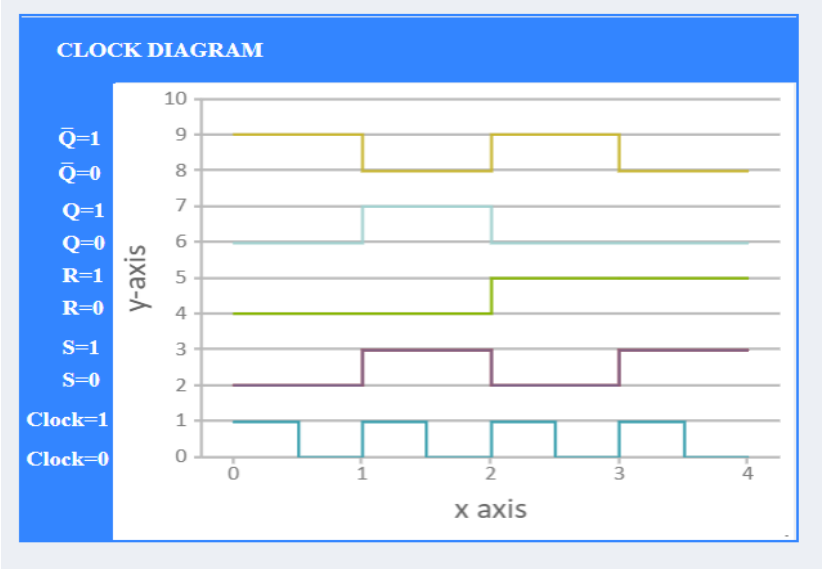


4) T flip flop :

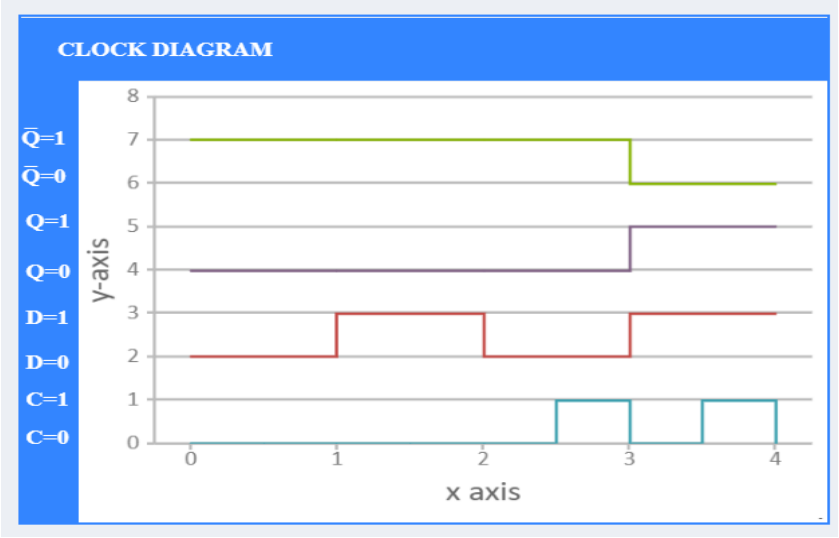


Results & Waveforms:

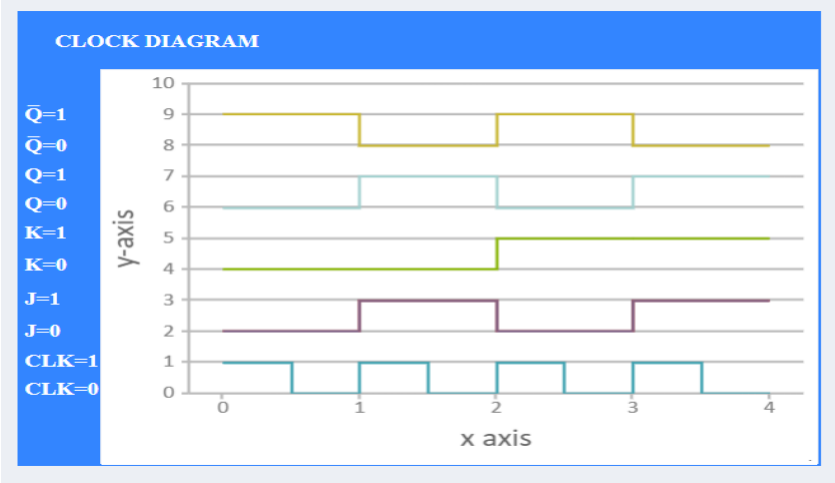
1) RS flip flop :



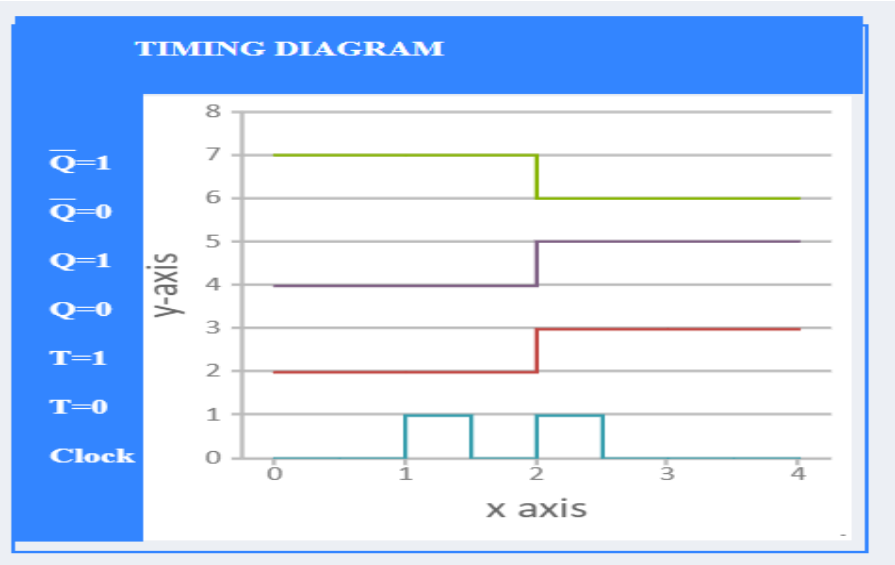
2) D flip flop :



3) JK flip flop :



4) **T flip flop :**



Observation Tables:

1) **RS flip flop :**

TRUTH TABLE PRINT Add

Serial No.	clock	S	R	Q(n-1)	$\overline{Q}$(n-1)	Q	$\overline{Q}$	Remark
1	1	0	0	0	1	0	1	No change
2	1	1	0	0	1	1	0	set
3	1	0	1	1	0	0	1	Reset
4	1	1	1	0	1	0	0	INVALID

2) **D flip flop :**

TRUTH TABLE PRINT Add

Serial No.	clock	D	Q(n-1)	Q'(n-1)	Q	Q'	Remark
1	0	0	X	X	0	1	No Change
2	0	1	0	1	0	1	No change
3	1	0	0	1	0	1	Reset
4	1	1	0	1	1	0	set

3) **JK flip flop :**

TRUTH TABLE PRINT Add

Serial No.	clock	J	K	Q(n-1)	$\overline{Q}$(n-1)	Q	$\overline{Q}$	Remark
1	1	0	0	0	1	0	1	No change
2	1	1	0	0	1	1	0	set
3	1	0	1	1	0	0	1	Reset
4	1	1	1	0	1	1	0	toggle

4) **T flip flop :**

TRUTH TABLE Add Print

Serial No.	Clock	T	Q_{n-1}	$\bar{Q}_{n-1}$	Q	$\bar{Q}$	Remarks
1	0	0	X	X	0	1	No Change
2	1	0	0	1	0	1	No change
3	1	1	0	1	1	0	Toggle
4	0	1	1	0	1	0	No Change

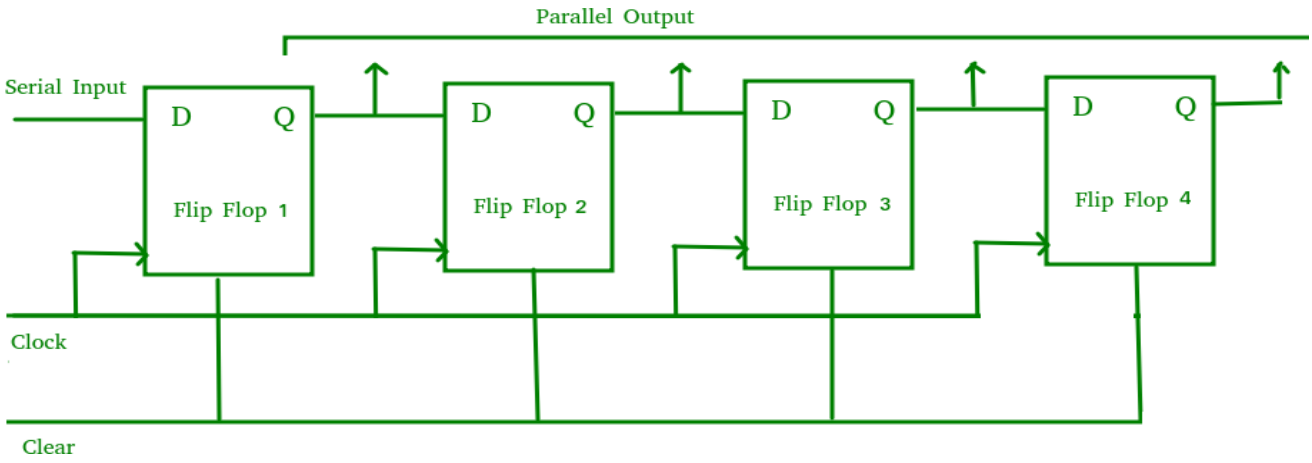
AIM: To analyze the circuit and truth table of 4-bit SIPO (serial input parallel output) shift register by using IC 7474 (D flip flop)

APPARATUS: D flip flop ICs, LED, Board

Theory:

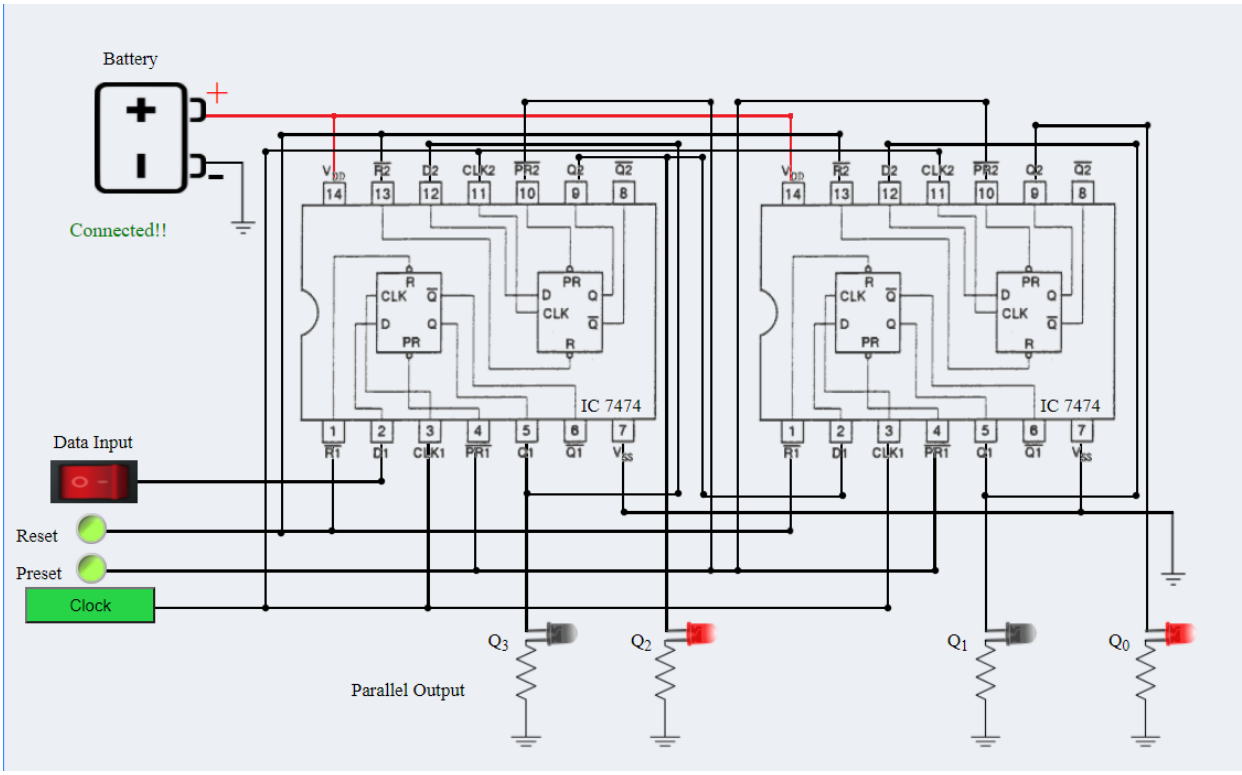
The shift register, which allows serial input (one bit after the other through a single data line) and produces a parallel output is known as Serial-In Parallel-Out shift register.

The logic circuit given below shows a serial-in-parallel-out shift register. The circuit consists of four D flip-flops which are connected. The clear (CLR) signal is connected in addition to the clock signal to all the 4 flip flops in order to RESET them. The output of the first flip flop is connected to the input of the next flip flop and so on. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop.



The above circuit is an example of shift right register, taking the serial data input from the left side of the flip flop and producing a parallel output. They are used in communication lines where demultiplexing of a data line into several parallel lines is required because the main use of the SIPO register is to convert serial data into parallel data.

Ciruit Diagram :



Observation Table :

TRUTH TABLE

Serial No.	Clock	Data Input	Q_3	Q_2	Q_1	Q_0
1	1	1	1	0	0	0
2	2	0	0	1	0	0
3	3	1	1	0	1	0
4	4	0	0	1	0	1

Aim : To verify the truth table and timing diagram of 4-bit synchronous parallel counter and 4-bit asynchronous parallel counter by using JK flip flop ICs and analyse the circuit of 4-bit synchronous parallel counter and 4-bit asynchronous parallel counter with the help of LEDs display.

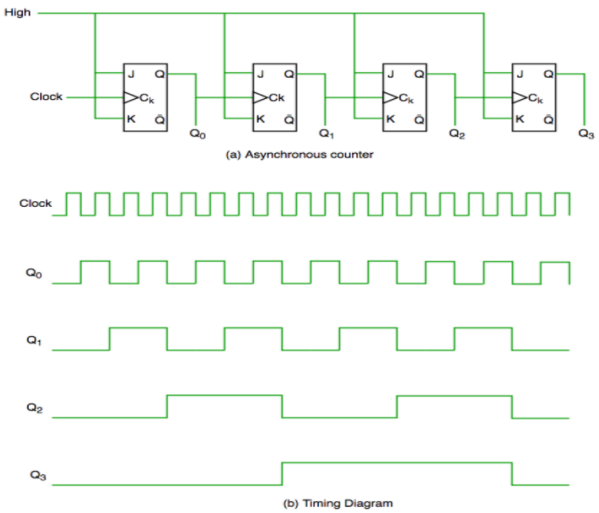
Apparatus : Virtual Lab.

Theory :

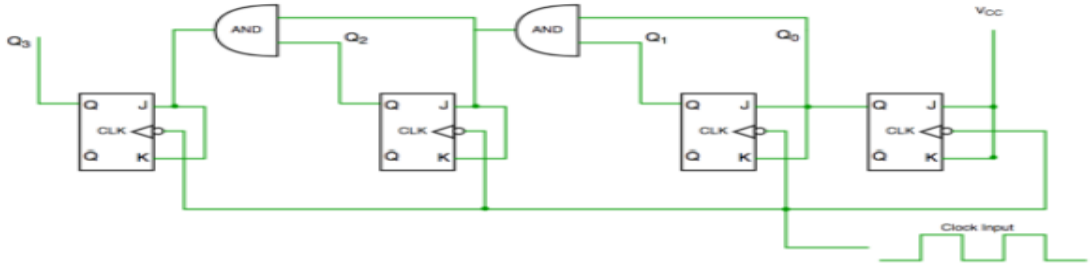
A counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. Counters are used in digital electronics for counting purpose, they can count specific event happening in the circuit. For example, in UP counter a counter increases count for every rising edge of clock.

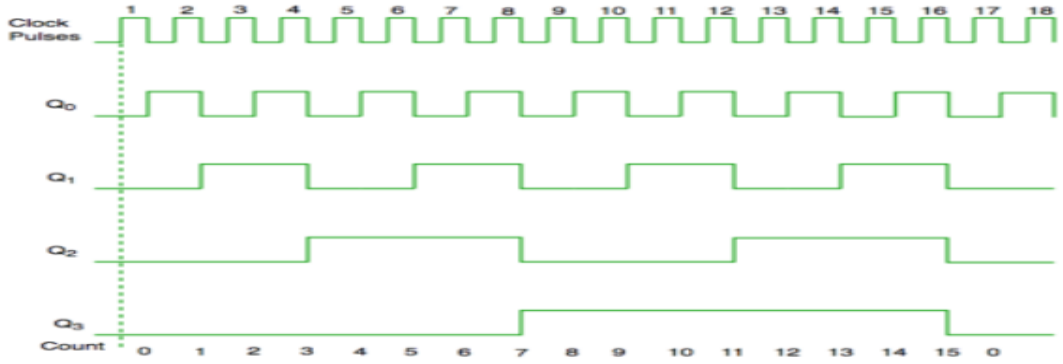
Counters are broadly divided into two categories :

1. **Asynchronous counter:** In asynchronous counter we don't use universal clock, only first flip flop is driven by main clock and the clock input of rest of the following counters is drivenby output of previous flip flops. It is also called the Ripple Counter.

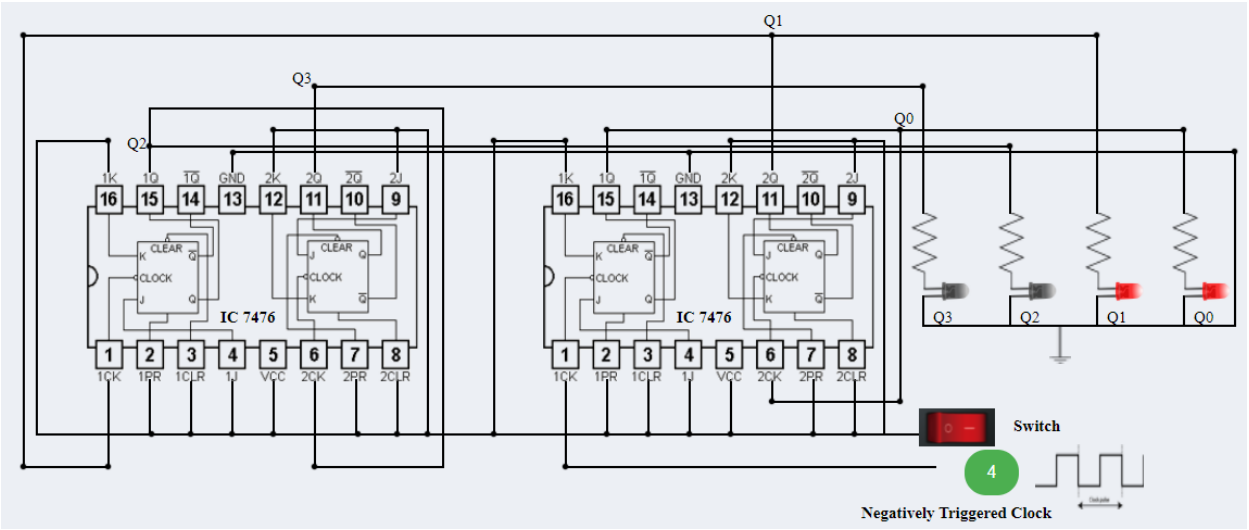


2. **Synchronous counter:** Unlike the asynchronous counter, synchronous counter has one global clock which drives each flip flop so output changes in parallel. The one advantage of synchronous counter over asynchronous counter is, it can operate on higher frequency than asynchronous counter as it does not have cumulative delay because of same clock is given to each flip flop.

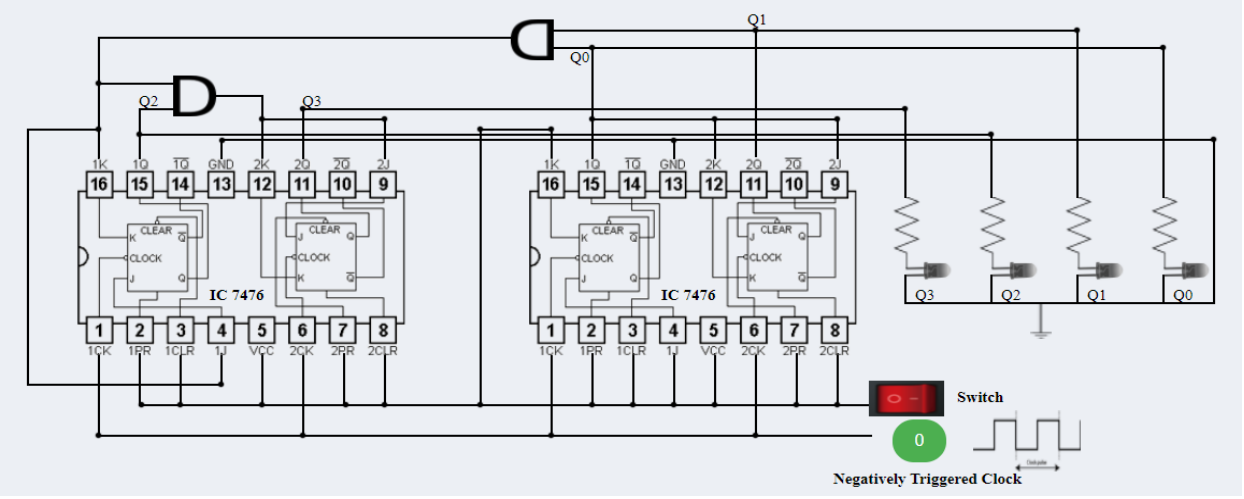




Circuit Diagram:

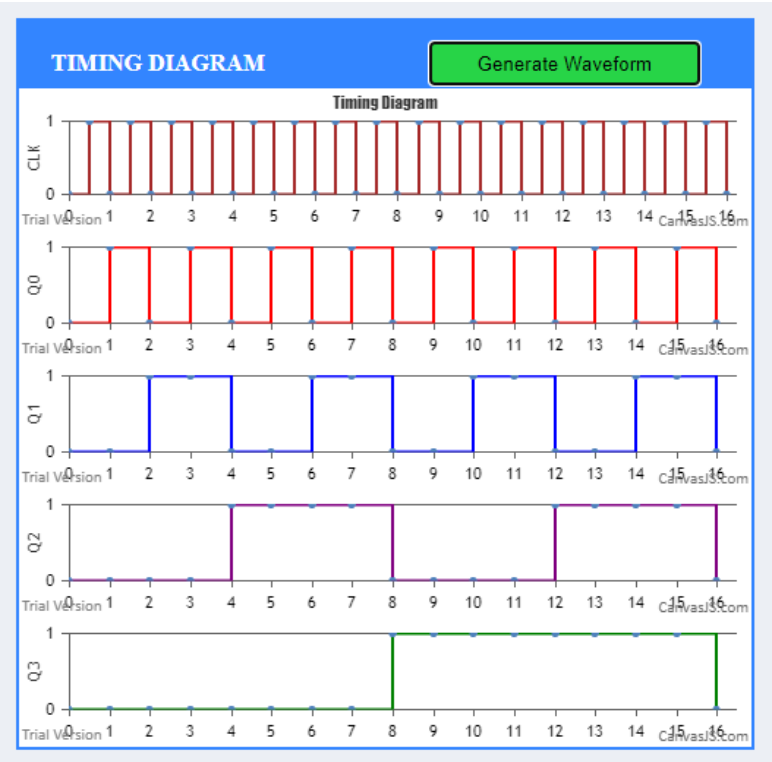


4-Bit Asynchronous Parallel Counter using J-K flip flop

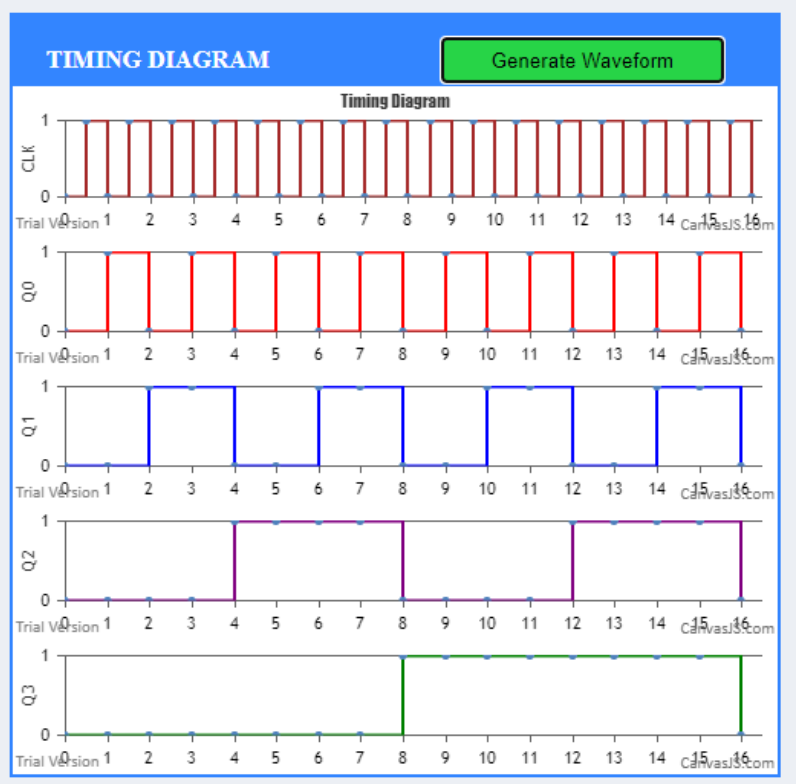


4-Bit Synchronous Parallel Counter using J-K flip flop

RESULTS AND WAVEFORMS:



Asynchronous Counter



Synchronous Counter

OBSERVATIONS:

TRUTH TABLE

Serial No.	Clock	Q3	Q2	Q1	Q0
1	0	X	X	X	X
2	1	0	0	0	0
3	2	0	0	0	1
4	3	0	0	1	0
5	4	0	0	1	1
6	5	0	1	0	0
7	6	0	1	0	1
8	7	0	1	1	0
9	8	0	1	1	1
10	9	1	0	0	0
11	10	1	0	0	1
12	11	1	0	1	0
13	12	1	0	1	1
14	13	1	1	0	0
15	14	1	1	0	1
16	15	1	1	1	0
17	16	1	1	1	1

Asynchronous Counter

TRUTH TABLE

Serial No.	Clock	Q3	Q2	Q1	Q0
1	0	X	X	X	X
2	1	0	0	0	0
3	2	0	0	0	1
4	3	0	0	1	0
5	4	0	0	1	1
6	5	0	1	0	0
7	6	0	1	0	1
8	7	0	1	1	0
9	8	0	1	1	1
10	9	1	0	0	0
11	10	1	0	0	1
12	11	1	0	1	0
13	12	1	0	1	1
14	13	1	1	0	0
15	14	1	1	0	1
16	15	1	1	1	0
17	16	1	1	1	1

Synchronous Counter