**ECE 585 FALL 2023**

**PROJECT REPORT**

“Simulation of schedular portion of a Memory Controller”

**TEAM 15**

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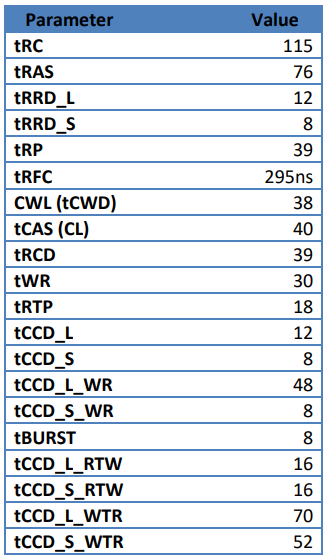
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**Project Requirements**

To simulate the schedular portion of a memory controller capable of serving a 12-core 4.8 GHz processor employing a single 16 GB PC-38400 DIMM.

The DIMM is constructed with memory chips organized as x8 devices with a 1KB page size and 40-39-39-76 timing. These devices have 8 bank groups of 4 banks each. The DIMM uses 1N mode for commands requiring two cycles. There is no system-level ECC.

All the issued DRAM commands must comply with the given DDR5 timing values.



Memory controller simulation must accept the input file name containing the all the request and output file name where all the scheduled DRAM commands will be stored. If not provided, consider default name. For Input file, default file name is trace.txt and for output file, default name is dram.txt.

**Block Diagram**

CPU Memory Requests

DRAM memory commands

Memory Controller

**Clocks:**

For implementation of schedular portion of a memory controller we will need two clocks to run parallelly i.e CPU Clock and DIMM Clock.

CPU Clock:

We need to consider 4.8 GHz CPU. That means one clock cycle of CPU clock will be of 208 ps.

DIMM Clock:

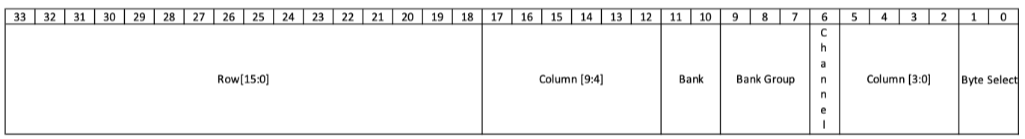
Considering DIMM PC5-38400, its clock frequency can be calculated to 2.4 GHz.

That means two CPU cycles per DIMM clock.

**Address Mapping:**

Address bits:

* 1 Channel Bit [6]
* 2 BA bits [11:10]
* 3 BG bits [9:7]
* 16 row bits [33:18]
* 10 column bits {[17:12] , [5:2]}

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**Language used for implantation:** SystemVerilog

**Implemented Scheduling Algorithms:**

LEVEL 0: Closed Page Policy

In-Order Scheduling. It closes the page once the required commands are issued in a bank.

LEVEL 1: Open Page Policy

In-Order Scheduling. It doesn’t explicitly close a page unless the queue is non-empty and the next in-order reference is to a different row in the same bank.

**Pseudo code for main loop:**

while not done {

while file is scanned till end of the file {

If cpu clock tick {

on every dim {

process any pending request

pop any completed request

update timers

}

If there is any space to add request in queue{

scan request from file

add request if request time has reached simulation time

}

}

Increment cpu clock

}

while queue is not empty {

on cpu and dimm clock {

process any pending request

pop any completed request

update timers

}

Increment cpu clock

}

If queue is empty set done

}

**Test Plan**

Testcase 1: ClosedPagePolicy: Timing Contraints check

Objectives:

* To check if tRCD is satisfied for each ACT0 -> RD0/WR0
* tCL + tBURST (RD0 -> pop out)
* tRP (PRE)
* tRAS (ACT0 to PRE)
* tWCD + tBURST + tWR (WR0 to PRE)

Test file:

60 2 1 01FF97000

61 2 1 01FF97001

62 2 1 01FF97002

63 2 1 01FF97003

64 2 1 01FF97004

30 0 2 01FF97000

31 1 2 01FF97001

32 2 2 01FF97002

33 3 2 01FF97003

34 4 2 01FF97004

Results:

62 0 ACT0 0 0 7FE

64 0 ACT1 0 0 7FE

140 0 WR0 0 0 170

142 0 WR1 0 0 170

292 0 PRE 0 0

370 0 ACT0 0 0 7FE

372 0 ACT1 0 0 7FE

448 0 WR0 0 0 170

450 0 WR1 0 0 170

600 0 PRE 0 0

678 0 ACT0 0 0 7FE

680 0 ACT1 0 0 7FE

756 0 WR0 0 0 170

758 0 WR1 0 0 170

908 0 PRE 0 0

986 0 ACT0 0 0 7FE

988 0 ACT1 0 0 7FE

1064 0 WR0 0 0 170

1066 0 WR1 0 0 170

1216 0 PRE 0 0

1294 0 ACT0 0 0 7FE

1296 0 ACT1 0 0 7FE

1372 0 WR0 0 0 171

1374 0 WR1 0 0 171

1524 0 PRE 0 0

1602 0 ACT0 0 0 7FE

1604 0 ACT1 0 0 7FE

1680 0 RD0 0 0 170

1682 0 RD1 0 0 170

1754 0 PRE 0 0

1832 0 ACT0 0 0 7FE

1834 0 ACT1 0 0 7FE

1910 0 RD0 0 0 170

1912 0 RD1 0 0 170

1984 0 PRE 0 0

2062 0 ACT0 0 0 7FE

2064 0 ACT1 0 0 7FE

2140 0 RD0 0 0 170

2142 0 RD1 0 0 170

2214 0 PRE 0 0

2292 0 ACT0 0 0 7FE

2294 0 ACT1 0 0 7FE

2370 0 RD0 0 0 170

2372 0 RD1 0 0 170

2444 0 PRE 0 0

2522 0 ACT0 0 0 7FE

2524 0 ACT1 0 0 7FE

2600 0 RD0 0 0 171

2602 0 RD1 0 0 171

2674 0 PRE 0 0

Testcase 2: ClosedPagePolicy: Back-to-back read on same bank and same bank group

Objective:

* To check if tRP is satisfied between first Pre and next ACT0.

Test file:

0 0 0 000000000

1 1 0 00001003F

2 2 1 00007F4BC

3 3 1 0000884B5

4 4 2 000084930

5 5 2 00008192F

Results:

2 0 ACT0 0 0 0

4 0 ACT1 0 0 0

80 0 RD0 0 0 0

82 0 RD1 0 0 0

154 0 PRE 0 0

232 0 ACT0 0 0 0

234 0 ACT1 0 0 0

310 0 RD0 0 0 10F

312 0 RD1 0 0 10F

384 0 PRE 0 0

408 0 ACT0 1 1 1

410 0 ACT1 1 1 1

486 0 WR0 1 1 3FF

488 0 WR1 1 1 3FF

638 0 PRE 1 1

716 0 ACT0 1 1 2

718 0 ACT1 1 1 2

794 0 WR0 1 1 8D

796 0 WR1 1 1 8D

946 0 PRE 1 1

948 0 ACT0 2 2 2

950 0 ACT1 2 2 2

1026 0 RD0 2 2 4C

1028 0 RD1 2 2 4C

1100 0 PRE 2 2

1178 0 ACT0 2 2 2

1180 0 ACT1 2 2 2

1256 0 RD0 2 2 1B

1258 0 RD1 2 2 1B

1330 0 PRE 2 2

Testcase 3: Advance timing enhancement

Objective:

* Checking the queue handling capability of memory controller

Test File:

0 0 0 00001F002

1 1 1 000076485

2 2 2 0000B090A

3 3 0 0000FFD8C

4 4 1 000108212

5 5 2 000156695

6 6 0 00018CB1B

2000 10 1 3DD77792B

Results:

2 0 ACT0 0 0 0

4 0 ACT1 0 0 0

80 0 RD0 0 0 1F0

82 0 RD1 0 0 1F0

154 0 PRE 0 0

178 0 ACT0 1 1 1

180 0 ACT1 1 1 1

256 0 WR0 1 1 361

258 0 WR1 1 1 361

408 0 PRE 1 1

410 0 ACT0 2 2 2

412 0 ACT1 2 2 2

488 0 RD0 2 2 302

490 0 RD1 2 2 302

562 0 PRE 2 2

586 0 ACT0 3 3 3

588 0 ACT1 3 3 3

664 0 RD0 3 3 3F3

666 0 RD1 3 3 3F3

738 0 PRE 3 3

762 0 ACT0 4 0 4

764 0 ACT1 4 0 4

840 0 WR0 4 0 84

842 0 WR1 4 0 84

992 0 PRE 4 0

994 0 ACT0 5 1 5

996 0 ACT1 5 1 5

1072 0 RD0 5 1 165

1074 0 RD1 5 1 165

1146 0 PRE 5 1

1170 0 ACT0 6 2 6

1172 0 ACT1 6 2 6

1248 0 RD0 6 2 C6

1250 0 RD1 6 2 C6

1322 0 PRE 6 2

2002 0 ACT0 2 2 F75D

2004 0 ACT1 2 2 F75D

2080 0 WR0 2 2 37A

2082 0 WR1 2 2 37A

2232 0 PRE 2 2

TestCase 4: OpenPagePolicy:

Objective:

* To Check the relative timing constraints: tCCD\_L\_WR, tCCD\_L\_WTR, tCCD\_S\_WTR

Test File:  
0 0 0 000040000

1 1 0 0000BF03D

2 2 0 00004103A

3 3 0 000082037

4 4 0 0000C44B0

5 5 0 0000C84AD

6 6 0 00009002A

7 7 1 000060927

8 8 1 000050920

9 9 1 0000C8D9D

10 10 1 000044D1A

11 11 0 000042017

12 12 1 000041010

13 0 0 0000C048D

14 1 1 0000E0D0C

15 2 0 0000FFD07

Results:

2 0 ACT0 0 0 1

4 0 ACT1 0 0 1

80 0 RD0 0 0 0

82 0 RD1 0 0 0

178 0 PRE 0 0

256 0 ACT0 0 0 2

258 0 ACT1 0 0 2

334 0 RD0 0 0 3FF

336 0 RD1 0 0 3FF

432 0 PRE 0 0

510 0 ACT0 0 0 1

512 0 ACT1 0 0 1

588 0 RD0 0 0 1E

590 0 RD1 0 0 1E

686 0 PRE 0 0

764 0 ACT0 0 0 2

766 0 ACT1 0 0 2

842 0 RD0 0 0 2D

844 0 RD1 0 0 2D

940 0 ACT0 1 1 3

942 0 ACT1 1 1 3

1018 0 RD0 1 1 4C

1020 0 RD1 1 1 4C

1116 0 RD0 1 1 8B

1118 0 RD1 1 1 8B

1214 0 RD0 0 0 10A

1216 0 RD1 0 0 10A

1312 0 ACT0 2 2 1

1314 0 ACT1 2 2 1

1390 0 WR0 2 2 209

1392 0 WR1 2 2 209

1486 0 WR0 2 2 108

1488 0 WR1 2 2 108

1580 0 ACT0 3 3 3

1582 0 ACT1 3 3 3

1658 0 WR0 3 3 87

1660 0 WR1 3 3 87

1752 0 ACT0 2 3 1

1754 0 ACT1 2 3 1

1830 0 WR0 2 3 46

1832 0 WR1 2 3 46

1924 0 PRE 0 0

2002 0 ACT0 0 0 1

2004 0 ACT1 0 0 1

2080 0 RD0 0 0 25

2082 0 RD1 0 0 25

2178 0 WR0 0 0 14

2180 0 WR1 0 0 14

2282 0 RD0 1 1 3

2284 0 RD1 1 1 3

2380 0 PRE 2 3

2458 0 ACT0 2 3 3

2460 0 ACT1 2 3 3

2536 0 WR0 2 3 203

2538 0 WR1 2 3 203

2676 0 RD0 2 3 3F1

2678 0 RD1 2 3 3F1