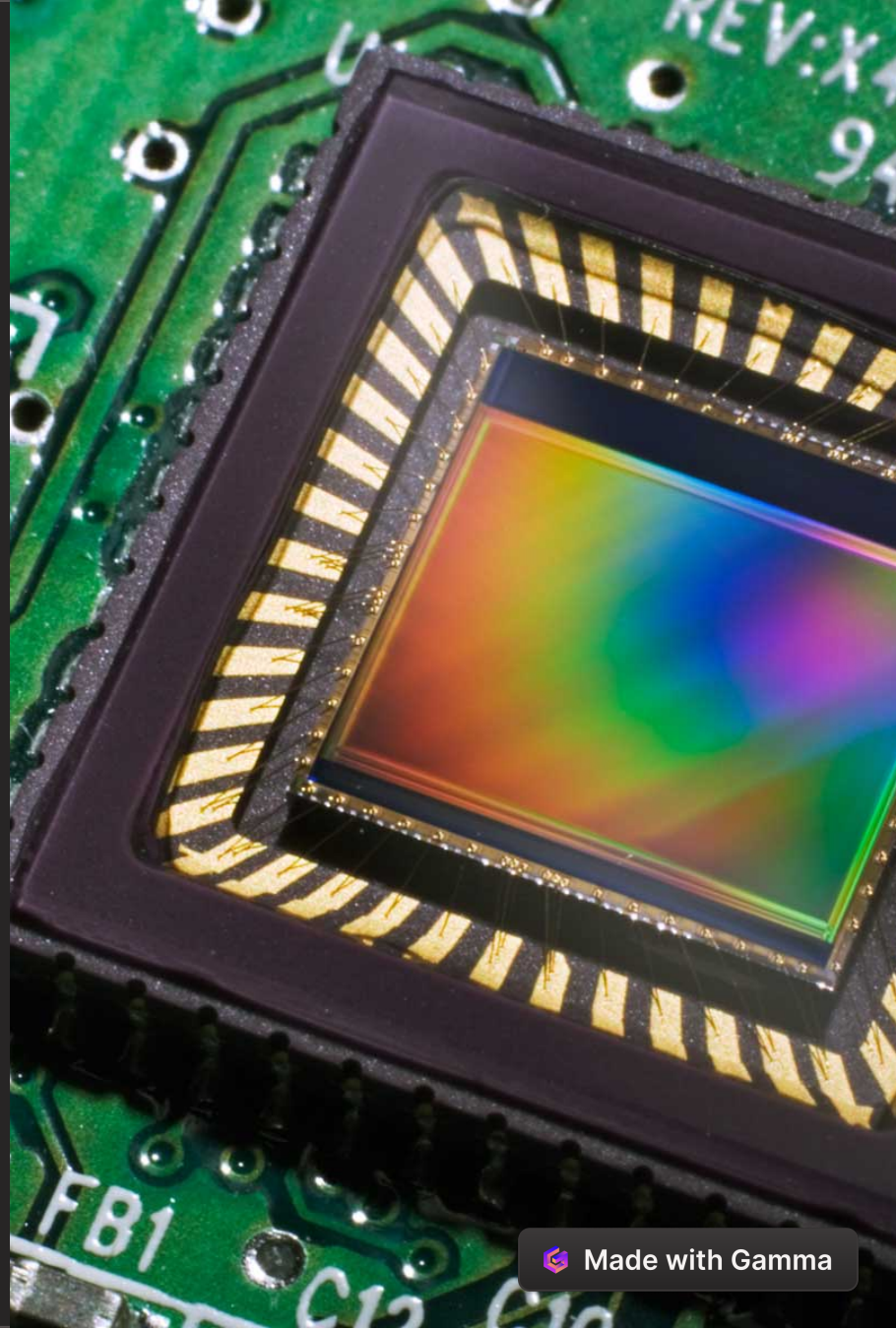
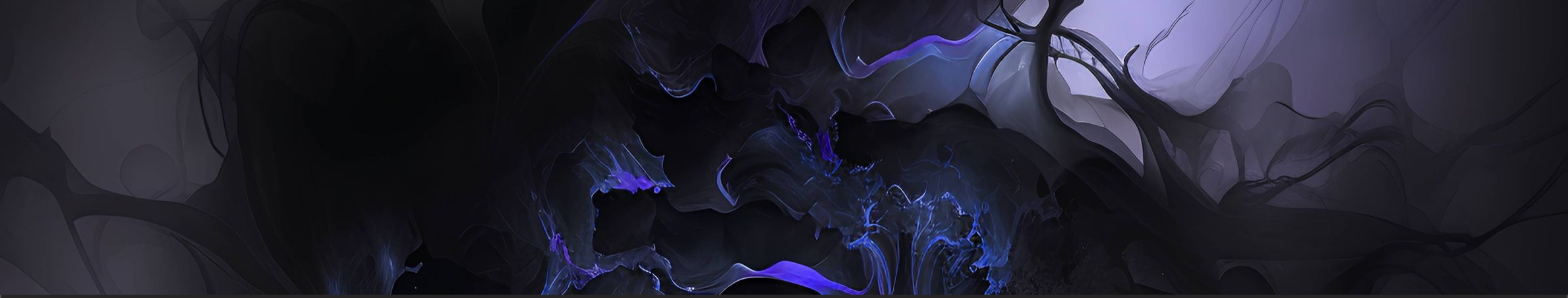
Introduction to CMOS and CMOS Level Gate Design

CMOS (Complementary Metal-Oxide-Semiconductor) is a popular technology used to design digital circuits. In this presentation, we'll go over the basics of CMOS and CMOS level gate design, and discuss their applications in the industry and academia.

by Anusha Amar





Basic and Universal Gates in CMOS Level Design

Basic Gates

Basic gates such as AND, OR, and NOT are the building blocks of digital circuits. CMOS technology allows us to implement these gates using transistors.

Universal Gates

A universal gate is a gate that can be used to implement any Boolean function. NAND and NOR are examples of universal gates. We'll discuss their implementation using CMOS technology.

Implementing Gates with Transistors

We'll take a closer look at how we can use MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) to implement gates in CMOS technology.

Designing General Boolean Circuits Using CMOS Gates

1

Combinational Logic

We'll discuss how we can design combinational logic circuits using CMOS gates. Combinational logic circuits have an output that depends only on the input.

2

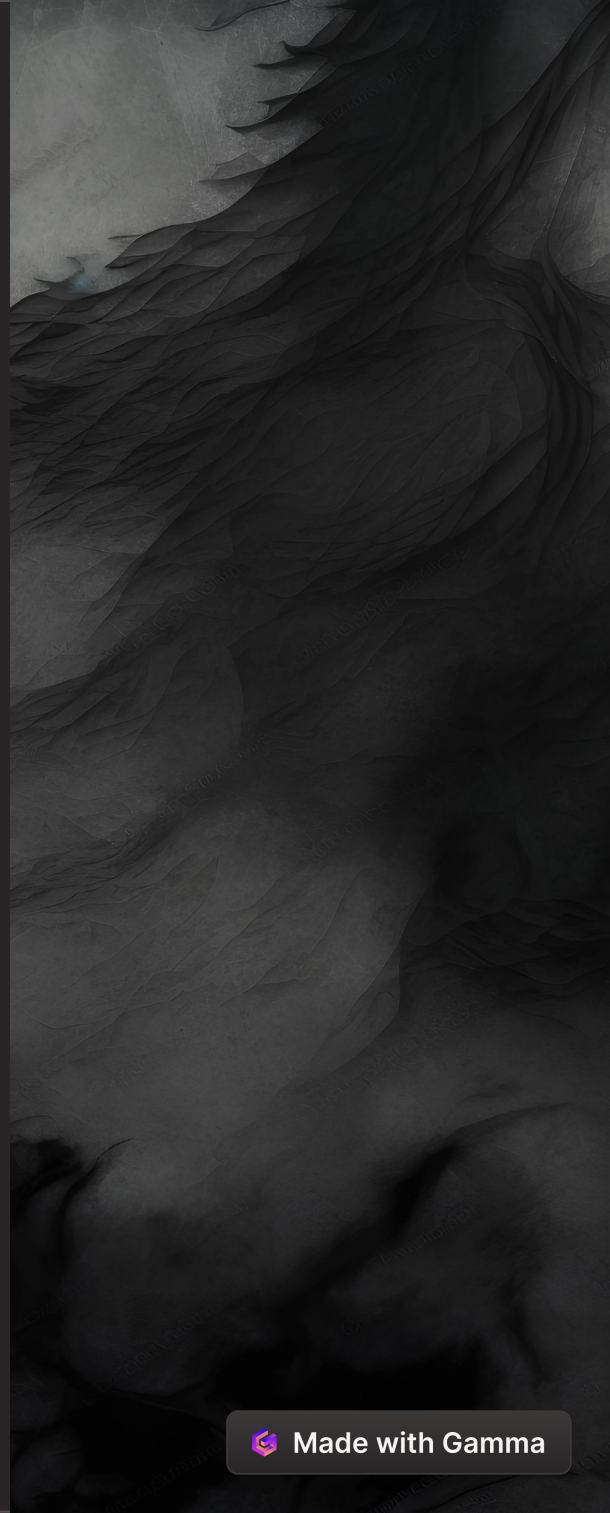
Sequential Logic

Sequential logic circuits have an output that depends on the input as well as the current state of the circuit. We'll discuss how we can design sequential logic circuits using CMOS gates.

3

Examples

We'll go over some examples of Boolean circuits and show how they can be implemented using CMOS gates.



CMOS Level Design of Latches and Flip-Flops

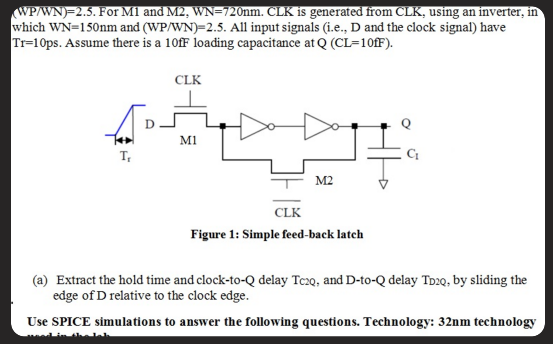
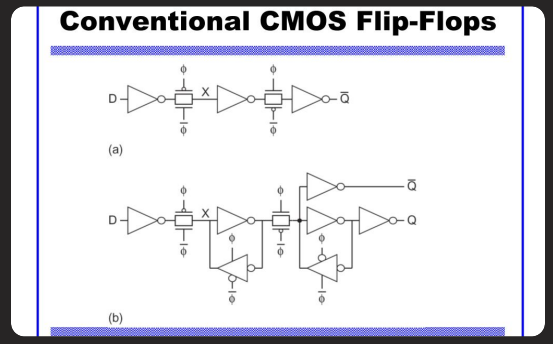
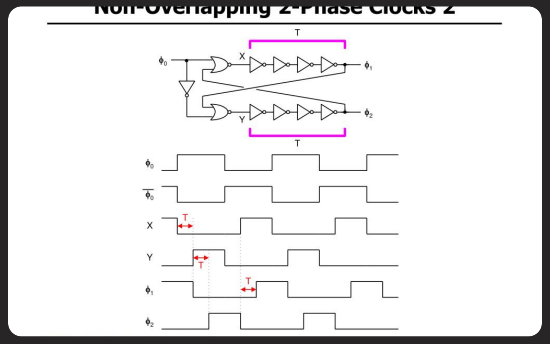

(WP/WN)=2.5. For M1 and M2, WN=720nm. CLK is generated from CLK, using an inverter, in which WN=150nm and (WP/WN)=2.5. All input signals (i.e., D and the clock signal) have Tr=10ps. Assume there is a 10fF loading capacitance at Q (CL=10fF).

Figure 1: Simple feed-back latch

(a) Extract the hold time and clock-to-Q delay T_{C2Q}, and D-to-Q delay T_{D2Q}, by sliding the edge of D relative to the clock edge.

Use SPICE simulations to answer the following questions. Technology: 32nm technology





CMOS Latch Design

A latch is a basic storage element that stores a single bit of data. We'll discuss how we can design a CMOS latch and go over its properties.

CMOS Flip-Flop Design

A flip-flop is another storage element that can store a single bit of data. We'll discuss how we can design a CMOS flip-flop and go over its properties.

Timing Analysis

We'll discuss how we can analyze the timing of our CMOS circuits, including the clock signal that drives the latches and flip-flops.

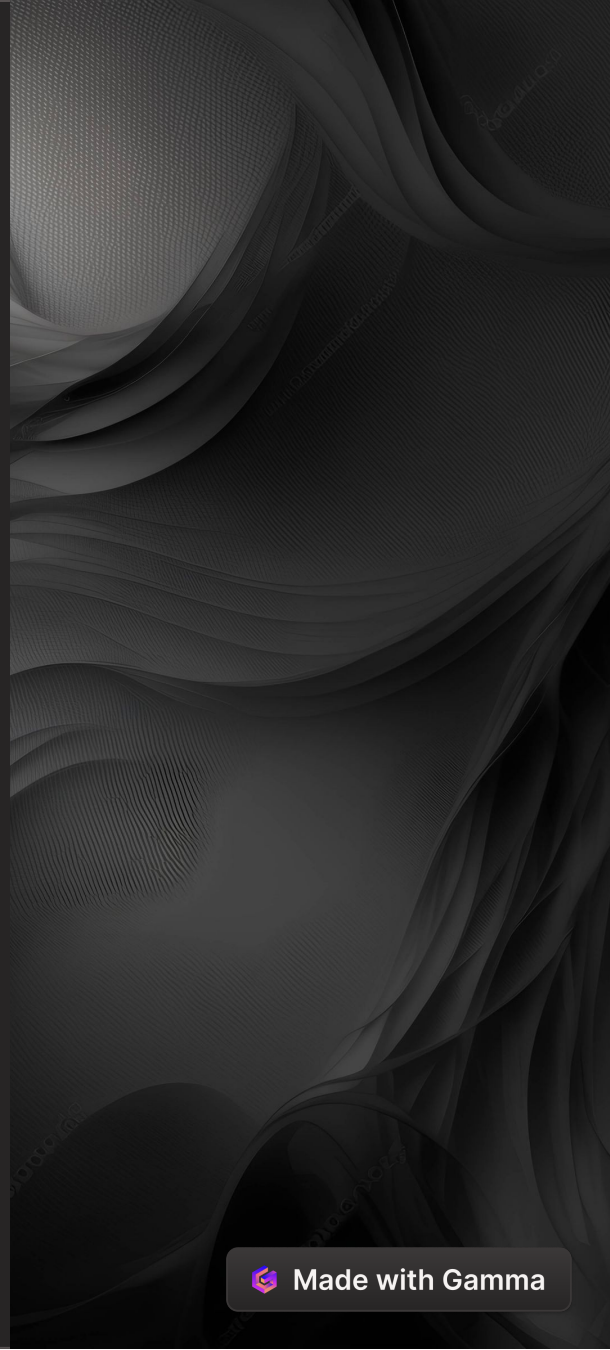
Verilog Description of CMOS Level Design

1 Verilog HDL

Verilog is a Hardware Description Language (HDL) used to describe digital systems. We'll discuss how we can use Verilog to describe CMOS circuits.

2 Simulation and Synthesis

We'll discuss how we can use Verilog to simulate and synthesize our CMOS designs, and go over some best practices for using Verilog.



Applications of CMOS Level Design in Industry and Academia

Industry

- CMOS circuits are used in a wide range of industries, including consumer electronics, aerospace, and telecommunications.
- CMOS technology is constantly evolving, and new advancements are being made to improve its power consumption, speed, and reliability.

Academia

- CMOS is a popular topic in academia, and many researchers are studying new ways to design CMOS circuits.
- CMOS technology is also being used to develop new computing paradigms, such as quantum computing.

Conclusion and Key Takeaways

CMOS technology has revolutionized the world of digital circuits. By using MOSFETs to implement gates, we can design circuits with low power consumption, high speed, and high reliability. We hope this presentation has given you a better understanding of CMOS and CMOS level gate design, and some ideas for how you can use it in your own projects.

Learn More

Contact Us