Intel APIC Architecture

From Wikipedia, the free encyclopedia

The Intel **APIC Architecture** is a system of advanced programmable interrupt controllers (APICs) designed by Intel for use in symmetric multiprocessor (SMP) computer systems. It was originally implemented by the Intel 82093AA and 82489DX, and is found in most x86 SMP motherboards. It is one of several attempts to solve interrupt routing efficiency issues in multiprocessor computer systems.

Contents

- 1 Overview
  - 1.1 Local APICs
  - 1.2 I/O APICs
- 2 Problems
- 3 More information
- 4 See also
- 5 References
- 6 External links

Overview

There are two components in the Intel APIC system, the *local APIC* (LAPIC) and the *I/O APIC*. There is one LAPIC in each CPU in the system. There is typically one I/O APIC for each peripheral bus in the system. In original system designs, LAPICs and I/O APICs were connected by a dedicated APIC bus. Newer systems use the system bus for communication between all APIC components.

In systems containing an 8259 PIC, the 8259 may be connected to the LAPIC in the system's bootstrap processor (BSP), or to one of the system's I/O APICs, or both. Logically, however, the 8259 is only connected once at any given time.

Local APICs

LAPICs manage all external interrupts for some specific processor in an SMP system. In addition, it is able to accept and generate inter-processor interrupts (IPIs) between LAPICs. LAPICs may support up to 224 usable interrupt vectors from an I/O APIC. Vectors numbers 0 to 31, out of 0 to 255, are reserved for exception handling by x86 processors.

I/O APICs

I/O APICs contain a redirection table, which is used to route the interrupts it receives from peripheral buses to one or more local APICs.

Problems

There are a number of known bugs in implementations of APIC systems, especially with concern to how the 8254 is connected. Defective BIOSes may not set up interrupt routing properly, or provide incorrect ACPI tables and Intel MultiProcessor Specification (MPS) tables. Finally, the APIC can also be a cause of system failure when the operating system does not support it properly. On older operating systems, people often had to disable the I/O and local APICs. While this is not possible anymore due to the prevalence of Symmetric multiprocessor and multi-core systems, the bugs in the firmware and the operating systems are now a rare occurrence.

More information

More information on the Intel APIC Architecture can be found in the *Intel 64 and IA-32 Intel Architecture Software Developer's Manual (http://www.intel.com/products/processor/manuals/index.htm), Volume 3A: System Programming Guide, Part 1, Chapter 10*, freely available on the Intel website.

See also

- Intel 8259
- Advanced Programmable Interrupt Controller (APIC)
- Programmable Interrupt Controller (PIC)
- Inter-processor interrupt (IPI)
- Interrupt
- Interrupt handler
- Message Signaled Interrupts (MSI)
- Non-maskable interrupt (NMI)
- x2APIC
- List of Intel CPU microarchitectures

References

External links

- Intel 64 and IA-32 Architectures Software Developer Manuals (http://www.intel.com/content/www/us/en/processors/architectures-software-developer-manuals.html)

- MultiProcessor Specification (http://www.intel.com/design/archives/processors/pro/docs/242016.htm)
- Intel 82093AA I/O Advanced Programmable Interrupt Controller (I/O APIC) Datasheet (http://www.intel.com/design/chipsets/datashts/290566.htm)
- Key Benefits of the I/O APIC (http://www.microsoft.com/whdc/archive/io-apic.mspx) Microsoft's explanation of I/O APIC
- Importance of Implementing APIC-Based Interrupt Subsystems on Uniprocessor PCs (http://www.microsoft.com/whdc/archive/apic.mspx)
- Advanced Programmable Interrupt Controller (http://osdev.berlios.de/pic.html) A short introduction of what APIC is and its benefits

Retrieved from "http://en.wikipedia.org/w/index.php?title=Intel_APIC_Architecture&oldid=566993620"
Categories: Intel products | IBM PC compatibles | X86 architecture | Interrupts

---