CO224 - Computer Architecture
Lab 6 - Building a Memory Hierarchy
Part 2 – Data Cache

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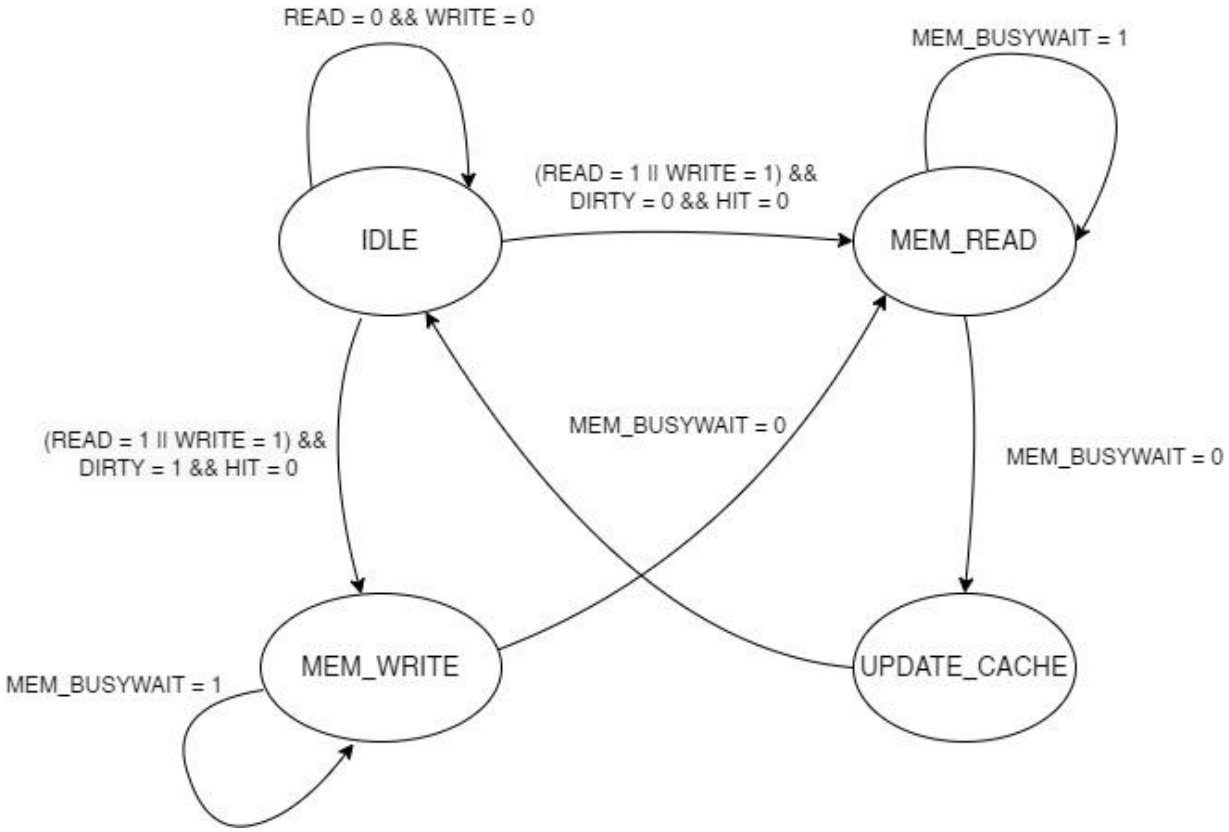
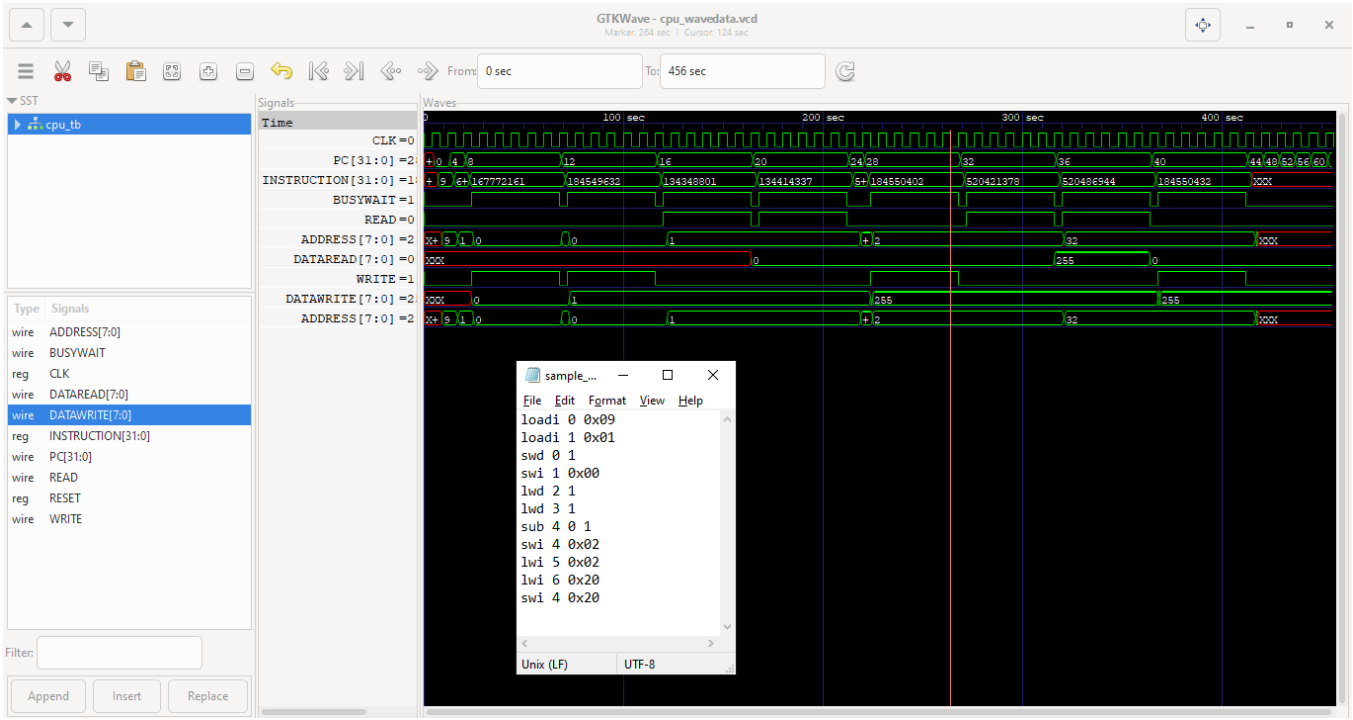
Finite State Machine in the cache



Timing Diagram without cache.



Timing Diagram with data cache.