mem4kBytesOr32kbitsSpec

SRAM (1024 x 32): (32kbits or 4kB), 1.8V and access time is <2.5ns

SRAM 4 kb or 32bits

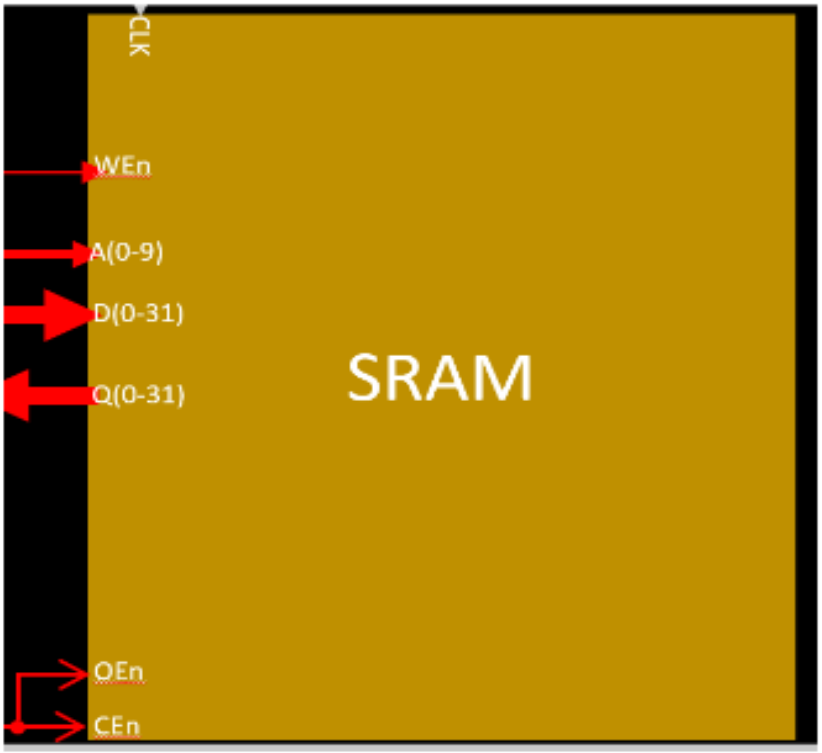
- **Specs released under APACHE LICENSE 2.0**

- **Contact Kunal in case of any clarifications needed at kunalpghosh@gmail.com**

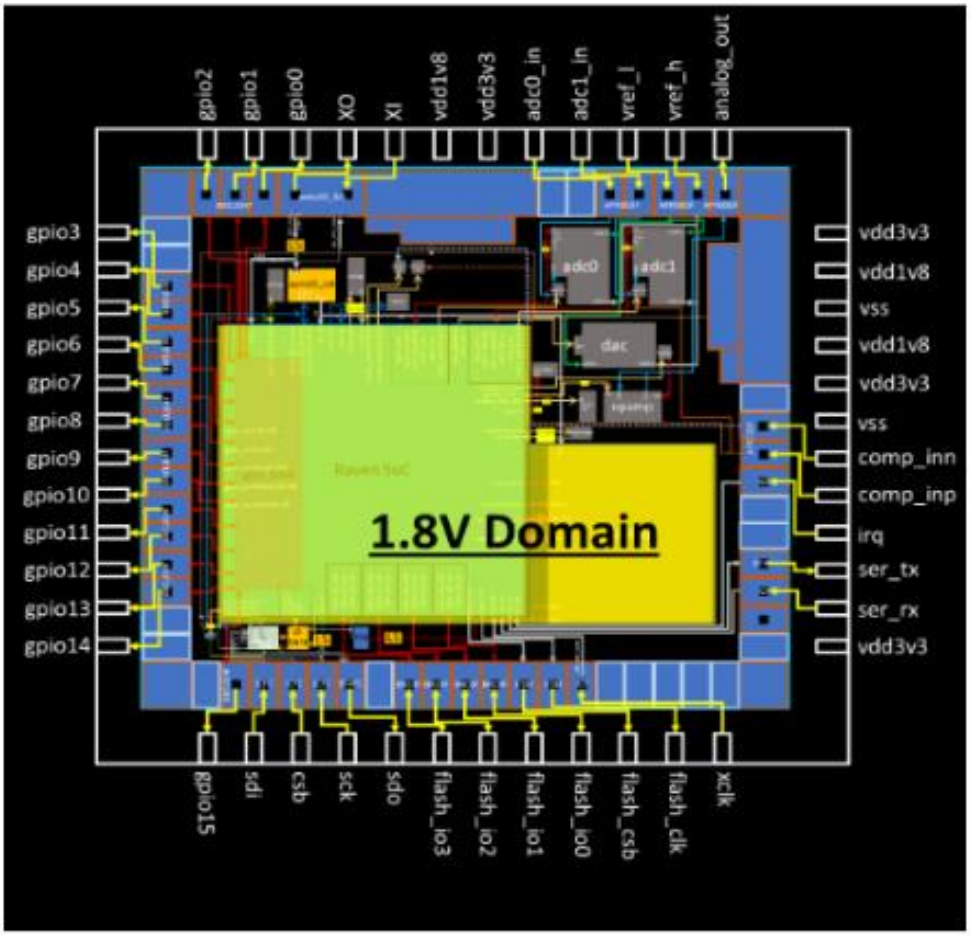
https://www.vlsisystemdesign.com/

What we need?

SRAM (1024 x 32): (32kbits or 4kB), 1.8V and access time is <2.5ns@scl180nm



On-chip Physical Location and voltage domain



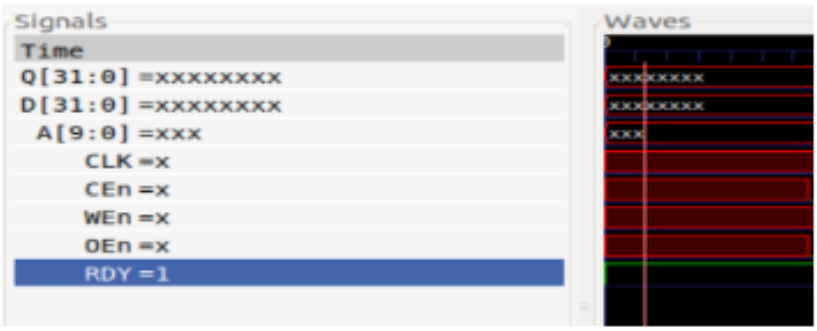
Port Names and preferred metal layers:

Port Name	Function	Preferred Metal	Preferred Pin dimension
output [31:0] Q	RAM data output	Metal 1	at-least 1.26m x 1um
Input [31:0] D	RAM data input bus	Metal 1	at-least 1.26m x 1um
Input [9:0] A	RAM address bus	Metal 1	at-least 1.26m x 1um
Input CLK	RAM clock	Metal 1	at-least 1.26m x 1um
Input CEn	RAM enable	Metal 1	at-least 1.26m x 1um
Input WEn	RAM write enable, 0-active	Metal 1	at-least 1.26m x 1um
Input OEn	RAM output enable, 0-active	Metal 1	at-least 1.26m x 1um
output RDY	Test output	Metal 1	at-least 1.26m x 1um
VDD18M	1.8v supply	Metal 4	4.41um x 1um
VSSM	Ground	Metal 3	4.46um x 1um

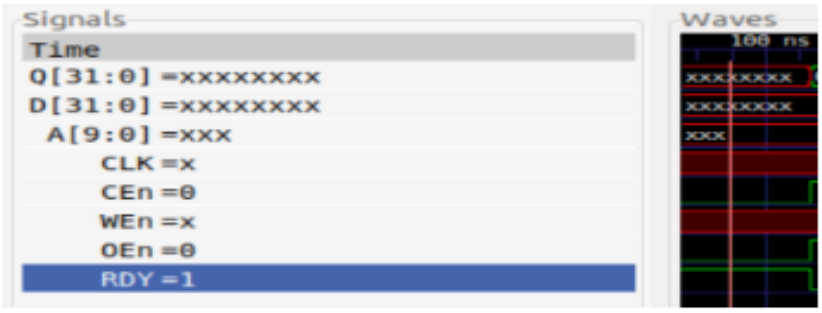
Functionality specs:

Case	CLK	CEn	WEn	OEn	A[10bits]	D[32bits]	Q[32bits]	RDY
1	x	x	x	x	x	x	x	Tie high
2	x	0	x	0	x	x	x	Tie high
3	x	0->1	x	0->1	x	x	0000_0000	0
4	0->1	1	1	1	x	x	0000_0000	0
5	0->1	0	1	0	x	x	Q<- mem[A] (read)	1
6	0->1	0	0	0	x	mem[A]<- D (write)	Q<- mem[A] (read)	1

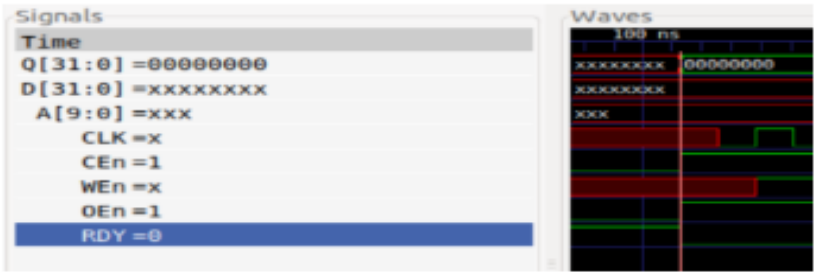
Case 1:



Case 2:

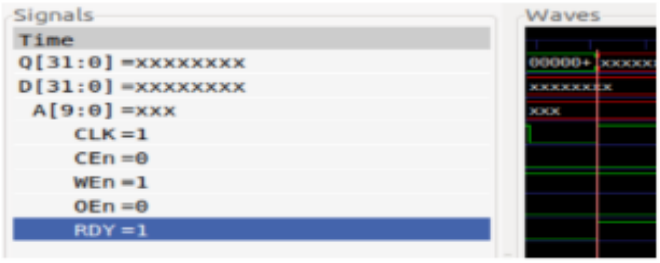


Case 3:

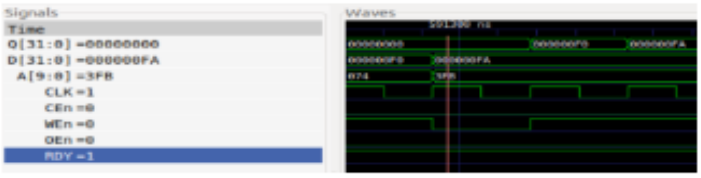


Case 4:

Case 5:



Case 6:



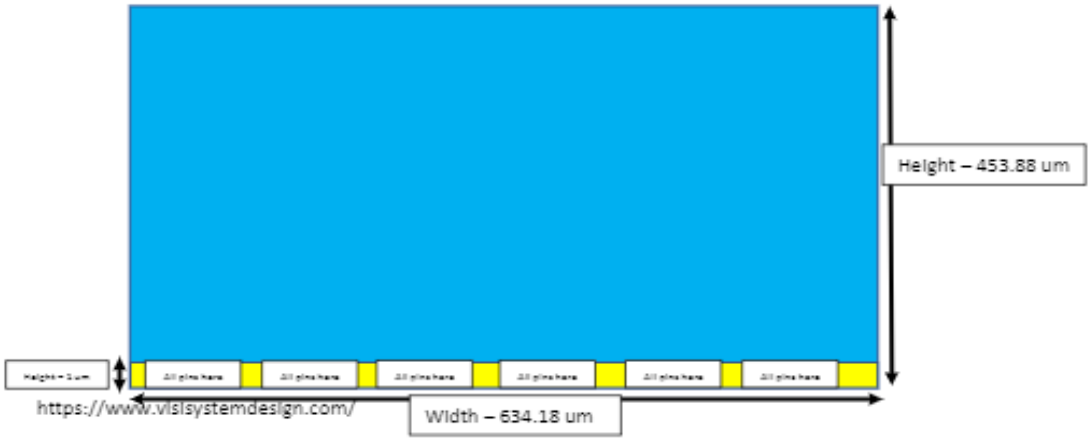
Full behavioral model in verilog:

https://github.com/efabless/raven-picorv32/blob/master/verilog/X5PRAM_1024X32_M8P.v

Layout specs:

Width – 634.18 um

Height – 453.88 um



https://www.vlsisystemdesign.com/