Homework 3

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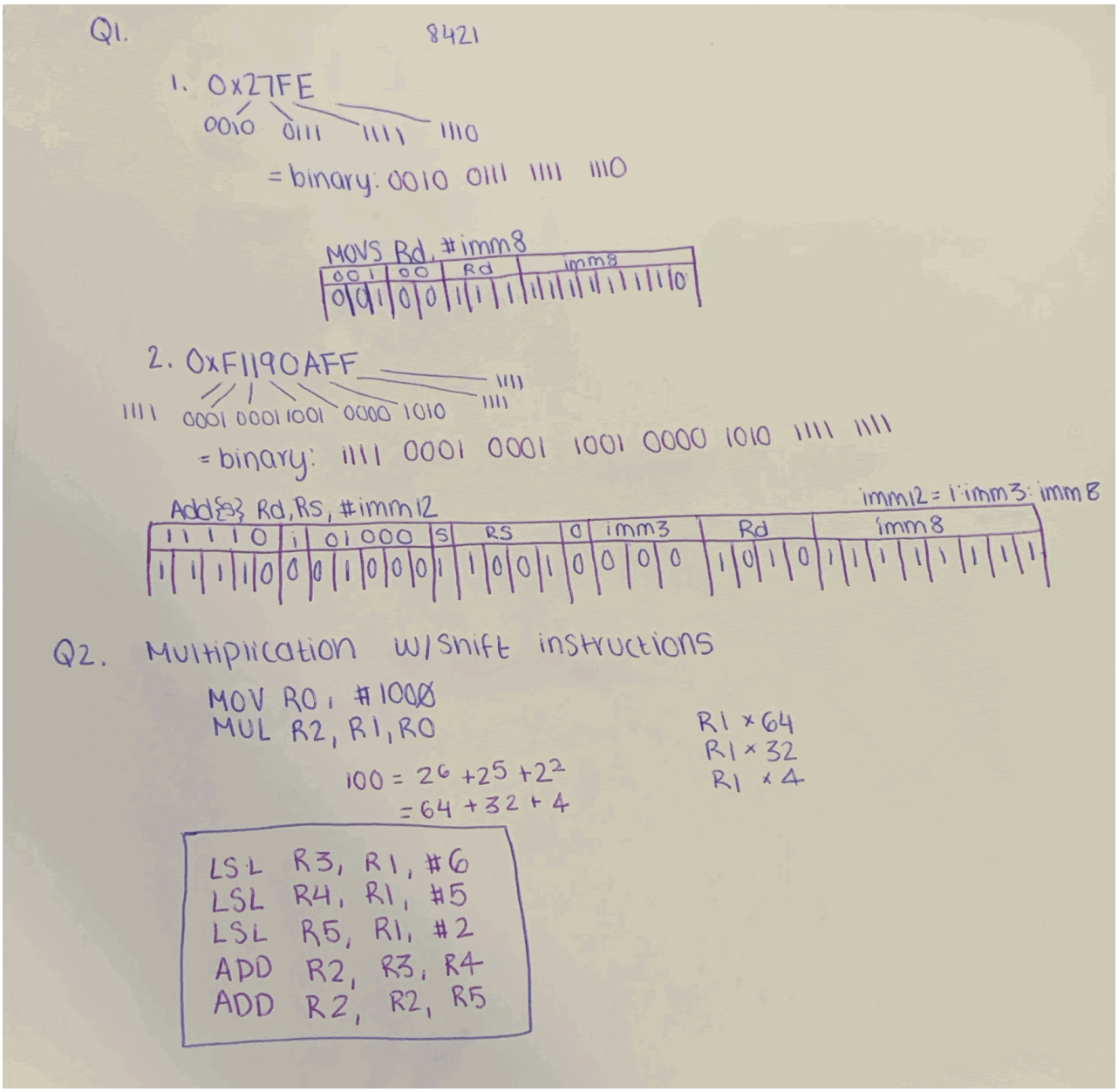


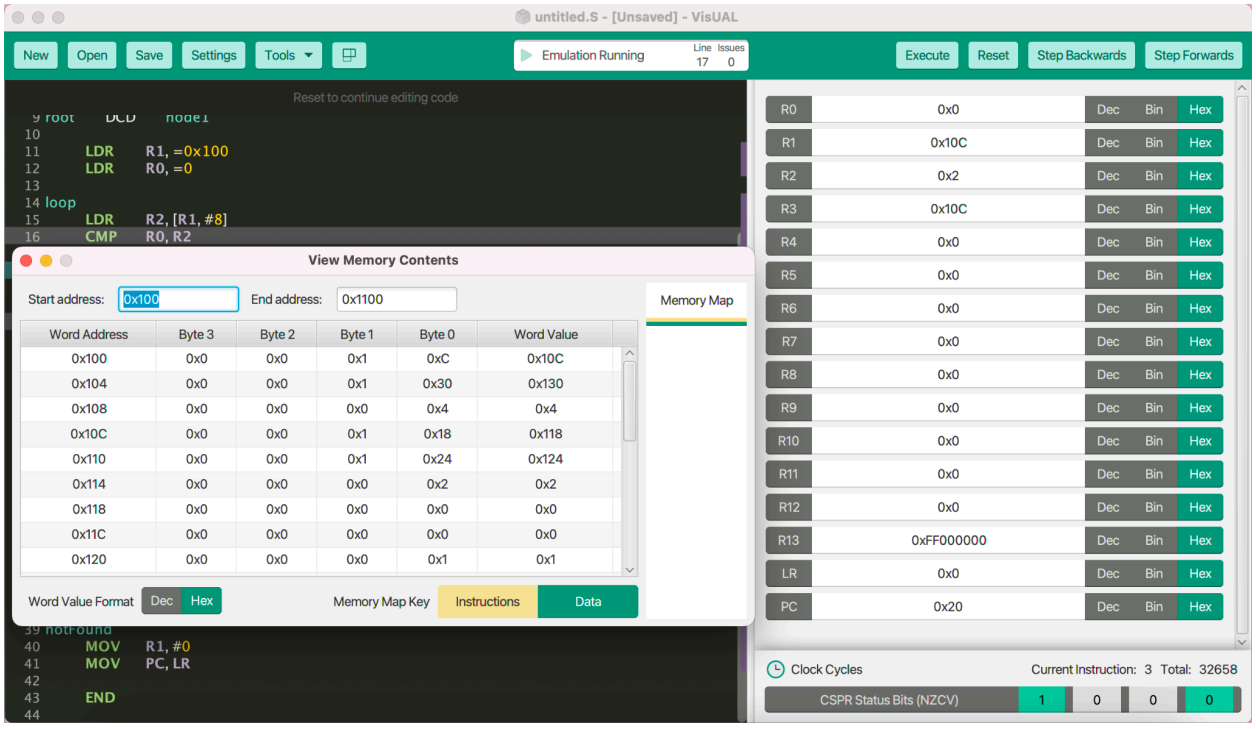
Q3.

Address	Contents
0x60000000	DRAM
0x40000000	Peripherals
0x20000008	SRAM
0x20000000	STACK
	…
	R3, [R0], #1
0x00000014	R2, =dst
0x00000012	R1, =src1
0x00000010	R0, =src0
0x0000000C	String "SSC" <- (explanation:CSS)
0x00000008	String "BWU" <- (explanation:UWB)
0x00000004	00000011
0x00000000	20000108

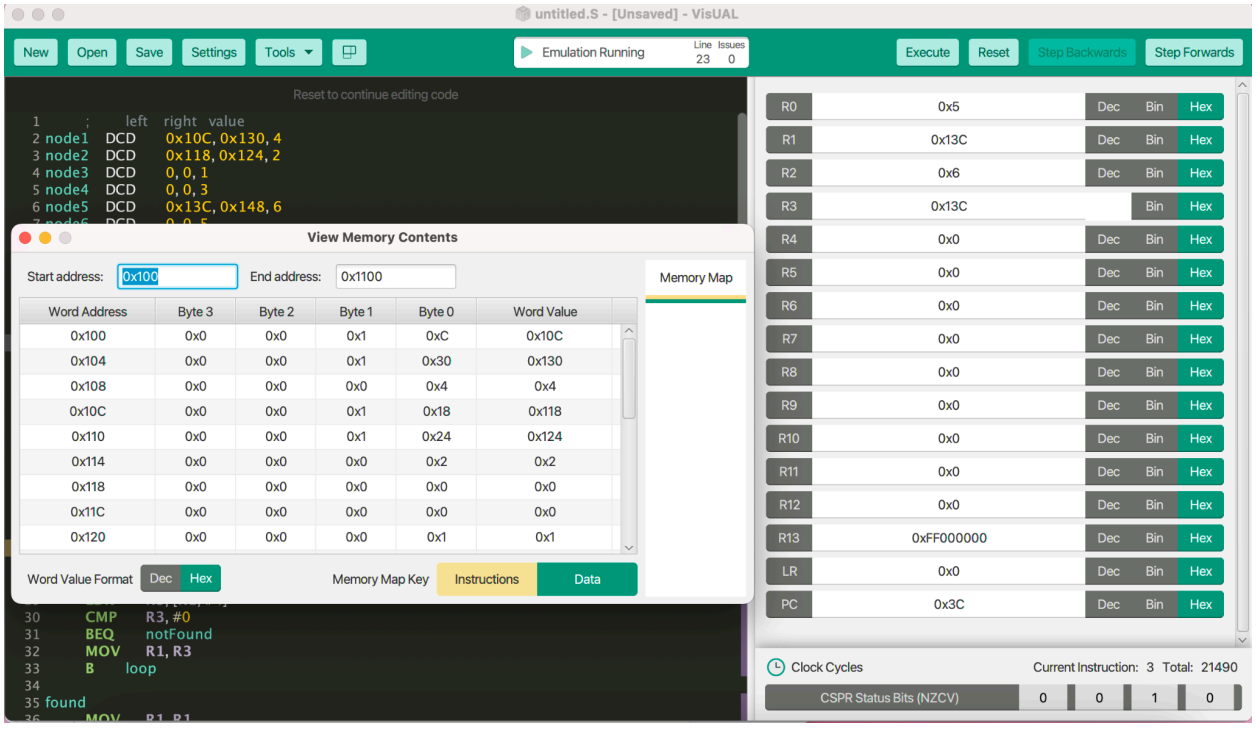
Q4. Source Code + Screen Shots:

```
          ; left    right   value
node1   DCD     0x10C, 0x130, 4
node2   DCD     0x118, 0x124, 2
node3   DCD     0, 0, 1
node4   DCD     0, 0, 3
node5   DCD     0x13C, 0x148, 6
node6   DCD     0, 0, 5
node7   DCD     0, 0, 7
root    DCD     node1

        LDR     R1, =0x100
        LDR     R0, =0

loop
        LDR     R2, [R1, #8]
        CMP     R0, R2
        BEQ     found
        BLT     goLeft
        BGT     goRight

goLeft
        LDR     R3, [R1]
        CMP     R3, #0
        BEQ     notFound
        MOV     R1, R3
        B       loop

goRight
        LDR     R3, [R1, #4]
        CMP     R3, #0
        BEQ     notFound
        MOV     R1, R3
        B       loop

found
        MOV     R1, R1
        MOV     PC, LR

notFound
        MOV     R1, #0
        MOV     PC, LR

        END
```

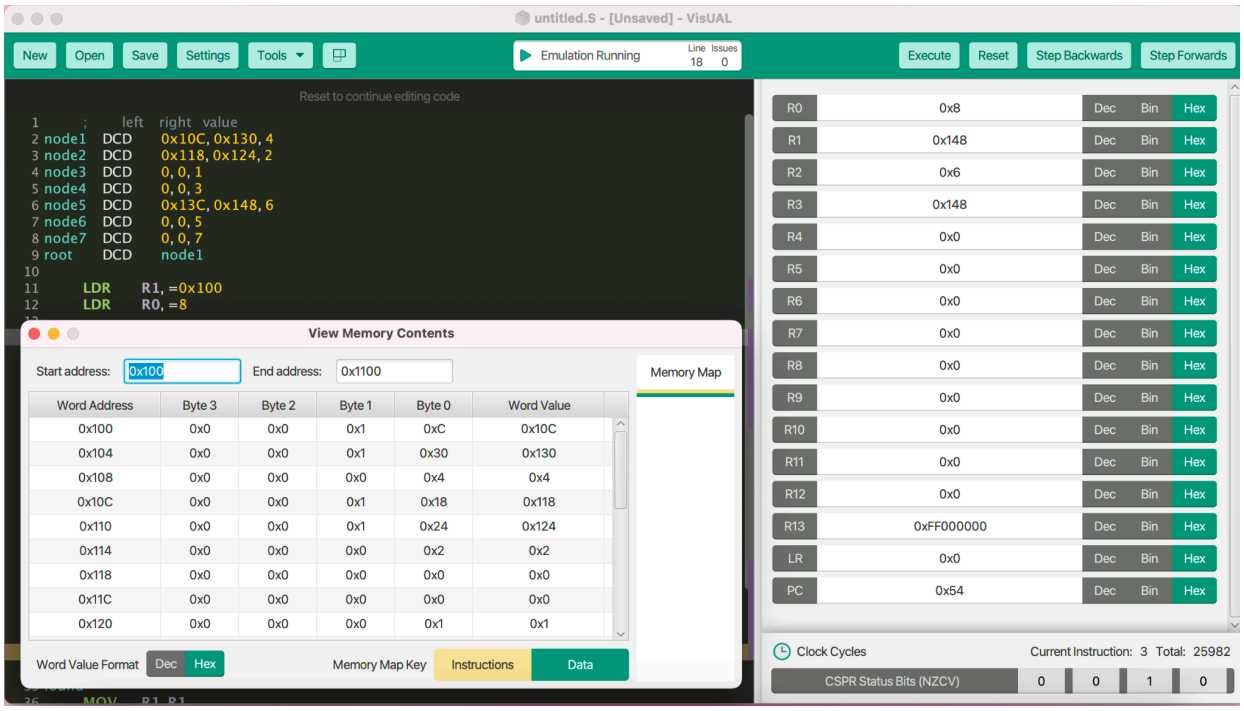
Test Case 1 :



Test Case 2



Test Case 3


untitled.S - [Unsaved] - VisUAL
New
Open
Save
Settings
Tools
Emulation Running
Line 18
Issues 0
Execute
Reset
Step Backwards
Step Forwards
Reset to continue editing code
; left right value
node1 DCD 0x10C, 0x130, 4
node2 DCD 0x118, 0x124, 2
node3 DCD 0, 0, 1
node4 DCD 0, 0, 3
node5 DCD 0x13C, 0x148, 6
node6 DCD 0, 0, 5
node7 DCD 0, 0, 7
root DCD node1
LDR R1, =0x100
LDR R0, =8
View Memory Contents
Start address: 0x100
End address: 0x1100
Memory Map
Word Address | Byte 3 | Byte 2 | Byte 1 | Byte 0 | Word Value
0x100 | 0x0 | 0x0 | 0x1 | 0xC | 0x10C
0x104 | 0x0 | 0x0 | 0x1 | 0x30 | 0x130
0x108 | 0x0 | 0x0 | 0x0 | 0x4 | 0x4
0x10C | 0x0 | 0x0 | 0x1 | 0x18 | 0x118
0x110 | 0x0 | 0x0 | 0x1 | 0x24 | 0x124
0x114 | 0x0 | 0x0 | 0x0 | 0x2 | 0x2
0x118 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0
0x11C | 0x0 | 0x0 | 0x0 | 0x0 | 0x0
0x120 | 0x0 | 0x0 | 0x0 | 0x1 | 0x1
Word Value Format Dec Hex
Memory Map Key Instructions Data
R0 0x8 Dec Bin Hex
R1 0x148 Dec Bin Hex
R2 0x6 Dec Bin Hex
R3 0x148 Dec Bin Hex
R4 0x0 Dec Bin Hex
R5 0x0 Dec Bin Hex
R6 0x0 Dec Bin Hex
R7 0x0 Dec Bin Hex
R8 0x0 Dec Bin Hex
R9 0x0 Dec Bin Hex
R10 0x0 Dec Bin Hex
R11 0x0 Dec Bin Hex
R12 0x0 Dec Bin Hex
R13 0xFF000000 Dec Bin Hex
LR 0x0 Dec Bin Hex
PC 0x54 Dec Bin Hex
Clock Cycles
Current Instruction: 3 Total: 25982
CSPR Status Bits (NZCV) 0 0 1 0