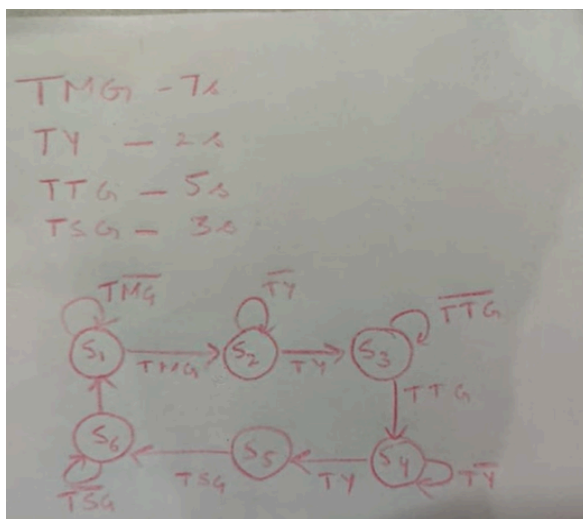
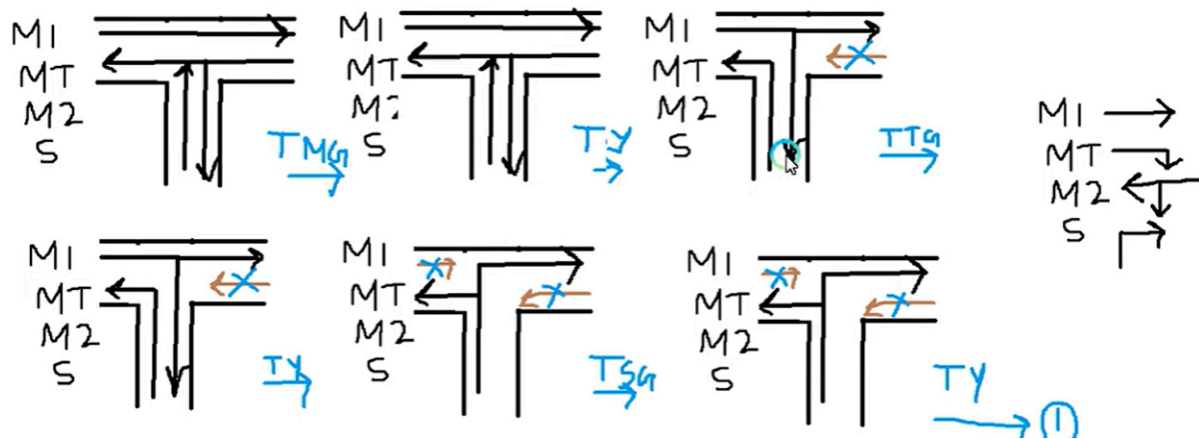


# Traffic Light Controller



State Table

Present state ABC	Input	NS A+B+C	ST	M1 R1G	M2 R2G	T R1Y	S R2Y
000	-	001	2	000	000	000	000
001	TMG	001	0	001	001	100	100
001	TMG	010	1				
010	TY	010	0	001	010	100	100
010	TY	011	1				
011	TTG	011	0	001	100	001	100
011	TTG	100	1				
100	TSG	100	0	010	100	010	100
100	TSG	101	1				
101	TSG	110	1				
110	TY	110	0	100	100	100	010
110	TY	001	1				
111	-	000	0	000	000	000	000

The traffic light controller is designed as a Moore finite state machine with six states representing different traffic phases. Each state activates a specific set of lights while others remain red. A counter is used to maintain each state for a predefined duration. After the timer expires, the FSM transitions to the next state in a cyclic manner. The reset initializes the system to the main road green state, ensuring safe and predictable traffic flow.

## Stage S0 – Main Road Green (TMG)

In this stage, the main straight roads **M1 and M2 are given green signals**, allowing vehicles to move straight through the junction. The main turn road (MT) and side road (S) remain red to avoid conflicts. This stage ensures smooth flow on the primary road and lasts for **7 seconds**.

**Stage S1 – Main Road Yellow (TY):** This stage acts as a transition phase for the main road. **M1 and M2 show yellow signals**, warning drivers that the green phase is about to end. All other roads remain red. The duration of this stage is **2 seconds**, allowing vehicles already in motion to slow down safely.

**Stage S2 – Main Turn Green (TTG):** In this stage, the **main turn road (MT) is given a green signal** to allow turning vehicles to pass safely. All straight roads (M1 and M2) and the side road (S) remain red. This prevents collision between turning and straight-moving traffic. This stage lasts for **5 seconds**.

**Stage S3 – Main Turn Yellow (TY):** This is the warning phase for the main turn road. **MT shows a yellow signal**, indicating the end of the turning green phase. All other directions stay red. The stage duration is **2 seconds**, ensuring a safe transition before switching to the next traffic flow.

**Stage S4 – Side Road Green (TSG):** In this stage, the **side road (S) is allowed to move with a green signal**, while all main roads (M1, M2, and MT) remain red. This stage gives priority to side-road traffic and lasts for **3 seconds**.

**Stage S5 – Side Road Yellow (TY):** This stage is the transition phase for the side road. The **side road signal turns yellow**, warning drivers that the green phase is ending. All other roads remain red. This stage lasts for **2 seconds**, after which the controller returns to the main road green stage.

## OUTPUT :

```
PS C:\verilog> iverilog -o trafficlight trafficlight.v trafficlight_tb.v
PS C:\verilog> vvp trafficlight
VCD info: dumpfile trafficlight_tb.vcd opened for output.
Time = 0: m1 = xxx, m2 = xxx, mt = xxx, s = xxx
Time = 5000: m1 = 000, m2 = 000, mt = 000, s = 000
Time = 15000: m1 = 001, m2 = 001, mt = 100, s = 100
Time = 105000: m1 = 001, m2 = 010, mt = 100, s = 100
Time = 135000: m1 = 001, m2 = 100, mt = 001, s = 100
Time = 195000: m1 = 010, m2 = 100, mt = 010, s = 100
Time = 225000: m1 = 100, m2 = 100, mt = 100, s = 001
Time = 265000: m1 = 100, m2 = 100, mt = 100, s = 010
Time = 295000: m1 = 001, m2 = 001, mt = 100, s = 100
Time = 375000: m1 = 001, m2 = 010, mt = 100, s = 100
Time = 405000: m1 = 001, m2 = 100, mt = 001, s = 100
Time = 465000: m1 = 010, m2 = 100, mt = 010, s = 100
Time = 495000: m1 = 100, m2 = 100, mt = 100, s = 001
Time = 535000: m1 = 100, m2 = 100, mt = 100, s = 010
Time = 565000: m1 = 001, m2 = 001, mt = 100, s = 100
Time = 645000: m1 = 001, m2 = 010, mt = 100, s = 100
Time = 675000: m1 = 001, m2 = 100, mt = 001, s = 100
Time = 735000: m1 = 010, m2 = 100, mt = 010, s = 100
Time = 765000: m1 = 100, m2 = 100, mt = 100, s = 001
Time = 805000: m1 = 100, m2 = 100, mt = 100, s = 010
Time = 835000: m1 = 001, m2 = 001, mt = 100, s = 100
Time = 915000: m1 = 001, m2 = 010, mt = 100, s = 100
Time = 945000: m1 = 001, m2 = 100, mt = 001, s = 100
Time = 1005000: m1 = 010, m2 = 100, mt = 010, s = 100
Time = 1035000: m1 = 100, m2 = 100, mt = 100, s = 001
Time = 1075000: m1 = 100, m2 = 100, mt = 100, s = 010
Time = 1105000: m1 = 001, m2 = 001, mt = 100, s = 100
Time = 1185000: m1 = 001, m2 = 010, mt = 100, s = 100
Time = 1215000: m1 = 001, m2 = 100, mt = 001, s = 100
Time = 1275000: m1 = 010, m2 = 100, mt = 010, s = 100
Time = 1305000: m1 = 100, m2 = 100, mt = 100, s = 001
Time = 1345000: m1 = 100, m2 = 100, mt = 100, s = 010
Time = 1375000: m1 = 001, m2 = 001, mt = 100, s = 100
Time = 1455000: m1 = 001, m2 = 010, mt = 100, s = 100
Time = 1485000: m1 = 001, m2 = 100, mt = 001, s = 100
```

