

TASK 4 : Functional Simulation of RISC-V Core

Objective: Perform a functional simulation of the given RISC-V Core Verilog netlist and testbench.

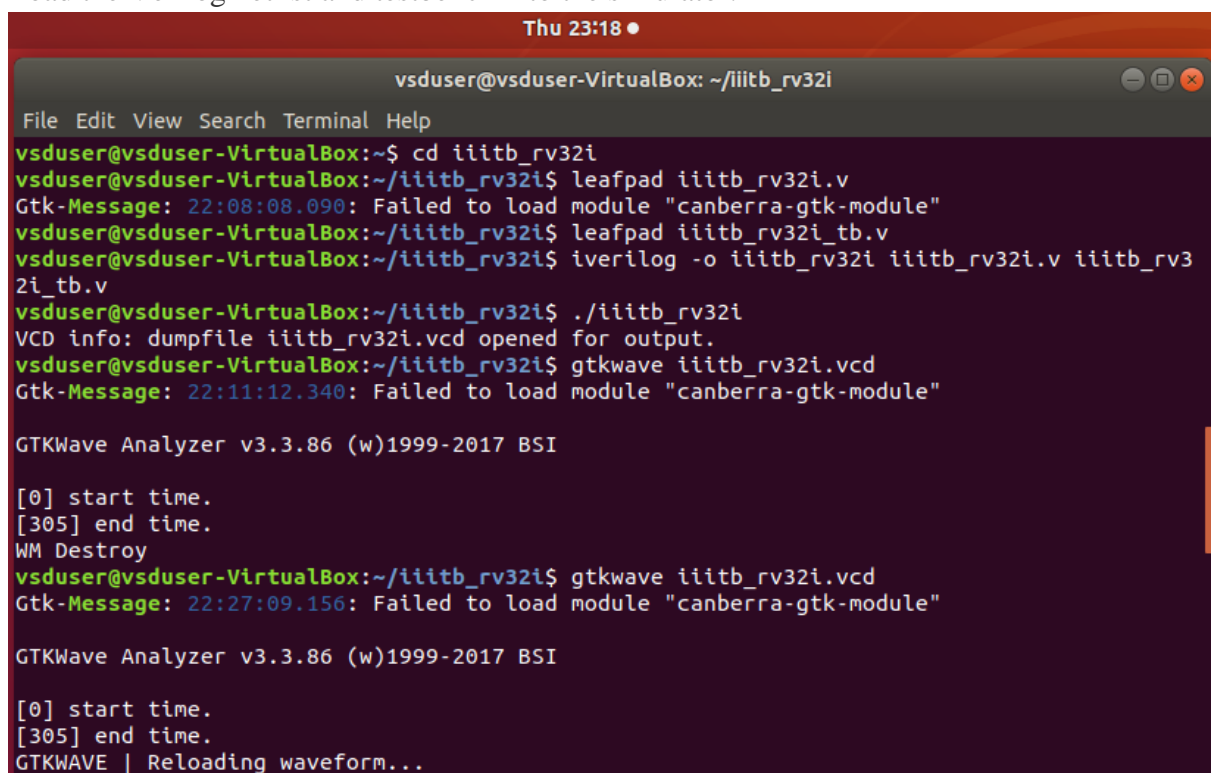
Steps:

1. Download Files:

- Get the Verilog netlist from RISC-V Core Verilog Netlist.
- Get the testbench from *Testbench for RISC-V Core*

2.. Set Up Simulation Environment:

- Ensure you have a suitable simulation tool (e.g., iverilog, gtkwave).
- Load the Verilog netlist and testbench into the simulator.



```
Thu 23:18 •
vsduser@vsduser-VirtualBox: ~/iiitb_rv32i
File Edit View Search Terminal Help
vsduser@vsduser-VirtualBox:~$ cd iiitb_rv32i
vsduser@vsduser-VirtualBox:~/iiitb_rv32i$ leafpad iiitb_rv32i.v
Gtk-Message: 22:08:08.090: Failed to load module "canberra-gtk-module"
vsduser@vsduser-VirtualBox:~/iiitb_rv32i$ leafpad iiitb_rv32i_tb.v
vsduser@vsduser-VirtualBox:~/iiitb_rv32i$ iverilog -o iiitb_rv32i iiitb_rv32i.v iiitb_rv32i_tb.v
vsduser@vsduser-VirtualBox:~/iiitb_rv32i$ ./iiitb_rv32i
VCD info: dumpfile iiitb_rv32i.vcd opened for output.
vsduser@vsduser-VirtualBox:~/iiitb_rv32i$ gtkwave iiitb_rv32i.vcd
Gtk-Message: 22:11:12.340: Failed to load module "canberra-gtk-module"

GTKWave Analyzer v3.3.86 (w)1999-2017 BSI

[0] start time.
[305] end time.
WM Destroy
vsduser@vsduser-VirtualBox:~/iiitb_rv32i$ gtkwave iiitb_rv32i.vcd
Gtk-Message: 22:27:09.156: Failed to load module "canberra-gtk-module"

GTKWave Analyzer v3.3.86 (w)1999-2017 BSI

[0] start time.
[305] end time.
GTKWAVE | Reloading waveform...
```

3. Creating files:

- Under the same directory create 2 files and uploading it with verilog netlist. We can create files ny using leafpad.

4. Run Functional Simulation:

- Simulate the design using the testbench.
- Check the functional correctness of the core by observing the output signals.

5.Capture Waveforms:

- Generate and save waveform snapshots for the executed commands during the simulation.

