TASK 4 : Functional Simulation of RISC-V Core

Objective: Perform a functional simulation of the given RISC-V Core Verilog netlist and testbench.

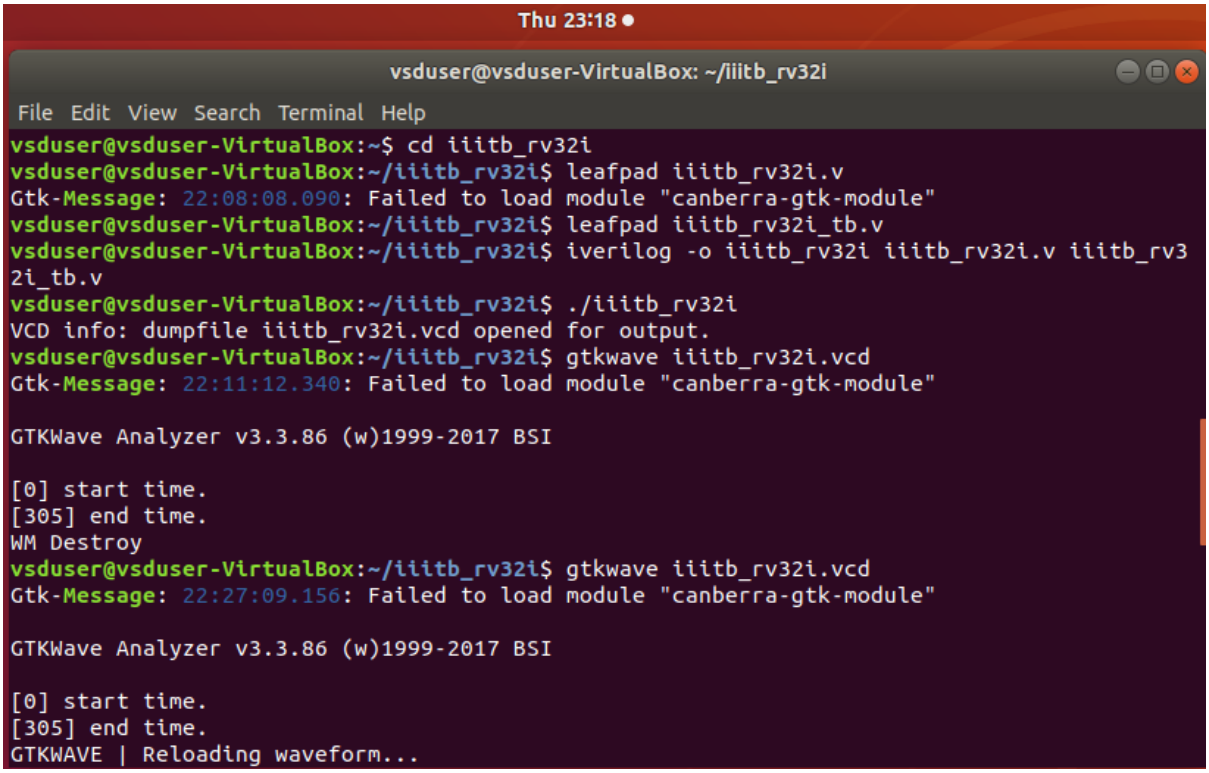
Steps:

1. Download Files:

- Get the Verilog netlist from RISC-V Core Verilog Netlist.
- Get the testbench from *Testbench for RISC-V Core*

2.. **Set Up Simulation Environment:**

- Ensure you have a suitable simulation tool (e.g., iverilog, gtkwave).
- Load the Verilog netlist and testbench into the simulator.



3. Creating files:

- *Under the same directory create 2 files and uploading it with verilog netlist.*
  We can create files ny using leafpad.

4. Run Functional Simulation:

- Simulate the design using the testbench.
- Check the functional correctness of the core by observing the output signals.

5.Capture Waveforms:

- Generate and save waveform snapshots for the executed commands during the simulation.