

Concept of Electrical Measurement :- The electrical and electronics measurement of materials are among the most powerful technique available for material characterization. These measurement can reveal information that completely characterizes the electrical transport properties of materials.

These are the methods devices and calculations used to measure electrical quantities. Conductivity measurement gives the information on conductivity (resistivity) of materials and indirectly the mobility of charge carriers. Resistivity is one of the most sensitive measure of electrical transport of materials.

In case of semiconductor, we can find the same parameters with some different values as compared to metals. Fermi level can be calculated with the help of e^- and holes concentration. Likewise Hall-effect is the most versatile technique to calculate the resistivity, mobility and carrier density of semiconductor materials.

Significance of resistivity

Resistivity or electrical resistivity is an intrinsic property which quantifies how strongly a given material opposes the flow of electrical current, that can be measured by several methods depending on magnitude of resistance involved in materials.

According to Ohm's law, we have

$$V = IR \quad R \text{ in ohm.}$$

& the constant of proportionality R , is called the resistance of the material.

Resistivity → At a given constant temperature, ~~resistance~~ resistance R of the conductor is proportional to length (L) and inversely proportional to its area of cross-section (A) ie

$$\rho = \frac{RA}{L} \quad \text{or} \quad R \propto \frac{L}{A} \quad (R = \rho \frac{L}{A})$$

It is defined as the resistance offered by a wire of material of unit length and unit cross-sectional area. Unit - ohm-meter.

It is the key to measure electrical resistance. It helps to compare the conductivity of various materials, depending on its length, area of cross-section and temperature of the conductor.

→ Significance of Hall mobility: \Rightarrow Mobility inferred from the Hall Effect measurement. (2)

It is the measure of the mobility of the e- and holes in a semiconductor. It is the product of conductivity and hall constant for a conductor or a semiconductor.

Equationally:-

$$N\text{-type} = \tau_n = n e M_e \quad \text{or} \quad M_e = \frac{\tau_n}{n e} = -\tau_n \cdot R_H$$

$$P\text{-type} = M_p = \frac{\tau_p}{p e} = \tau_p \cdot R_H \quad \text{So, by measuring } \tau \text{ & } R_H, M \text{ can be calculated.}$$

This is very important parameter for semiconductor materials. Higher mobility leads to better device performance, with other things equal.

Depending on drift velocity $v_d = M E$

where v_d = drift velocity, E = Electric field
& M = carrier mobility (Hall mobility)

With the help of this, we can find

(i) Whether the conductivity is due to holes or e^-

(ii) to determine magnetic flux density.

(iii) To determine Hall voltage, Hall current, Hall coefficient & Hall angle etc.

→ Significance of carrier density ⇒ Also called as carrier concentration denoting the no. of charge carrier per volume.

$$N = \frac{\text{No. of charge carriers}}{\text{over a volume } V} = \int_V n(r) dV,$$

where $n(r) = \text{position-dependent charge carrier density.}$

This is important for semiconductors, for the process of chemical doping.

$$\text{for N-type} - n_e = 2 \left(\frac{2\pi m_e^* kT}{h^2} \right)^{3/2} \exp \left(\frac{E_F - E_C}{kT} \right) \quad \textcircled{1}$$

$$\text{for P-type} - p_e = 2 \left(\frac{2\pi m_h^* kT}{h^2} \right)^{3/2} \exp \left(\frac{E_V - E_F}{kT} \right) \quad \textcircled{2}$$

It is helpful to find the Hall coefficient, location of Fermi level (either for n or for p-type), even in intrinsic semiconductor also, we can get the location of Fermi level and conductivity of intrinsic semiconductors.

In case of metals, we have the free electrons as the carrier density calculated from the Drude model. We can infer conductivity of metals, current density

Semiconductors \Rightarrow

Hall Coeff. $R_H = -\frac{1}{ne}$ or $\frac{1}{p_e}$ (N & p-type respectively)

Fermi level

Intrinsic Semiconductor - $E_F = \frac{E_C + E_V}{2}$

N-type - $E_C - kT \ln \frac{N_c}{N_d}$

P-type - ~~$E_V + kT \ln \frac{N_v}{N_a}$~~

TWO-POINT PROBE TECHNIQUE-

This is one of the standard and most commonly used method for the resistivity measurement of very high resistivity samples - near insulators. The conductivity or resistivity of a bulk-sample is based on accurate measurement of both resistance and the sample dimensions. Let us consider a long thin wire of length L , and uniform cross-section A , or the materials with long parallelopiped shaped with uniform cross-section as shown in fig below.

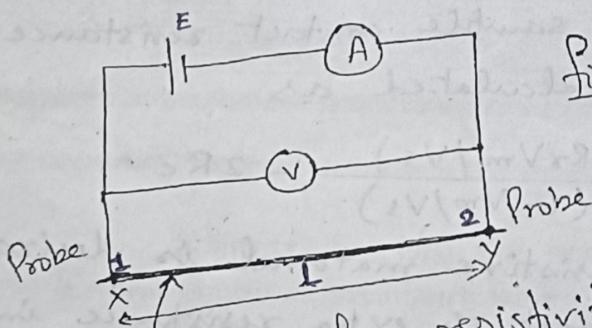


Fig:- Schematic of two-probe setup

Specimen whose resistivity is to be measured.

Resistivity can be measured by measuring voltage drop across the wire due to passage of known current supplied by the battery E through the probes 1 and 2.

Voltmeter - measures the potential difference between two contacts at the wire ends, then the resistance $R = \frac{V}{I}$ is related to resistivity (ρ)

$$\boxed{\rho = \left(\frac{V}{I}\right) \left(\frac{A}{L}\right)}$$

Two probe method is a simple and advantages method for measuring resistance above 1Ω directly.

$$(R = \frac{\rho L}{A})$$

A more realistic view of a two point measurement using an ohmmeter is shown in fig.(2). A voltage source and a variable range of resistor (R_r) supply the current, where (R_r) is adjustable to provide a conventional voltage across the voltmeter.

Typical values of R_r range from 100 to 10000 Ω . R_c represents series resistance in the cable and the wire to sample contact resistance. The resistance in the bar is calculated as

$$R = \frac{(R_r V_m / V_s)}{(1 - V_m / V_s)} - 2 R_c$$

A long bar of resistance material is desirable to minimize the effect of extra resistance in the measurement system or inaccurate length measurement.

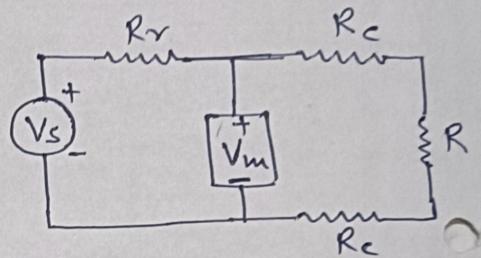


Fig-(2), Two-point ohmmeter measurement circuit.

Problems: Two probe method suffers few issues as stated below -

- (i) Error due to contact resistance of the measuring leads
- (ii) Materials having random shapes,
- (iii) Soldering of the test leads on some materials could be difficult.
- (iv) Heating of the ~~test~~ leads, during soldering may inject additional impurities in materials
→ Eliminated by pressure contacts.

CONCEPT OF PHOTOLUMINESCENCE

Luminescence → When crystalline solid absorbs energy & re-emits it in the visible region of the spectrum. It is a two process - (i) excitation of e⁻ from a lower energy state to higher energy state (ii) Emission of light radiation when e⁻ fall back to lower energy state.

When the luminescence is produced by the bombardment of photons of electromagnetic radiation lying in the range from IR to X-rays — Photoluminescence.

Luminescence observation depends on the time interval between excitation and emission.

If emission takes place within 10^{-8} seconds of excitation or if emission takes place as long as excitation is maintained — Fluorescence.

If luminescence continues for some time even after the excitation has been ceased — Phosphorescence / after glow.

Four-Point Probe Method :- A more accurate method to determine the low-resistance of material is provided by the four-point probe measurement.

In the four point probe method we consider the resistance is now considered as a function of length between the voltage probe L , so from the resistance to resistivity relation

$$R = \rho \frac{L}{A}$$

The Four Probe or Kelvin probe measurement is most common way to measure the resistance of semiconductor. Using four-probe eliminate the errors due to probe resistance & the spreading resistance & contact resistance of each probe.

Sample Preparation :- Making an accurate resistance measurement requires good electrical contact to the sample. The minimum spacing between voltage and current contact

1.5 X cross-sectional perimeter of sample

Dr. Mudit Srivastava

FOUR PROBE METHOD \Rightarrow This method is an electrical impedance measuring technique which uses separate pairs of current-carrying and voltage sensing electrodes to make more accurate measurements than the simpler & more usual two-terminal (2T) sensing.

This is also known as 'Kelvin Sensing' Method

Principle: \Rightarrow When current is supplied via a pair of source, it generates a voltage drop across the impedance ^{that} to be measured as per Ohm's law.

Note: \Rightarrow Since almost no current flows to the measuring instrument, the voltage drops seems to be negligible.

TECHNIQUES: \Rightarrow

(i) Four point Collinear-method and (ii) Vander Pauw method.

(I) COLLINEAR METHOD: \Rightarrow Most common way of measuring resistivity of material that involves four equally spaced probes.

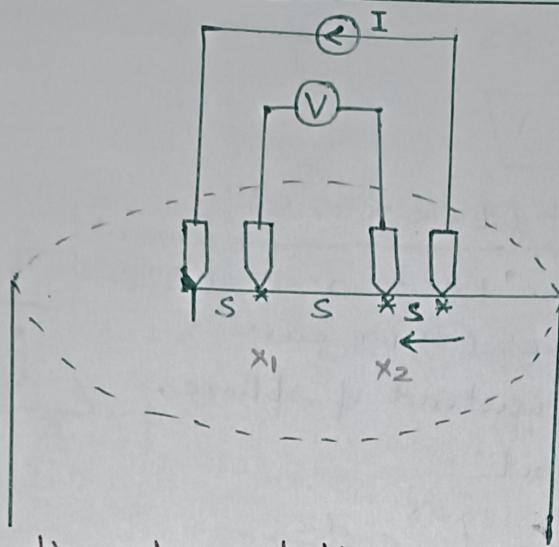


Fig. ⇒ Schematic representation of Four-Point collinear Probe method.

This is applicable for Bulk and thin films.

- ① For Bulk - ($t \gg s$ or x) :- Consider a bulk material with thickness (t) of the material is such higher than the space between probes (s). The differential resistance due to spherical protrusion of current emanating from the outer probe is

$$\Delta R = \rho \left(\frac{dx}{A} \right)$$

$$\text{Area of tip in one probe} = \pi r^2$$

$$\text{Area of tip in 2nd probe} = \pi r^2$$

$$\therefore \pi r^2 + \pi r^2 = 2\pi r^2$$

$$R = \int_{x_1}^{x_2} \rho \frac{dx}{2\pi r^2} = \int_s^{2s} \rho \frac{dx}{2\pi r^2}$$

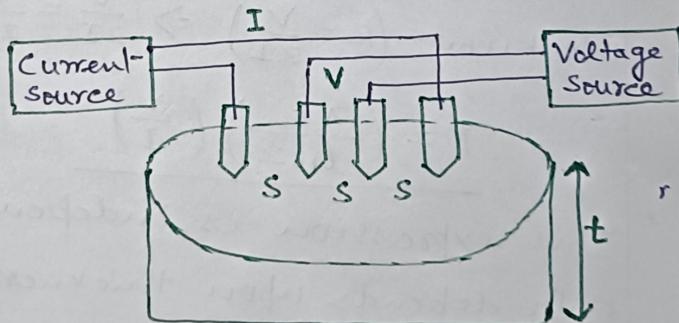
$$R = + \frac{\rho}{2\pi} \left(-\frac{1}{r} \right) \int_s^{2s} \quad [x_1 = s, x_2 = 2s] \quad [\text{Probe Spacing is uniform}]$$

$$R = - \frac{\rho}{2\pi} \left(\frac{1}{2s} - \frac{1}{s} \right) \Rightarrow R = \frac{\rho}{2 \cdot 2\pi s}$$

Due to superposition theorem of current at outer probe of tips

$$R = \frac{V}{2I}, \quad \text{so} \quad \frac{V}{2I} = \frac{\rho}{2\pi} \cdot \frac{1}{2s}$$

$$\Rightarrow \rho \cdot 2I = V \cdot 2\pi \cdot 2s$$



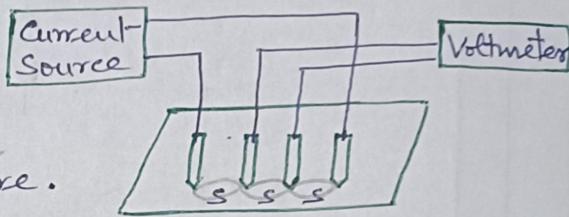
$$\rho = \frac{V}{2I} \cdot 2\pi \cdot \cancel{\rho} s \Rightarrow \frac{V}{I} \cdot 2\pi s$$

$$\boxed{\rho = \frac{V}{I} (2\pi s)}$$

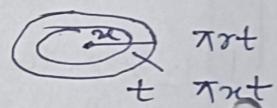
2. For Thin Sheet ($t \ll x$ or s):-

For thin sheet where $t \ll x$ or space between probes (s) we can get current rings instead of sphere.

$$\text{So, Area } A = 2\pi xt$$



$$R = \int_{x_1}^{x_2} \rho \frac{dx}{2\pi xt} = \int_s^{2s} \rho \frac{dx}{2\pi xt}$$



$$R = \frac{\rho}{2\pi t} \ln(x) \Big|_s^{2s}$$

$$R = \frac{\rho}{2\pi t} (\ln 2s - \ln s)$$

$$R = \frac{\rho}{2\pi t} \ln \frac{2s}{s}$$

$$\text{We know } (R = \frac{V}{2I}) \Rightarrow \frac{V}{2I} = \frac{\rho}{2\pi t} \cdot \ln 2$$

$$\underline{\rho = \left(\frac{\pi t}{\ln 2}\right) \left(\frac{V}{I}\right)} \quad (\text{Independent of Probe Spacing})$$

This expression is independent of probe spacing (s). It only depends upon thickness (t) of sample. Here $(\pi/\ln 2)$ is known as correction factor.

VAN-DER PAUL METHOD: In this current and measuring voltage is applied using four small contact on the circumference of a flat, arbitrarily shaped sample of uniform thickness.

$$P_A = \left(\frac{\pi}{\ln 2} \right) f_A t_s \left[\frac{(V_1 - V_2 + V_3 - V_4)}{4I} \right] \quad (1)$$

$$P_B = \left(\frac{\pi}{\ln 2} \right) f_B t_s \left[\frac{(V_5 - V_6 + V_7 - V_8)}{4I} \right] \quad (2)$$

where P_A and P_B are volume resistivity in $\Omega \text{ cm}$.

t_s = sample thickness (cm)

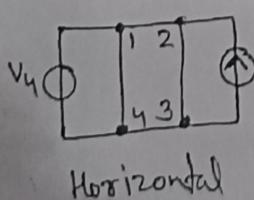
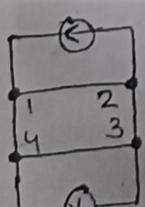
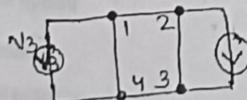
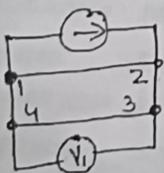
V_1 to V_8 represent voltages measured by the voltmeter under eight geometries respectively.

I is the current through the sample in amperes. For a perfect symmetry system

$$f_A = f_B \approx 1 \quad \text{or} \quad f_A = f_B \approx 1$$

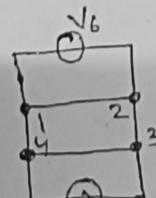
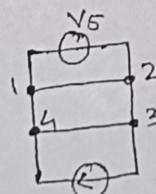
$$\text{Avg. resistivity} = P_{\text{avg}} = \left(\frac{P_A + P_B}{2} \right)$$

Eight geometries are \Rightarrow

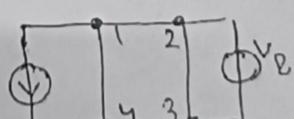
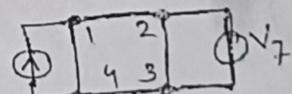


Vertical

Horizontal



Vertical



Horizontal

Hot-Point Probe Method: \Rightarrow Hot point probe is a method of determining quickly whether a semiconductor sample is n-type or p-type. A voltmeter or ammeter is attached to the sample and a heat source such as soldering iron is placed on one of the leads.

According to this method one can measure and calculate the majority charge carrier concentration & its dynamic parameters.

Principle :- A heat region of a wafer has large no. of carriers that will diffuse cooler regions. With the majority carriers diffuse away from hot probe to cold probe. And the voltage meter will show a +ve or -ve reading depending on type of majority carriers of semiconductors.

Heat \downarrow probe creates an increased no. & higher energy carriers which are diffuse from the junction/contact point. This will cause a current/voltage difference

HOT-POINT PROBE METHOD \Rightarrow This is a simple method to determine whether a semiconductor is N or P-type.

Principle \Rightarrow

- Two probes touches the wafer, one is warmer than the other.

\rightarrow Voltmeter reads the potential difference between the probes.

\rightarrow for N-type \rightarrow Warmer probe is more positive than the colder probe.

\rightarrow for P-type - Warmer probe is more negative than the colder probe.

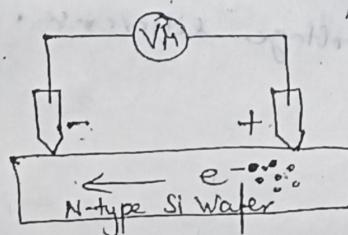
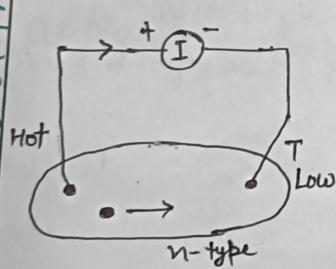
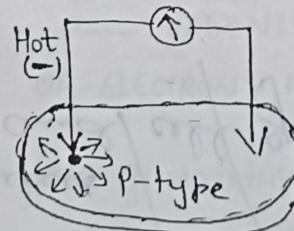
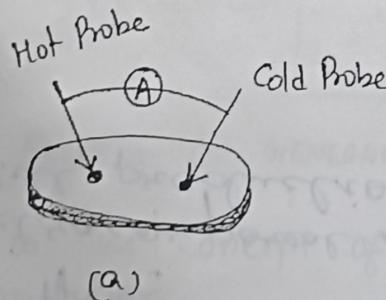
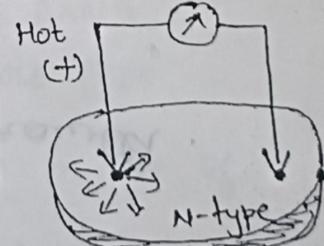


Fig - Basic principle of the hot probe, illustrated for N-type sample, for determining N/P type behavior in semiconductor



Energetic holes
diffuses away



Energetic
electrons
diffuses
away

Note \Rightarrow Net Effect \Rightarrow

(i) Deficient of holes \Rightarrow (net +ve charge for P-type)

(ii) Deficient of e- (~~net -ve~~ charge for n-type)

From this measurement hence, following quantities can be calculated -

- (1) Resistivity of the material.
- (2) Doping type.
- (3) Sheet carrier density of the majority carrier
- (4) Mobility of majority carrier..

Imp. Conditions - (1) Sample must have a flat shape of uniform thickness.

- (2) Sample must not have any isolated holes.
- (3) Sample must be homogeneous & isotropic.
- (4) All four contacts must be located at the edge of the sample.
- (5) Area of contact of any individual contact should be at least an order of magnitude smaller than the area of the entire sample.

The identification and control of defects have always been among the most important and crucial task in material. DLTS probe, the temperature dependence of charge carriers escaping from trapping centers formed by point defects. This technique is able to characterise each type of trapping center by proving activation energy.

Capacitance and Voltage Measurement (C.V. Measurement)

The capacitance-voltage measurement is used to determine the majority carriers concentration in semiconductor as a function of distance (depth) from the junction. The C.V. measurement can quantitatively describe the free carriers concentration together with information about traps. Defect appearing as traps at energies deep within the following gaps of semiconductor can add or remove the free carriers.

Principle of Method : \Rightarrow The capacitance at p-n junction depends upon the properties of the charge-depletion layer formed at the junction. Fig 1(a) shows a abrupt p-n junction and it is depleted of free carriers.

Fig 1(b) shows the electric field distribution in equilibrium condition for charge neutrality. The difference in energy between conduction bands.

Fig 1(c) :- shows that if one carrier crosses the p-n junction it needed a potential called the diffusion potential V_{bi} (built-in potential).

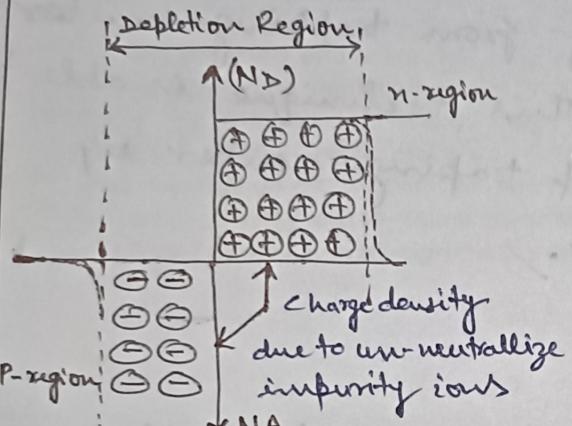


Fig. 1 (a) Charge density

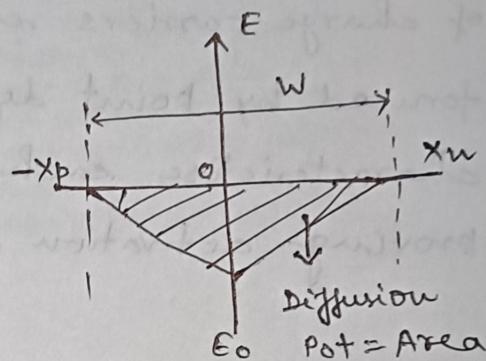


Fig 1 (b) Electric Field distribution

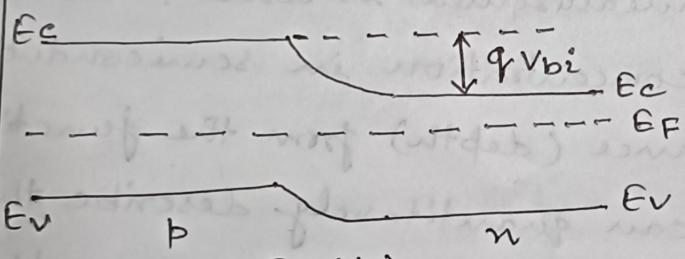


Fig. 1 (c)

To calculate the electric field distribution within the transition region we begin with Poisson's Eqn.

$$\frac{\partial E}{\partial x} = \frac{q}{\epsilon} [P - N + ND^+ - NA^-]$$

For region predominating doped p-type

$$\frac{\partial E}{\partial x} \approx \frac{q}{\epsilon} ND^+ \quad \text{for } 0 < x \leq xn$$

or for region predominately doped n-type

$$\frac{\partial E}{\partial x} \approx \frac{q}{\epsilon} NA^- \quad \text{for } -xp \leq x < 0$$

Capacitance-voltage profiling/ Measurement

Is a technique for characterizing semiconductor materials and devices. The applied voltage is varied, and the capacitance is measured and plotted as a function of voltage. The technique uses a metal-semiconductor junction (Schottky barrier) or a p-n junction or a MOSFET to create a depletion region, a region which is empty of conducting electrons and holes, but may contain ionized donors and electrically active defects or traps. The depletion region with its ionized charges inside behaves like a capacitor. By varying the voltage applied to the junction it is possible to vary the depletion width. The dependence of the depletion width upon the applied voltage provides information on the semiconductor's internal characteristics, such as its doping profile and electrically active defect densities.^{[2], [3]} Measurements may be done at DC, or using both DC and a small-signal AC signal or using a large-signal transient voltage.

C-V characteristics metal-oxide-semiconductor structure

A metal-oxide-semiconductor structure is critical part of a MOSFET by controlling the height of potential barrier in the channel via the gate oxide.

An n-channel MOSFET's operation can be divided into three regions, shown below and corresponding to the right figure

Depletion

When a small voltage is applied to the metal, the valence band edge is driven far from the Fermi level, and holes from the body are driven away from the gate, resulting in a low carrier density, so the capacitance is low.

Inversion

At larger gate bias still, near the semiconductor surface the conduction band edge is brought close to the Fermi level, populating the surface with electrons in an inversion layer or n-channel at the interface between the semiconductor and the oxide. This results in a capacitance increase.

Accumulation

When a negative gate-source voltage (positive source-gate) is applied, it creates a p-channel at the surface of the n region, analogous to the n-channel case, but with opposite polarities of charges and voltages. The increase in hole density corresponds to increase in capacitance.

C-V Characteristics

The low frequency and high frequency C-V characteristics curves of a MOS capacitor are shown in fig1. below,

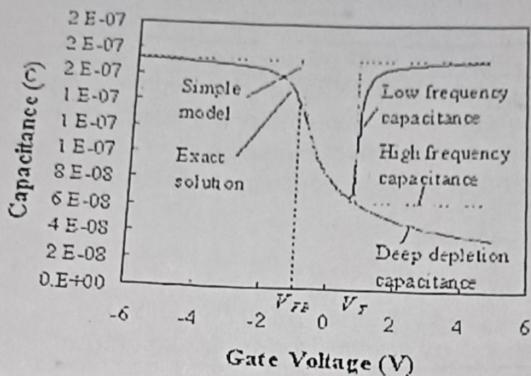


Fig 1 : Low & High Frequency C-V curves

The **low frequency** or quasi-static measurement maintains thermal equilibrium at all times. The capacitance is the ratio of the change in charge to the change in gate voltage, measured when the capacitor is in equilibrium. A typical measurement is performed with an electrometer, which measures the charge added per unit time as one slowly varies the applied gate voltage.

The **high frequency** capacitance is obtained from a small-signal capacitance measurement at high frequency. The bias voltage on the gate is varied slowly to obtain the capacitance versus voltage. Under such conditions, one finds that the charge in the inversion layer does not change from the equilibrium value corresponding to the applied DC voltage. The high frequency capacitance therefore reflects only the charge variation in the depletion layer and the (rather small) movement of the inversion layer charge.

Applications-

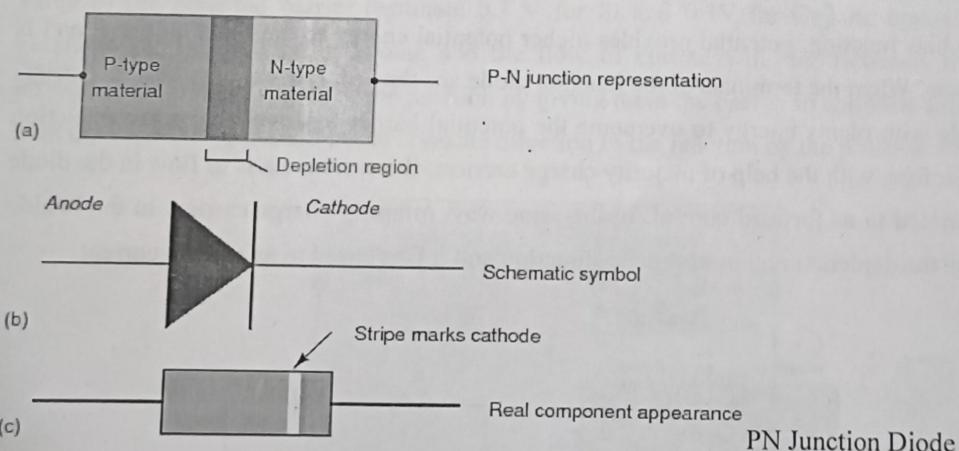
1. used to analyze the doping profiles of semiconductor devices by the obtained C-V graphs.
2. used to characterize threshold voltages and other parameters during reliability and basic device testing and to model device performance.
3. used to characterize other types of semiconductor devices and technologies, including bipolar junction transistors, JFETs, III-V compound devices, photovoltaic cells, MEMS devices, organic thin-film transistor (TFT) displays, photodiodes, and carbon nanotubes (CNTs).

I-V characteristics of a Diode:

A current-voltage characteristic or I-V curve (current-voltage curve) is a relationship, typically represented as a chart or graph, between the electric current through a circuit, device, or material, and the corresponding voltage, or potential difference across it.

There are three possible biasing conditions and two operating regions for the typical PN-Junction Diode, they are: zero bias, forward bias and reverse bias.

When no voltage is applied across the PN junction diode then the electrons will diffuse to P-side and holes will diffuse to N-side through the junction and they combine with each other. Therefore, the acceptor atom close to the P-type and donor atom near to the N-side are left unutilized. An electronic field is generated by these charge carriers. This opposes further diffusion of charge carriers. Thus, no movement of the region is known as depletion region or space charge.

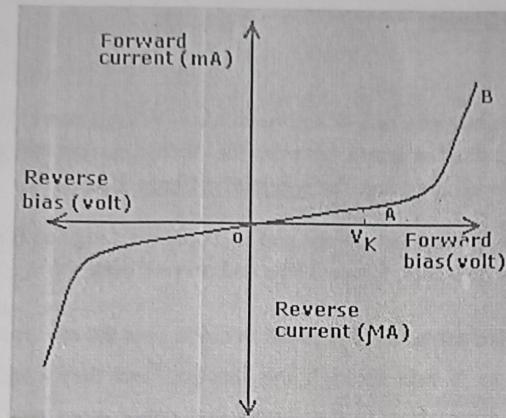


If we apply forward bias to the PN-junction diode, that means negative terminal is connected to the ~~N~~-type material and the positive terminal is connected to the ~~P~~-type material across the diode which has the effect of decreasing the width of the PN junction diode.

If we apply reverse bias to the PN-junction diode, that means positive terminal is connected to the ~~N~~-type material and the negative terminal is connected to the ~~P~~-type material across the diode which has the effect of increasing the width of the PN junction diode and no charge can flow across the junction.

(3)

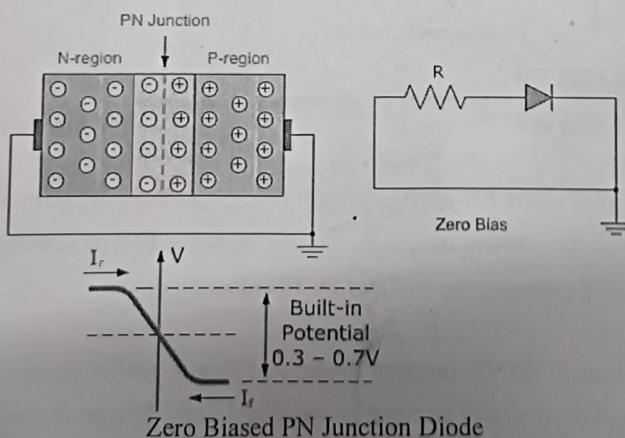
(2)



VI Characteristics of PN Junction Diode

Zero Biased PN Junction Diode

In the zero bias junction, potential provides higher potential energy to the holes on the P and N side terminals. When the terminals of the junction diode are shorted, few majority charge carriers in the P-side with plenty energy to overcome the potential barrier to travel across the depletion region. Therefore, with the help of majority charge carriers, the current starts to flow in the diode and it is denoted to as forward current. In the same way, minority charge carriers in the N-side move across the depletion region in reverse direction and it is referred to as reverse current.



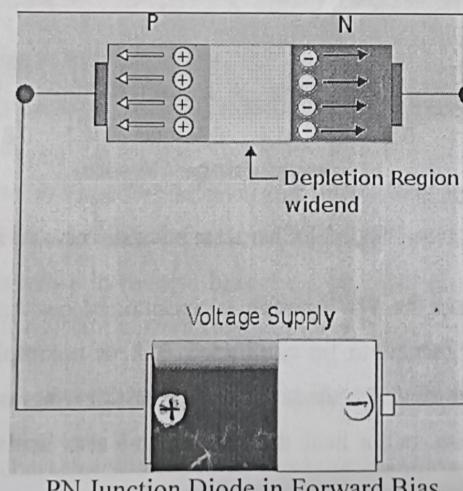
(3)

Potential barrier opposes the movement of electrons & holes across the junction and permits the minority charge carriers to drift across the PN junction. However, the potential barrier helps minority charge carriers in P-type and N-type to drift across the PN-junction, then an equilibrium will be established when the majority charge carriers are equal and both moving in reverse directions, so that the net result is zero current flowing in the circuit. This junction is said to be in a state of dynamic equilibrium.

When the temperature of the semiconductor is increased, minority charge carriers have been endlessly generated and thus leakage current starts to rise. But, electric current cannot flow since no external source has been connected to the PN-junction.

PN Junction Diode in Forward Bias

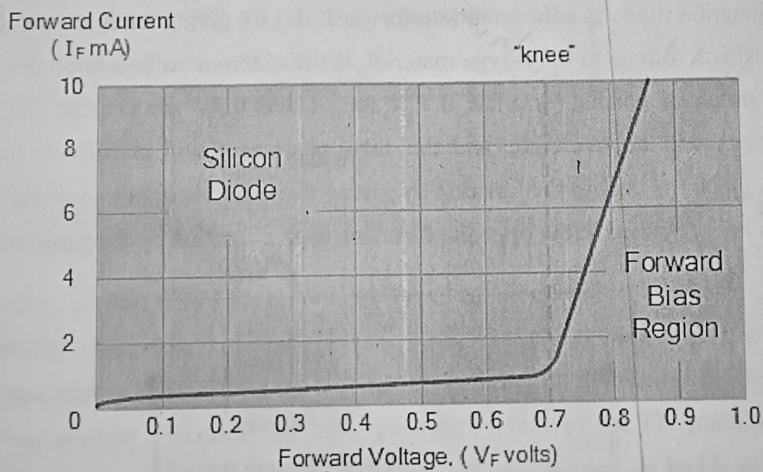
When a PN-junction diode is connected in a forward bias by giving a negative voltage to the N-type and a positive voltage to the P-type material. If the external voltage becomes more than the value of the potential barrier (estimate 0.7 V for Si and 0.3V for Ge), the opposition of the potential barriers will be overcome and the flow of current will start. Because, the negative voltage repels electrons near to the junction by giving them the energy to combine and cross over with the holes being pushed in the opposite direction to the junction by the positive voltage.



The result of this in a characteristic curve of zero current flowing up to built in potential is called as "knee current" on the static curves & then a high current flow through the diode with a slight increase in the external voltage as shown below.

VI Characteristics of PN Junction Diode in Forward Bias

The VI characteristics of PN junction diode in forward bias are non linear, that is, not a straight line. This nonlinear characteristic illustrates that during the operation of the PN junction, the resistance is not constant. The slope of the PN junction diode in forward bias shows the resistance is very low. When forward bias is applied to the diode then it causes a low impedance path and permits to conduct a large amount of current which is known as infinite current. This current starts to flow above the knee point with a small amount of external potential.



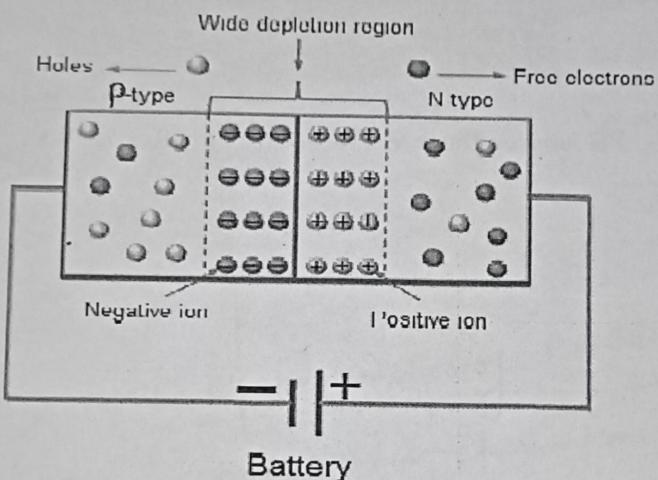
PN Junction Diode VI Characteristics in Forward Bias

The potential difference across the PN junction is maintained constant by the depletion layer action. The max amount of current to be conducted is kept incomplete by the load resistor, because when the PN junction diode conducts more current than the normal specifications of the diode, the extra current results in the heat dissipation and also leads to serve damage to the device.

PN Junction Diode in Reverse Bias

When a PN junction diode is connected in a Reverse Bias condition, a positive (+ Ve) voltage is connected to the N type material & a negative (-Ve) voltage is connected to the P-type material.

When the +Ve voltage is applied to the N-type material, then it attracts the electrons near the positive electrode and goes away from the junction, whereas the holes in the P-type end are also attracted away from the junction near the negative electrode.

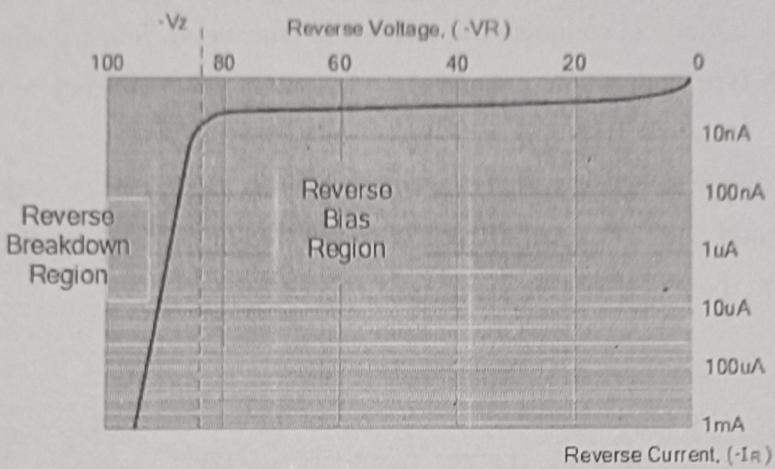


PN Junction Diode in Reverse Bias

In this type of biasing, current flow through the PN junction diode is zero. Though, the current leakage due to minority charge carriers flows in the diode that can be measured in a uA (micro amperes). As the potential of the reverse bias to the PN junction diode ultimately increases and leads to PN junction reverse voltage breakdown and the current of the PN junction diode is controlled by an external circuit. Reverse breakdown depends on the doping levels of the P & N regions. Further, with the increase in reverse bias the diode will become short circuited due to overheating in the circuit and max circuit current flows in the PN junction diode.

VI Characteristics of PN Junction Diode in Reverse Bias

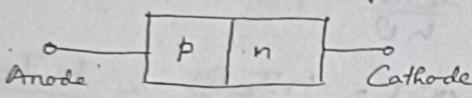
In this type of biasing, the characteristic curve of diode is shown in the fourth quadrant of the below figure. The current in this biasing is low till breakdown is reached and hence the diode looks like as open circuit. When the input voltage of the reverse bias has reached the breakdown voltage, reverse current increases enormously.



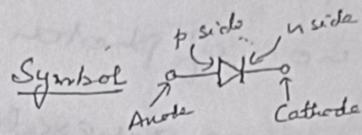
PN Junction Diode VI Characteristics in Reverse Bias

P-N Junction Diode

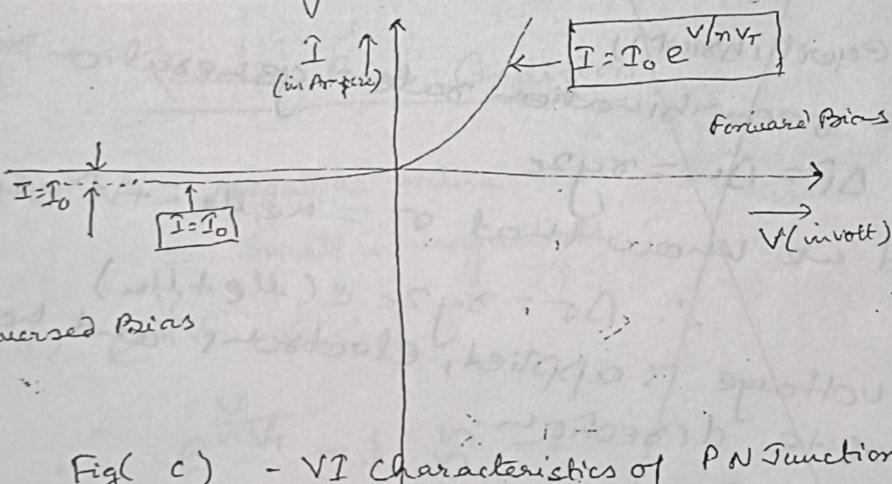
The P-N junction itself forms the ^{most} basic semiconductor device called Semiconductor Diode. The meaning of the term DIODE is the device having two electrodes (di-ode).



Fig(a) A p-n junction diode
forms semiconductor diode



Fig(b) Circuit symbol of
a diode

Biasing of P-N Junction diodesV-I Characteristics of P-N Junction diode

Fig(c) - VI Characteristics of P-N Junction Diode

As Diode Equation from P-N-V-I characteristics shows that

$$\boxed{I = I_0 / (e^{V/nV_T} - 1)} \rightarrow ①$$

$$= I_{FB} + I_{RB}$$

Where I_0 = Reverse saturation current

γ = Constant value

= 1 for Ge element

= 2 for Si element

V_T = Voltage equivalent to Temperature (T)

$$= \frac{T}{11600} \text{ volt}$$

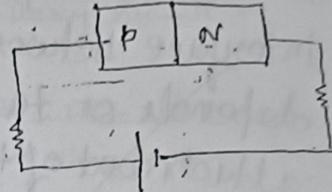
Case IForward Bias Condition

Dr. Mudit Srivastava

- (i) $V = \text{positive value}$
 $= \text{Small in magnitude}$

(ii) $e^{\frac{V}{nV_T}} \gg 1$

$\therefore e^{\frac{V}{nV_T}} - 1 \approx e^{\frac{V}{nV_T}}$



So equation ① reduces to

$$\boxed{I = I_0 e^{\frac{V}{nV_T}}} \quad \dots \rightarrow ②$$

Case IIReverse Bias Condition

- (i) $V = \text{Negative value}$
 $= \text{Small in magnitude}$

(ii) $e^{\frac{V}{nV_T}} \ll 1$

$\therefore e^{\frac{V}{nV_T}} - 1 \approx -1$

so equation ② reduces to

$$\boxed{I = -I_0} \quad \dots \rightarrow ③$$

So based on Case I & Case II, the VI characteristics of P-N Junction diode was drawn.

Reverse saturation Current (I_o)

- It is the current flowing through the PN Junction in the reverse biased condition.
- It depends upon the minority charge carrier concentration and its magnitude is very small in the order of μA .
- This current is independent of the Reverse biased applied so long as the magnitude of this reverse bias is large.
- This current is temperature dependent and is doubled for every 10° rise in temperature.

$$I_o' = I_o \cdot 2^{\frac{(T' - T)}{10}}$$

I_o' = Reverse saturation current at temperature T'

I_o = Reverse saturation current at temperature T

Junction Capacitance in a PN Junction diode

Junction Capacitance

Transition Capacitance (C_T)

- Exists in Reverse Biased junction
- Occurs due to Majority Charge Concentration

Abrupt
P-N Ju

Linearly
graded P-N Ju

Diffusion Capacitance (C_D)

- Exists in forward Bias Condition
- Occurs due to Minority Charge Concentration

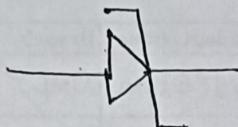
C_n
(Electron)

C_p
(Holes)

ZENER DIODE

- * → PN Junction diode with heavy doping
- Always operated in Reverse Biased condition
- Operation depends upon
 - (a) Zener Breakdown
 - (b) Avalanche Breakdown

Symbol



Zener Diode Phenomenon

- (a) It is a PN Junction diode with very heavy doping
- (b) The magnitude of Reverse Bias applied is relatively low in the order of 6V

$$\boxed{\begin{array}{l} \text{doping} \uparrow \rightarrow d \downarrow \\ \text{RB} \uparrow \rightarrow d \uparrow \end{array}}$$

- (c) The junction width (d) and therefore the depletion width (d) is always narrow (i.e. in the range of Å)
- (d) The applied electric field near the junction is very large, is of the order of 10^7 V/m

$$\boxed{E = \frac{V}{d}}$$

- (e) At a given RB voltage, the electric field is sufficiently high so that there is direct rupture of covalent bonds near the junction.
- (f) A large number of carrier is generated. At each region, conductivity increases and hence the current increases maintaining a constant potential across the junction.