PES University, Bengaluru

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UE20CS252

MAY 2022: END SEMESTER ASSESSMENT (ESA) B TECH 4th SEMESTER

UE20CS252 – MICROPROCESSOR AND COMPUTER ARCHITECTURE

Time: 3 Hrs	Answer All Questions	Max Marks: 100

Note: ARM7TDMI – ISA stands for ARM Instruction Set Architecture,
ALP – Assembly Language Program

1 a) Convert the following pseudo code into an ALP using ARM7TDMI – ISA. **06**

```
IF([A]==[B]) then C=[A]*[B];
ELSE IF ([B]==[C]) D=[A]-[B];
ELSE E=[A]+[B].
```

[Note: Use Conditional Execution Instructions].

Assume that the registers R1, R2, R3 contain the addresses of memory locations A, B and C respectively.

Also, Let registers R6, R7, to carry the contents of memory locations A and B respectively.

b) The code snippet given below performs matrix multiplication. Complete the code by writing the missing instructions. **06**

```
.DATA
A: .WORD 1,2,3,4,5,6,7,8,9
B: .WORD 1,2,3,4,5,6,7,8,9
C: .WORD 0,0,0,0,0,0,0,0,0
.TEXT
        LDR R0,=A
        LDR R1,=B
        LDR R2,=C
        MOV R3,#0
        MOV R4,#0
          MOV R10,#3
        MOV R8,#0

// to be completed

        MUL R11,R5,R6
        ADD R9,R9,R11
        ADD R8,R8,#1
        CMP R8,#3
        BNE LOOP1
```

```
// to be completed

        MOV R8,#0
        MOV R9,#0
        ADD R4,R4,#1
        CMP R4,#3
          BNE LOOP1
        MOV R4,#0
        ADD R3,R3,#1
        CMP R3,#3
        BNE LOOP1
        SWI 0X011
.END
```

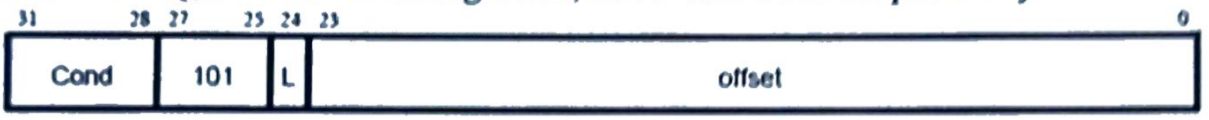
c) How are the parameters passed to the functions in ARM7TDMI-ISA using stack? Explain with an example. **04**

d) Consider the following code snippet. Assume ARM7TDMI - 3 stage pipeline processor. The execution of the branch instruction happens in the execute stage.

```
.TEXT
LDR R3,=A
LDR R4,=B
LDR R0,[R3]
LDR R1,[R4]
GCD: CMP R0, R1
     BEQ RES
     BLT LOOP
     SUB R0,R0,R1
     B GCD
LOOP: SUB R1, R1, R0
      B GCD
RES: MOV R2,R0
     SWI 0X011
.END
```

Determine the hexadecimal equivalent instruction encoding for the branch instruction BEQ and B instructions.

Note: The encoding pattern for a branch instruction is as given below with the condition code for EQ,LT and AL being 0000, 1011 and 1110 respectively.



2 a) Consider five stage pipeline architecture of a processor. Assume that the individual stages of the data path have the following latencies.

IF – 300ps, ID – 400ps, EX – 350ps, MEM – 500ps and WB – 100ps.

What is the clock cycle time in a pipelined and non-pipelined processor?

If there are 50 instructions compute the ratio of non-pipelined to pipelined processors.

b) Examine how data dependencies affect execution in the basic 5-stage pipeline processor.

```
LW   $1, 40($6)
ADD  $6, $2, $2
SW   $6, 50($1)
```

i. Assuming there is no forwarding in this pipelined processor,
   Indicate the hazards and add NOP instructions to eliminate the same.

ii. Assuming there is full forwarding,
   Indicate the hazards and add NOP instructions to eliminate the same.

Write the instructions sequence with NOP for both the cases.

Show the same using pipeline execution diagrams.

	c)	Consider the following sequence of instructions. LABEL1: LW $1, 40 ($6) BEQ $2, $3, LABEL2 ; branch taken ADD $1, $6, $4 LABEL2: BEQ $1, $2, LABEL1 ; branch not taken SW $2, 20 ($4) AND $1, $1, $4 i. Draw the pipeline execution diagram for the code assuming there are no delay slots and the branches execute in the EX stage. ii. Draw the pipeline execution diagram for the code assuming delay slots are used and branch instructions are executed in the ID stage. NOTE: $1,$2, $3, indicates register1, register2, register3 respectively and so on.	06
	d)	Consider a program with the following behavior. T, T, T, NT, NT, T, T, T, T, NT, NT, T (where NT –branch Not Taken & T – branch Taken). How many miss predictions are seen if the initial state is strongly taken for a 2 bit prediction?	04
3	a)	A computer system with a word length of 32 bits has a 64MB byte-addressable main memory and a 128KB; 4-way set associative cache memory with a block size of 2048 bytes. i. Determine the block number of the address $(546888)_{10}$ and find the set number in the cache memory and the tag bits. ii. Compute the total number of bits required for direct mapped cache?	06
	b)	Assume cache memory of 16KB with a block size of 512 bytes. If the hit time is 1.08ns and miss rate is 3.4%, what is the average memory access time if the system has 90 clock cycles overhead and takes 4CC to transfer every 64 bytes from main memory?	04
	c)	Consider a scenario of multilevel cache memory system. It is given that the write policies of L1 and L2 cache memory are write-back policy and write through policy respectively. Describe the procedure of handling L1 write miss considering the component involved and the possibility of replacing a dirty block.	05
	d)	Consider a memory system that has 512 byte cache with 64 byte blocks. Assume that the main memory is 2KB large. Main memory has 64 byte blocks: M0, M1, M2, M3,....M31. The figure below sketches the memory blocks that can reside in different cache blocks if the cache was fully associative.	05

Cache block	Set #	Associativity	Memory Block
0	0	0	M0, M1, M2, ..M31
1	0	1	M0, M1, M2,...M31
....	0	...	.....
7	0	7	M0, M1, M2, ..M31

Show the contents of the table if cache is organized as

i. Direct Mapped Cache ii. 4 –Way Set Associative Cache.

4	a)	Consider the following data Cache size Block size | 4K | 16K | 64K | 256K 16 | 8.57% | 3.94% | 2.04% | 1.09% 32 | 7.24% | 2.87% | 1.35% | 0.70% 64 | 7.00% | 2.64% | 1.06% | 0.51% 128 | 6.78% | 2.77% | 1.02% | 0.49% 256 | 6.41% | 3.29% | 1.15% | 0.49% What are the observations with respect to cache size and block size based on miss rate? Justify. Discuss with respect to AMAT as well.	06
	b)	Consider a system that has 64 bit logical address and 41 bit physical address. If the page size is 16KB and the TLB with direct mapped cache can store 512 entries, determine the number of tag bits required for i. 16KB - L1 cache with a block size of 128 words. ii. 16MB - L2 cache with a block size of 128 words	04
	c)	When an interrupt is detected, the status register is saved and all but the highest priority interrupt is disabled. Why low priority interrupts are disabled? Why is the status register saved prior to disabling interrupts?	04
	d)	Direct memory access allows devices to access memory directly rather than working through the CPU. This improves the performance of the peripherals, but adds to complexity to memory system implementations. i. Does CPU relinquish (giveup) control of the memory when DMA is active? ii. For example, can a peripheral simply communicate with the memory directly, avoiding the CPU completely? iii. How will graphics card benefit from DMA?	06
5	a)	Consider the operation of finding the dot product of 2 vectors as mentioned below: Let a=[a1, a2, a3,..an] and b=[b1,b2,b3...bn] is defined as $\Sigma a_i b_i$ = a1b1+a2b2+a3b3+...+anbn. Realize the problem to be solved on parallel computing system. Write the loops using pseudo code. The value of n is 100K. Note: You may need 2 levels of computation.	04
	b)	Consider a parallel computing system with 128 processors. i. Compute the speedup if the code has 15% serial processing. ii. Compute the scaled speedup if the code can be 95% parallelized. { Hint: Use Amdahl's and Gustafson's Laws formulae appropriately}.	04
	c)	Mention the design constraints or issues in a parallel computing system.	04
	d)	What are the 3-ways of accelerating applications in GPU system? Actual computations are done on the streaming multiprocessors [SM]. What are the components of each SM? How many warp schedulers would be in GPU that has 1536 cores? "GPU has better throughput than the speed of a Multicore processor" – Justify.	08