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UE16CS253

PES University, Bangalore
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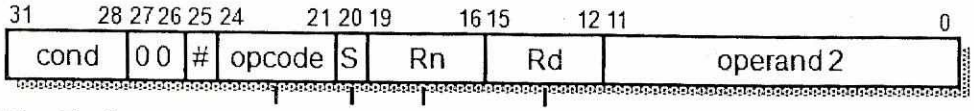
END SEMESTER ASSESSMENT (ESA) B.TECH. IV SEMESTER-MAY 2018
UE16CS253- Microprocessor and Computer Architecture

Time: 3 hrs **Answer All Questions** **Max Marks: 100**

1	a	Differentiate between microprocessor and micro-controller	4

	b	Write the conditional code for the following C code snippets.
		i)
		if(r0<5){
		sub1()}
		else{
		sub2()
		}
		ii)
		if (r0 > r1) {
		r2= 5
		r3 = r4 + r5 }
		else
		r6 = r4 –r5
		iii)
		if (r0 != 5) then
		r1 = r1 + r0 - r2
		iv)
		if ((r0==r1) && (r2==r3))
		then
		R4 = r4 + 1
			4

	c	I. Mention 3 ways of specifying offsets in data transfer instructions. Give an example for each II. Write ARM assembly code to perform the following operation f= (g + h) - (i+ j); III. Write a **single line** of ARM assembly code to perform the operation r0=r2x7 (Note: without using MUL instruction)	3+2 +2
	d	The address for the memory system starts from 1000. It is byte addressable and follows little endian representation. Show the memory allocated for the following data declaration in ARM memory organization. a:.hword 200 b:.byte 20,10,60 c:.hword 30 d:.hword 100 e:.word 600	5
2	a	Perform Multiplication of following by constant using barrel shifter. Give an example for each. I) 2^n II) 2^n+1 III) 2^n-1	1+2 +2
	b	What are the handshaking signals used by ARM and its coprocessor for execution of coprocessor instructions?	3
	c	Define software interrupt? Mention different software interrupts available in ARM with their purpose	6
	d	Given Binary encoding format of data processing instruction  Identify the instruction for the given hexadecimal representation of the instructions I. E0532008 II. E3A0200A III. 10844005 Given binary representation of condition codes and opcodes NE=0001, CS=0010, EQ=0000, LE=1101, GT=1100,LT=1011 AND=0000, ADD=0100, SUB=0010,BIC=1110, ORR=1100, CMP=1010,EOR=0001,MOV=1101	6
3	a	Major functional units are used in different cycles. Hence, overlapping the execution of multiple instructions introduces relatively few conflicts. How these conflicts are resolved?	6
	b	Write the pipeline stages to execute High Level Language statement A=B+C where A,B,C are memory locations. How many stalls are introduced.(Note: Write Assembly code For MIPS to draw pipeline stages)	5+1

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	c	Given a sequence of instructions below for MIPS architecture. Considering
		EX-stage for Load / Store operations takes 1 clock cycle (EX);
		EX-stage for ADD or SUB operations takes 1 clock cycle
		EX-stage for MUL operation takes 3 clock cycles
		EX-stage for DIV operation takes 4 clock cycles
		
		LW R6, 20(R5)
		LW R2, 28(R5)
		MUL R0,R2,R4
		SUB R8,R6, R3
		DIV R10,R0,R6
		ADD R6, R8,R2
		SW R8, 50(R5)
		I. What kind of hazards are between following instructions
		i) LW R2, 28(R5) and MUL R0,R2,R4
		ii) DIV R10,R0,R6 and ADD R6, R8,R2
		iii) MUL R0,R2,R4 and SW R8, 50(R5)
		II. What kind of Data hazards are between the following instructions.
		I) MUL R0,R2,R4 and DIV R10,R0,R6
		ii) DIV R10,R0,R6 and ADD R6, R8,R2
		iii) MUL R0,R2,R4 and SW R8, 50(R5)
			6

	d	Why a designer allows structural hazard?	2
4	a	What are the most commonly used write strategies when the processor executes a write cycle?	6
	b	When a new data is to be placed in the cache, a decision must be taken to place in it. What are the policies are available to place new data in the cache when there is no free block available for placing	3
	c	Which cache optimization technique used in the following I. Increase Cache Capacity to reduce capacity misses. II. Global cache miss rate should be used when evaluating second level caches III. This optimization serves reads before writes have been completed. IV. Higher associativity to reduce miss rate V. Avoiding Address Translation during Indexing of the Cache to Reduce Hit Time	5
	d	Assume the memory system takes 80 clock cycles of overhead and then delivers 16 bytes every 2 clock cycles. That is, it can supply 16 bytes in 82 clock cycles, 32 bytes in 84 clock cycles, and so on… What is the average memory access time for block size of 256 and cache size of 256K? Figure 4d shows various cache, block sizes and miss rate	6
5	a	If a cache has a capacity of 16 kB and a block size of 128 bytes, find how many sets does the cache have if it is 2-way, 4-way, or 8-way set-associative.	6
	b	What are the factors on which the design of the exception stack depends?	4
	c	What are the modes in which processor executes the instructions and also specify their purpose	4
	d	What are the classes of parallelism in applications and architecture of a super scalar processor?	6

	Cache size			
Block size	4K	16K	64K	256K
16	8.57%	3.94%	2.04%	1.09%
32	7.24%	2.87%	1.35%	0.70%
64	7.00%	2.64%	1.06%	0.51%
128	7.78%	2.77%	1.02%	0.49%
256	9.51%	3.29%	1.15%	0.49%