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PES UNIVERSITY

(Estd. Under Karnataka Act 10 of 2013)

BSK 3RD STAGE, BENGALURU-560085

UE17CS253

May 2019: END SEMESTER ASSESSMENT, B.TECH., IV SEMESTER

UE17CS253 Microprocessor & Computer Architecture

Time: 3 hrs — Briefly Answer All the Questions. — Max Marks: 100

1.	a)	Consider that the initial contents of the registers are as follows. R0 = 0x0000F0F0 Mem Loc[0x00005000] contains 0x0F0F0020 R2 = 0x00000505 Mem Loc[0xF0F00020] contains 0x02020202 R12 = 0xF0F00000 R13=0x00005000 Write the contents of the destination registers after the execution of the following instructions. [Every instruction is independent] i. **LDRH R0, [R13,#0]** ii. **STRB R2, [R12, #20]** Note: Assume Little Endian format.	02
	b)	Write the sequence of instructions to load the following 32 bit data into the register R10 using immediate addressing mode. **0000 0000 1101 1001 0000 0000 0000 0000.** [Note : No instruction allows immediate transfer of 32 bit data. Do not use LDR instruction. Initialize with the 8 bit number. Use only data processing instruction].	04
	c)	i. Implement the following C statement using ARM assembly instructions. **A = A ? B: C[0]** ii. Implement the C statement using ARM conditional assembly instructions. **While(i < 10)** **{ C[i] = B + i;** **i + = 1;** **}** [Note: i. Let A & B are memory locations and C is an array. The starting address of these locations are in registers R2, R3 and R4 respectively ii. i - count in register R5].	02 + 04
	d)	Differentiate between i. Computer Organization and Computer Architecture ii. Microprocessor & Microcontroller iii. RISC & CISC	06
	e)	Mention the 3 - addressing modes used in ARM instruction set architecture	02
2.	a)	Define the following terms with respect to pipeline i. Throughput ii. Registers Delay	02

	b)	Consider the following instructions executed on a 5 stage pipeline processor with Von Neumann architecture. Determine what hazards are observed and how many stalls are introduced? How are those hazards overcome? Explain.
		LDR R10, =A
		SUB R11, R2, R3
		LOOP: ADD R12, R3, R4
		LDR R13,[R10]
		ADD R14, R12, R6
		BNE LOOP
			07

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	c)	i. Assume that in the 5 stage pipeline the longest stage requires 0.8ns. The pipeline register delay is 0.1ns and clock skew is 0.01ns. What is the clock cycle time of the pipeline? ii. Consider an ideal 5 stage pipeline processor. How much is the speedup (performance of the system) for such a system?	03
	d)	How data hazards are minimized using data forwarding in a 5 stage pipeline architecture? Explain with a neat diagram.	04
	e)	What is delayed branch? Explain scheduling the branch delay slot for branch taken and branch not taken and replacing by a 'SAFE' instruction.	04
3.	a)	Assume a computer system with CPI as 1.0, when all the memory access are hits. The only data accesses are loads and stores with 40% of the instructions. If the miss penalty is 50 clock cycles and the miss rate is 4%, how much faster would the computer be if all the instructions were cache hits?	04
	b)	What is principle of locality? Explain the each type of locality of reference with an example	05
	c)	Write the corresponding miss category in each of the following scenario. i. Initially, the cache is empty. The very first access to the block will generate a miss. ii. During the execution of the program, cache generated a miss. This is because the cache could not contain all the blocks needed during the execution of the program. iii. Multiple blocks map to its set(set=1 for direct cache) higher in the hierarchy .	03
	d)	For the memory references given below, identify the binary address, the tag and the set bits in a direct mapped cache with 16 one word blocks. Also list if each reference is a hit or a miss, assuming that the cache is initially empty. Assume 8 Address Machine. 1, 134, 212, 1, 135, 162	06
	e)	Write the protocols used in "Handling Writes ".	02
4.	a)	Consider a 32 bit address machine with cache memory of 16KBytes. Each cache block has 64 words. Assume each set has 16 blocks. Determine the SET number, TAG number of the 20044. Compute Average Memory Access Time if the bandwidth is 32bit and transfer rate is 2clock cycles with a miss rate of 4% and hit time is 1.0 clock cycle.	06
	b)	"Multi level cache reduces miss penalty". Justify the statement with an example.	04
	c)	Consider a scenario of transferring data between device (say printer) and the memory. Explain how DMA is used to perform the task of data transfer?	04
	d)	Explain the following techniques i. Polling ii. Daisy Chain Technique iii. Vectored Interrupts	06
5.	a)	Write the limitations of serial computing and the applications of parallel computing.	05
	b)	Mention Flynn's Classification of parallel computing. Explain any one with an example.	05
	c)	Compute the speedup and scaled speedup in a parallel computing system that has 16 cores with 20% serial code. [Note: Speedup – Amdahl's Law & Scaled Speedup- Gustafson's Law]	04
	d)	Write a function in C language to find the sum of n elements in a array. Do you advice the code be executed in a parallel environment for n < 1000. Justify your answer. Convert the code to execute on a parallel computing system if the value of n is very large.	02 + 04

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Answer:

Hazards encountered:

1. **Structural Hazard:** Inst1 and inst4 would access memory at the same time in the pipeline. Resolved by using **Harvard architecture – Using separate cache for both data and instructions.**
2. **Data Hazard:** Inst3 and inst5 has data dependency. Can be resolved by **data forwarding.**
3. **Control Hazard: Instruction6 is a branch instruction. Hence will have a branch or control hazard. It can be resolved by using a safe instruction.**
4. Explanation – 2 Marks.

c) i. Assume that in the 5 stage pipeline the longest stage requires 0.8ns. The pipeline register delay is 0.1ns and clock skew is 0.01ns. What is the clock cycle time of the pipeline? — 02

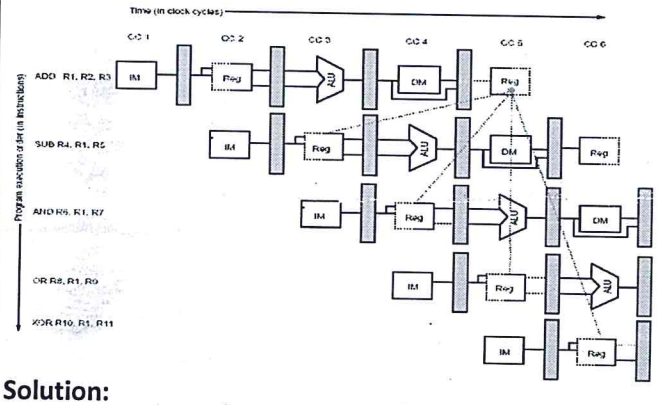
ii. Consider an ideal 5 stage pipeline processor. How much is the speedup (performance of the system) for such a system? — + 01

Answer: i. longest Pipeline Time + Register Delay + Clock Skew = 0.8+0.1+0.01=0.91ns.

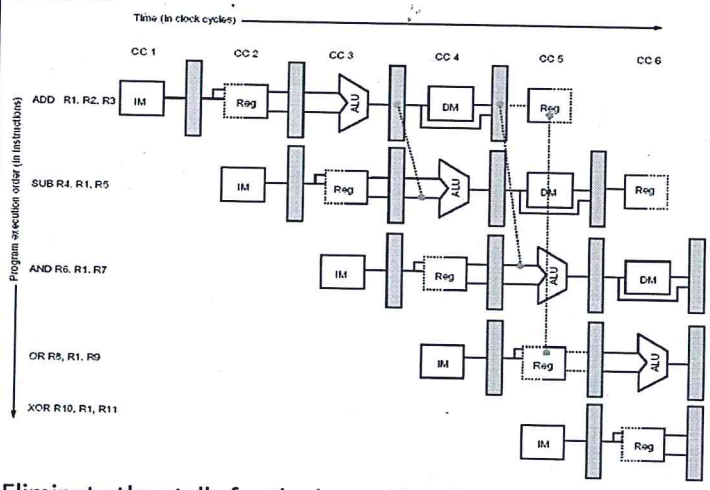
Ii. Pipeline depth= 5.

d) How data hazards are minimized using data forwarding in a 5 stage pipeline architecture? Explain with a neat diagram. — 04

Data Hazard:



Solution:



Eliminate the stalls for the hazard involving SUB and AND instructions using a technique called ***Data forwarding***

e) What is delayed branch? Explain scheduling the branch delay slot for branch taken and branch not taken and replacing by a 'SAFE' instruction. — 04

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SCHEDULING BRANCH DELAY SLOTS

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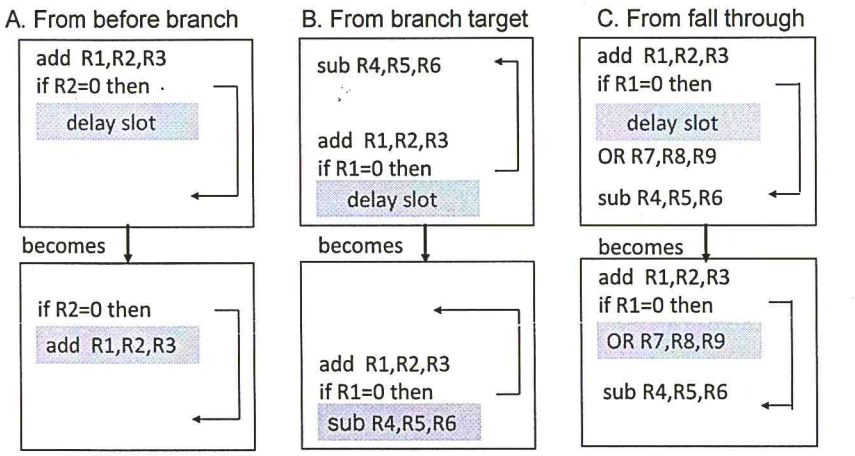

- A is the best choice, fills delay slot and reduces IC
- In B and C, the `sub` instruction may need to be copied, increasing IC
- In B and C, must be okay to execute `sub` when branch fails

3.	a)	Assume a computer system with CPI as 1.0, when all the memory access are hits. The only data accesses are loads and stores with 40% of the instructions. If the miss penalty is 50 clock cycles and the miss rate is 4%, how much faster would the computer be if all the instructions were cache hits? **Answer:** CPU execution time = [CPU Clock Cycles + Memory Clock Cycles] x Clock Cycles (Always Hits) = [IC x CPI + 0] x Clock Cycles = 1.0 Clock Cycle. Memory Stall Cycles = IC x $\frac{\text{Memory accesses}}{\text{Instruction}}$ x Miss Rate x Miss Penalty = IC x (1+0.4) x 0.04 x 50 = IC x 2.8 CPU execution time = [CPU Clock Cycles + Memory Clock Cycles] x Clock Cycles = (IC x 1.0 + IC x 2.8) x Clock Cycles = 3.8 x IC x Clock Cycles Performance = $\frac{\text{CPU execution time}}{\text{CPU execution time (Always Hit)}}$ = 3.8 times. **Computer with no cache is 3.8 times faster.**	04
	b)	What is principle of locality? Explain the each type of locality of reference with an example • Temporal locality (locality in time): if an item is referenced, it will tend to be referenced again soon. • Spatial locality (locality in space): if an item is referenced, items whose addresses are close by will tend to be referenced soon.	05