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PES UNIVERSITY

# PES University, Bangalore

(Established under Karnataka Act No. 16 of 2013)

**UE14CS253**

## JUNE_JULY 2016: END SEMESTER ASSESSMENT (ESA) B.E IV SEMESTER

## UE14CS253

Time: 3 Hrs | Answer All Questions | Max Marks: 100

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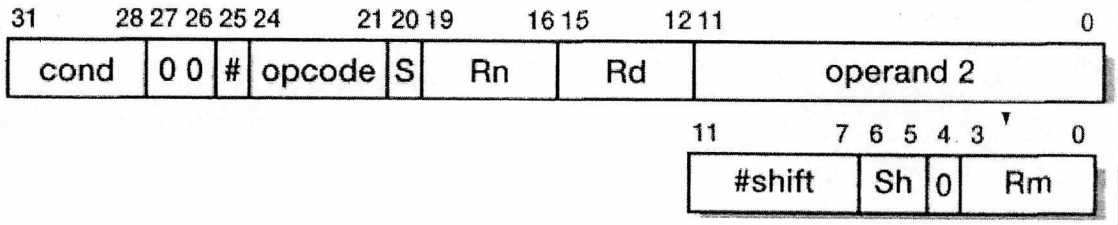
|---|---|---|---|
| 1. | a) | Explain the various modes of operation in core ARM processor | 5 |
| | b) | Differentiate between RISC and CISC | 5 |
| | c) | What's the role of Barrel shifter in 3 stage pipeline? | 5 |
| | d) | How is harvard and Von neumann architecture different from each other. | 5 |
| 2. | a) | Explain the following instructions of ARM processor<br>i) TSTEQ R1, R2, R3 ii) BIC R5, R6, R7 | 5 |
| | b) | What is the output of the following code snippet?<br>LDR r1,=A<br>LDMIA r1,{r5,r0,r4,r3}<br>A: .word 10,20,30,40 | 5 |
| | c) |  <br>Given the instruction format show the binary encoding of the following instruction.<br>(cond-1110,opcode-0100, sh-11)<br>ADDS R2, R3, R6, LSL #2 | 4 |
| | d) | What are the contents of registers r0 and r1 after the execution of each instruction?<br>a) LDR r0,=B<br>b) LDR r1,[r0]<br>c) LDR r1,[r0],#4<br>d) LDR r1,[r0,#4]<br>e) LDR r1, [r0, #4]!<br>B: .WORD 10,20,40,60,80 | 6 |
| 3. | a) | Write an assembly language program to find average of n numbers | 5 |
| | b) | What is pipelining? Explain how pipelining improves the performance | 5 |
| | c) | A procedure to compute the statement in high level language using ARM ALP.<br>if (R0>=R1)<br>R2-- ;<br>Else<br>R2++;<br>Data in Regs. R0, R1 are parameters. Result in Reg. R2. | 5 |
| | d) | How is 5 stage pipeline different from 3 stage pipeline? | 5 |

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| 4. | a) | A cache is 4-way set-associative and has 128 KB data. Each block contains 16 bytes. The address is 32 bits wide. What are the sizes of the tag, index, and block offset fields? | 5 |
| | b) | What are the handshaking signals used to communicate between ARM and coprocessor | 6 |
| | c) | What is cache misses? Explain the different categories of misses. | 4 |
| | d) | Assume we have a computer where the cycles per instruction (CPI) is 1.0 when all memory accesses hit in the cache. The only data accesses are loads and stores, and these total 50% of the instructions. If the miss penalty is 25 clock cycles and the miss rate is 2%, how much faster would the computer be if all instructions were cache hits? | 5 |
| 5. | a) | What are interrupts and explain the handling mechanism of nested interrupt calls | 5 |
| | b) | What is pipeline scheduling? Explain with an example | 5 |
| | c) | Write a short note on<br>1) Cache replacement algorithm<br>2) Cache optimization technique(Any two) | 10 |