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# PES University, Bengaluru

(Established under Karnataka Act No. 16 of 2013)

**UE19CS252/ UE18/17CS253**

**JULY/AUGUST 2021: END SEMESTER ASSESSMENT (ESA) B TECH 4th SEMESTER**

**UE18/17CS253 /UE19CS252 – MICROPROCESSOR AND COMPUTER ARCHITECTURE**

**Time: 3 Hrs** | **Answer All Questions** | **Max Marks: 100**

Note: ARM7TDMI – ISA stands for ARM Instruction Set Architecture,
ALP – Assembly Language Program

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| 1 | a) | Write the ARM7TDMI ALP code snippet for the following code written in C–language. Let **R1, R2, R3** contain the starting addresses of arrays **X, Y** and **Z** respectively. Use Register **R5** for variable **i**.<br>**While ( i ++ <= 10 )**<br>**{**<br>**If ( X [ i ] == Y [ i ] )**<br>**Z [ i ] = X [ i ] * Y [ i ] ;**<br>**}**<br>{Hint: X[i] is written as [R1,R5] , Y[i] as [R2,R5] and Z[i] as [R3,R5] } | 06 |
| | b) | What are the different parameter passing techniques in ARM7TDMI – ISA? What parameter passing technique is used in the following ARM7TDMI - ISA code snippet? Explain.<br>.text<br>LDR R4, =A<br>MOV R1, #52<br>MOV R2, #25<br>STMFD R13!, { R1, R2}<br>BL LINK<br>STR R0, [R4]<br>SWI 0x11<br>LINK: LDMFD R13!, { R6, R5}<br>ADD R0, R6, R5<br>MOV PC, LR<br>.data<br>A: .WORD 0 | 04 |
| | c) | Is **FIQ exception or interrupt** accepted by the ARM processor, **while** the data abort Exception is **currently** being serviced? Explain. | 04 |

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d) I. Consider the following coding used in ARM7TDMI encoding. **06**

**Conditional codes : 1110 - AL, GE - 1010 , LE – 1101**

**Operation codes : RSB - 0011, AND – 0000, ORR - 0001**

What ARM instructions do these encoding represent?

| Inst | Condition | F (format) | I (immediate) | OPCODE | S (Set cond Code) | Rn | Rd | Operand2 |
|---|---|---|---|---|---|---|---|---|
| i. | 1010 | 0 | 0 | 3 | 0 | 0 | 1 | 2 |
| ii. | 1101 | 0 | 1 | 0 | 1 | 2 | 3 | #12 |

II. Write the instruction to multiply a number X by 17. Use **only ADD / SUB / RSB** Instructions. Store the result in the source register itself.

{Assume the number is in the register **R9, that is R9 = R9 x 17**}.

2 a) Consider Von Neumann architecture. A machine has only one memory unit. But under certain conditions, the pipeline might want to perform two operations (like read instruction / write operation) simultaneously during the same clock cycle. Is it possible? What type of hazard is introduced? Explain. How can this hazard be resolved? Explain with neat diagrams. **04**

b) Consider the following sequence of instructions written in ARM7TDMI - ISA. Assume A, B and C are memory locations storing data. **04**

```
LDR R1, [A]
LDR R2, [B]
LDR R3, =C
ADD R0, R1, R2
SUB R4, R0, R2
AND R5, R4, R1
STR R5, [R3].
```

How many clock cycles does it take to execute and stall cycles are introduced in the following cases?

Case i. No data forwarding is supported.

Case ii. Data or operand forwarding is supported.

Note: Write operation is performed during the first half of the clock cycle time while read operation is done during the Second half of the clock cycle time. Show the working for the same.

c) What are the types of data hazards? Explain each with an example **06**

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| | d) | Consider a program with the following behavior..<br>T T NT T NT T T T NT T T T T T NT T T T T NT (NT – Not Taken & T – Taken).<br>i. How many miss predictions are seen if the initial state is NT for a 1 bit prediction?<br>ii. With a neat 2- bit prediction state diagram, show how many miss predictions occur if the initial state is 10 (weak taken state). Write the working for both the cases.<br>Note: In a 2 bit predictor, If prediction is taken, next state is strong taken otherwise, strong not taken. | 06 |
| 3 | a) | A computer system with a word length of 32 bits has a 16 MB byte-addressable main memory and a 64 KB, 4-way set associative cache memory with a block size of 256 bytes. Consider the following four addresses represented in hexadecimal notation.<br>A1 = 0x42C8A4, A2 = 0x546888, A3 = 0x6A289C, A4 = 0x5E4880<br>Determine which of these addresses map on to the same set in the cache memory. Show the computations.<br>Note: Determine the number of bits required to represent word and set numbers. | 07 |
| | b) | What are the categories of misses? Explain how to avoid address translation in cache indexing to reduce hit time? | 05 |
| | c) | If a direct mapped cache has a hit rate of 90%, a hit time of 5ns, and a miss penalty of 100ns, what is the AMAT? If an L2 cache is added with a hit time of 25ns and a hit rate of 50%, what is the new AMAT, if the penalty for an L2 miss is 200ns? Also compute local miss rates of L1 and L2 caches and the global miss rate. | 04 |
| | d) | Assume a processor where the cycles per instruction (CPI) is 1.0 when all memory accesses hit the cache. The only memory accesses are loads and stores, and these make up 60% of the instructions. If the miss penalty is 50 clock cycles and the miss rate is 5%, how much faster would the computer be if all instructions were cache hits? | 04 |
| 4 | a) | Assume that the memory system takes 100 clock cycles of overhead and then delivers 32 bytes every 4 clock cycles. That is, it can supply 32 bytes in 104 clock cycles, 64 bytes in 108 clock cycles, and so on... Compute the average memory access time for a block size of 128bytes and cache size of 64KB that has a miss rate of 1.02%. Assume hit time is 1cc. | 04 |
| | b) | Consider the following code sequence. Assume Direct mapped cache.<br>STR R3, 256 (R0)<br>LDR R1, 2048 ( R0)<br>LDR R2, 256 (R0)<br>Write-through cache maps 256 and 2048 to the same block. A four words write buffer is not checked on a read miss. Will the value in register R2 always be equal to the value in register R3 or R2? Discuss. | 05 |
| | c) | What is an interrupt vector table? Write the interrupt table of ARM7TDMI processor. How simultaneous multiple interrupts are handled? Explain. | 05 |

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| | d) | How does user enable and disable FIQ and IRQ interrupts? Explain with appropriate code using ARM7TDMI- ISA. | 06 |
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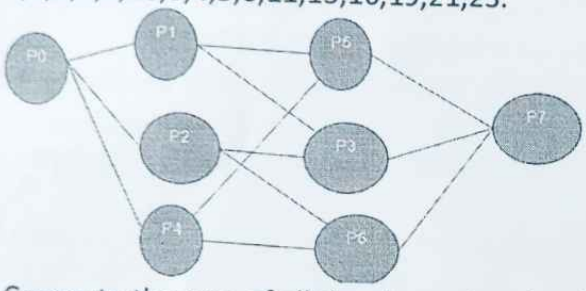
| 5 | a) | With neat diagrams discuss parallel computing memory architectures. | 06 |
| | b) | Explain the features of Very Long Instruction Word (VLIW) processor. | 05 |
| | c) | Consider an input sequence of data elements as shown below.<br>7,8,1,2,9,10,3,4,5,6,11,13,16,19,21,23.<br>  <br><br>Compute the sum of all the elements using the hypercube parallel model.<br>Hint: Initial assignment of data items may be as follows:<br>Iteration1: P0 adds (7, 8), P1 adds (1,2), P2 adds (9,10) and so on where p7 adds 21 & 23. Perform the computations for each iteration to show the computations for all the iterations. | 05 |
| | d) | Consider a parallel computing system with 16 processors. Compute the speedup if the code has 4% of seria! processing. Also, compute the scaled speedup if the code can be 90% parallelized.<br>{ Hint: Use Amdahl's and Gustafson's Laws formulae appropriately}. | 04 |