FPOAs: Pushing Programmable Logic Performance Beyond FPGAs

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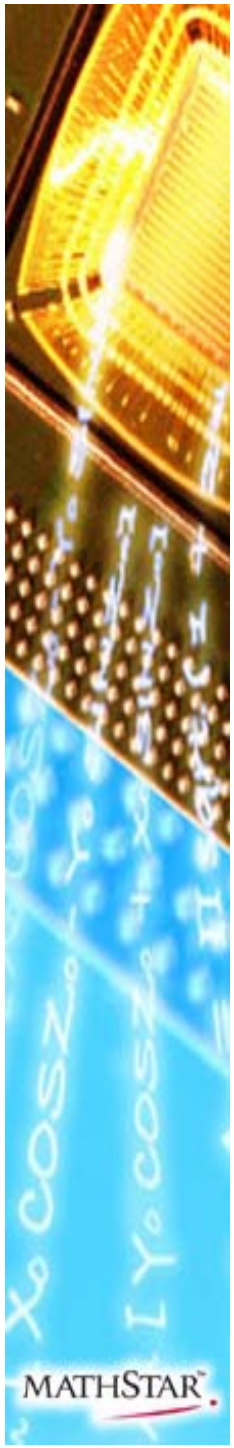
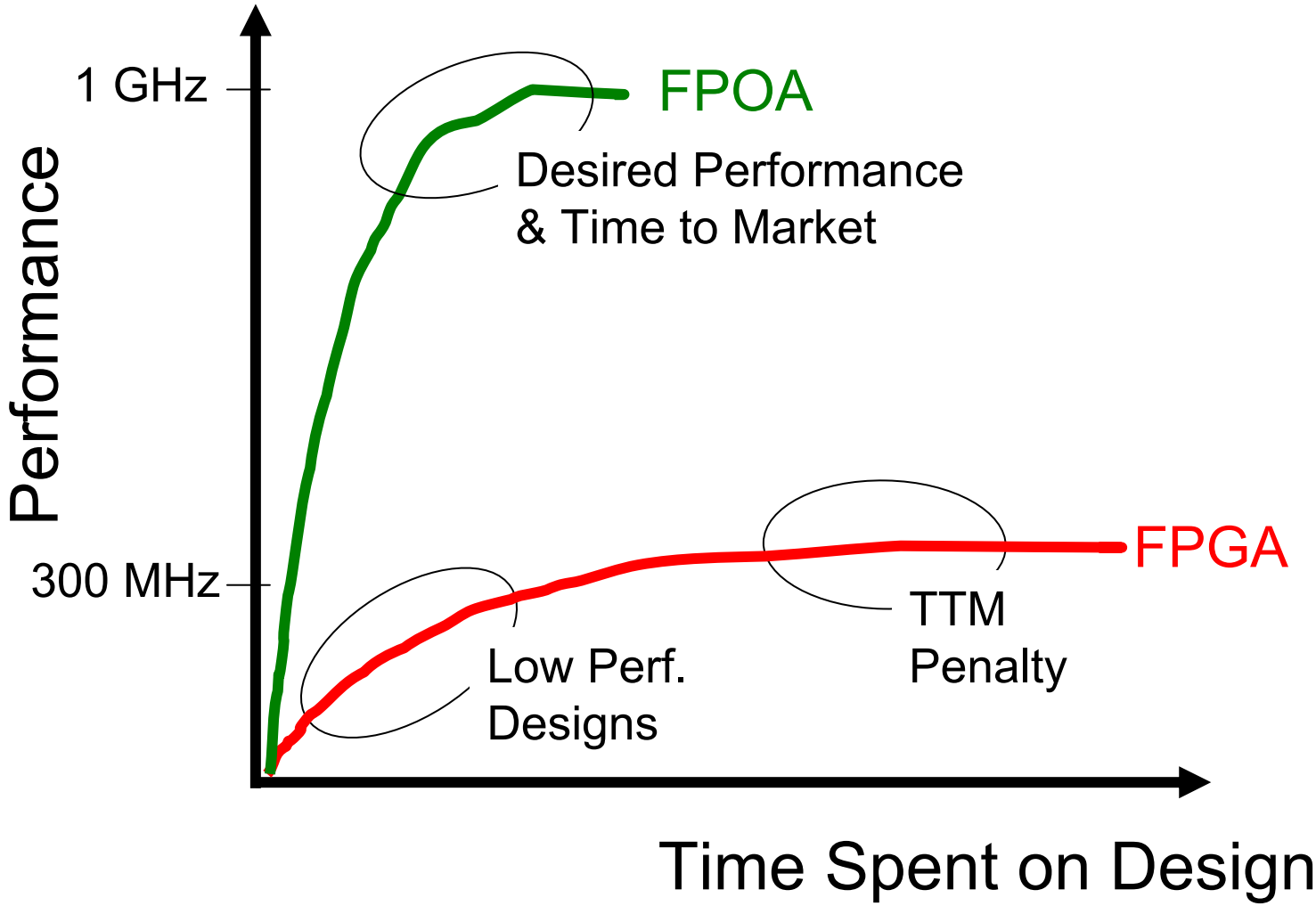
EMEA Field Applications Engineer

Oct 2007

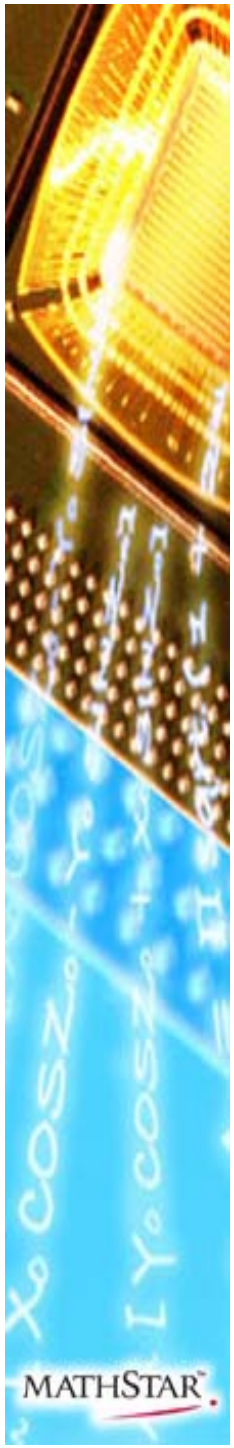
MATHSTAR™



The FPOA Solution



Assumes “apples-to-apples” application comparison –
Same density, same requirements, etc.



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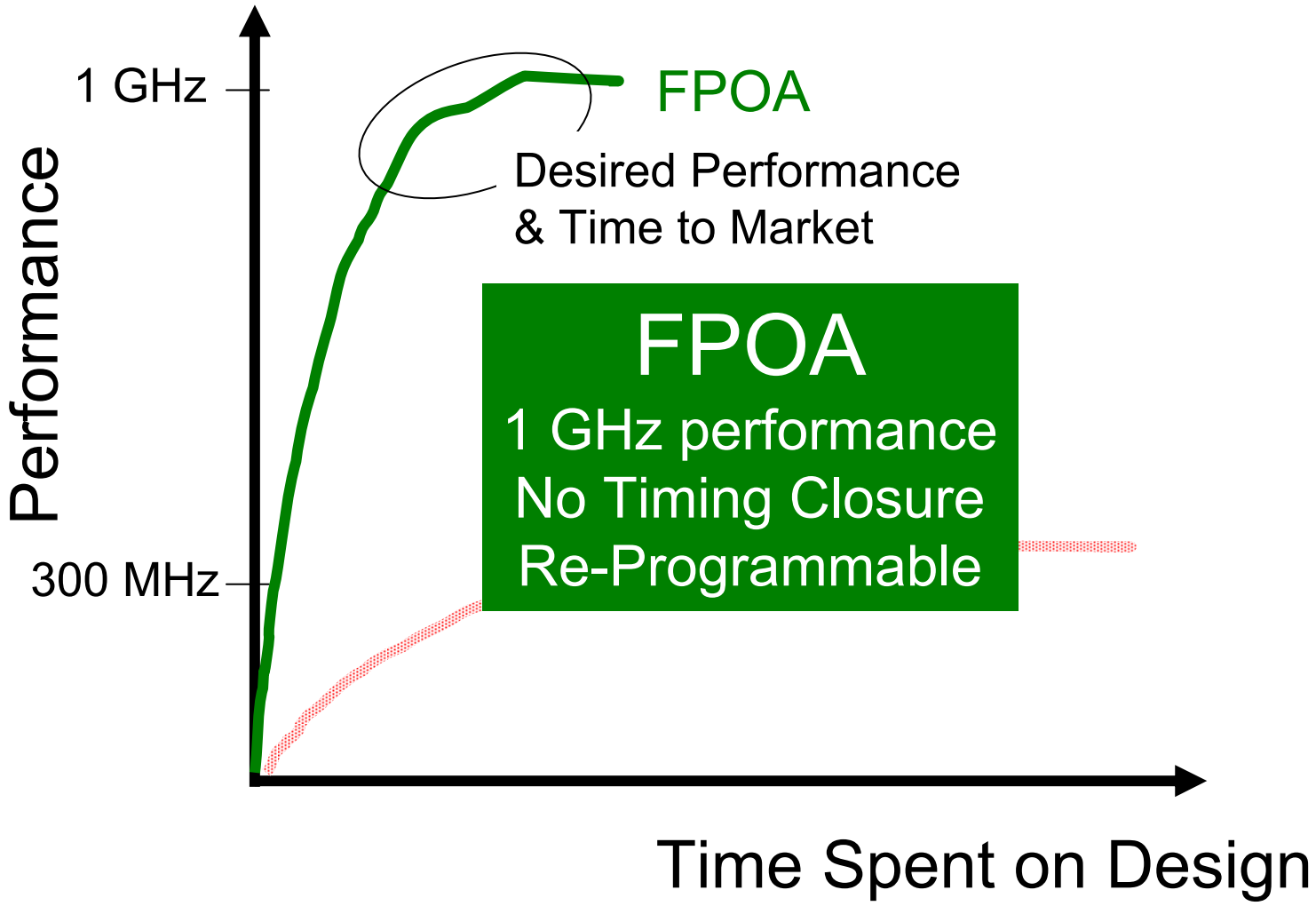

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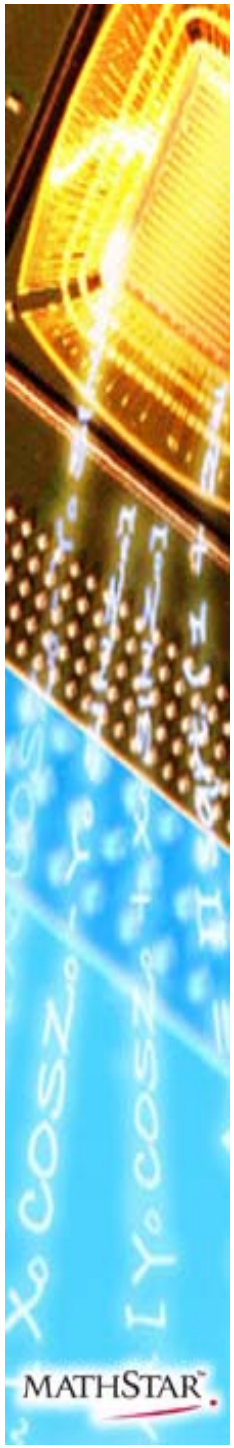


Arrix Family of FPOAs Out-perform FPGAs & DSPs

Parallel Processing Capability

Clock Rate

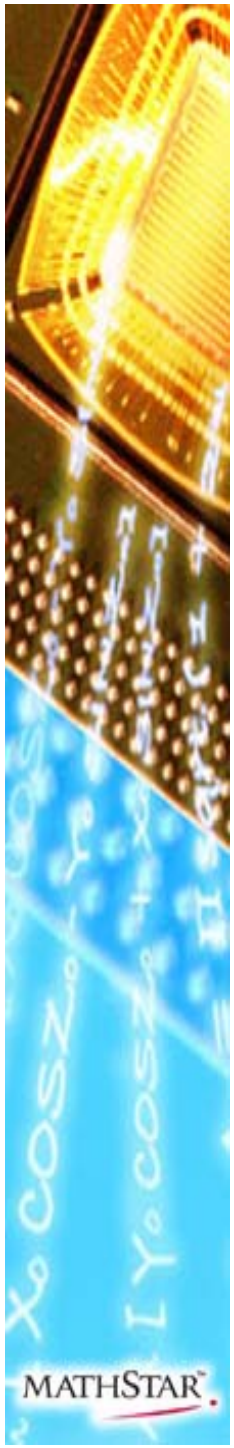
FPGAs

Many Parallel Resources
Slow Clock Speed
Requires Timing Closure

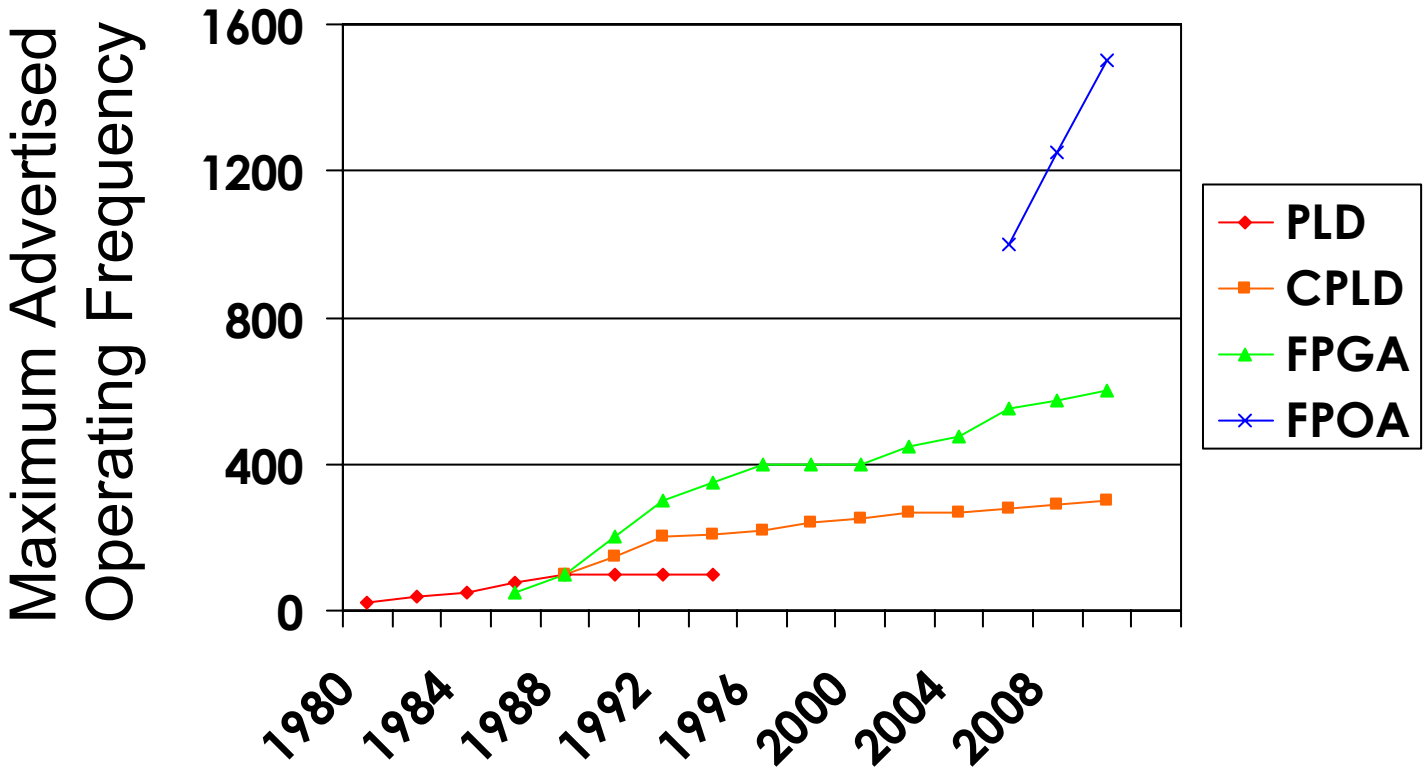
DSPs

Few Parallel Resources
Fast Clock Speed
No Visibility into Timing

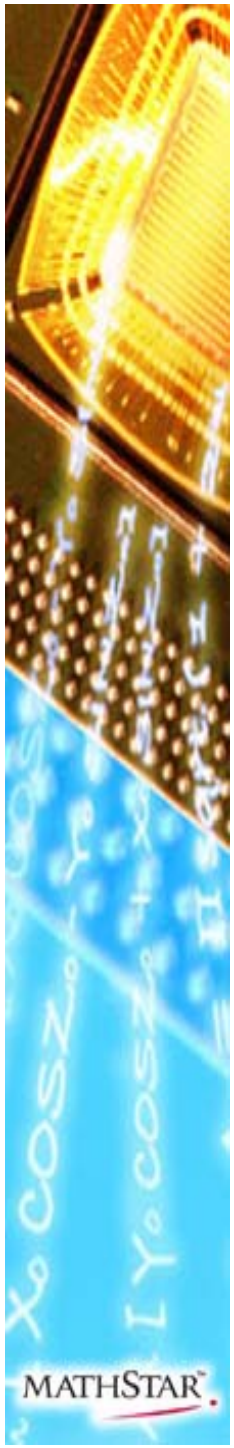
400 Parallel Resources
1 GHz Clock Speed
Timing Closure not Required



FPOA Architecture
Scaleable Operating Frequency



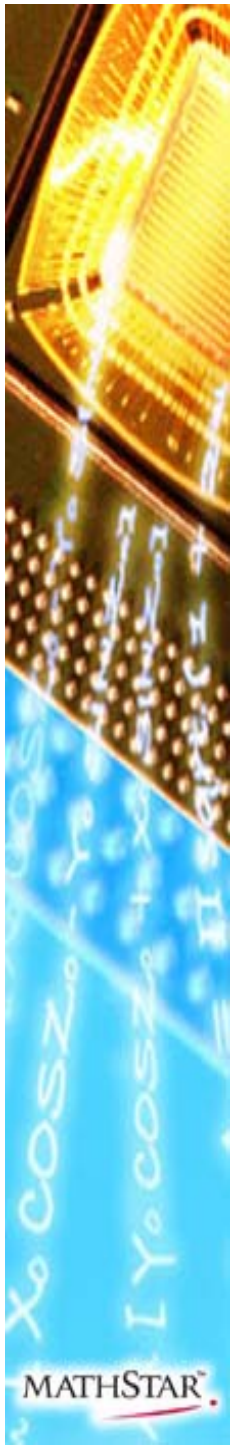
FPGA, CPLD, PLD cites maximum advertised frequency
FPOA cites actual clock rates
All historical and forecasted numbers are estimates of MathStar, Inc.



FPOA Value Proposition

- 1 GHz “ASIC-like” Performance → Up to 4x FPGA performance
- Customer Re-programmable Device → Fast TMM, No NRE
- Application support → Quick Start with Libraries of IP Cores
- Industry-Recognized Design Flow → Reduced design Complexity

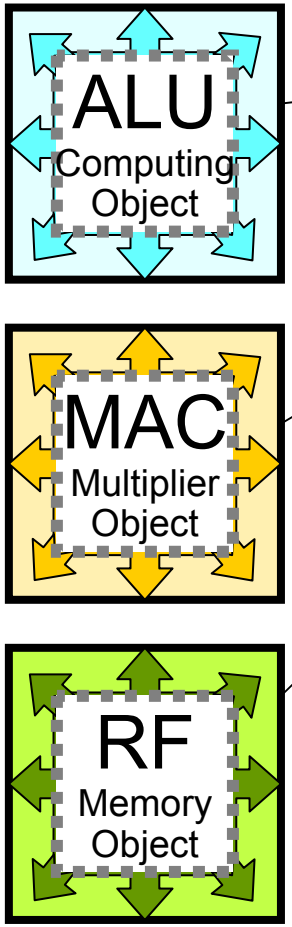
FPOA Architecture



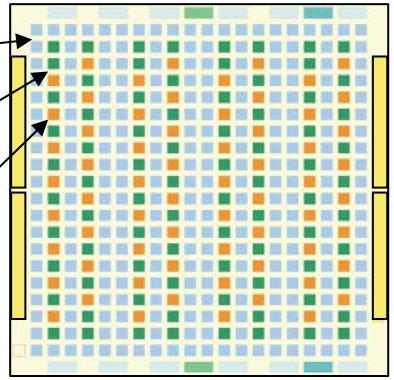
What is an FPOA?

Silicon Objects™

Building Blocks



1 GHz Object Array



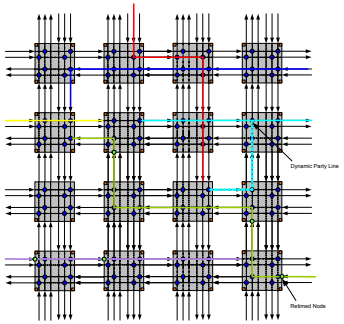
Object Architecture

- Object size identical
- Same inter-object communication
- All synchronized at 1GHz clock

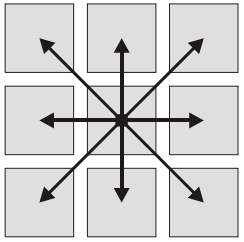
Objects ‘snap’ together by abutment

- Enables 1 GHz performance
- Manageable design with hundreds of objects –vs- millions of gates

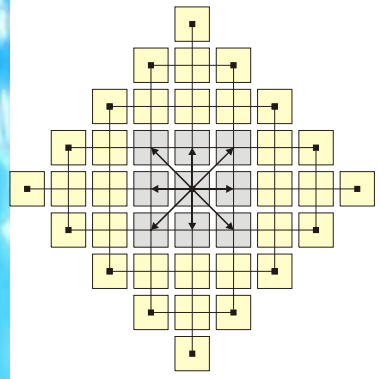
Two Layer Interconnect



- 21-Bit Interconnect Lanes
  - 16 data bits,
  - 1 valid bit,
  - 4 control bits



- Nearest Neighbor Routes
  - 8 Per Object
  - Range of 1 Object (N/E/S/W, diagonals) in one clock cycle



- Party Line Routes
  - 10 Per Object
  - Range of up to 4 Objects away in one clock cycle
  - Ability to add clocks for data alignment
  - Ability to add clocks to cross entire chip

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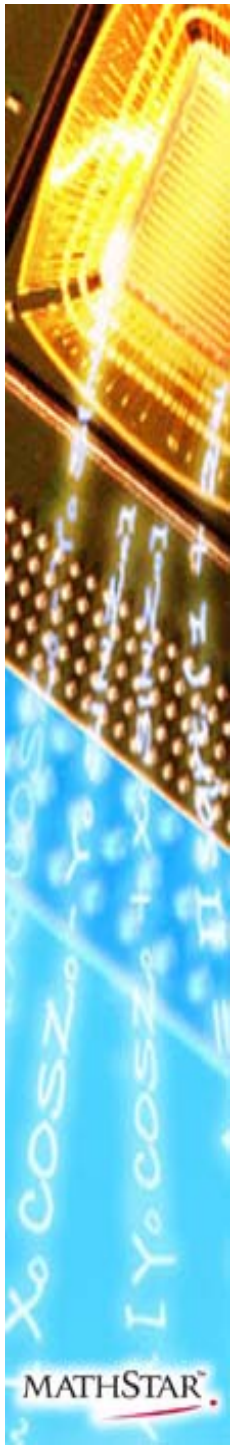
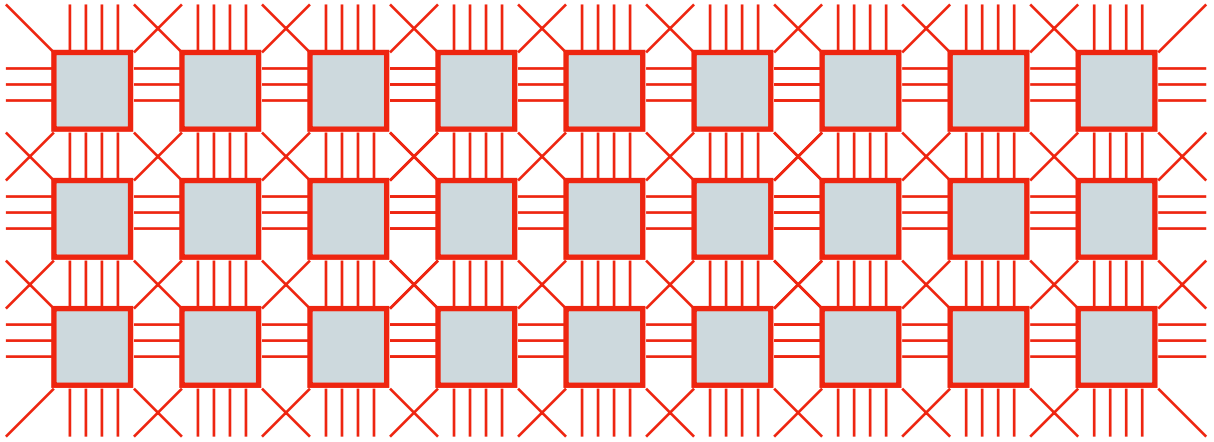
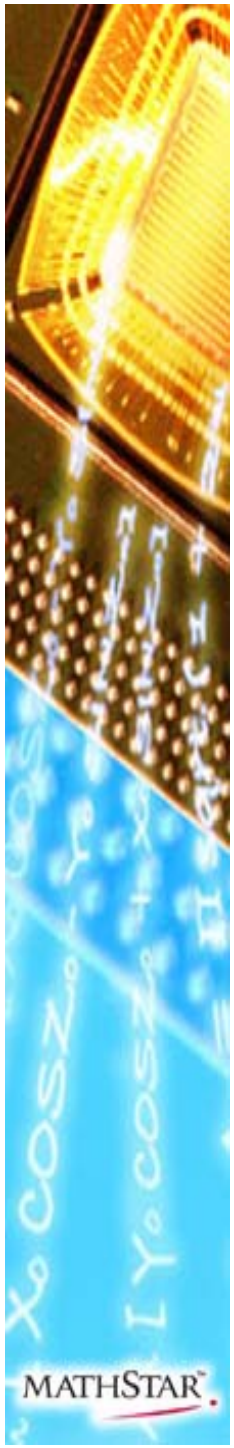


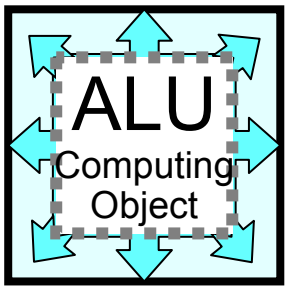
Generous Interconnect Resources Ensures Successful Design Porting



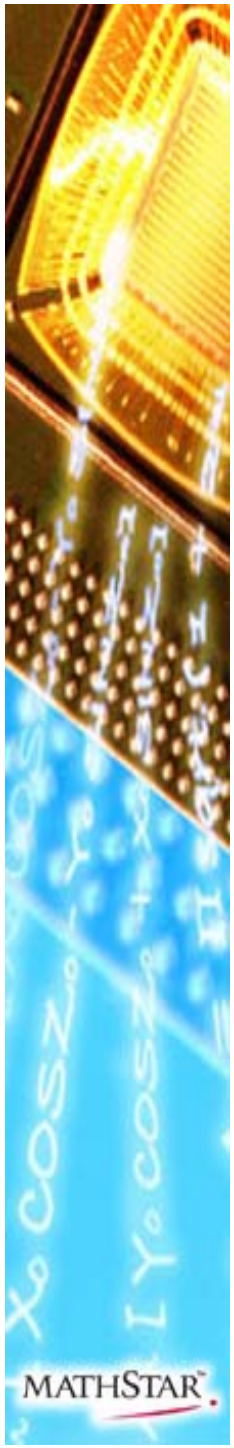
- 18 connections to each silicon object
  - 8 Nearest Neighbor Links
    - Full Duplex links
  - 10 Party Line Links
    - (3 North, 3 South, 2 East, 2 West)
- Each connection is 21 bits, 1 GHz



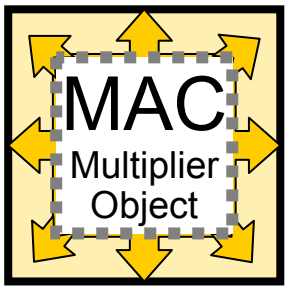
ALU / TF Objects



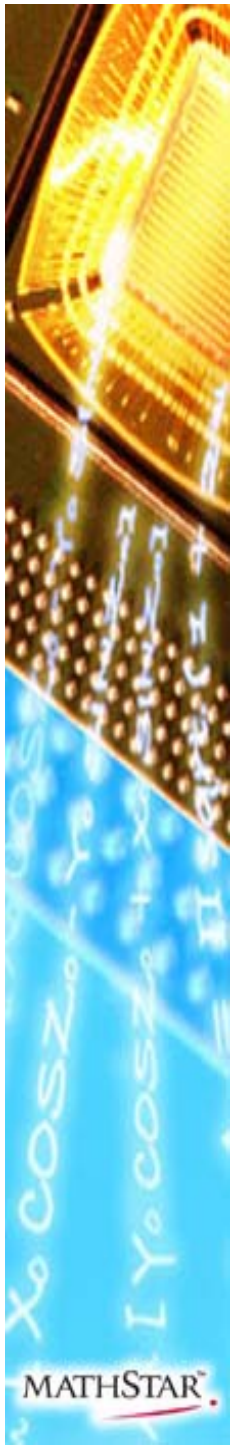
- ALU
  - 40+ ALU Instructions
    - 16-bit add/sub, shift/rot, AND/OR/XOR, MOV
    - Cascade larger words via status bit (SB)
  - 8 configured instructions per object
  - 1 of 9 outputs or broadcast
  - 4-way branch, conditional exec/bypass
    - Configurable to follow C/V/SB/Carry bits
- Truth Function (TF) generates 4 C bits
  - Implement control functions
  - Input 4 C/V/SB/Carry bits per output C bit
  - Arbitrary functions via 4:1 lookup tables
  - Cascade large control expressions across multiple objects



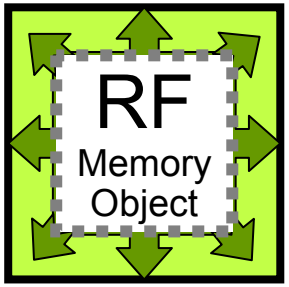
MAC Object



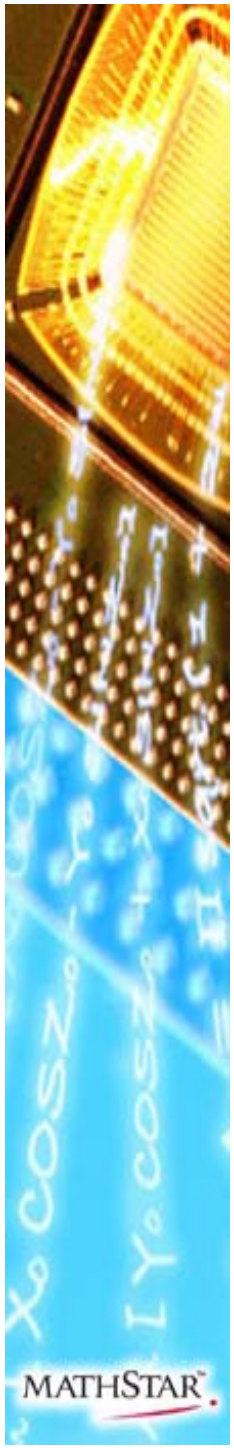
- Fixed Point Multiply-Accumulator
  - 1 GHz 16x16 Multiplier
    - 2 Clock Latency (Fully Pipelined)
  - 1 GHz 40-bit Single Cycle Accumulator
    - 1 Clock Latency (Non-Pipelined)
  - Fixed Point Formats:
    - Integer or Fractional Q15 (15 bits right of decimal)
    - IEEE Saturation Enable
    - Rounding Enable (add 0x8000 to 32 bit result)
- Two MAC's for Complex Operation
  - 2 Cycle Bandwidth, 3 Cycle Latency
  - Accumulate Results in MAC No external ALU Required
  - Cascade MACs for 32-bit operation



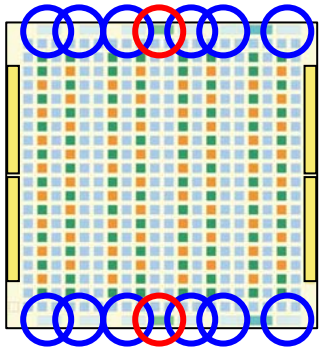
Register File Object



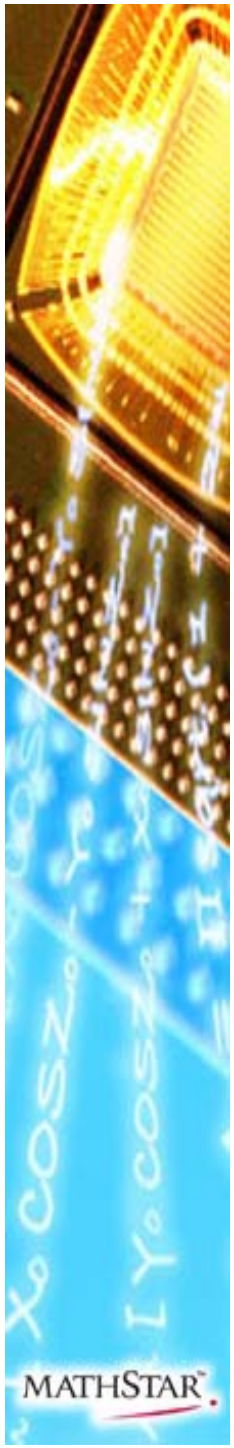
- Register File - Fast, Small Memory
  - 32) 40-bit or 64) 20-bit words
  - Dual-Port RAM
  - FIFO
  - Auto-increment Address for Pattern Generation



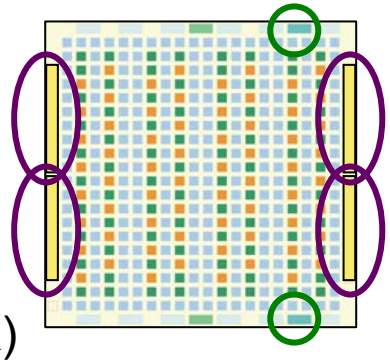
Internal & External Memory



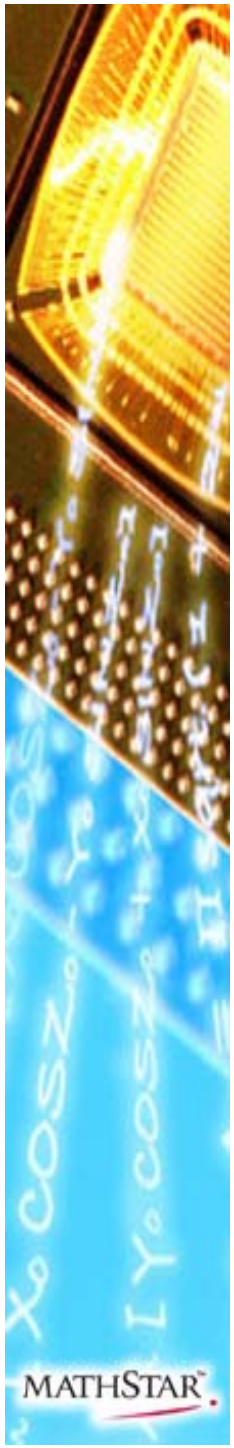
- IRAM – Internal Block SRAM
  - 12 Banks, 2K x 76b each
  - Operates at core clock
  - 228 KB total
  - 4.75 GB/s data throughput per bank
- XRAM – External Memory Controllers
  - 2 Independent XRAM Controllers
  - 36 Bits Wide, 266 MHz DDR, RLDRAM II
  - 288 MB addressable space
  - 2.3 GB/s data throughput
  - Single 8-entry Command and Data FIFO's

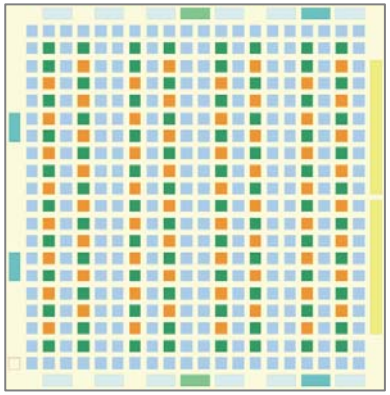


Data and Signal I/O



- High Speed I/O
  - 2 Independent LVDS Interfaces
  - Each interface is 32 bits
    - Separate 16 bit Transmit (TX) & Receive (RX) interfaces
  - Two Modes of Operation
    - 8/16 bit LVDS, 500 MHz DDR
    - 8/16 bit LVDS, 640 MHz SDR
  - 32 Gbps data transfer rate per RX/TX pair
- General Purpose I/O
  - 96 pins
  - Up to 100 MHz LVCMOS
  - Flexible clocking: internal, external, asynchronous





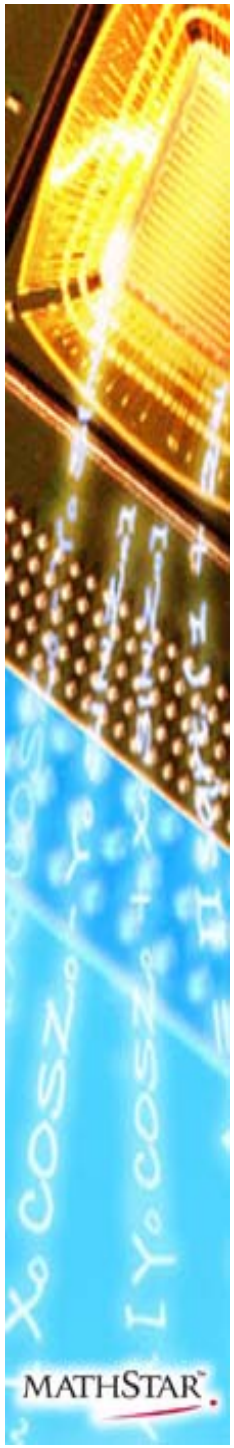
Field Programmable Object Array Comparison

2-4x FPGA Performance

Technology	FPGA	FPOA
Advertised Performance	500MHz	1 GHz
Performance after Timing Closure	256MHz *	1 GHz
Full Suite of Design Tools	Yes	Yes
Programming Model	Gate-Level	Object-Level

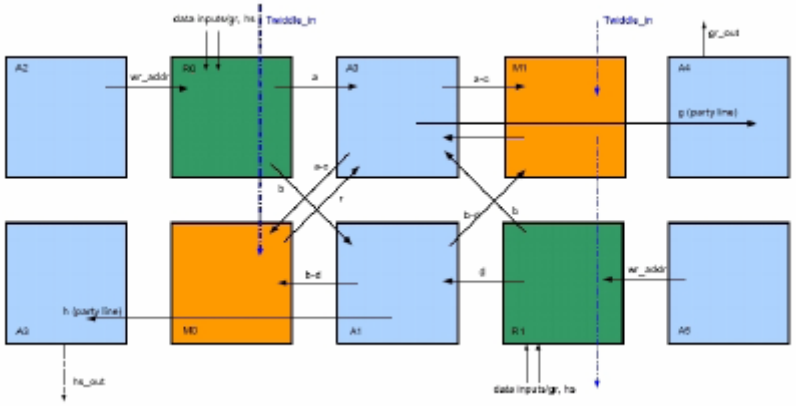
** 1K FFT Virtex4-11*

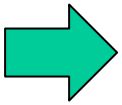
Performance Benchmarks



DSP Processing Example

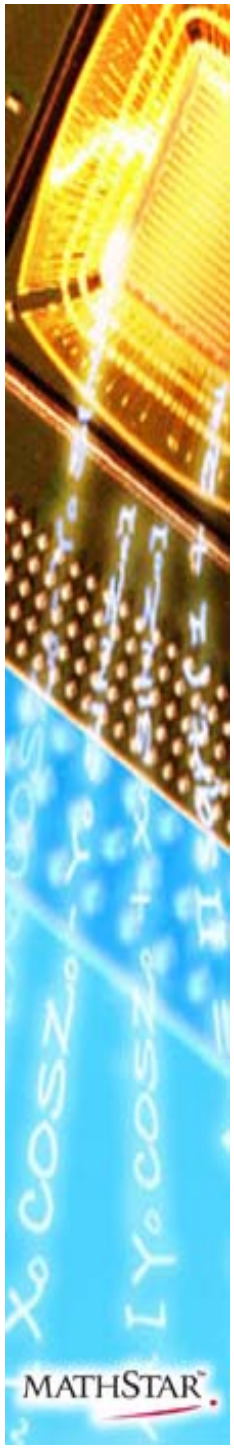
FFT – Radix 2 Butterfly





Points	Sample Rate	Throughput	CH	ALU (256)	RF (80)	MAC (64)	Memory
64	2 GSPS	2 samples/cycle	2	76	24	24	2 IRAM *
256	2 GSPS	2samples/cycle	2	122	32	32	4 IRAM *
1K	2 GSPS	2 samples/cycle	2	192	40	40	12 IRAM *
4K	1 GSPS	1 sample/cycle	1	184	24	24	9 IRAM
8K	500 MSPS	0.5 sample/cycle	1	200	36	26	12 IRAM
16K	500 MSPS	0.5 sample/cycle	1	216	48	28	12 IRAM

* Assuming no I/O limitation and uses two copies of resources to double the sample rate across two channels



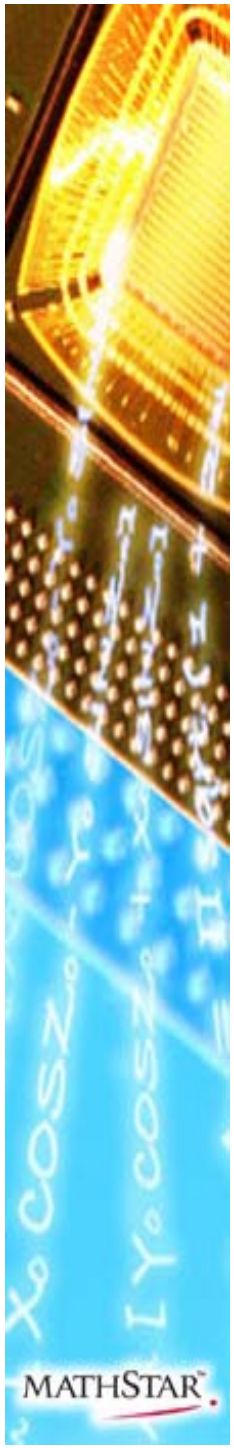
FIR Performance

Taps	Sample Rate	Number of Channels	ALU (256)	RF (80)	MAC (64)	Memory
8	8 GSPS	8	140	32	64	8 IRAM *
16	4 GSPS	4	114	32	64	4 IRAM *
32	2 GSPS	2	112	32	64	2 IRAM
64	1 GSPS	1	116	32	64	1 IRAM
128	500 MSPS	1	125	33	64	1 IRAM
256	250 MSPS	1	142	34	64	1 IRAM
512	125 MSPS	1	168	40	64	1 IRAM

* Assuming no I/O limitation and uses multiple copies of resources

- FIR implementations do not consume many ALU and RF resources
- Ample room for additional signal processing functions

Example Applications



Professional Video Library

for the Arrix Family of FPOAs

- MathStar's Professional Video Library of IP Cores
  - MPEG2 Multi-Stream Decoder Core
  - MPEG2 Encoder Core
  - JPEG2000 Encoder Core
  - H.264 Encoder Core
  - H.264 Decoder Core

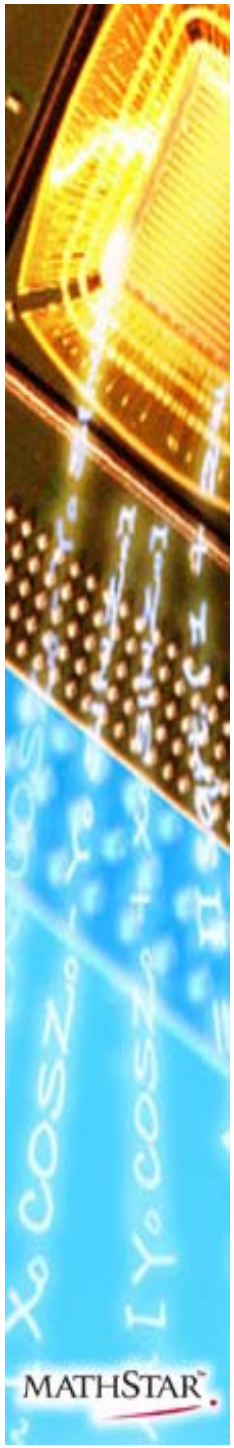
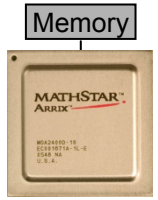
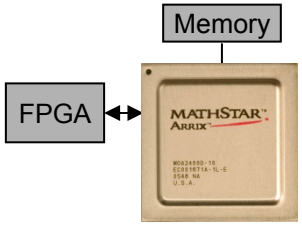


Image Processing and Video Platforms

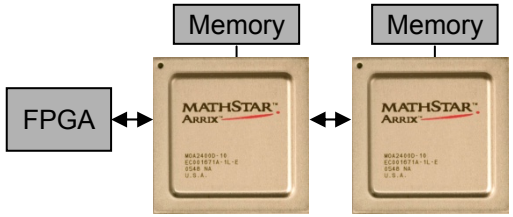
Sobel Edge Detection
Flat Field Error Correction
Motion Estimation
…

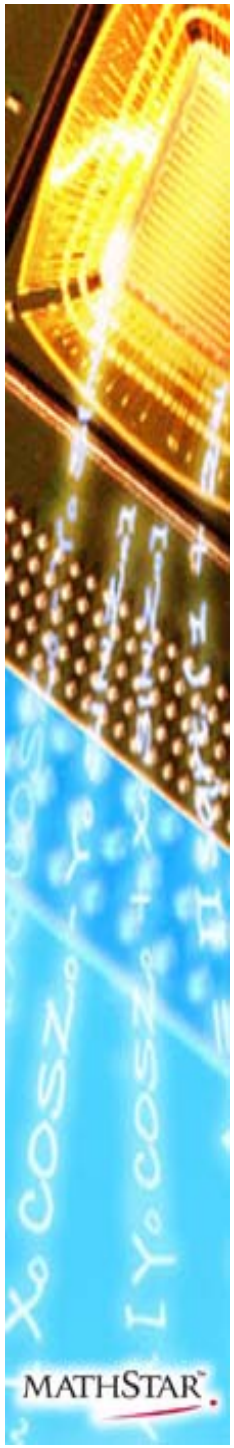


JPEG2000 “HD” Encode / Decode
MPEG2 HD Encode / Decode
…



H.264 HD Encode / Decode
Military Applications
CT Filtered Backprojection
…

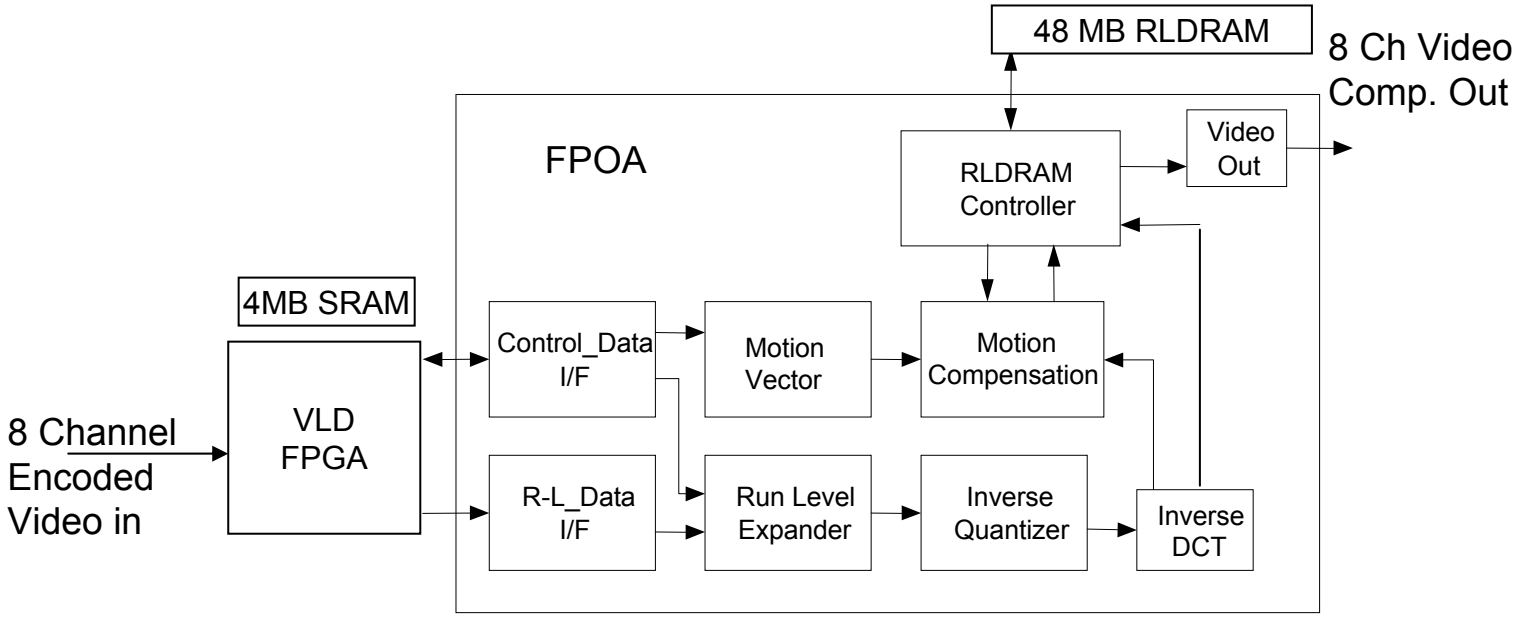




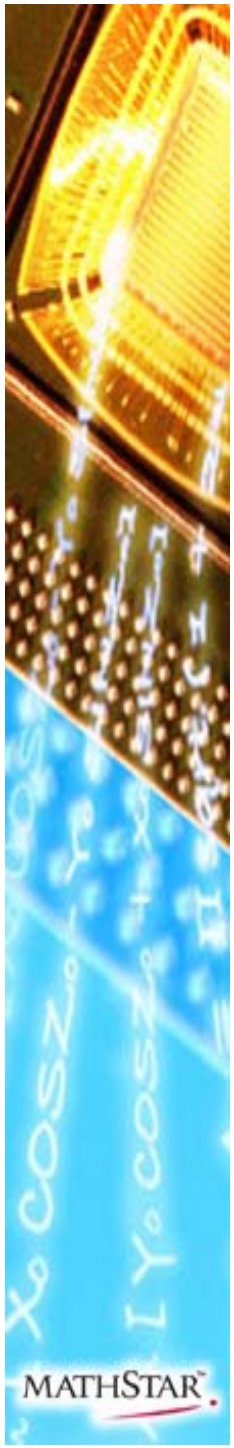
MPEG2 Multi-Stream Decoder Specification

Feature	Specification	Notes
Target Device	MOA2400D-08	800 MHz Arrix FPOA
Input SD Streams	8 SD or 1 HD	8 SD 4:2:0, 8 SD 4:2:2
Profiles @ Levels Supported	MP @ ML, MP @ HL 422P @ ML, 422P @ HL	SD and HD
Input Color Format	4:2:2 or 4:2:0, 8 bits Encoded bit stream	4:2:2 and 4:2:0 channels can co-exist
Output Color Format	4:2:2, 8 bits	
Frame Accurate Timing	Yes	Does not maintain a display clock
Input Interface	960J Host Bus	32 bit, 33/66 MHz
Output Interface	16 bit LVDS, 150 MHz DDR	
VLD Implementation	VHDL Design suitable for Lattice ECP-50 or Spartan3 FPGA	May be integrated into existing customer FPGA

MPEG2 Multi-Stream Decoder Block Diagram



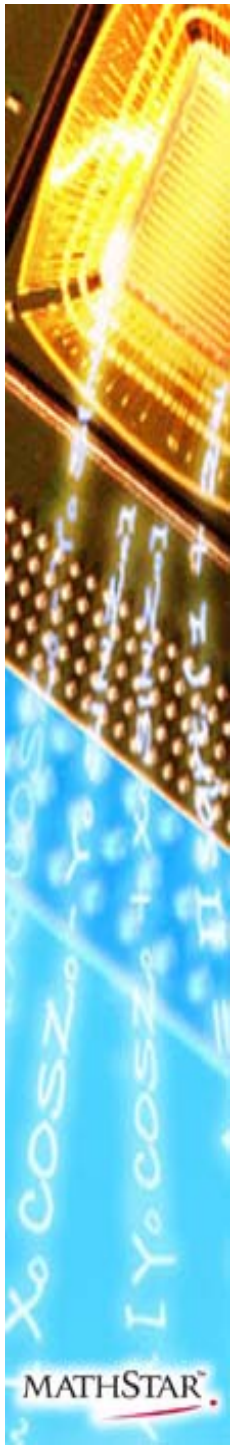
- **FPOA Functionality:**
  - RLE expander, IQ, IDCT, Motion Compensation
  - XRAM Controller: manages reference frame fetch, saves reconstructed frames, and retrieves output video
  - Output Interface sends output video in 4:2:2 format
  - Rebuilds motion vectors
  - Decodes R-L pairs



FPOA Resource Allocation

Module	ALU	RF	MAC	IRAM
Control_Data I/F	5	1	1	
R-L Data I/F	20	8		2
Motion Vector	8	2	2	
Motion Compensation	60	10	4	
Run Length Expander	15	4		
Inverse Quantization	22	6	2	
Inverse DCT	24	12	6	4
XRAM Controller	17	3		
Video Out	45	6	2	2
Debug Logic	12	4		
Sub total	228	56	17	8
SO total	301			

Note 1: Two copies of IDCT are used to achieve 8-channel SD and are included above



Summary

- The FPOA is the next generation of Programmable Logic
  - Up to 4 times faster than FPGAs
  - Fixed deterministic timing – 1 GHz
  - No timing closure
  - No synthesis required
  - The MOA2400D is in production

Taking Programmable Logic beyond FPGA's!