Hardware – Software Interaction

P1

- Configure the transfer speed to the desired value by writing 0/1/2/3 to the CFG_SPD field of the CTRL register (located at offset 2)
- While there is more data {
  - Write one byte data to the TX register (offset 0)
  - Write 1 to the STRT_TX field of the CTRL register (offset 2)
  - Loop and read the TX_CMP field of the STS register (offset 3) until it becomes 1
  - Loop and read the RX_AVL field of the STS register (offset 3) until it becomes 1
  - Read one byte data from the RX register (offset 1)

}

P2

- Configure the transfer speed to the desired value by writing 0/1/2/3 to the CFG_SPD field of the CTRL register (offset 2)
- While there is more data {
  - Loop and read the RX_AVL field of the STS register (offset 3) until it becomes 1
  - Read one byte data from the RX register (offset 1)
  - Write one byte data to the TX register (offset 0)
  - Write 1 to the STRT_TX field of the CTRL register (offset 0)
  - Loop and read the TX_CMP field of the STS register (offset 3) until it becomes 1

}

Hardware-Software Interaction – uses registers

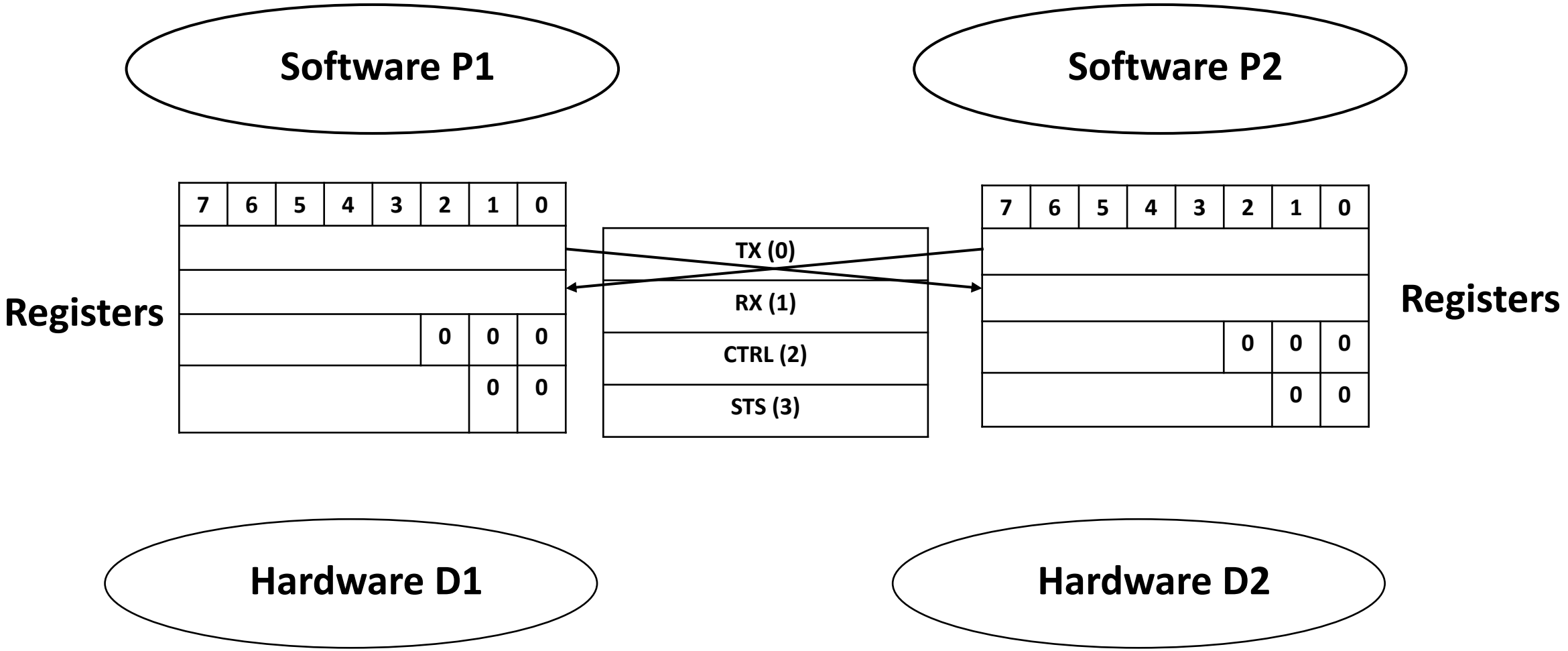
Software

	7	6	5	4	3	2	1	0
TX (0)								
RX(1)								
CTRL(2)						CFG_SPD	CFG_SPD	TX_STRT
STS(3)							RX_AVL	TX_CMP

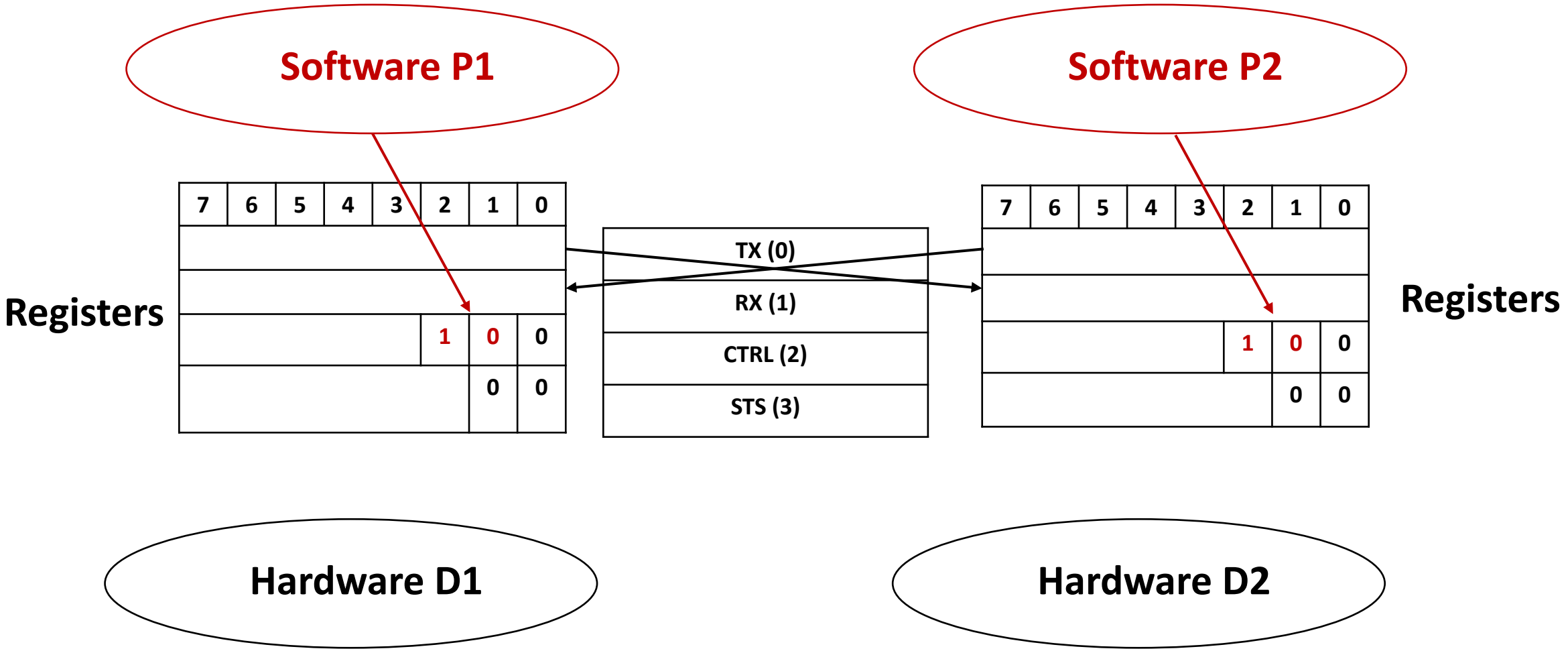
Registers

Hardware – Electronic circuitry for Tx, Rx, Cfg etc

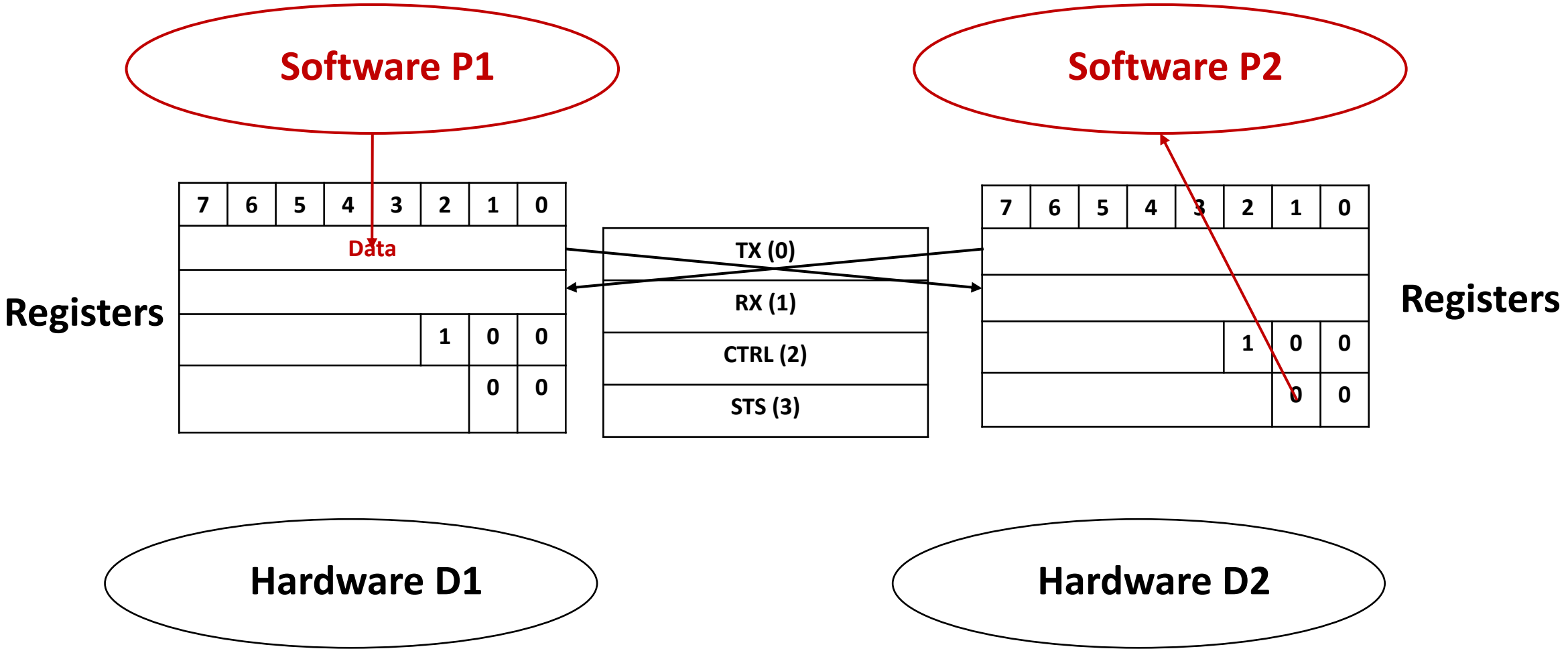
Hardware-Software Interaction



Configure speed to 9600 on both devices - Software

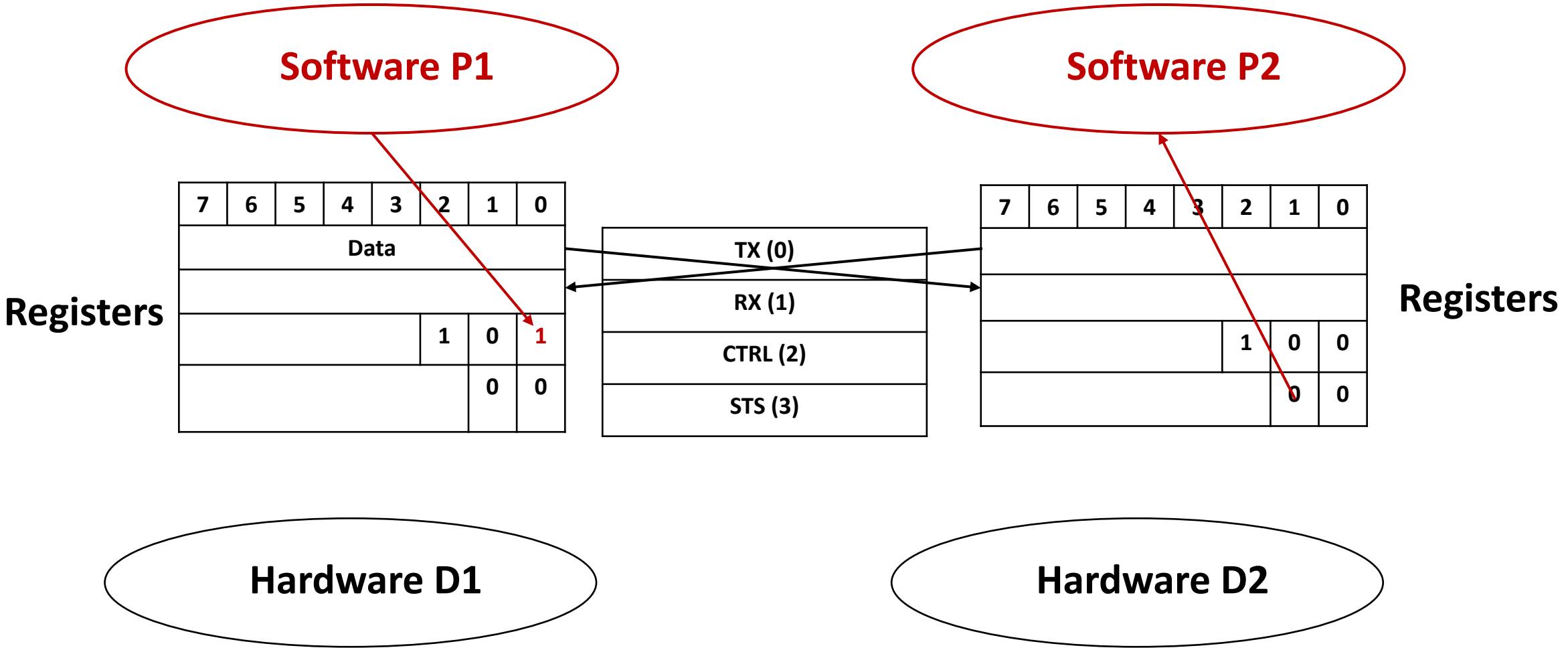


D1 -Tx data - Software writes data into Tx Reg
D2 – Wait to receive data



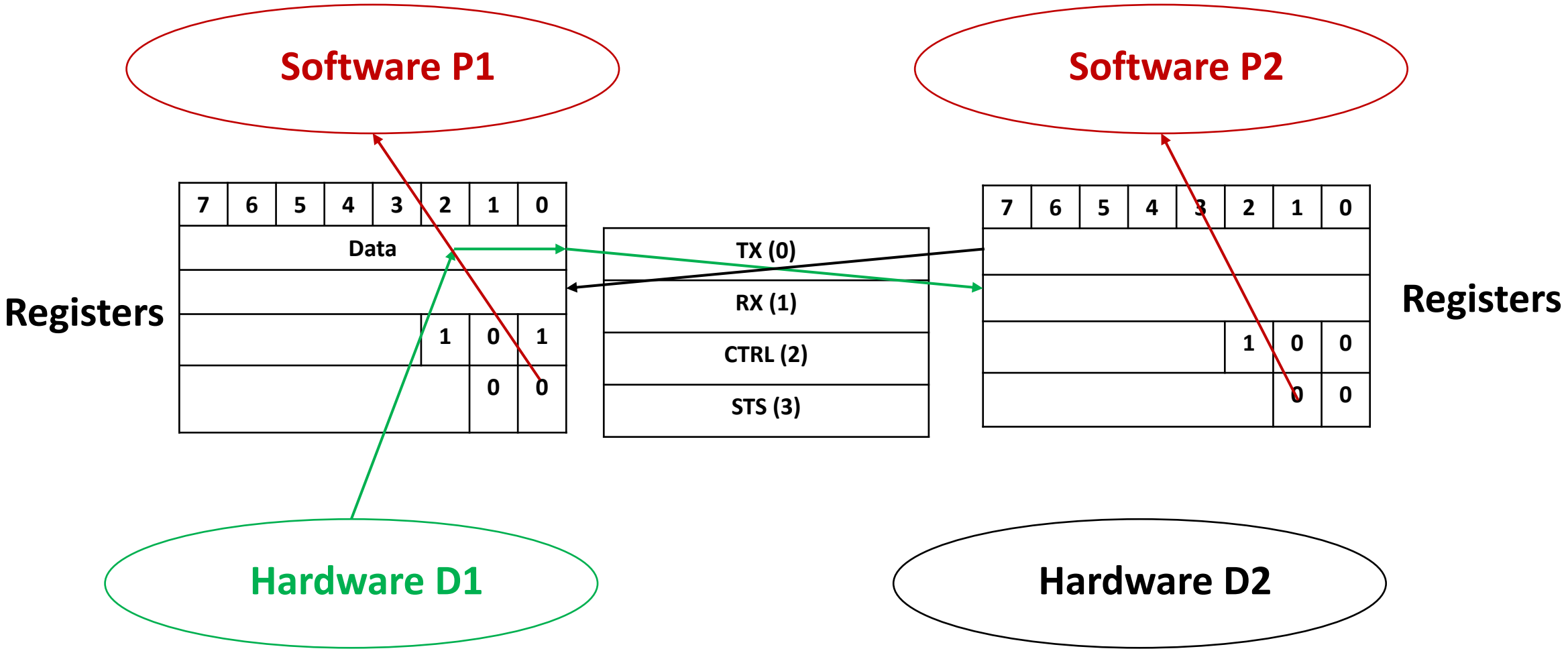
D1 – start data transmit - Software writes 1 into the TX_STRT field of CTRL register

D2 – Wait to receive data

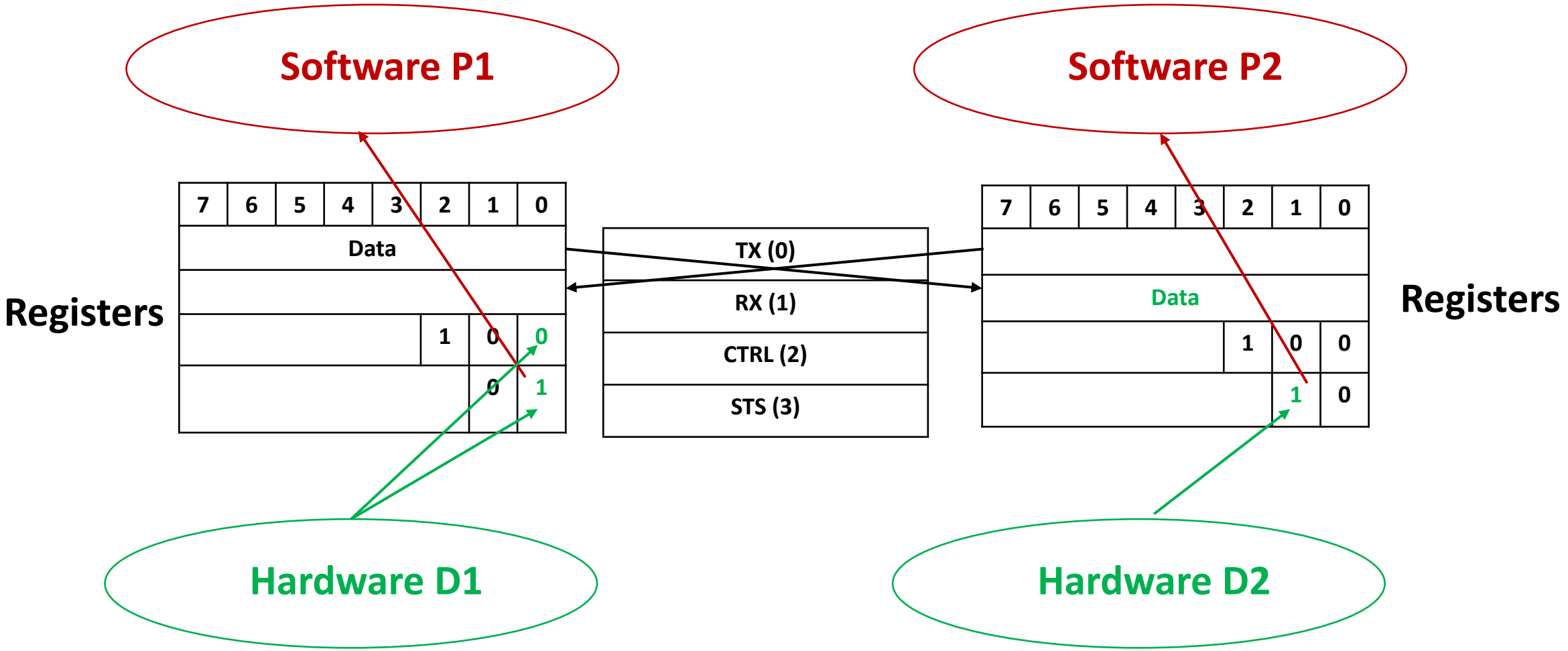


D1 - Tx data – Hardware starts to transmit data via Tx pin into wire connected to Tx pin. P1 waits for Tx completion

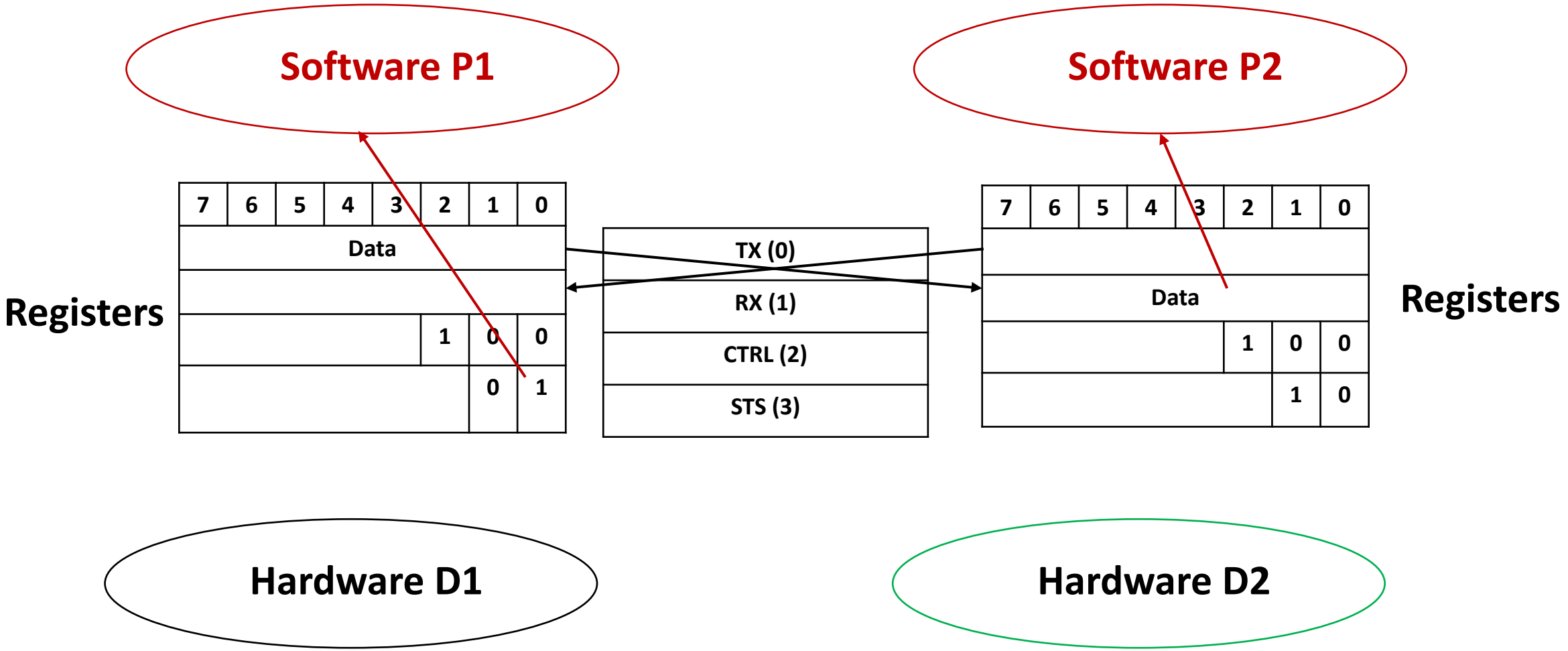
D2 – Wait to receive data



D1 - Tx transfer complete – hardware sets TX_CMP bit in CTRL register and resets TX_STRT of CTRL register. D2 – data received in Rx register and hardware sets RX_AVL bit in the STS register



D1 - Tx transfer complete – software detects Tx is complete since bit TX_CMP in CTRL register is 1. D2 – Software finds RX_AVL bit in the STS register is 1 and proceeds to read data from Rx register



D1 - Tx transfer complete – reading of TX_CMP in CTRL register resets the bit. D2 – Reading of RX_AVL bit in the STS register resets the bit