QP CODE: 20101288

20101288

Reg No : .....

Name : .....

B.Sc./BCA DEGREE (CBCS) EXAMINATION, NOVEMBER 2020

Second Semester

Core Course - CS2CRT05 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Common for B.Sc Computer Science Model III,B.Sc Information Technology Model III,Bachelor of Computer Application)

2017 ADMISSION ONWARDS

5F91E0C8

Time: 3 Hours Max. Marks : 80

Part A

Answer any ten questions.

Each question carries 2 marks.

1. What is an instruction register?
2. Which are the different fields in Instruction Formats?
3. What is byte addressability?
4. What is a bus?
5. What is the purpose of using status registers?
6. Write the classification of computer instructions.
7. What is the use of condition code bits?
8. Differentiate between RAM and ROM
9. Compare Static and dynamic RAM
10. What are the features of PROM?
11. What are multiprocessor systems?
12. How the efficiency of a pipeline can be measured?

(10×2=20)

Part B

Answer any six questions.

Each question carries 5 marks.

13. Explain the basic operational concept between processor and memory.

14. How micro processor differentiates between data and instruction?Explain.

15. Explain the use of timing and control signals. Give example.

16. Explain register addressing mode with example

17. Explain memory hierarchy.

18. Distinguish between associative memory and cache memory.

19. What is virtual memory? How is it useful?

20. What is parallel processing?

21. List and explain some techniques to prevent pipeline conflicts.

(6×5=30)

Part C

Answer any two questions.

Each question carries 15 marks.

22. Explain stack organization in detail.

23. Explain and distinguish magnetic storage devices and optical storage devices.

24. Explain Flynn's architectural classification scheme.

25. What is an array processor? Explain with the help of neat diagrams.

(2×15=30)