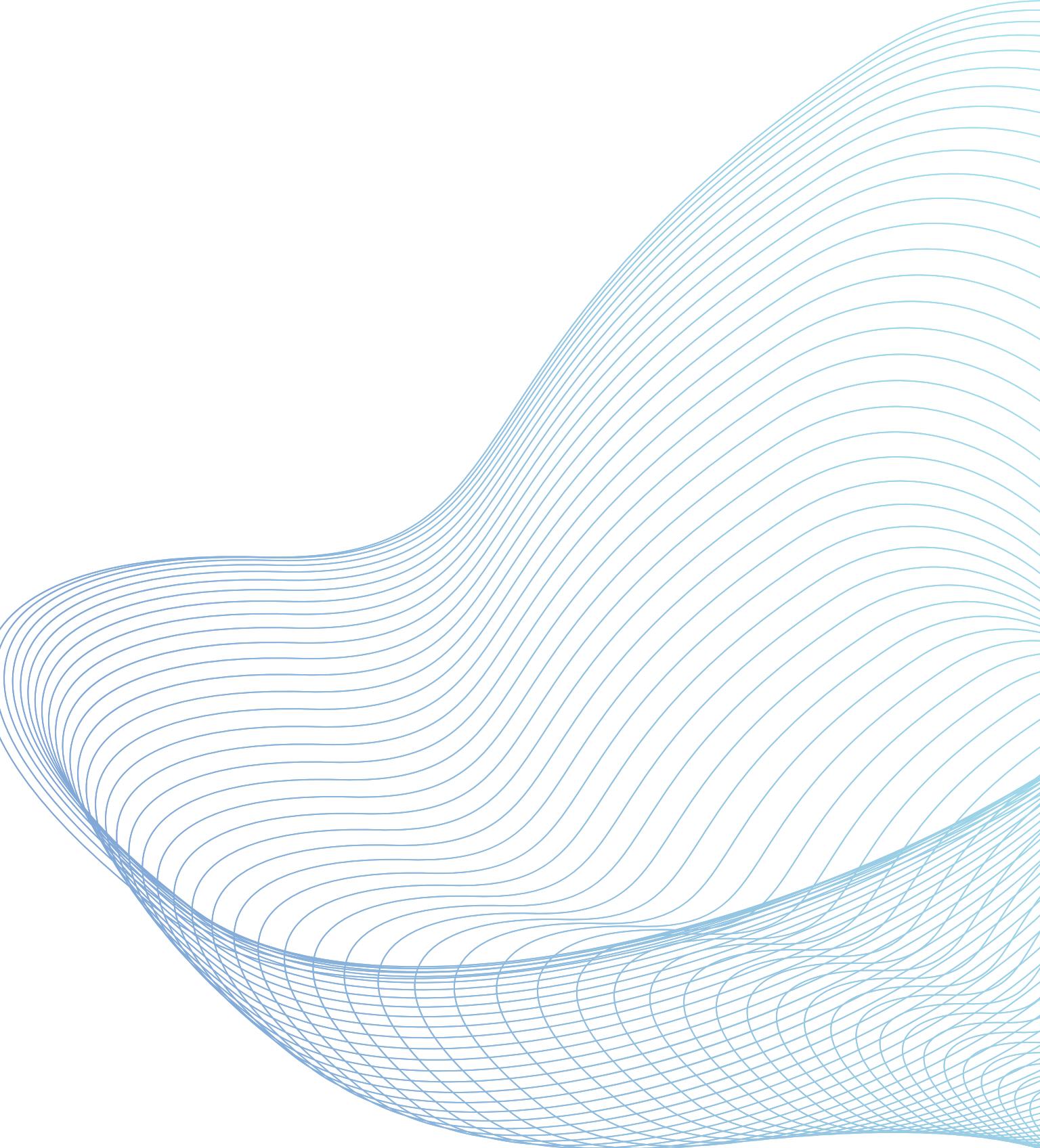


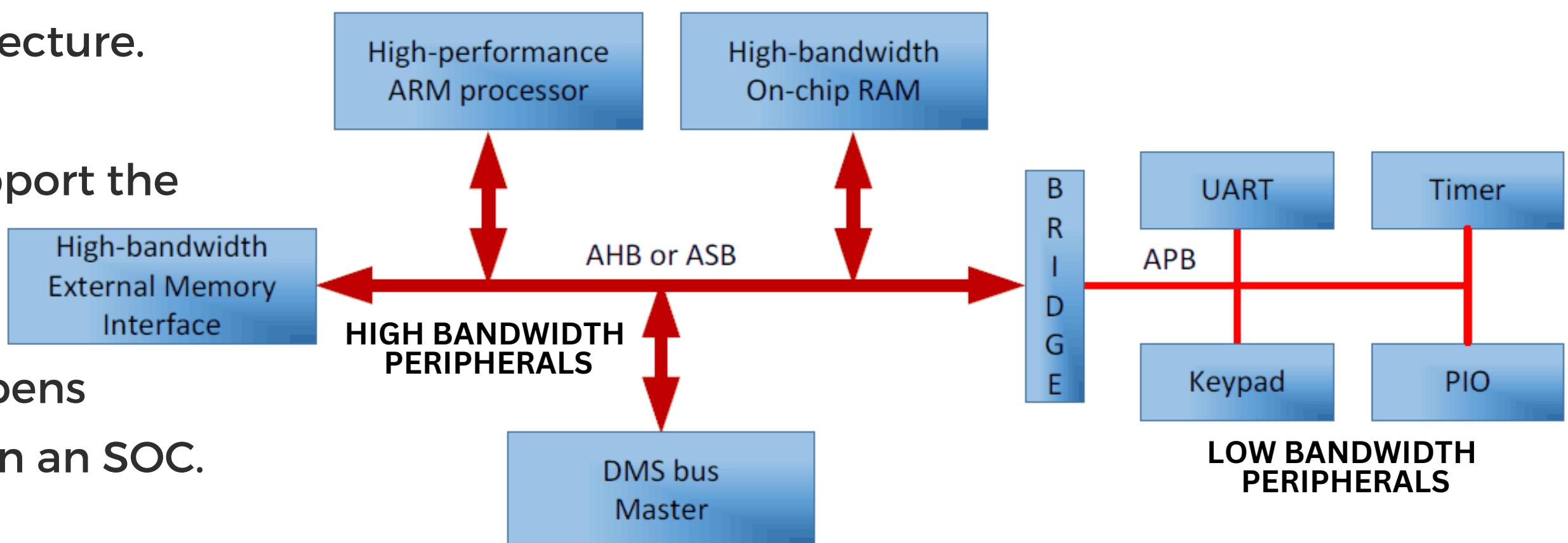
AMBA APB PROTOCOL

Version : 2.0



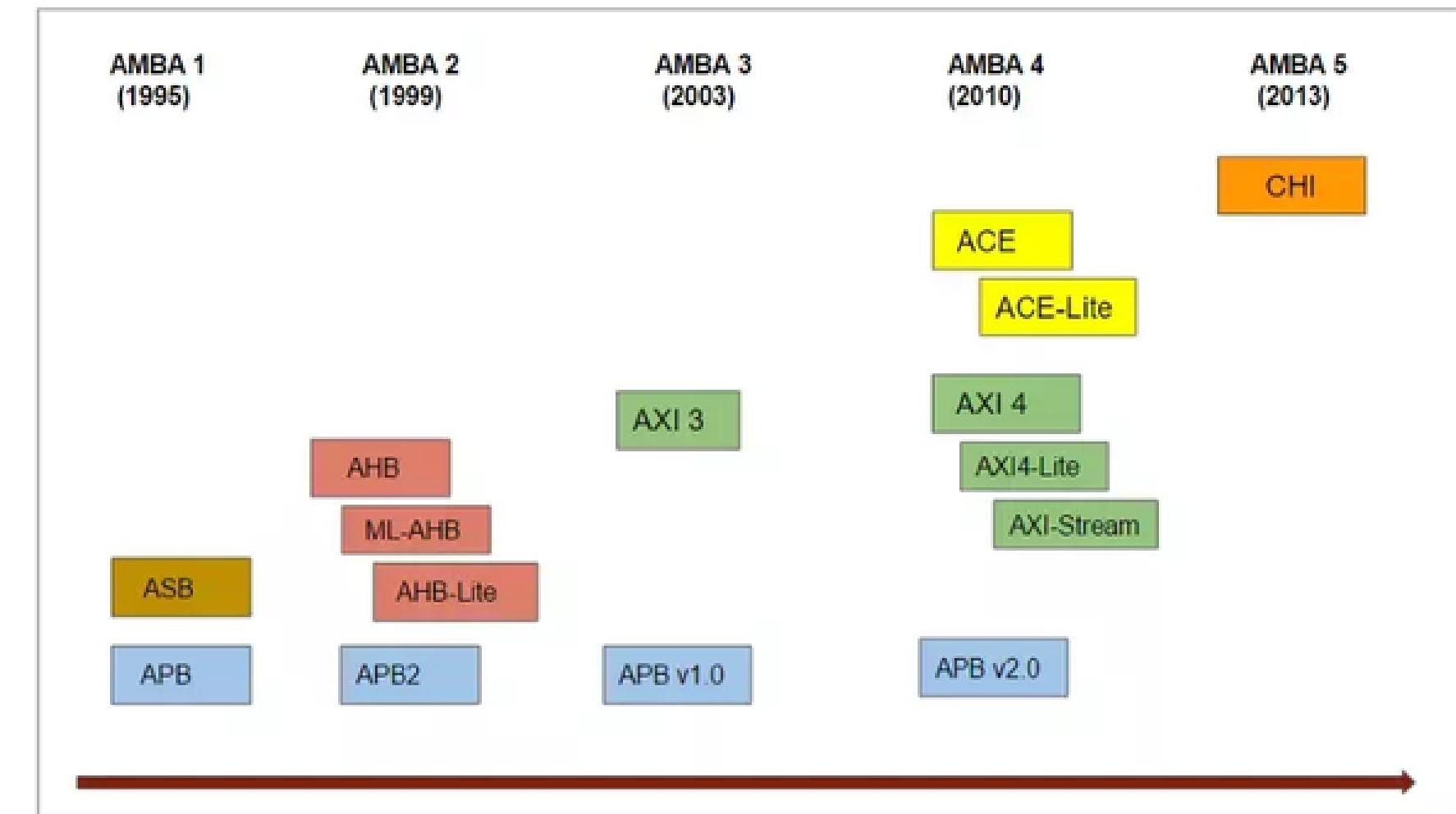
AMBA ARCHITECTURE

- AMBA stands for advanced microcontroller bus architecture.
- Backbone structure to support the communication.
- how communication happens between different blocks in an SOC.



APB PROTOCOL

- It's a synchronous interface, has only 1 clock.
- It is not pipelined.
- Low cost interface optimized for minimal power consumption and reduced interface complexity.
- One transaction takes at least 2 cycles.
- It has a single channel. At a time, we can either read the data or write the data. Cannot perform two operations at a time.



AMBA 2 APB

Defines interface signals, basics read and write transfers, the two APB components master and slave.

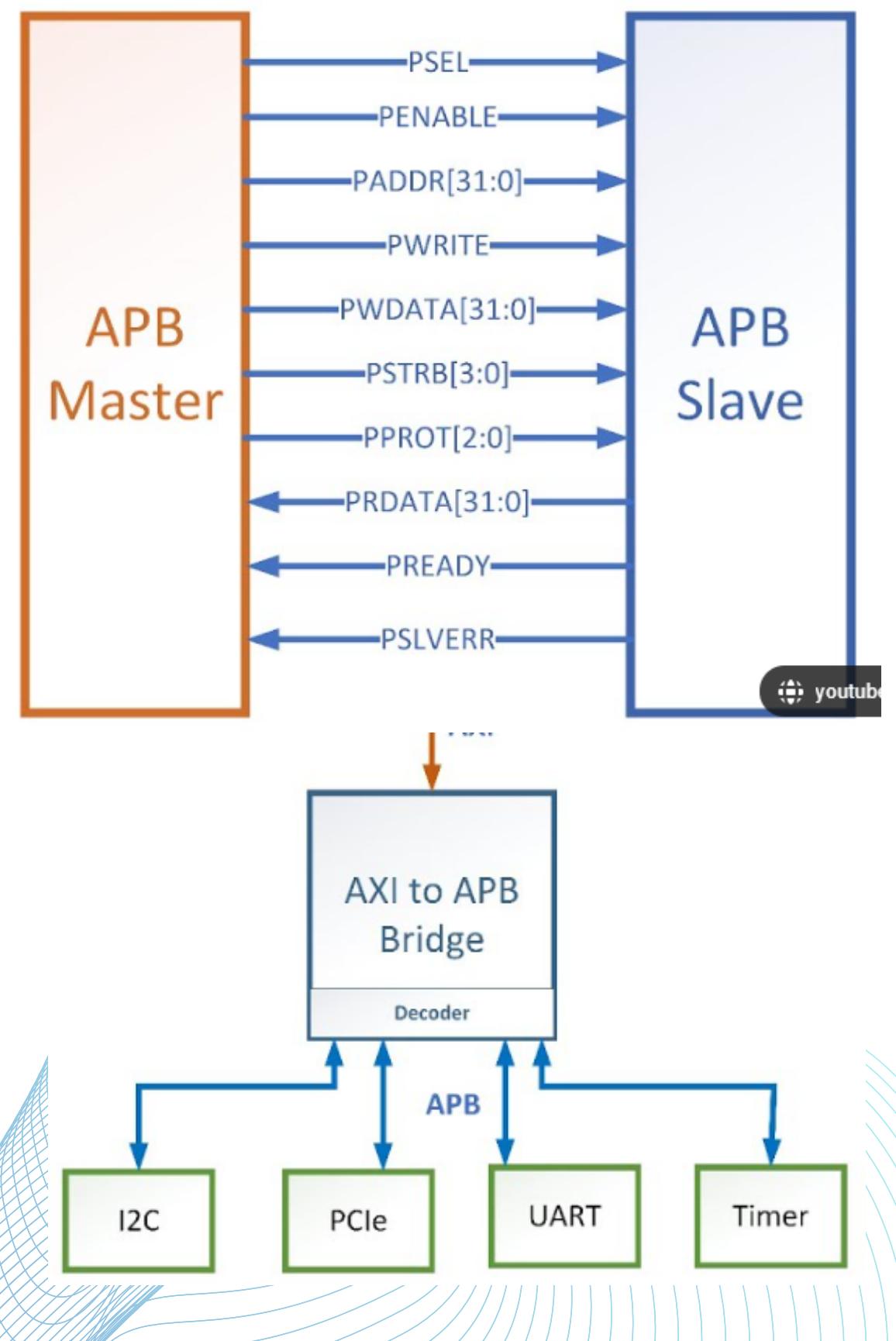
AMBA 3 APB v 1.0

Additional Functionality
Wait states : PREADY signal
Error Reporting: PSLVERR signal

AMBA 4 APB v 2.0

Additional Functionality
Protection : PPROT signal
Sparse Data Transfer: Strobe signal

SIGNALS



Signal	Source	Description
PCLK	Clock source	Clock. The rising edge of PCLK times all transfers on the APB.
PRESETn	System bus equivalent	Reset. The APB reset signal is active LOW. This signal is normally connected directly to the system bus reset signal.
PADDR	APB bridge	Address. This is the APB address bus. It can be up to 32 bits wide and is driven by the peripheral bus bridge unit.
PPROT	APB bridge	Protection type. This signal indicates the normal, privileged, or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
PSELx	APB bridge	Select. The APB bridge unit generates this signal to each peripheral bus slave. It indicates that the slave device is selected and that a data transfer is required. There is a PSELx signal for each slave.
PENABLE	APB bridge	Enable. This signal indicates the second and subsequent cycles of an APB transfer.
PWRITE	APB bridge	Direction. This signal indicates an APB write access when HIGH and an APB read access when LOW.
PWDATA	APB bridge	Write data. This bus is driven by the peripheral bus bridge unit during write cycles when PWRITE is HIGH. This bus can be up to 32 bits wide.
PSTRB	APB bridge	Write strobes. This signal indicates which byte lanes to update during a write transfer. There is one write strobe for each eight bits of the write data bus. Therefore, PSTRB[n] corresponds to PWDATA[(8n + 7):(8n)]. Write strobes must not be active during a read transfer.
PREADY	Slave interface	Ready. The slave uses this signal to extend an APB transfer.
PRDATA	Slave interface	Read Data. The selected slave drives this bus during read cycles when PWRITE is LOW. This bus can be up to 32-bits wide.
PSLVERR	Slave interface	This signal indicates a transfer failure. APB peripherals are not required to support the PSLVERR pin. This is true for both existing and new APB peripheral designs. Where a peripheral does not include this pin then the appropriate input to the APB bridge is tied LOW.

STATE DIAGRAM

- IDLE

This is the default state of the APB.

- SETUP

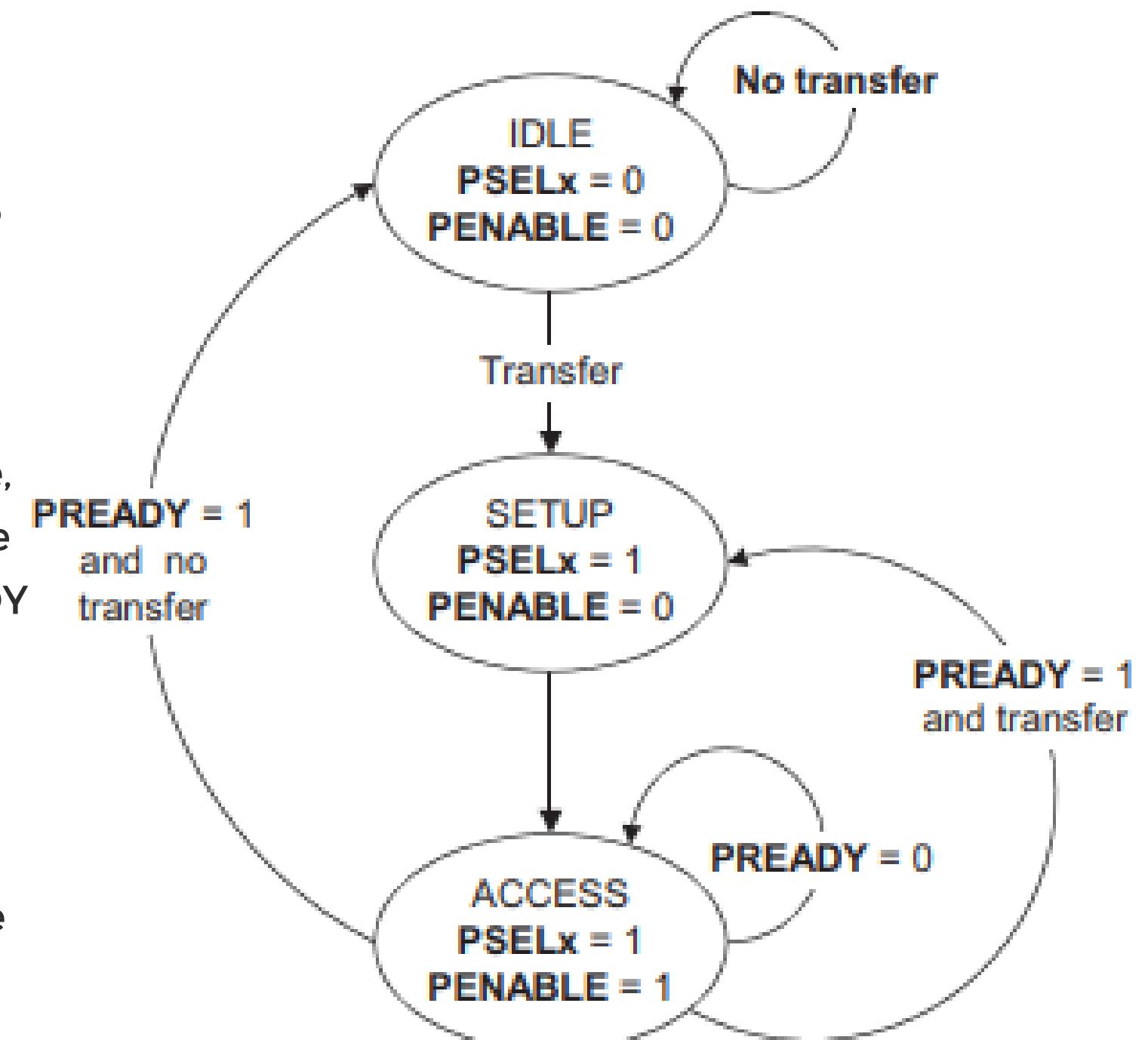
When a transfer is required the bus moves into the SETUP state, where the appropriate select signal, PSEL x , is asserted. The bus only remains in the SETUP state for one clock cycle and always moves to the ACCESS state on the next rising edge of the clock.

- ACCESS

The enable signal, PENABLE, is asserted in the ACCESS state. The address, write, select, and write data signals must remain stable during the transition from the SETUP to ACCESS state. Exit from the ACCESS state is controlled by the PREADY signal from the slave: .

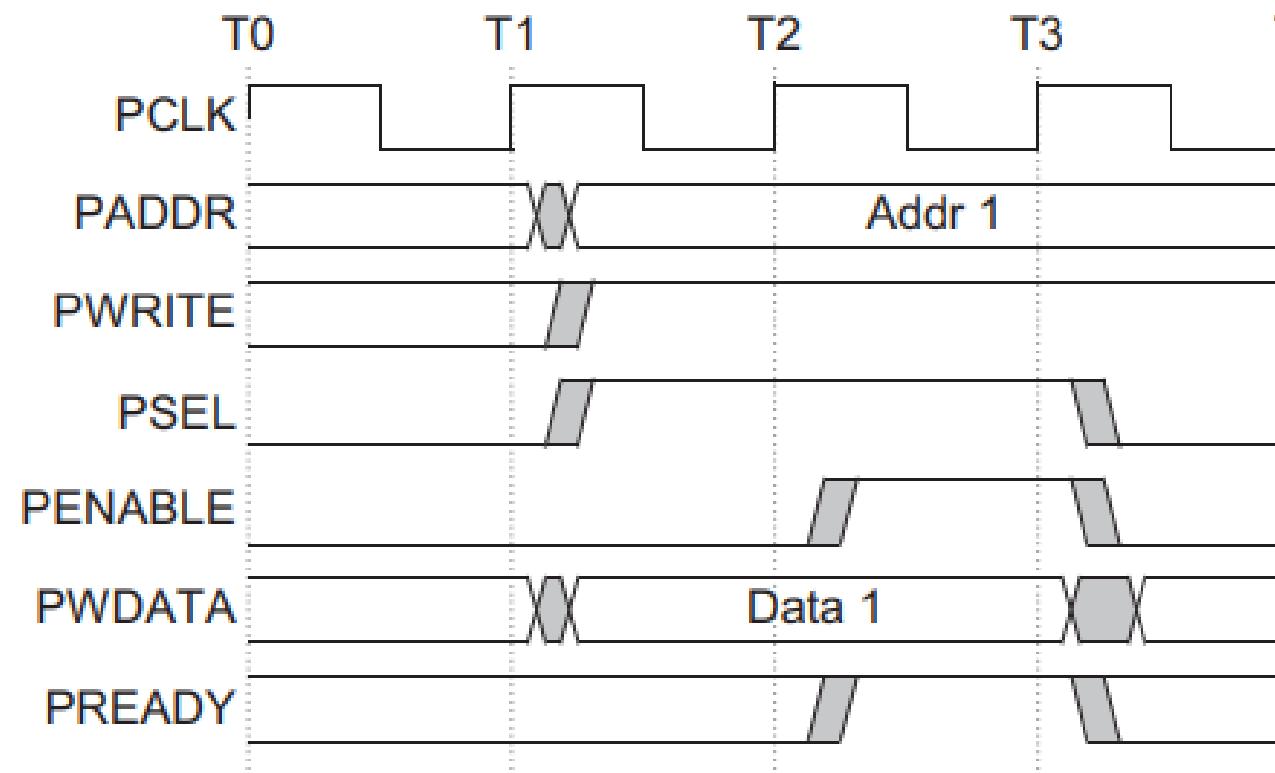
If PREADY is held LOW by the slave then the peripheral bus remains in the ACCESS state. .

If PREADY is driven HIGH by the slave then the ACCESS state is exited and the bus returns to the IDLE state if no more transfers are required. Alternatively, the bus moves directly to the SETUP state if another transfer follows.

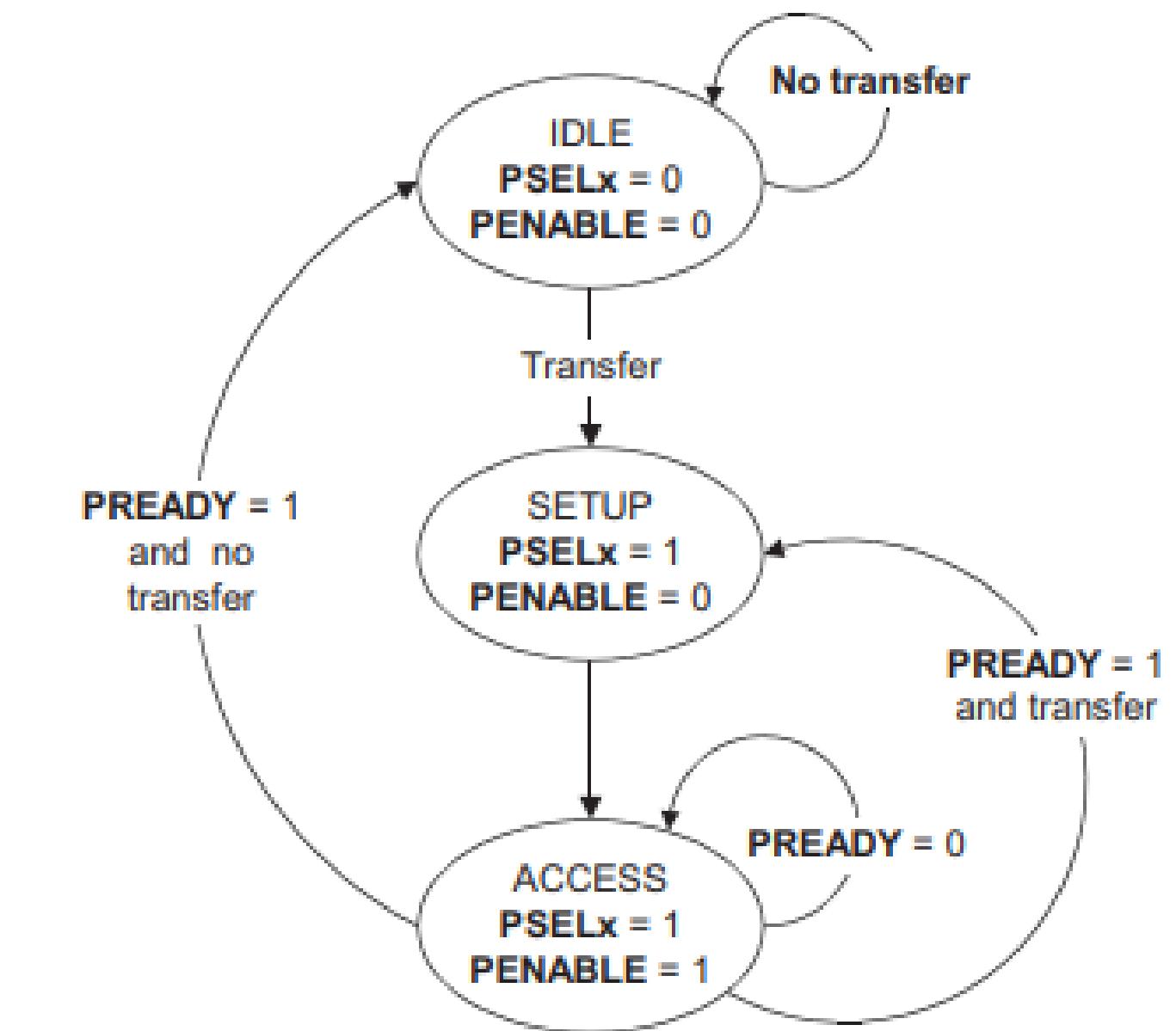
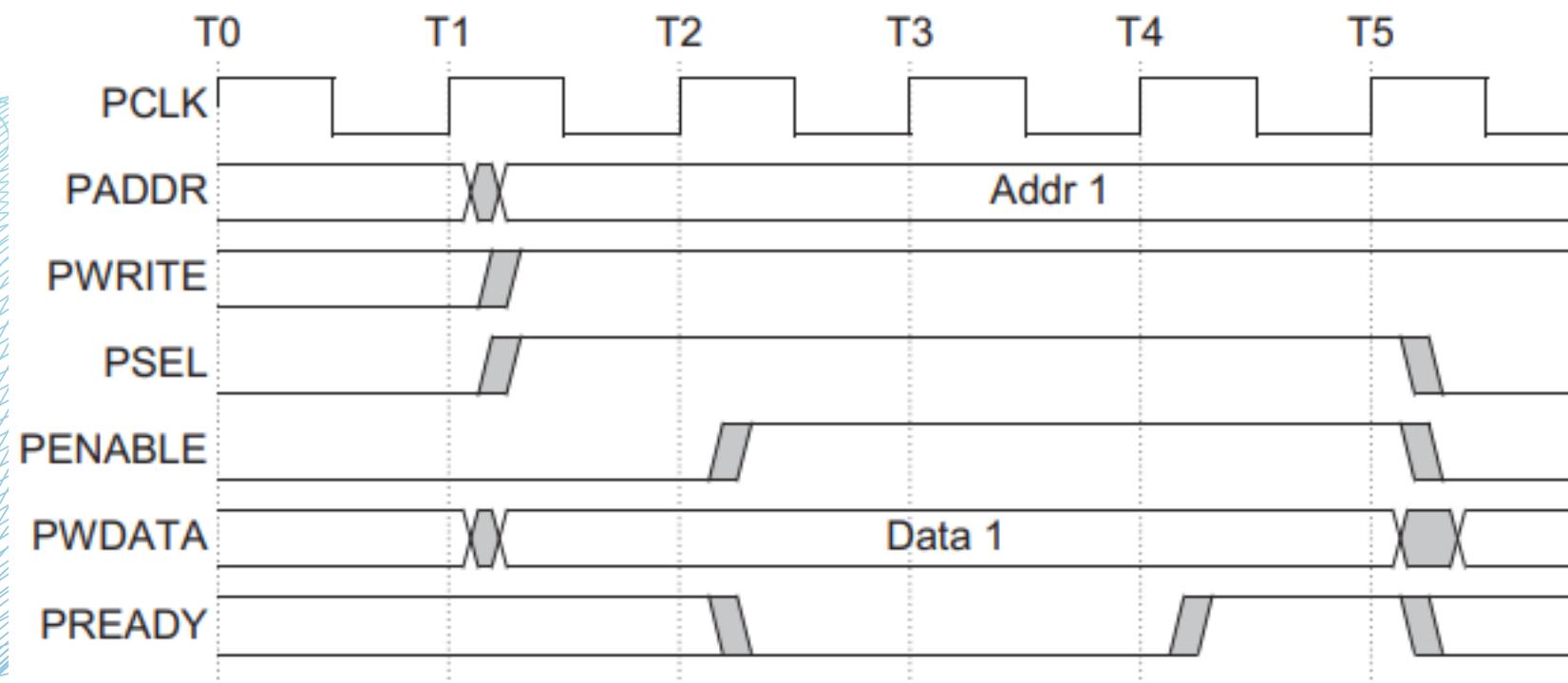


WRITE TRANSFERS

WITHOUT WAIT STATE



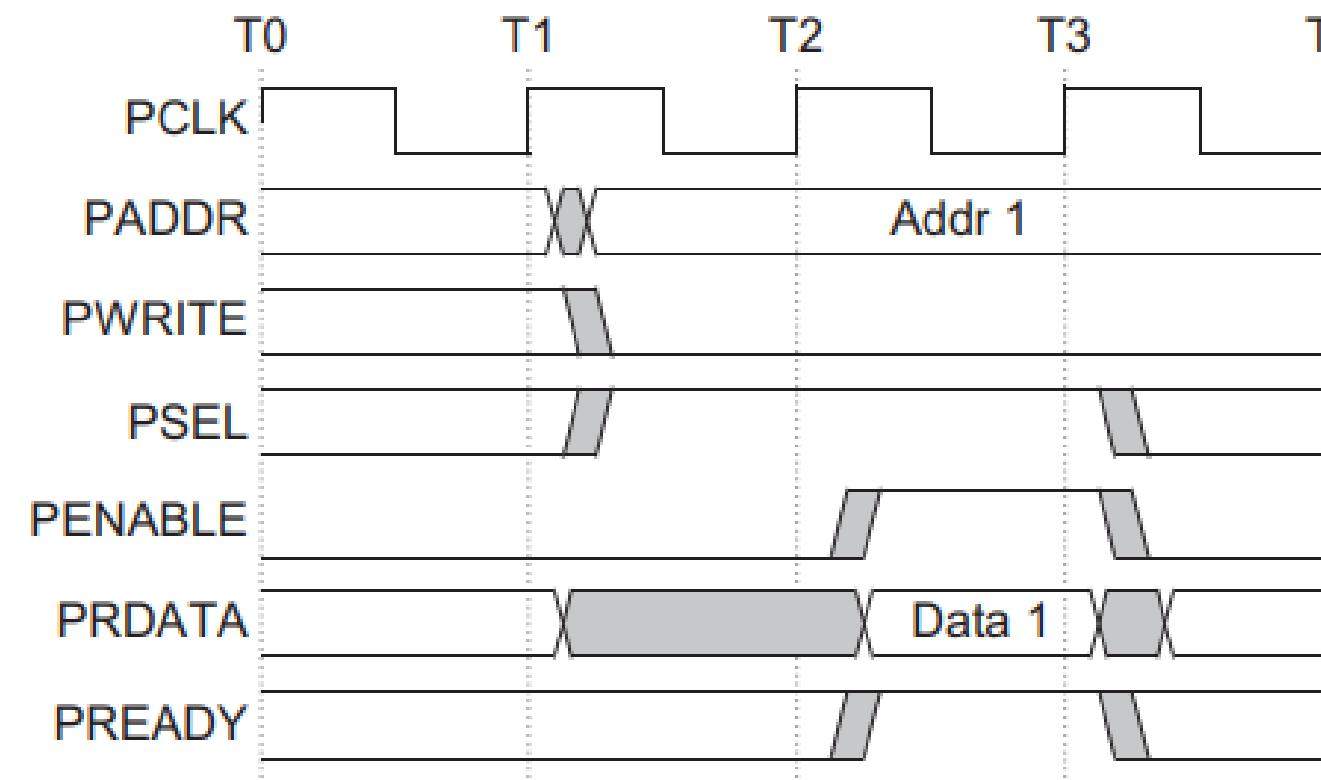
WITH WAIT STATE



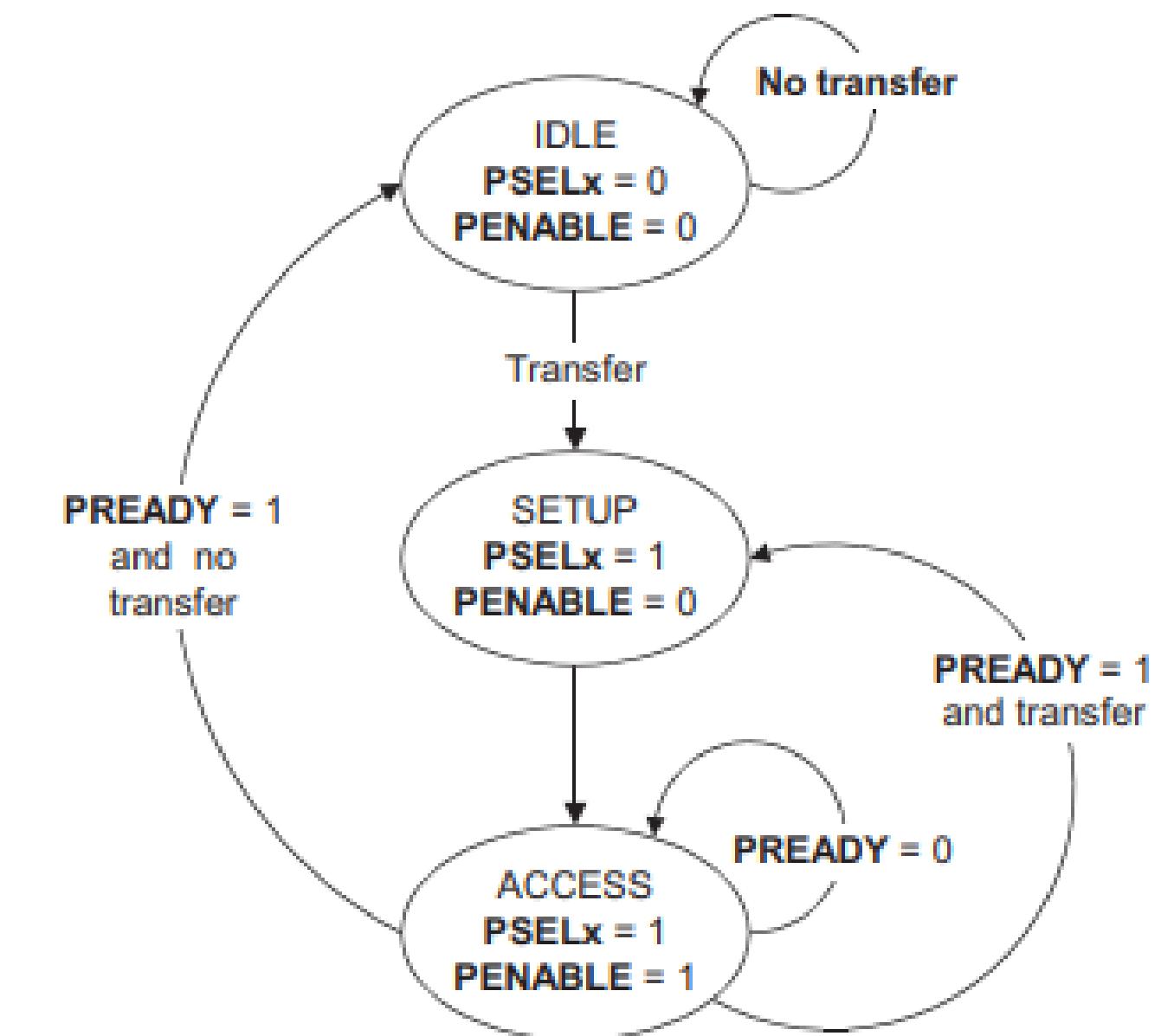
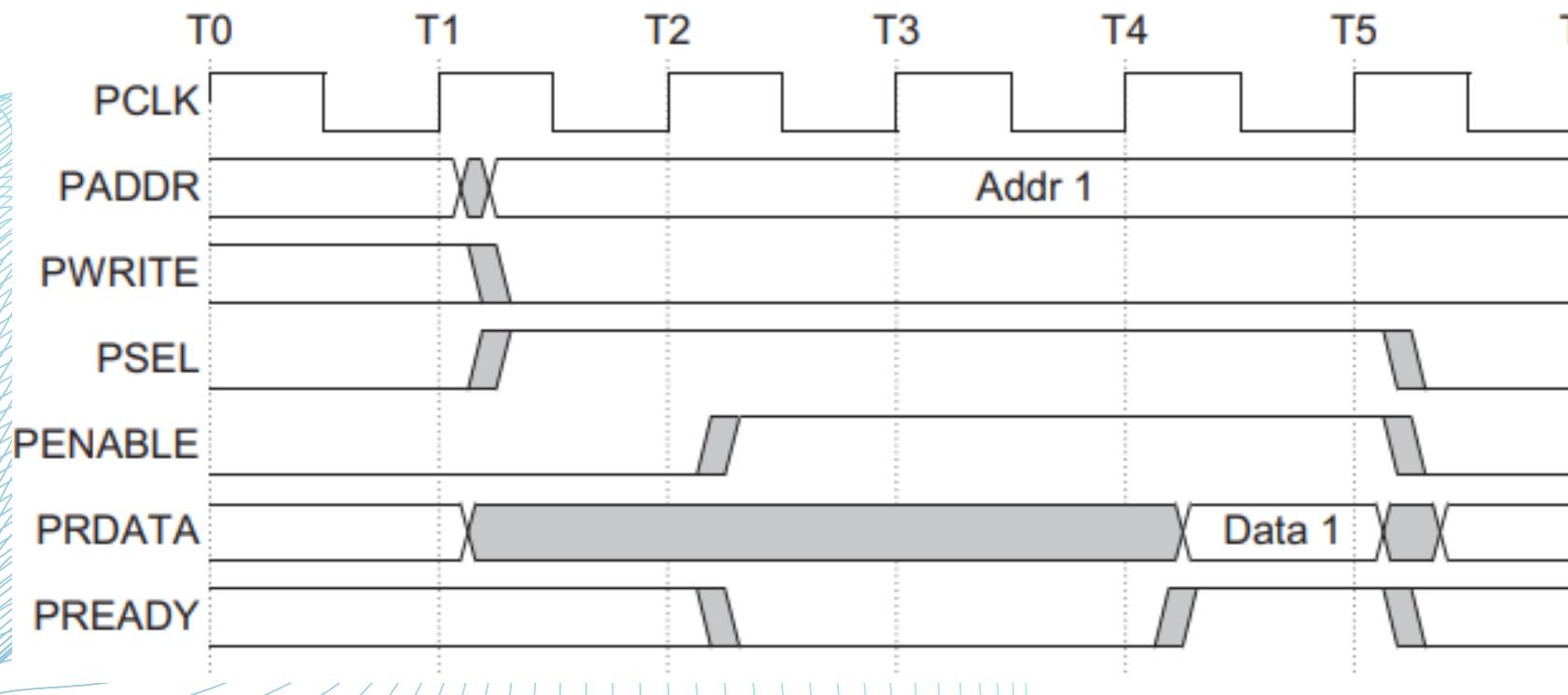
- The data is not being written until PREADY is high.
- Hence we are stretching the access state until PREADY is high. It is called a wait state.

READ TRANSFERS

WITHOUT WAIT STATE

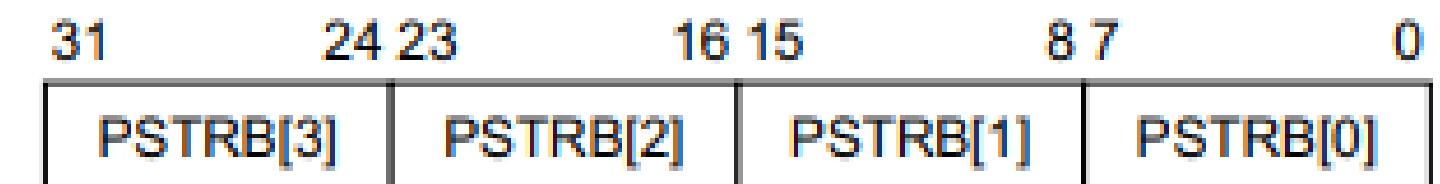


WITH WAIT STATE

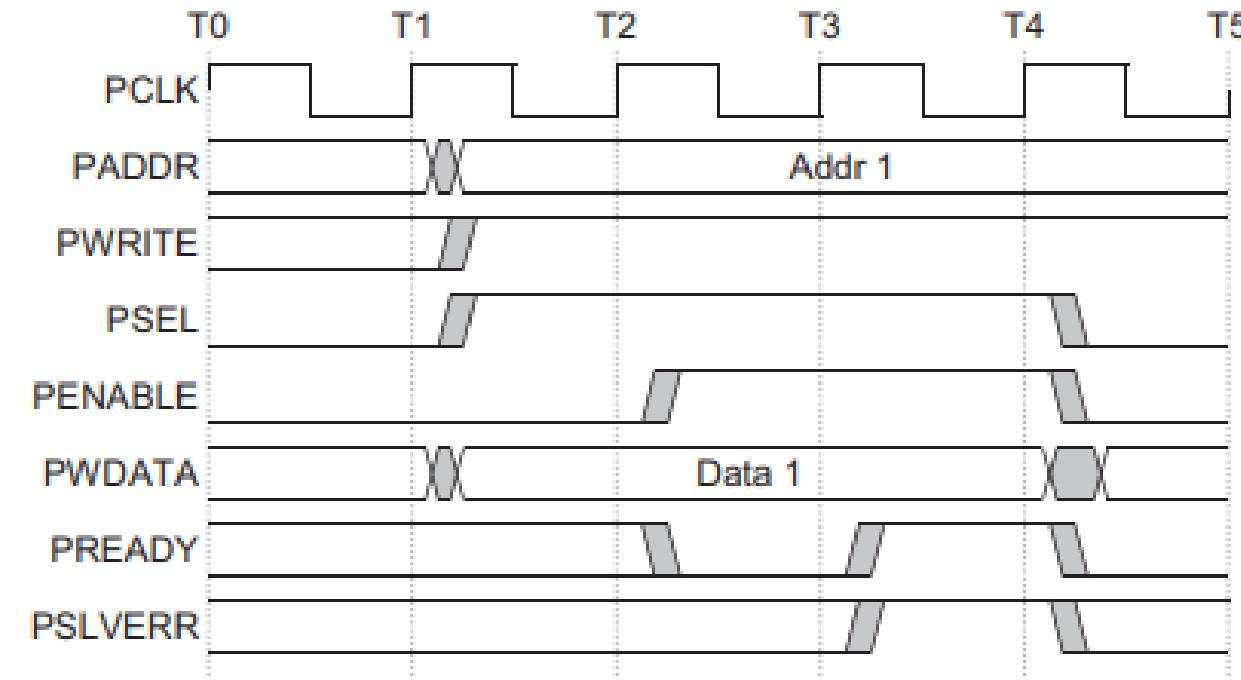


WRITE STROBE

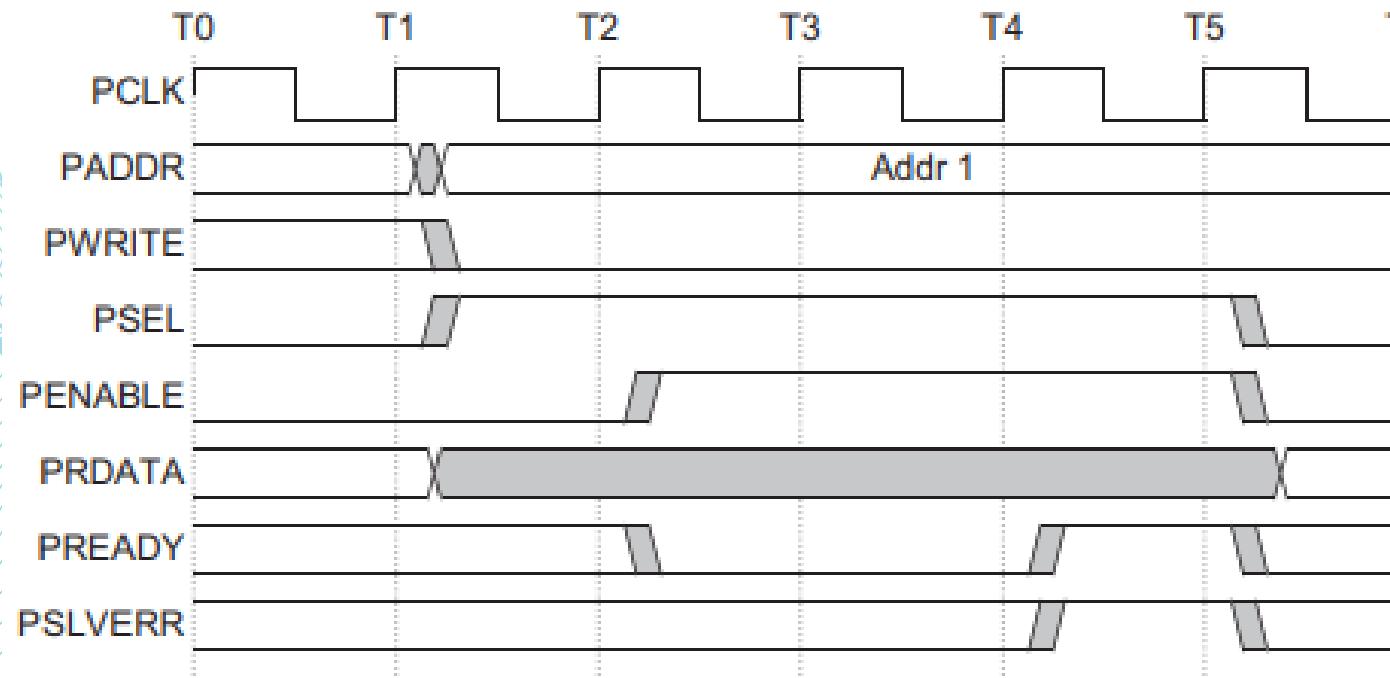
- The 32 bit data is divided into 4 bytes.
- There is one write strobe for each eight bits of the write data bus, so PSTRB[n] corresponds to PWDATA[(8n + 7):(8n)].
- It enables sparse data transfer.
- When asserted HIGH, a write strobe indicates that the corresponding byte lane of the write data bus contains valid information.



ERROR RESPONSE



WRITE TRANSFER



READ TRANSFER

You can use PSLVERR to indicate an error condition on an APB transfer. Error conditions can occur on both read and write transactions

PSLVERR is only considered valid during the last cycle of an APB transfer, when PSEL, PENABLE, and PREADY are all HIGH.

When a write transaction receives an error this does not mean that the register within the peripheral has not been updated. Read transactions that receive an error can return invalid data. There is no requirement for the peripheral to drive the data bus to all Os for a read error.

PROTECTION SUPPORT

Data or Instruction, PPROT[2]

- LOW indicates a data access
- HIGH indicates an instruction access.

This bit gives an indication if the transaction is a data or instruction access.

Note: This indication is provided as a hint and is not accurate in all cases. For example, where a transaction contains a mix of instruction and data items. It is recommended that, by default, an access is marked as a data access unless it is specifically known to be an instruction access.

Normal or privileged, PPROT[0]

- LOW indicates a normal access
- HIGH indicates a privileged access.

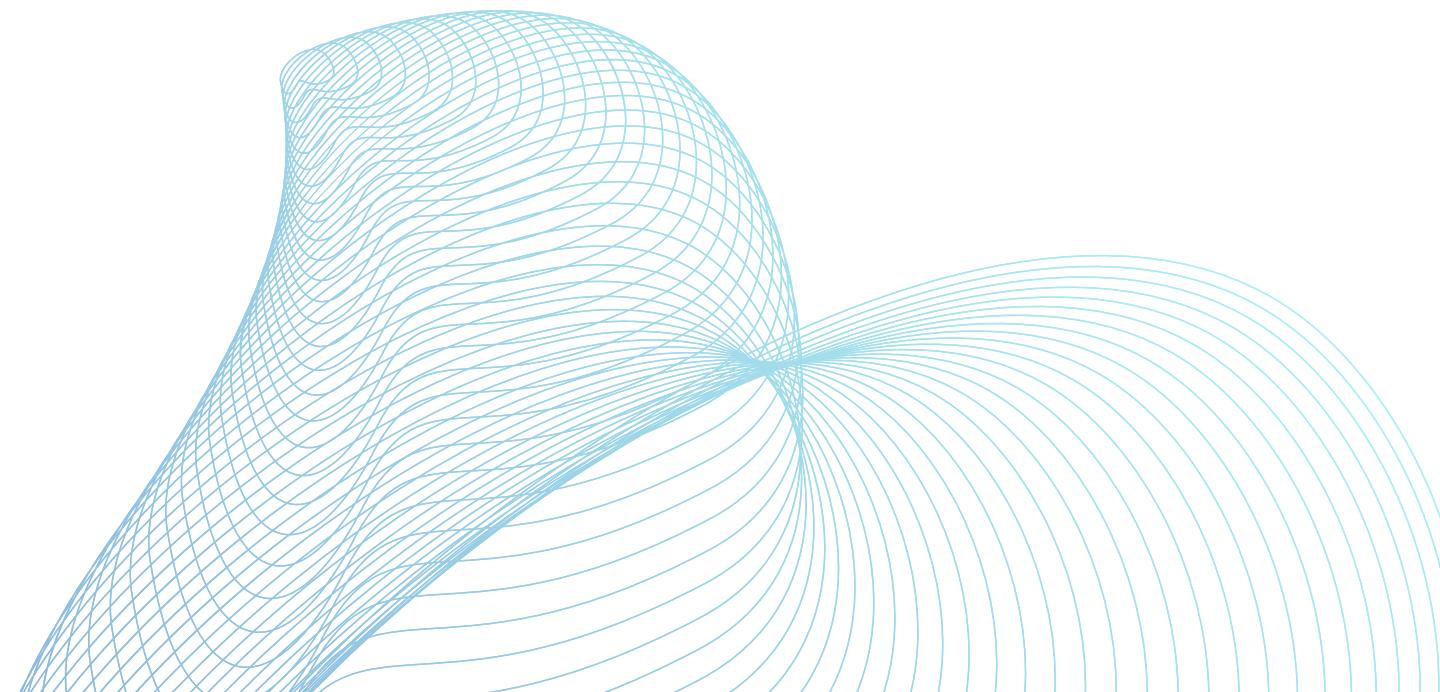
This is used by some masters to indicate their processing mode. A privileged processing mode typically has a greater level of access within a system.

Secure or non-secure, PPROT[1]

- LOW indicates a secure access
- HIGH indicates a non-secure access.

This is used in systems where a greater degree of differentiation between processing modes is required.

Note: This bit is configured so that when it is HIGH then the transaction is considered non-secure and when LOW, the transaction is considered as secure.



**THANK
YOU**

