```
# KERNEL: UVM_INFO /home/build/vlib1/vlib/uvm-1.2/src/base/uvm_report_server.svh(869) @ 4295000:
# KERNEL: --- UVM Report Summary ---
# KERNEL:
# KERNEL: ** Report counts by severity
# KERNEL: UVM_INFO :  667
# KERNEL: UVM_WARNING :    0
# KERNEL: UVM_ERROR :    0
# KERNEL: UVM_FATAL :    0
# KERNEL: ** Report counts by id
# KERNEL: [DRV]   145
# KERNEL: [MON]   153
# KERNEL: [RNTST]     1
# KERNEL: [SCO]   214
# KERNEL: [SEQ]   144
# KERNEL: [TEST]     8
# KERNEL: [TEST_DONE]     1
# KERNEL: [UVM/RELNOTES]     1
# KERNEL:
# RUNTIME: Info: RUNTIME_0068 uvm_root.svh (521): $finish called.
# KERNEL: Time: 4295 ns,  Iteration: 57,  Instance: /tb,  Process: @INITIAL#781_2@.
# KERNEL: stopped at time: 4295 ns
# VSIM: Simulation has finished. There are no more test vectors to simulate.
acdb save;
acdb report -db  fcover.acdb -txt -o cov.txt -verbose
# ACDB: Coverage report "cov.txt" was generated successfully.
exec cat cov.txt;
# ++++++++++++++++++++++++++++++++++++++++++++
# ++++++++++       REPORT INFO       ++++++++++
# ++++++++++++++++++++++++++++++++++++++++++++
#
#
# SUMMARY
# ================================================
# |     Property     |          Value           |
# ================================================
# | User             | runner                   |
# | Host             | e7793c0cb2eb             |
# | Tool             | Riviera-PRO 2023.04      |
# | Report file      | /home/runner/cov.txt     |
# | Report date      | 2025-08-14 04:15         |
# | Report arguments | -verbose                 |
# | Input file       | /home/runner/fcover.acdb |
# | Input file date  | 2025-08-14 04:15         |
# | Number of tests  | 1                        |
# ================================================
#
#
# TEST DETAILS
# ============================================
# | Property |              Value              |
# ============================================
# | Test     | fcover.acdb:fcover              |
```

```
# | Status   | Ok                              |
# | Args     | asim +access+r                  |
# | Simtime  | 4295000 ps                      |
# | Cputime  | 2.073 s                         |
# | Seed     | 1                               |
# | Date     | 2025-08-14 04:15                |
# | User     | runner                          |
# | Host     | e7793c0cb2eb                    |
# | Host os  | Linux64                         |
# | Tool     | Riviera-PRO 2023.04 (simulator) |
# ================================================
#
#
# ++++++++++++++++++++++++++++++++++++++++++++++
# ++++++++++     DESIGN HIERARCHY    ++++++++++
# ++++++++++++++++++++++++++++++++++++++++++++++
#
#
# CUMULATIVE SUMMARY
# ================================================
# |    Coverage Type    | Weight | Hits/Total |
# ================================================
# | Covergroup Coverage |      1 |   100.000% |
# |---------------------|--------|------------|
# | Types               |        |      1 / 1 |
# ================================================
# CUMULATIVE INSTANCE-BASED COVERAGE: 100.000%
# COVERED INSTANCES: 1 / 1
# FILES: 1
#
#
# CLASS - /monitor : work.monitor
#
#
#     SUMMARY
#     ================================================
#     |    Coverage Type    | Weight | Hits/Total |
#     ================================================
#     | Covergroup Coverage |      1 |   100.000% |
#     |---------------------|--------|------------|
#     | Types               |        |      1 / 1 |
#     ================================================
#     WEIGHTED AVERAGE LOCAL: 100.000%
#
#
#     COVERGROUP COVERAGE
#     ============================================================================
#     |            Covergroup             |   Hits   |  Goal /  |  Status  |
#     |                                   |          | At Least |          |
#     ============================================================================
#     | TYPE /monitor/apb_data            | 100.000% | 100.000% | Covered  |
#     ============================================================================
```

```
#      | INSTANCE <UNNAMED1>                | 100.000% | 100.000% | Covered  |
#      |------------------------------------|----------|----------|----------|
#      | COVERPOINT <UNNAMED1>::Read_Write  | 100.000% | 100.000% | Covered  |
#      |------------------------------------|----------|----------|----------|
#      | bin read                           |       67 |        1 | Covered  |
#      | bin write                          |       67 |        1 | Covered  |
#      |------------------------------------|----------|----------|----------|
#      | COVERPOINT <UNNAMED1>::Addr        | 100.000% | 100.000% | Covered  |
#      |------------------------------------|----------|----------|----------|
#      | bin valid_addr[0]                  |        3 |        1 | Covered  |
#      | bin valid_addr[1]                  |        4 |        1 | Covered  |
#      | bin valid_addr[2]                  |        6 |        1 | Covered  |
#      | bin valid_addr[3]                  |        5 |        1 | Covered  |
#      | bin valid_addr[4]                  |        5 |        1 | Covered  |
#      | bin valid_addr[5]                  |        5 |        1 | Covered  |
#      | bin valid_addr[6]                  |        3 |        1 | Covered  |
#      | bin valid_addr[7]                  |        4 |        1 | Covered  |
#      | bin valid_addr[8]                  |        4 |        1 | Covered  |
#      | bin valid_addr[9]                  |        4 |        1 | Covered  |
#      | bin valid_addr[10]                 |        4 |        1 | Covered  |
#      | bin valid_addr[11]                 |        2 |        1 | Covered  |
#      | bin valid_addr[12]                 |        3 |        1 | Covered  |
#      | bin valid_addr[13]                 |        3 |        1 | Covered  |
#      | bin valid_addr[14]                 |        6 |        1 | Covered  |
#      | bin valid_addr[15]                 |        5 |        1 | Covered  |
#      | bin valid_addr[16]                 |        3 |        1 | Covered  |
#      | bin valid_addr[17]                 |        4 |        1 | Covered  |
#      | bin valid_addr[18]                 |        4 |        1 | Covered  |
#      | bin valid_addr[19]                 |        5 |        1 | Covered  |
#      | bin valid_addr[20]                 |        2 |        1 | Covered  |
#      | bin valid_addr[21]                 |        5 |        1 | Covered  |
#      | bin valid_addr[22]                 |        3 |        1 | Covered  |
#      | bin valid_addr[23]                 |        2 |        1 | Covered  |
#      | bin valid_addr[24]                 |        4 |        1 | Covered  |
#      | bin valid_addr[25]                 |        3 |        1 | Covered  |
#      | bin valid_addr[26]                 |        4 |        1 | Covered  |
#      | bin valid_addr[27]                 |        3 |        1 | Covered  |
#      | bin valid_addr[28]                 |        6 |        1 | Covered  |
#      | bin valid_addr[29]                 |        5 |        1 | Covered  |
#      | bin valid_addr[30]                 |        2 |        1 | Covered  |
#      | bin valid_addr[31]                 |        3 |        1 | Covered  |
#      | default bin invalid_addr           |       10 |    -     | Occurred |
#      |------------------------------------|----------|----------|----------|
#      | COVERPOINT <UNNAMED1>::Error       | 100.000% | 100.000% | Covered  |
#      |------------------------------------|----------|----------|----------|
#      | bin valid_trans                    |      124 |        1 | Covered  |
#      | bin error                          |       10 |        1 | Covered  |
#      |------------------------------------|----------|----------|----------|
#      | COVERPOINT <UNNAMED1>::Write_Data  | 100.000% | 100.000% | Covered  |
#      |------------------------------------|----------|----------|----------|
#      | bin low                            |       18 |        1 | Covered  |
#      | bin mid1                           |       50 |        1 | Covered  |
```

```
#      | bin mid2                          |       26 |        1 | Covered  |
#      | bin high                          |       40 |        1 | Covered  |
#      |-----------------------------------|----------|----------|----------|
#      | COVERPOINT <UNNAMED1>::Read_Data  | 100.000% | 100.000% | Covered  |
#      |-----------------------------------|----------|----------|----------|
#      | bin low                           |       46 |        1 | Covered  |
#      | bin mid1                          |       10 |        1 | Covered  |
#      | bin mid2                          |       12 |        1 | Covered  |
#      | bin high                          |       14 |        1 | Covered  |
#      |-----------------------------------|----------|----------|----------|
#      | CROSS <UNNAMED1>::Addr_cvr_write  | 100.000% | 100.000% | Covered  |
#      |-----------------------------------|----------|----------|----------|
#      | bin <write,valid_addr[0]>         |        2 |        1 | Covered  |
#      | bin <write,valid_addr[1]>         |        2 |        1 | Covered  |
#      | bin <write,valid_addr[2]>         |        3 |        1 | Covered  |
#      | bin <write,valid_addr[3]>         |        1 |        1 | Covered  |
#      | bin <write,valid_addr[4]>         |        3 |        1 | Covered  |
#      | bin <write,valid_addr[5]>         |        2 |        1 | Covered  |
#      | bin <write,valid_addr[6]>         |        2 |        1 | Covered  |
#      | bin <write,valid_addr[7]>         |        2 |        1 | Covered  |
#      | bin <write,valid_addr[8]>         |        3 |        1 | Covered  |
#      | bin <write,valid_addr[9]>         |        2 |        1 | Covered  |
#      | bin <write,valid_addr[10]>        |        2 |        1 | Covered  |
#      | bin <write,valid_addr[11]>        |        1 |        1 | Covered  |
#      | bin <write,valid_addr[12]>        |        1 |        1 | Covered  |
#      | bin <write,valid_addr[13]>        |        1 |        1 | Covered  |
#      | bin <write,valid_addr[14]>        |        3 |        1 | Covered  |
#      | bin <write,valid_addr[15]>        |        2 |        1 | Covered  |
#      | bin <write,valid_addr[16]>        |        2 |        1 | Covered  |
#      | bin <write,valid_addr[17]>        |        3 |        1 | Covered  |
#      | bin <write,valid_addr[18]>        |        2 |        1 | Covered  |
#      | bin <write,valid_addr[19]>        |        4 |        1 | Covered  |
#      | bin <write,valid_addr[20]>        |        1 |        1 | Covered  |
#      | bin <write,valid_addr[21]>        |        2 |        1 | Covered  |
#      | bin <write,valid_addr[22]>        |        1 |        1 | Covered  |
#      | bin <write,valid_addr[23]>        |        1 |        1 | Covered  |
#      | bin <write,valid_addr[24]>        |        1 |        1 | Covered  |
#      | bin <write,valid_addr[25]>        |        1 |        1 | Covered  |
#      | bin <write,valid_addr[26]>        |        1 |        1 | Covered  |
#      | bin <write,valid_addr[27]>        |        2 |        1 | Covered  |
#      | bin <write,valid_addr[28]>        |        3 |        1 | Covered  |
#      | bin <write,valid_addr[29]>        |        3 |        1 | Covered  |
#      | bin <write,valid_addr[30]>        |        1 |        1 | Covered  |
#      | bin <write,valid_addr[31]>        |        2 |        1 | Covered  |
#      | ignore bin unused                 |       62 |    -     | Occurred |
#      |-----------------------------------|----------|----------|----------|
#      | CROSS <UNNAMED1>::Addr_cvr_read   | 100.000% | 100.000% | Covered  |
#      |-----------------------------------|----------|----------|----------|
#      | bin <read,valid_addr[0]>          |        1 |        1 | Covered  |
#      | bin <read,valid_addr[1]>          |        2 |        1 | Covered  |
#      | bin <read,valid_addr[2]>          |        3 |        1 | Covered  |
#      | bin <read,valid_addr[3]>          |        4 |        1 | Covered  |
```

```
#     | bin <read,valid_addr[4]>          |        2 |        1 | Covered  |
#     | bin <read,valid_addr[5]>          |        3 |        1 | Covered  |
#     | bin <read,valid_addr[6]>          |        1 |        1 | Covered  |
#     | bin <read,valid_addr[7]>          |        2 |        1 | Covered  |
#     | bin <read,valid_addr[8]>          |        1 |        1 | Covered  |
#     | bin <read,valid_addr[9]>          |        2 |        1 | Covered  |
#     | bin <read,valid_addr[10]>         |        2 |        1 | Covered  |
#     | bin <read,valid_addr[11]>         |        1 |        1 | Covered  |
#     | bin <read,valid_addr[12]>         |        2 |        1 | Covered  |
#     | bin <read,valid_addr[13]>         |        2 |        1 | Covered  |
#     | bin <read,valid_addr[14]>         |        3 |        1 | Covered  |
#     | bin <read,valid_addr[15]>         |        3 |        1 | Covered  |
#     | bin <read,valid_addr[16]>         |        1 |        1 | Covered  |
#     | bin <read,valid_addr[17]>         |        1 |        1 | Covered  |
#     | bin <read,valid_addr[18]>         |        2 |        1 | Covered  |
#     | bin <read,valid_addr[19]>         |        1 |        1 | Covered  |
#     | bin <read,valid_addr[20]>         |        1 |        1 | Covered  |
#     | bin <read,valid_addr[21]>         |        3 |        1 | Covered  |
#     | bin <read,valid_addr[22]>         |        2 |        1 | Covered  |
#     | bin <read,valid_addr[23]>         |        1 |        1 | Covered  |
#     | bin <read,valid_addr[24]>         |        3 |        1 | Covered  |
#     | bin <read,valid_addr[25]>         |        2 |        1 | Covered  |
#     | bin <read,valid_addr[26]>         |        3 |        1 | Covered  |
#     | bin <read,valid_addr[27]>         |        1 |        1 | Covered  |
#     | bin <read,valid_addr[28]>         |        3 |        1 | Covered  |
#     | bin <read,valid_addr[29]>         |        2 |        1 | Covered  |
#     | bin <read,valid_addr[30]>         |        1 |        1 | Covered  |
#     | bin <read,valid_addr[31]>         |        1 |        1 | Covered  |
#     | ignore bin unused                 |       62 |    -     | Occurred |
#     |-----------------------------------|----------|----------|----------|
#     | CROSS <UNNAMED1>::WData_cvr_write | 100.000% | 100.000% | Covered  |
#     |-----------------------------------|----------|----------|----------|
#     | bin <write,low>                   |       15 |        1 | Covered  |
#     | bin <write,mid1>                  |       14 |        1 | Covered  |
#     | bin <write,mid2>                  |       16 |        1 | Covered  |
#     | bin <write,high>                  |       22 |        1 | Covered  |
#     | ignore bin unused                 |       67 |    -     | Occurred |
#     |-----------------------------------|----------|----------|----------|
#     | CROSS <UNNAMED1>::RData_cvr_read  | 100.000% | 100.000% | Covered  |
#     |-----------------------------------|----------|----------|----------|
#     | bin <read,low>                    |       28 |        1 | Covered  |
#     | bin <read,mid1>                   |        9 |        1 | Covered  |
#     | bin <read,mid2>                   |       11 |        1 | Covered  |
#     | bin <read,high>                   |       14 |        1 | Covered  |
#     | ignore bin unused                 |       20 |    -     | Occurred |
#     |-----------------------------------|----------|----------|----------|
#     | CROSS <UNNAMED1>::Err_cvr_write   | 100.000% | 100.000% | Covered  |
#     |-----------------------------------|----------|----------|----------|
#     | bin <write,error>                 |        5 |        1 | Covered  |
#     | ignore bin unused_write           |       67 |    -     | Occurred |
#     | ignore bin no_error               |      124 |    -     | Occurred |
#     |-----------------------------------|----------|----------|----------|
```

```
#     | CROSS <UNNAMED1>::Err_cvr_read    | 100.000% | 100.000% | Covered  |
#     |-----------------------------------|----------|----------|----------|
#     | bin <read,error>                  |        5 |        1 | Covered  |
#     | ignore bin unused_read            |       67 |    -     | Occurred |
#     | ignore bin no_error               |      124 |    -     | Occurred |
#     ============================================================================
#
#
# ++++++++++++++++++++++++++++++++++++++++++++
# ++++++++++       DESIGN UNITS      ++++++++++
# ++++++++++++++++++++++++++++++++++++++++++++
#
#
# CUMULATIVE SUMMARY
# ===========================================
# |    Coverage Type    | Weight | Hits/Total |
# ===========================================
# | Covergroup Coverage |      1 |   100.000% |
# |---------------------|--------|------------|
# | Types               |        |      1 / 1 |
# ===========================================
# CUMULATIVE DESIGN-BASED COVERAGE: 100.000%
# COVERED DESIGN UNITS: 1 / 1
# FILES: 1
#
#
# CLASS - work.monitor
#
#
#     SUMMARY
#     ===============================================
#     |    Coverage Type    | Weight | Hits/Total |
#     ===============================================
#     | Covergroup Coverage |      1 |   100.000% |
#     |---------------------|--------|------------|
#     | Types               |        |      1 / 1 |
#     ===============================================
#     WEIGHTED AVERAGE: 100.000%
#
#
#     COVERGROUP COVERAGE
#     ============================================================================
#     |            Covergroup             |   Hits   |  Goal /  |  Status  |
#     |                                   |          | At Least |          |
#     ============================================================================
#     | TYPE /monitor/apb_data            | 100.000% | 100.000% | Covered  |
#     ============================================================================
#     | INSTANCE <UNNAMED1>               | 100.000% | 100.000% | Covered  |
#     |-----------------------------------|----------|----------|----------|
#     | COVERPOINT <UNNAMED1>::Read_Write | 100.000% | 100.000% | Covered  |
#     |-----------------------------------|----------|----------|----------|
#     | bin read                          |       67 |        1 | Covered  |
```

```
#      | bin write                          |       67 |        1 | Covered  |
#      |------------------------------------|----------|----------|----------|
#      | COVERPOINT <UNNAMED1>::Addr        | 100.000% | 100.000% | Covered  |
#      |------------------------------------|----------|----------|----------|
#      | bin valid_addr[0]                  |        3 |        1 | Covered  |
#      | bin valid_addr[1]                  |        4 |        1 | Covered  |
#      | bin valid_addr[2]                  |        6 |        1 | Covered  |
#      | bin valid_addr[3]                  |        5 |        1 | Covered  |
#      | bin valid_addr[4]                  |        5 |        1 | Covered  |
#      | bin valid_addr[5]                  |        5 |        1 | Covered  |
#      | bin valid_addr[6]                  |        3 |        1 | Covered  |
#      | bin valid_addr[7]                  |        4 |        1 | Covered  |
#      | bin valid_addr[8]                  |        4 |        1 | Covered  |
#      | bin valid_addr[9]                  |        4 |        1 | Covered  |
#      | bin valid_addr[10]                 |        4 |        1 | Covered  |
#      | bin valid_addr[11]                 |        2 |        1 | Covered  |
#      | bin valid_addr[12]                 |        3 |        1 | Covered  |
#      | bin valid_addr[13]                 |        3 |        1 | Covered  |
#      | bin valid_addr[14]                 |        6 |        1 | Covered  |
#      | bin valid_addr[15]                 |        5 |        1 | Covered  |
#      | bin valid_addr[16]                 |        3 |        1 | Covered  |
#      | bin valid_addr[17]                 |        4 |        1 | Covered  |
#      | bin valid_addr[18]                 |        4 |        1 | Covered  |
#      | bin valid_addr[19]                 |        5 |        1 | Covered  |
#      | bin valid_addr[20]                 |        2 |        1 | Covered  |
#      | bin valid_addr[21]                 |        5 |        1 | Covered  |
#      | bin valid_addr[22]                 |        3 |        1 | Covered  |
#      | bin valid_addr[23]                 |        2 |        1 | Covered  |
#      | bin valid_addr[24]                 |        4 |        1 | Covered  |
#      | bin valid_addr[25]                 |        3 |        1 | Covered  |
#      | bin valid_addr[26]                 |        4 |        1 | Covered  |
#      | bin valid_addr[27]                 |        3 |        1 | Covered  |
#      | bin valid_addr[28]                 |        6 |        1 | Covered  |
#      | bin valid_addr[29]                 |        5 |        1 | Covered  |
#      | bin valid_addr[30]                 |        2 |        1 | Covered  |
#      | bin valid_addr[31]                 |        3 |        1 | Covered  |
#      | default bin invalid_addr           |       10 |    -     | Occurred |
#      |------------------------------------|----------|----------|----------|
#      | COVERPOINT <UNNAMED1>::Error       | 100.000% | 100.000% | Covered  |
#      |------------------------------------|----------|----------|----------|
#      | bin valid_trans                    |      124 |        1 | Covered  |
#      | bin error                          |       10 |        1 | Covered  |
#      |------------------------------------|----------|----------|----------|
#      | COVERPOINT <UNNAMED1>::Write_Data  | 100.000% | 100.000% | Covered  |
#      |------------------------------------|----------|----------|----------|
#      | bin low                            |       18 |        1 | Covered  |
#      | bin mid1                           |       50 |        1 | Covered  |
#      | bin mid2                           |       26 |        1 | Covered  |
#      | bin high                           |       40 |        1 | Covered  |
#      |------------------------------------|----------|----------|----------|
#      | COVERPOINT <UNNAMED1>::Read_Data   | 100.000% | 100.000% | Covered  |
#      |------------------------------------|----------|----------|----------|
```

```
#      | bin low                            |       46 |        1 | Covered  |
#      | bin mid1                           |       10 |        1 | Covered  |
#      | bin mid2                           |       12 |        1 | Covered  |
#      | bin high                           |       14 |        1 | Covered  |
#      |------------------------------------|----------|----------|----------|
#      | CROSS <UNNAMED1>::Addr_cvr_write   | 100.000% | 100.000% | Covered  |
#      |------------------------------------|----------|----------|----------|
#      | bin <write,valid_addr[0]>          |        2 |        1 | Covered  |
#      | bin <write,valid_addr[1]>          |        2 |        1 | Covered  |
#      | bin <write,valid_addr[2]>          |        3 |        1 | Covered  |
#      | bin <write,valid_addr[3]>          |        1 |        1 | Covered  |
#      | bin <write,valid_addr[4]>          |        3 |        1 | Covered  |
#      | bin <write,valid_addr[5]>          |        2 |        1 | Covered  |
#      | bin <write,valid_addr[6]>          |        2 |        1 | Covered  |
#      | bin <write,valid_addr[7]>          |        2 |        1 | Covered  |
#      | bin <write,valid_addr[8]>          |        3 |        1 | Covered  |
#      | bin <write,valid_addr[9]>          |        2 |        1 | Covered  |
#      | bin <write,valid_addr[10]>         |        2 |        1 | Covered  |
#      | bin <write,valid_addr[11]>         |        1 |        1 | Covered  |
#      | bin <write,valid_addr[12]>         |        1 |        1 | Covered  |
#      | bin <write,valid_addr[13]>         |        1 |        1 | Covered  |
#      | bin <write,valid_addr[14]>         |        3 |        1 | Covered  |
#      | bin <write,valid_addr[15]>         |        2 |        1 | Covered  |
#      | bin <write,valid_addr[16]>         |        2 |        1 | Covered  |
#      | bin <write,valid_addr[17]>         |        3 |        1 | Covered  |
#      | bin <write,valid_addr[18]>         |        2 |        1 | Covered  |
#      | bin <write,valid_addr[19]>         |        4 |        1 | Covered  |
#      | bin <write,valid_addr[20]>         |        1 |        1 | Covered  |
#      | bin <write,valid_addr[21]>         |        2 |        1 | Covered  |
#      | bin <write,valid_addr[22]>         |        1 |        1 | Covered  |
#      | bin <write,valid_addr[23]>         |        1 |        1 | Covered  |
#      | bin <write,valid_addr[24]>         |        1 |        1 | Covered  |
#      | bin <write,valid_addr[25]>         |        1 |        1 | Covered  |
#      | bin <write,valid_addr[26]>         |        1 |        1 | Covered  |
#      | bin <write,valid_addr[27]>         |        2 |        1 | Covered  |
#      | bin <write,valid_addr[28]>         |        3 |        1 | Covered  |
#      | bin <write,valid_addr[29]>         |        3 |        1 | Covered  |
#      | bin <write,valid_addr[30]>         |        1 |        1 | Covered  |
#      | bin <write,valid_addr[31]>         |        2 |        1 | Covered  |
#      | ignore bin unused                  |       62 |    -     | Occurred |
#      |------------------------------------|----------|----------|----------|
#      | CROSS <UNNAMED1>::Addr_cvr_read    | 100.000% | 100.000% | Covered  |
#      |------------------------------------|----------|----------|----------|
#      | bin <read,valid_addr[0]>           |        1 |        1 | Covered  |
#      | bin <read,valid_addr[1]>           |        2 |        1 | Covered  |
#      | bin <read,valid_addr[2]>           |        3 |        1 | Covered  |
#      | bin <read,valid_addr[3]>           |        4 |        1 | Covered  |
#      | bin <read,valid_addr[4]>           |        2 |        1 | Covered  |
#      | bin <read,valid_addr[5]>           |        3 |        1 | Covered  |
#      | bin <read,valid_addr[6]>           |        1 |        1 | Covered  |
#      | bin <read,valid_addr[7]>           |        2 |        1 | Covered  |
#      | bin <read,valid_addr[8]>           |        1 |        1 | Covered  |
```

```
#     | bin <read,valid_addr[9]>          |        2 |        1 | Covered  |
#     | bin <read,valid_addr[10]>         |        2 |        1 | Covered  |
#     | bin <read,valid_addr[11]>         |        1 |        1 | Covered  |
#     | bin <read,valid_addr[12]>         |        2 |        1 | Covered  |
#     | bin <read,valid_addr[13]>         |        2 |        1 | Covered  |
#     | bin <read,valid_addr[14]>         |        3 |        1 | Covered  |
#     | bin <read,valid_addr[15]>         |        3 |        1 | Covered  |
#     | bin <read,valid_addr[16]>         |        1 |        1 | Covered  |
#     | bin <read,valid_addr[17]>         |        1 |        1 | Covered  |
#     | bin <read,valid_addr[18]>         |        2 |        1 | Covered  |
#     | bin <read,valid_addr[19]>         |        1 |        1 | Covered  |
#     | bin <read,valid_addr[20]>         |        1 |        1 | Covered  |
#     | bin <read,valid_addr[21]>         |        3 |        1 | Covered  |
#     | bin <read,valid_addr[22]>         |        2 |        1 | Covered  |
#     | bin <read,valid_addr[23]>         |        1 |        1 | Covered  |
#     | bin <read,valid_addr[24]>         |        3 |        1 | Covered  |
#     | bin <read,valid_addr[25]>         |        2 |        1 | Covered  |
#     | bin <read,valid_addr[26]>         |        3 |        1 | Covered  |
#     | bin <read,valid_addr[27]>         |        1 |        1 | Covered  |
#     | bin <read,valid_addr[28]>         |        3 |        1 | Covered  |
#     | bin <read,valid_addr[29]>         |        2 |        1 | Covered  |
#     | bin <read,valid_addr[30]>         |        1 |        1 | Covered  |
#     | bin <read,valid_addr[31]>         |        1 |        1 | Covered  |
#     | ignore bin unused                 |       62 |    -     | Occurred |
#     |-----------------------------------|----------|----------|----------|
#     | CROSS <UNNAMED1>::WData_cvr_write | 100.000% | 100.000% | Covered  |
#     |-----------------------------------|----------|----------|----------|
#     | bin <write,low>                   |       15 |        1 | Covered  |
#     | bin <write,mid1>                  |       14 |        1 | Covered  |
#     | bin <write,mid2>                  |       16 |        1 | Covered  |
#     | bin <write,high>                  |       22 |        1 | Covered  |
#     | ignore bin unused                 |       67 |    -     | Occurred |
#     |-----------------------------------|----------|----------|----------|
#     | CROSS <UNNAMED1>::RData_cvr_read  | 100.000% | 100.000% | Covered  |
#     |-----------------------------------|----------|----------|----------|
#     | bin <read,low>                    |       28 |        1 | Covered  |
#     | bin <read,mid1>                   |        9 |        1 | Covered  |
#     | bin <read,mid2>                   |       11 |        1 | Covered  |
#     | bin <read,high>                   |       14 |        1 | Covered  |
#     | ignore bin unused                 |       20 |    -     | Occurred |
#     |-----------------------------------|----------|----------|----------|
#     | CROSS <UNNAMED1>::Err_cvr_write   | 100.000% | 100.000% | Covered  |
#     |-----------------------------------|----------|----------|----------|
#     | bin <write,error>                 |        5 |        1 | Covered  |
#     | ignore bin unused_write           |       67 |    -     | Occurred |
#     | ignore bin no_error               |      124 |    -     | Occurred |
#     |-----------------------------------|----------|----------|----------|
#     | CROSS <UNNAMED1>::Err_cvr_read    | 100.000% | 100.000% | Covered  |
#     |-----------------------------------|----------|----------|----------|
#     | bin <read,error>                  |        5 |        1 | Covered  |
#     | ignore bin unused_read            |       67 |    -     | Occurred |
#     | ignore bin no_error               |      124 |    -     | Occurred |
```

```
#      ================================================================================
#
exit
# VSIM: Simulation has finished.
 Done
```