```
# KERNEL: UVM_INFO /home/build/vlib1/vlib/uvm-1.2/src/base/uvm_report_server.svh(869) @ 4295000:
# KERNEL: --- UVM Report Summary ---
# KERNEL:
# KERNEL: ** Report counts by severity
# KERNEL: UVM_INFO: 667
# KERNEL: UVM_WARNING :
# KERNEL: UVM_ERROR :
# KERNEL: UVM_FATAL :
# KERNEL: ** Report counts by id
# KERNEL: [DRV]
               145
# KERNEL: [MON]
# KERNEL: [RNTST]
# KERNEL: [SCO]
                214
# KERNEL: [SEQ]
# KERNEL: [TEST]
# KERNEL: [TEST_DONE]
# KERNEL: [UVM/RELNOTES]
# KERNEL:
# RUNTIME: Info: RUNTIME_0068 uvm_root.svh (521): $finish called.
# KERNEL: Time: 4295 ns, Iteration: 57, Instance: /tb, Process: @INITIAL#781_2@.
# KERNEL: stopped at time: 4295 ns
# VSIM: Simulation has finished. There are no more test vectors to simulate.
acdb save;
acdb report -db fcover.acdb -txt -o cov.txt -verbose
# ACDB: Coverage report "cov.txt" was generated successfully.
exec cat cov.txt;
REPORT INFO
# +++++++++
# SUMMARY
                  Property
                            Value
# | User
                   | runner
                  | e7793c0cb2eb
# | Host
# | Tool
                  | Riviera-PRO 2023.04
# | Report file
                  | /home/runner/cov.txt
# | Report date
                  | 2025-08-14 04:15
# | Report arguments | -verbose
# | Input file
                  | /home/runner/fcover.acdb |
# | Input file date | 2025-08-14 04:15
# | Number of tests | 1
#
# TEST DETAILS
 | Property |
                         Value
           | fcover.acdb:fcover
# | Test
```

```
# | Status | Ok
     | asim +access+r
# | Args
# | Simtime | 4295000 ps
# | Cputime | 2.073 s
# | Seed
       | 1
# | Date
       | 2025-08-14 04:15
       runner
# | User
       | e7793c0cb2eb
# | Host
 | Host os | Linux64
      | Riviera-PRO 2023.04 (simulator) |
 _____
 +++++++++
          DESIGN HIERARCHY
                      +++++++++
 # CUMULATIVE SUMMARY
 Coverage Type | Weight | Hits/Total |
# | Covergroup Coverage |
                 1 | 100.000% |
# |-----|
 Types
            1
                   | 1/1|
 _____
# CUMULATIVE INSTANCE-BASED COVERAGE: 100.000%
# COVERED INSTANCES: 1 / 1
# FILES: 1
 CLASS - /monitor : work.monitor
#
   SUMMARY
      Coverage Type | Weight | Hits/Total |
   _____
   | Covergroup Coverage |
                     1 | 100.000% |
   |-----|
                         1 / 1 |
   Types
   WEIGHTED AVERAGE LOCAL: 100.000%
#
   COVERGROUP COVERAGE
           Covergroup
                         1
                            Hits | Goal / | Status |
#
                                | At Least |
                         ______
#
   | TYPE /monitor/apb_data
                         | 100.000% | 100.000% | Covered |
#
   _____
```

# COVERPOINT <unnamedi>::Read_write 100.000% 100.000% Covered # bin read 67 1 Covered # bin write 67 1 Covered # bin write 67 1 Covered # bin write 67 1 Covered # bin valid_addr[0] 3 1 Covered # bin valid_addr[1] 4 1 Covered # bin valid_addr[3] 5 1 Covered # bin valid_addr[4] 5 1 Covered # bin valid_addr[6] 5 1 Covered # bin valid_addr[6] 3 1 Covered # bin valid_addr[6] 4 1 Covered # bin valid_addr[6] 4 1 Covered # bin valid_addr[6] 4 1 Covered # bin valid_addr[7] 4 1 Covered # bin valid_addr[8] 4 1 Covered # bin valid_addr[9] 4 1 Covered # bin valid_addr[1] 5 1 Covered # bin valid_addr[1] 5 1 Covered # bin valid_addr[1] 5 1 Covered # bin valid_addr[1] 6 1 Covered # bin valid_addr[1] 7 1 1 1 Covered # bin valid_addr[1] 7 1 1 1 1 1 1 1 1 1</unnamedi>				_10.3V - LDA1 lay	_
# COVERPOINT <unnamedi>::Read_write 100.000% 100.000% Covered # bin read 67 1 Covered # bin write 67 1 Covered # bin write 67 1 Covered # bin write 67 1 Covered # bin valid_addr[0] 3 1 Covered # bin valid_addr[1] 4 1 Covered # bin valid_addr[2] 6 1 Covered # bin valid_addr[3] 5 1 Covered # bin valid_addr[4] 5 1 Covered # bin valid_addr[6] 3 1 Covered # bin valid_addr[6] 3 1 Covered # bin valid_addr[6] 3 1 Covered # bin valid_addr[6] 4 1 Covered # bin valid_addr[1] 5 1 Covered # bin valid_addr[1] 5 1 Covered # bin valid_addr[1] 6 1 Covered # bin valid_addr[1] 7 7 7 7 7 7 7 7 7 </unnamedi>	#	INSTANCE <unnamed1></unnamed1>	•		
# bin read		COVERPOINT <unnamed1>::Read_Write</unnamed1>	100.000%	1	
# bin write			1	 1	 Covered
# COVERPOINT <unnamedi>::Addr 100.000% 100.000% Covered </unnamedi>				•	
# bin valid_addr[0]		•		•	
# bin valid_addr[0]			•	100.000%	Covered
# bin valid_addr[1]		1		 1	 Covered
# bin valid_addr[2]		·		'	
# bin valid_addr[3]			I 6	1	
# bin valid_addr[4]			I 5		
# bin valid_addr[5]					
# bin valid_addr[6]			:	•	
# bin valid_addr[7]				•	
# bin valid_addr[8]					
# bin valid_addr[9]			I 4	•	
# bin valid_addr[10]					
# bin valid_addr[11]					
# bin valid_addr[12]				'	
# bin valid_addr[13]				•	
# bin valid_addr[14]					
# bin valid_addr[15]					
# bin valid_addr[16]				•	
# bin valid_addr[17]					
# bin valid_addr[18]					
# bin valid_addr[19]					
# bin valid_addr[20]					
# bin valid_addr[21] 5 1 Covered # bin valid_addr[22] 3 1 Covered # bin valid_addr[23] 2 1 Covered # bin valid_addr[24] 4 1 Covered # bin valid_addr[25] 3 1 Covered # bin valid_addr[26] 4 1 Covered # bin valid_addr[27] 3 1 Covered # bin valid_addr[28] 6 1 Covered # bin valid_addr[28] 5 1 Covered # bin valid_addr[30] 2 1 Covered # bin valid_addr[31] 3 1 Covered # default bin invalid_addr 10 - Occurred # COVERPOINT <unnamed1>::Error 100.000% 100.000% Covered # bin valid_trans 124 1 Covered # bin error 10 1 Covered</unnamed1>					
# bin valid_addr[22]				•	
# bin valid_addr[23]			•	•	
# bin valid_addr[24]				•	
# bin valid_addr[25]					
# bin valid_addr[26]					
# bin valid_addr[27]					
# bin valid_addr[28]				•	
# bin valid_addr[29] 5 1 Covered # bin valid_addr[30] 2 1 Covered # bin valid_addr[31] 3 1 Covered # default bin invalid_addr 10 - Occurred #					
# bin valid_addr[30]					
# bin valid_addr[31]				•	
# default bin invalid_addr 10 - Occurred					
# # COVERPOINT <unnamed1>::Error 100.000% 100.000% Covered # # bin valid_trans 124 1 Covered # bin error 10 1 Covered # </unnamed1>					
# COVERPOINT <unnamed1>::Error 100.000% 100.000% Covered # </unnamed1>			•	•	Occurred
# bin valid_trans 124 1 Covered # bin error 10 1 Covered #			•		
# bin error 10 1 Covered		•	•		
# iiii	#	bin valid_trans	124	1	Covered
		•		•	
# COVERPOINT <unnamed1>::Write_Data 100.000% 100.000% Covered </unnamed1>	#	COVERPOINT <unnamed1>::Write_Data</unnamed1>	100.000%	100.000%	Covered
# bin low 18 1 Covered		'	•	•	
# bin mid1 50 1 Covered	#	bin mid1	50	1	Covered

#	bin mid2	26	l 1	Covered
#	bin high	40	1	
#				
#	COVERPOINT <unnamed1>::Read_Data</unnamed1>	100.000%	100.000%	Covered
#				
#	bin low	46	1	Covered
#	bin mid1	10		Covered
#	bin mid2	12	1	Covered
#	bin high	14	1	Covered
#	CDOSS (UNIVAMEDI) Addr. svg. write	100.000%	100 000%	
# #	CROSS <unnamed1>::Addr_cvr_write</unnamed1>	100.000%	1	Covered
#	bin <write,valid_addr[0]></write,valid_addr[0]>	1 2	1	Covered
#	bin <write,valid_addr[1]></write,valid_addr[1]>	1 2	1	Covered
#	bin <write,valid_addr[2]></write,valid_addr[2]>	1 3	1	Covered
#	bin <write,valid_addr[3]></write,valid_addr[3]>		1	Covered
#	bin <write,valid_addr[4]></write,valid_addr[4]>	1 3	1	Covered
#	bin <write,valid_addr[5]></write,valid_addr[5]>	1 2	1	Covered
#	bin <write,valid_addr[6]></write,valid_addr[6]>	. 2	1	Covered
#	bin <write,valid_addr[7]></write,valid_addr[7]>	. 2	1	Covered
#	bin <write,valid_addr[8]></write,valid_addr[8]>	3	1	Covered
#	bin <write,valid_addr[9]></write,valid_addr[9]>	2	1	Covered
#	bin <write,valid_addr[10]></write,valid_addr[10]>	2	1	Covered
#	bin <write,valid_addr[11]></write,valid_addr[11]>	1	1	Covered
#	bin <write,valid_addr[12]></write,valid_addr[12]>	1	1	Covered
#	bin <write,valid_addr[13]></write,valid_addr[13]>	1	1	Covered
#	bin <write,valid_addr[14]></write,valid_addr[14]>	3	1	Covered
#	bin <write,valid_addr[15]></write,valid_addr[15]>	2	1	Covered
#	bin <write,valid_addr[16]></write,valid_addr[16]>	2	1	Covered
#	bin <write,valid_addr[17]></write,valid_addr[17]>	3	1	Covered
#	bin <write,valid_addr[18]></write,valid_addr[18]>	2	1	Covered
#	bin <write,valid_addr[19]></write,valid_addr[19]>	4	1	Covered
#	bin <write,valid_addr[20]></write,valid_addr[20]>	1	1	Covered
#	bin <write,valid_addr[21]></write,valid_addr[21]>	2	1	Covered
#	bin <write,valid_addr[22]></write,valid_addr[22]>	1	1	Covered
#	bin <write,valid_addr[23]></write,valid_addr[23]>	1		Covered
#	bin <write,valid_addr[24]></write,valid_addr[24]>	1		Covered
#	bin <write,valid_addr[25]></write,valid_addr[25]>	1		Covered
#	bin <write,valid_addr[26]></write,valid_addr[26]>	1	1	Covered
#	bin <write,valid_addr[27]></write,valid_addr[27]>	2		Covered
#	bin <write,valid_addr[28]></write,valid_addr[28]>	3		Covered
#	bin <write,valid_addr[29]></write,valid_addr[29]>	3		Covered
#	bin <write,valid_addr[30]></write,valid_addr[30]>	1		Covered
#	bin <write,valid_addr[31]> ignore bin unused</write,valid_addr[31]>	2 62] <u> </u>	Covered
# #	Tyllore bill ullused		- 	Occurred
#		100.000%	•	'
#				
#	 bin <read,valid_addr[0]></read,valid_addr[0]>	1		Covered
#	bin <read,valid_addr[1]></read,valid_addr[1]>	1 2		Covered
#	bin <read,valid_addr[2]></read,valid_addr[2]>	3		Covered
#	bin <read,valid_addr[3]></read,valid_addr[3]>	4		Covered

,	- · ···		,	J
#	bin <read,valid_addr[4]></read,valid_addr[4]>	2	1	Covered
#	bin <read,valid_addr[5]></read,valid_addr[5]>	3	1	Covered
#	bin <read,valid_addr[6]></read,valid_addr[6]>	1	1	Covered
#	bin <read,valid_addr[7]></read,valid_addr[7]>	2	1	Covered
#	bin <read,valid_addr[8]></read,valid_addr[8]>	1	1	Covered
#	bin <read,valid_addr[9]></read,valid_addr[9]>	2	1	Covered
#	bin <read,valid_addr[10]></read,valid_addr[10]>	2	1	Covered
#	bin <read,valid_addr[11]></read,valid_addr[11]>	1	1	Covered
#	bin <read,valid_addr[12]></read,valid_addr[12]>	2	1	Covered
#	bin <read,valid_addr[13]></read,valid_addr[13]>	2	1	Covered
#	bin <read,valid_addr[14]></read,valid_addr[14]>	3	1	Covered
#	bin <read,valid_addr[15]></read,valid_addr[15]>	3	1	Covered
#	bin <read,valid_addr[16]></read,valid_addr[16]>	1	1	Covered
#	bin <read,valid_addr[17]></read,valid_addr[17]>	1	1	Covered
#	bin <read,valid_addr[18]></read,valid_addr[18]>	2	1	Covered
#	bin <read,valid_addr[19]></read,valid_addr[19]>	1	1	Covered
#	bin <read,valid_addr[20]></read,valid_addr[20]>	1	1	Covered
#	bin <read,valid_addr[21]></read,valid_addr[21]>	3	1	Covered
#	bin <read,valid_addr[22]></read,valid_addr[22]>	2	1	Covered
#	bin <read,valid_addr[23]></read,valid_addr[23]>	1	1	Covered
#	bin <read,valid_addr[24]></read,valid_addr[24]>	3	1	Covered
#	bin <read,valid_addr[25]></read,valid_addr[25]>	2	1	Covered
#	bin <read,valid_addr[26]></read,valid_addr[26]>	3	1	Covered
#	bin <read,valid_addr[27]></read,valid_addr[27]>	1	1	Covered
#	bin <read,valid_addr[28]></read,valid_addr[28]>	3	1	Covered
#	bin <read,valid_addr[29]></read,valid_addr[29]>	2	1	Covered
#	bin <read,valid_addr[30]></read,valid_addr[30]>	1	1	Covered
#	bin <read,valid_addr[31]></read,valid_addr[31]>	1	1	Covered
#	ignore bin unused	62	-	Occurred
#				
#	CROSS <unnamed1>::WData_cvr_write</unnamed1>	100.000%	100.000%	Covered
#				
#	bin <write,low></write,low>	15	1	Covered
#	bin <write,mid1></write,mid1>	14	1	Covered
#	bin <write,mid2></write,mid2>	16	1	Covered
#	bin <write,high></write,high>	22	1	Covered
#	ignore bin unused	67	-	Occurred
#				
#	CROSS <unnamed1>::RData_cvr_read</unnamed1>	•		
#				
#	bin <read,low></read,low>	28		Covered
#	bin <read,mid1></read,mid1>	9	1	Covered
#	bin <read,mid2></read,mid2>	11	1	Covered
#	bin <read,high></read,high>	14	1	Covered
#	ignore bin unused	20		Occurred
#		•	•	
#	CROSS <unnamed1>::Err_cvr_write</unnamed1>			
# #	 bin <write,error></write,error>	5	•	 Covered
#	ignore bin unused_write			Covered Occurred
#	ignore bin no_error	1 124		Occurred Occurred
#		•	'	
#		1		

```
| CROSS <UNNAMED1>::Err_cvr_read | 100.000% | 100.000% | Covered |
#
   #
   | bin <read,error>
                               5 l
                                     1 | Covered |
#
   | ignore bin unused_read
                          67 |
                                      | Occurred |
#
   | ignore bin no_error
                              124 |
                          | Occurred |
 ++++++++
          DESIGN UNITS
 CUMULATIVE SUMMARY
 _____
    Coverage Type | Weight | Hits/Total |
 _____
 | Covergroup Coverage | 1 | 100.000% |
|-----|
# | Types
                   CUMULATIVE DESIGN-BASED COVERAGE: 100.000%
# COVERED DESIGN UNITS: 1 / 1
# FILES: 1
CLASS - work.monitor
#
   SUMMARY
      Coverage Type | Weight | Hits/Total |
   | Covergroup Coverage |
                     1 | 100.000% |
   |-----|
                 - 1
   WEIGHTED AVERAGE: 100.000%
   COVERGROUP COVERAGE
           Covergroup
                          1
                           Hits
                                | Goal / | Status |
                                | At Least |
                         | 100.000% | 100.000% | Covered |
#
   | TYPE /monitor/apb_data
   _____
   | INSTANCE <UNNAMED1>
                         | 100.000% | 100.000% | Covered |
#
   |-----|----|-----|-----|
   | COVERPOINT <UNNAMED1>::Read_write | 100.000% | 100.000% | Covered |
#
   |-----|----|-----|-----|
   | bin read
                               67 I
                                      1 | Covered |
```

#	bin write	67	_	Covered
# # #	COVERPOINT <unnamed1>::Addr</unnamed1>	100.000%	100.000%	 Covered
# #	 bin valid_addr[0]	3	 1	 Covered
#	bin valid_addr[1]	3	1 1	Covered Covered
#	bin valid_addr[2]	1 6	1 1	Covered
#	bin valid_addr[3]	l 5	1 1	Covered
#	bin valid_addr[4]	, 5 5	1 1	Covered Covered
#	bin valid_addr[5]	, 5 5	1 1	Covered
	bin valid_addr[6]	, 3 3		Covered Covered
#	bin valid_addr[6] bin valid_addr[7]		1 1	•
#		4		Covered
#	bin valid_addr[8]	4	1	Covered
#	bin valid_addr[9]	4	1	Covered
#	bin valid_addr[10]	4	1	Covered
#	bin valid_addr[11]	2	1	Covered
#	bin valid_addr[12]	3	1	Covered
#	bin valid_addr[13]	3	1	Covered
#	bin valid_addr[14]	6	1	Covered
#	bin valid_addr[15]	5	1	Covered
#	bin valid_addr[16]	3	1	Covered
#	bin valid_addr[17]	4	1	Covered
#	bin valid_addr[18]	4	1	Covered
#	bin valid_addr[19]	5	1	Covered
#	bin valid_addr[20]	2	1	Covered
#	bin valid_addr[21]	5	1	Covered
#	bin valid_addr[22]	3	1	Covered
#	bin valid_addr[23]	2	1	Covered
#	bin valid_addr[24]	4	1	Covered
#	bin valid_addr[25]] 3	1	Covered
#	bin valid_addr[26]	4	1	Covered
#	bin valid_addr[27]] 3	1	Covered
#	bin valid_addr[28]	6	1	Covered
#	bin valid_addr[29]	5	1	Covered
#	bin valid_addr[30]	2	1	Covered
#	bin valid_addr[31]	3	1	Covered
# #	default bin invalid_addr	10	'	Occurred
# #	COVERPOINT <unnamed1>::Error</unnamed1>	100.000%	100.000%	Covered
#	bin valid_trans	124	•	 Covered
# #	bin error 	10	'	Covered
#	COVERPOINT <unnamed1>::Write_Data</unnamed1>	100.000%	100.000%	Covered
# #	 bin low	•	•	 Covered
#	bin mid1	50	1	Covered
#	bin mid2	26	1	Covered
#	bin high 	•	•	Covered
# # #	COVERPOINT <unnamed1>::Read_Data</unnamed1>	100.000%	100.000%	Covered

			= -	=
#	bin low	46	1	Covered
#	bin mid1	10	1	Covered
#	bin mid2	12	1	Covered
#	bin high	14	1	Covered
#				
#	CROSS <unnamed1>::Addr_cvr_write</unnamed1>	100.000%	100.000%	Covered
#				
#	bin <write,valid_addr[0]></write,valid_addr[0]>	2	1	Covered
#	bin <write,valid_addr[1]></write,valid_addr[1]>	2	1	Covered
#	bin <write,valid_addr[2]></write,valid_addr[2]>	3	1	Covered
#	bin <write,valid_addr[3]></write,valid_addr[3]>	1	1	Covered
#	bin <write,valid_addr[4]></write,valid_addr[4]>	3	1	Covered
#	bin <write,valid_addr[5]></write,valid_addr[5]>	2	1	Covered
#	bin <write,valid_addr[6]></write,valid_addr[6]>	2	1	Covered
#	bin <write,valid_addr[7]></write,valid_addr[7]>	2	1	Covered
#	bin <write,valid_addr[8]></write,valid_addr[8]>	3	1	Covered
#	bin <write,valid_addr[9]></write,valid_addr[9]>	2	1	Covered
#	bin <write,valid_addr[10]></write,valid_addr[10]>	2	1	Covered
#	bin <write,valid_addr[11]></write,valid_addr[11]>	1	1	Covered
#	bin <write,valid_addr[12]></write,valid_addr[12]>	1	1	Covered
#	bin <write,valid_addr[13]></write,valid_addr[13]>	1	1	Covered
#	bin <write,valid_addr[14]></write,valid_addr[14]>	3	1	Covered
#	bin <write,valid_addr[15]></write,valid_addr[15]>	2	1	Covered
#	bin <write,valid_addr[16]></write,valid_addr[16]>	2	1	Covered
#	bin <write,valid_addr[17]></write,valid_addr[17]>	3	1	Covered
#	bin <write,valid_addr[18]></write,valid_addr[18]>	2	1	Covered
#	bin <write,valid_addr[19]></write,valid_addr[19]>	4	1	Covered
#	bin <write,valid_addr[20]></write,valid_addr[20]>	1	1	Covered
#	bin <write,valid_addr[21]></write,valid_addr[21]>	2	1	Covered
#	bin <write,valid_addr[22]></write,valid_addr[22]>	1	1	Covered
#	bin <write,valid_addr[23]></write,valid_addr[23]>	1	1	Covered
#	bin <write,valid_addr[24]></write,valid_addr[24]>	1	1	Covered
#	bin <write,valid_addr[25]></write,valid_addr[25]>	1	1	Covered
#	bin <write,valid_addr[26]></write,valid_addr[26]>	1	1	Covered
#	bin <write,valid_addr[27]></write,valid_addr[27]>	2	1	Covered
#	bin <write,valid_addr[28]></write,valid_addr[28]>	3		Covered
#	bin <write,valid_addr[29]></write,valid_addr[29]>	3		Covered
#	bin <write,valid_addr[30]></write,valid_addr[30]>	1		Covered
#	bin <write,valid_addr[31]></write,valid_addr[31]>	2	1	Covered
#	ignore bin unused	62	-	Occurred
#	ļ		'	
#		100.000%		
#	I	•		•
#	bin <read,valid_addr[0]></read,valid_addr[0]>	1		Covered
#	bin <read, valid_addr[1]=""></read,>	2		Covered
#	bin <read, valid_addr[2]=""></read,>	3		Covered
#	bin <read,valid_addr[3]></read,valid_addr[3]>	4		Covered
#	bin <read, valid_addr[4]=""></read,>	2		Covered
#	bin <read,valid_addr[5]></read,valid_addr[5]>	3		Covered
#	bin <read,valid_addr[6]></read,valid_addr[6]>	1		Covered
#	bin <read,valid_addr[7]></read,valid_addr[7]>	2		Covered
#	bin <read,valid_addr[8]></read,valid_addr[8]>	1	1	Covered

— . , —	-		,	J
#	bin <read,valid_addr[9]></read,valid_addr[9]>	2	1	Covered
#	bin <read,valid_addr[10]></read,valid_addr[10]>	2	1	Covered
#	bin <read,valid_addr[11]></read,valid_addr[11]>	1	1	Covered
#	bin <read,valid_addr[12]></read,valid_addr[12]>	2	1	Covered
#	bin <read,valid_addr[13]></read,valid_addr[13]>	2	1	Covered
#	bin <read,valid_addr[14]></read,valid_addr[14]>	3	1	Covered
#	bin <read,valid_addr[15]></read,valid_addr[15]>	3	1	Covered
#	bin <read,valid_addr[16]></read,valid_addr[16]>	1	1	Covered
#	bin <read,valid_addr[17]></read,valid_addr[17]>	1	1	Covered
#	bin <read,valid_addr[18]></read,valid_addr[18]>	2	1	Covered
#	bin <read,valid_addr[19]></read,valid_addr[19]>	1	1	Covered
#	bin <read,valid_addr[20]></read,valid_addr[20]>	1	1	Covered
#	bin <read,valid_addr[21]></read,valid_addr[21]>	3	1	Covered
#	bin <read,valid_addr[22]></read,valid_addr[22]>	2	1	Covered
#	bin <read,valid_addr[23]></read,valid_addr[23]>	1	1	Covered
#	bin <read,valid_addr[24]></read,valid_addr[24]>	3	1	Covered
#	bin <read,valid_addr[25]></read,valid_addr[25]>	2	1	Covered
#	bin <read,valid_addr[26]></read,valid_addr[26]>	3	1	Covered
#	bin <read,valid_addr[27]></read,valid_addr[27]>	1	1	Covered
#	bin <read,valid_addr[28]></read,valid_addr[28]>	3	1	Covered
#	bin <read,valid_addr[29]></read,valid_addr[29]>	2	1	Covered
#	bin <read,valid_addr[30]></read,valid_addr[30]>	1	1	Covered
#	bin <read,valid_addr[31]></read,valid_addr[31]>	1	1	Covered
#	ignore bin unused	62	-	Occurred
#				
#	CROSS <unnamed1>::WData_cvr_write</unnamed1>		100.000%	Covered
# #	bin <write,low></write,low>		 1	 Covered
#	bin <write,mid1></write,mid1>	14	1	Covered Covered
#	bin <write,mid2></write,mid2>	16	1 1	Covered Covered
#	bin <write,high></write,high>	22	1	Covered
#	ignore bin unused	67	-	Occurred
#		•	 	
#	CROSS <unnamed1>::RData_cvr_read</unnamed1>			
# #	 bin <read,low></read,low>	•		
#	bin <read, row=""> bin <read, mid1=""></read,></read,>	•		Covered Covered
#	bin <read, mid2=""></read,>	11		Covered Covered
#	bin <read,mid2> bin <read,high></read,high></read,mid2>	•		Covered Covered
#	ignore bin unused	•		Covered Occurred
#		•		
#	CROSS <unnamed1>::Err_cvr_write</unnamed1>	1	'	
#				
#	bin <write,error></write,error>	5	1	Covered
#	ignore bin unused_write	67	-	Occurred
#	. 5	124		Occurred
#	[
#	CROSS <unnamed1>::Err_cvr_read</unnamed1>			
#				
#	bin <read,error></read,error>	5		Covered
#	ignore bin unused_read	67		Occurred
#	ignore bin no_error	124	-	Occurred

VSIM: Simulation has finished.

Done