

# EE 303

## Course Project



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## Objective

To design schematic of beta multiplier, cascode amplifier and cascode current mirror in LTSpice and design layout is Magic VLSI tool in 180 nm with 1.8V Voltage supply and to design only schematic of cascode amplifier, beta multiplier and cascode current mirror in 22 nm (with 0.8V supply) technology node to see the impact of lowering the technology node.

## Approach

To address the problem, we took a theoretical approach, starting by calculating the bias voltages for each MOSFET in the cascode amplifier circuit. Using these values, we then determined the W/L ratio parameters for all MOSFETs in the design. We simulated the circuit in LTSpice based on these initial values and analyzed the resulting performance. To meet the specified requirements, we fine-tuned the W/L ratios using a trial-and-error method, carefully monitoring both gain and bandwidth. This approach was also applied for 22 nm technology nodes. Finally, we adjusted the bias voltages to ensure the circuit met the desired specifications while maintaining operation in the saturation region.

## Circuit Diagram

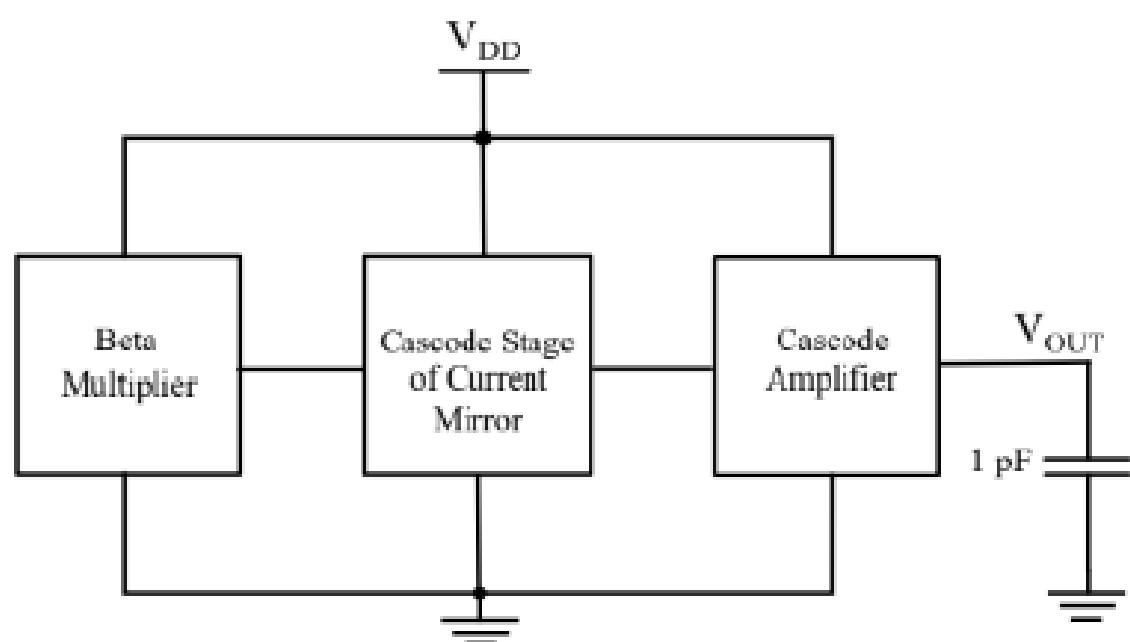


Figure 1: Block diagram of cascode amplifier with other blocks

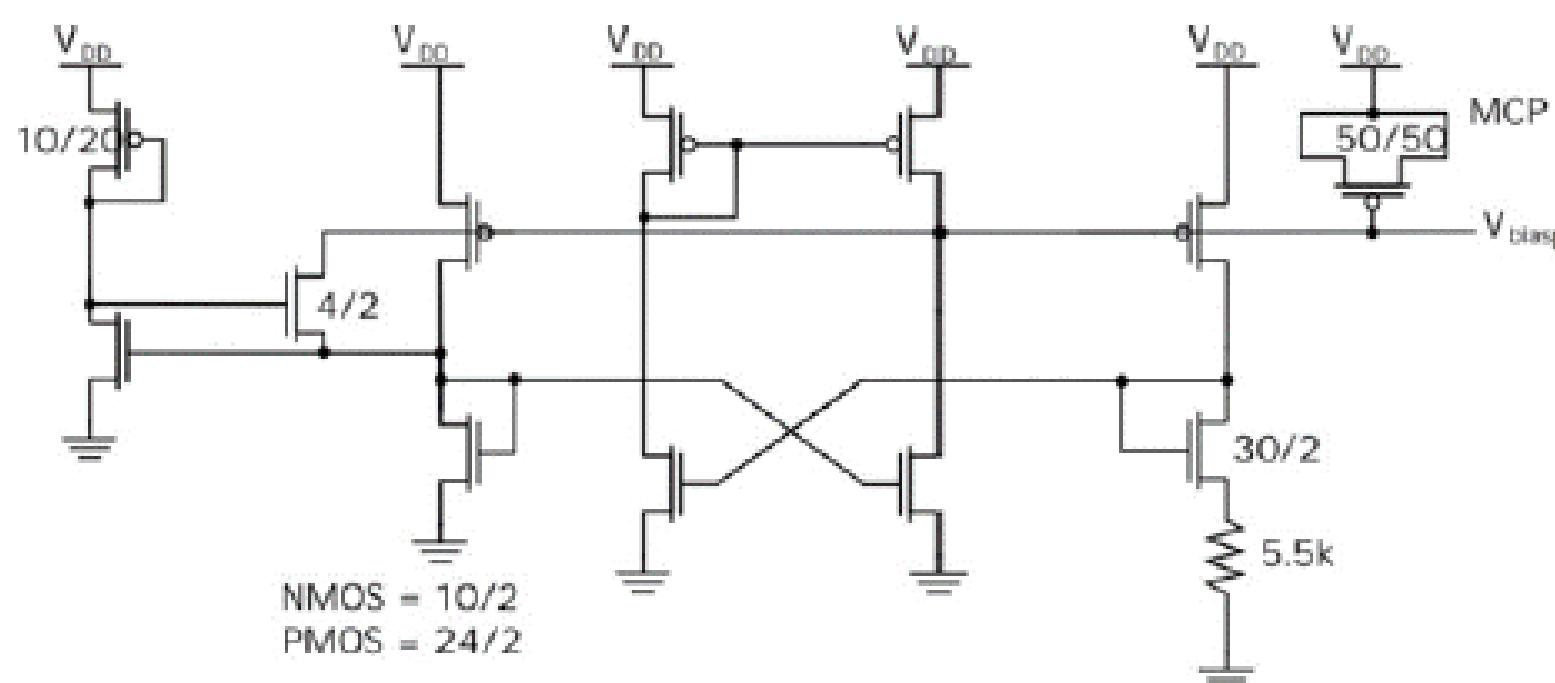


Figure 2: Circuit for beta multiplier circuit

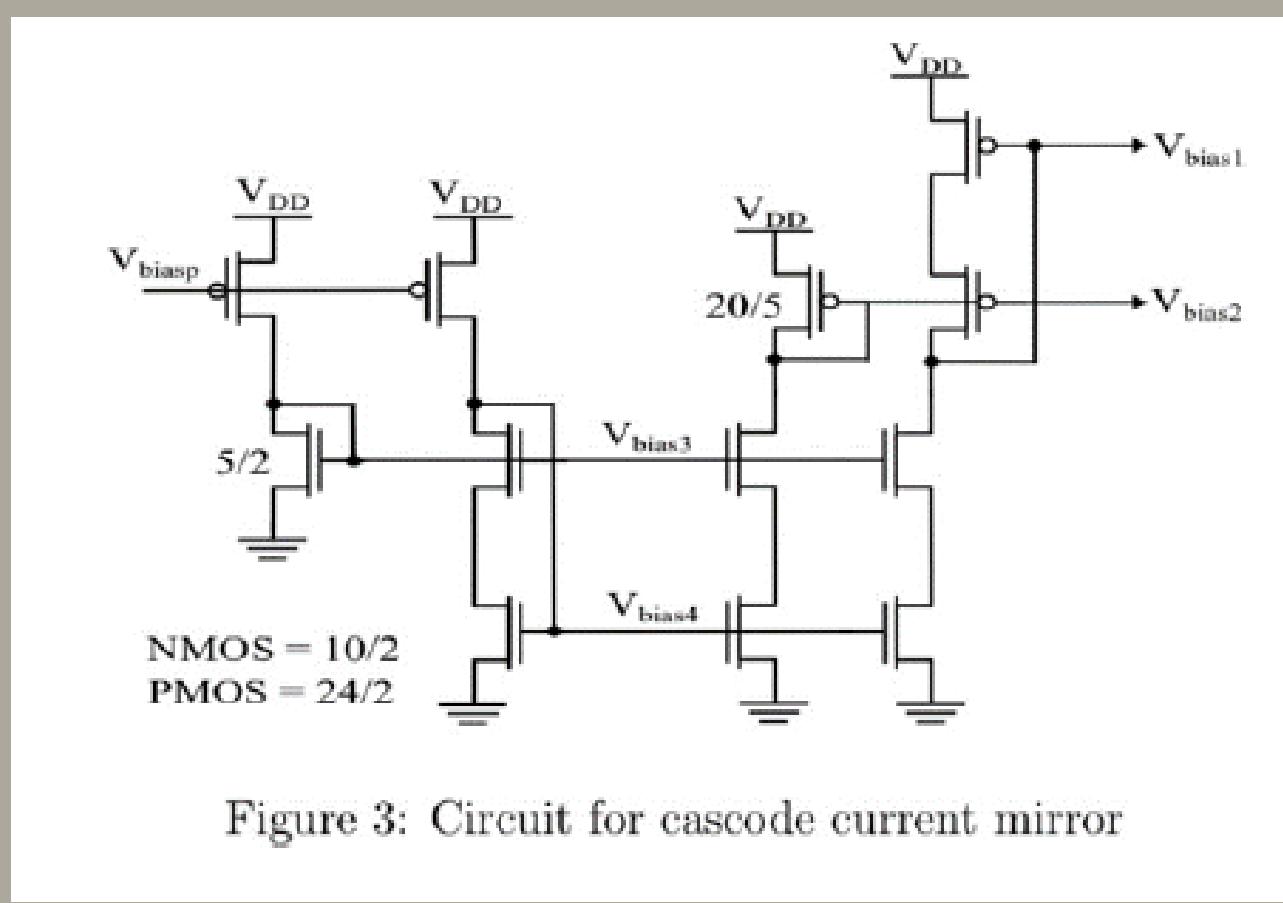


Figure 3: Circuit for cascode current mirror

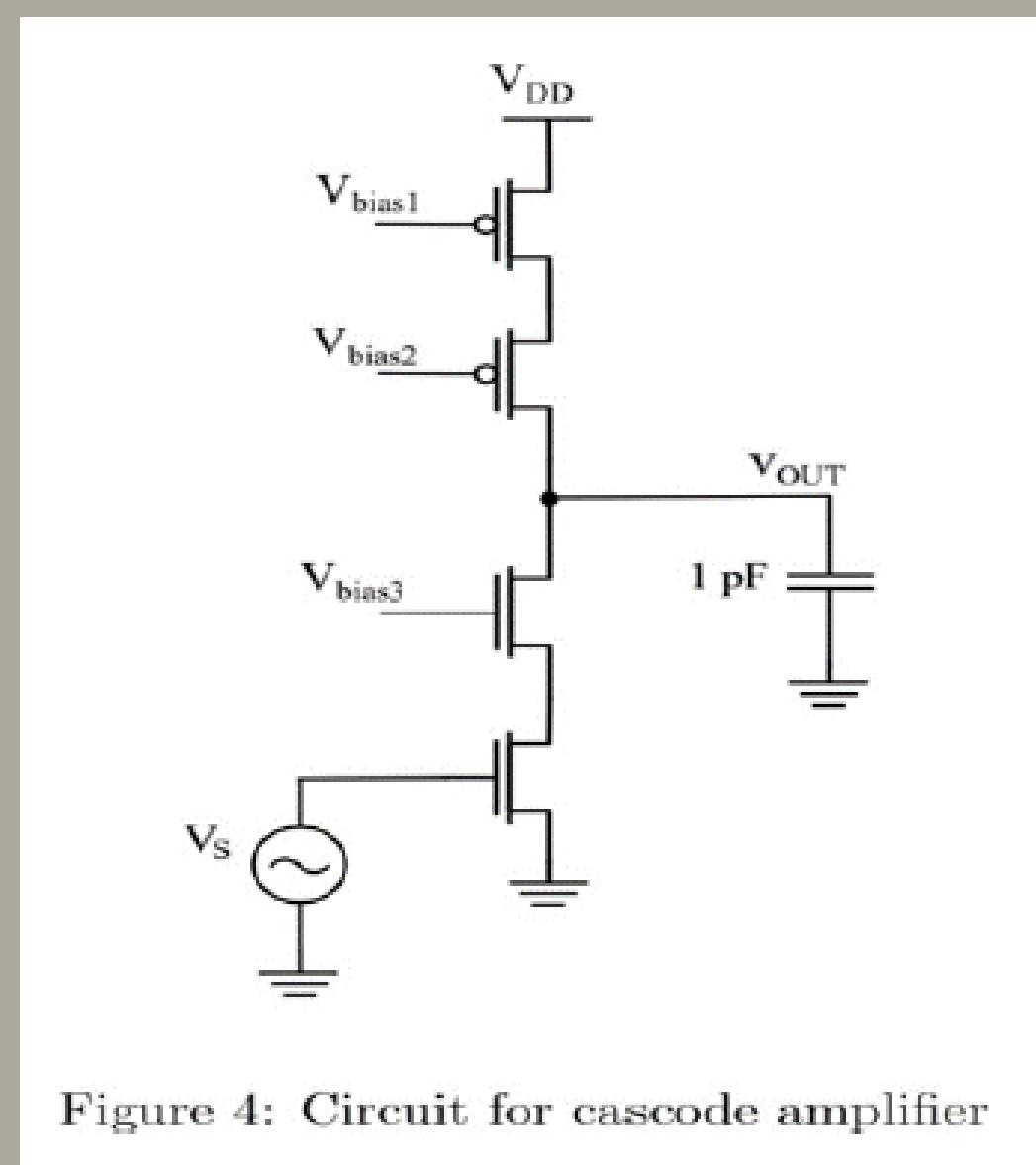
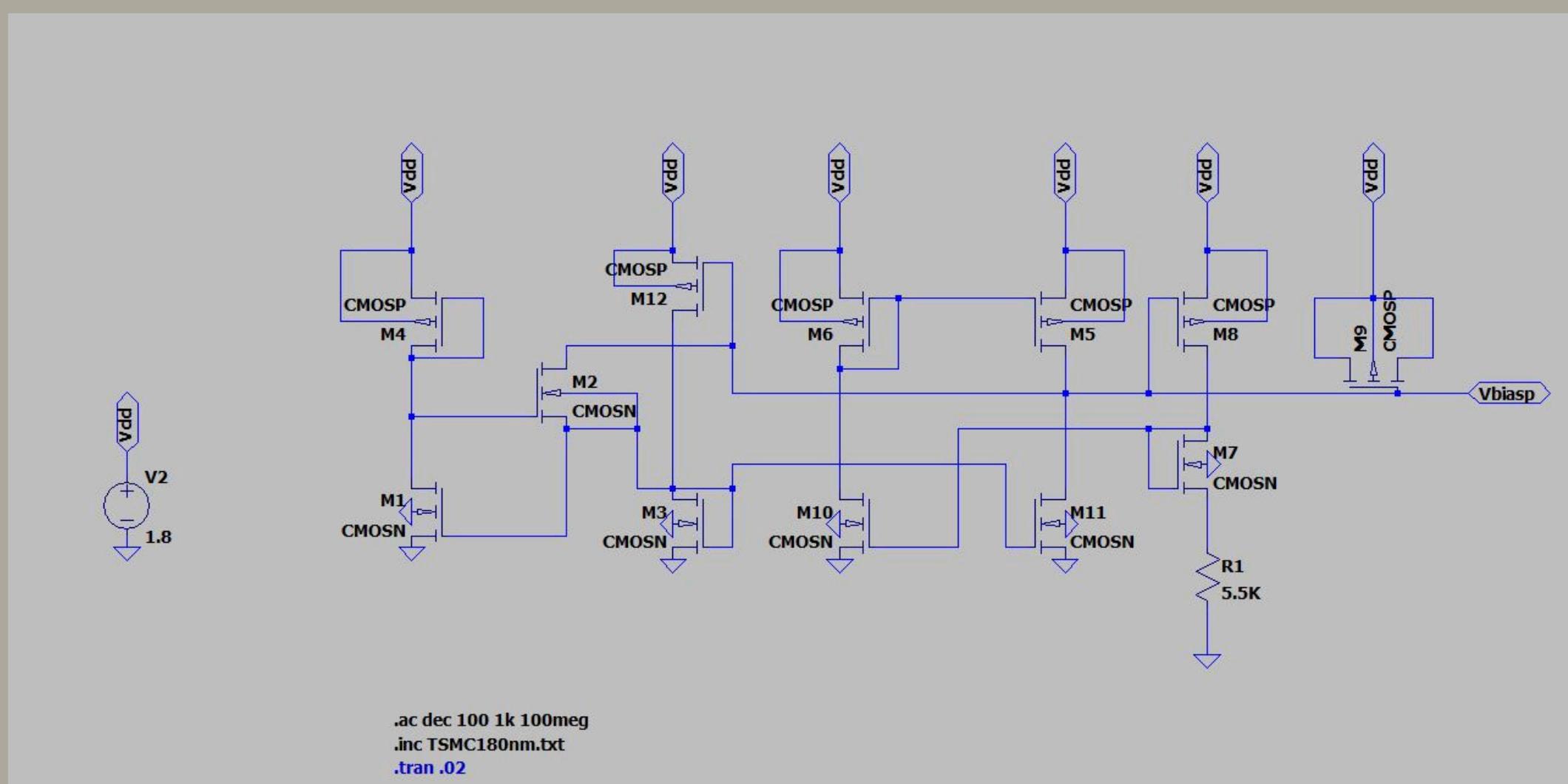


Figure 4: Circuit for cascode amplifier

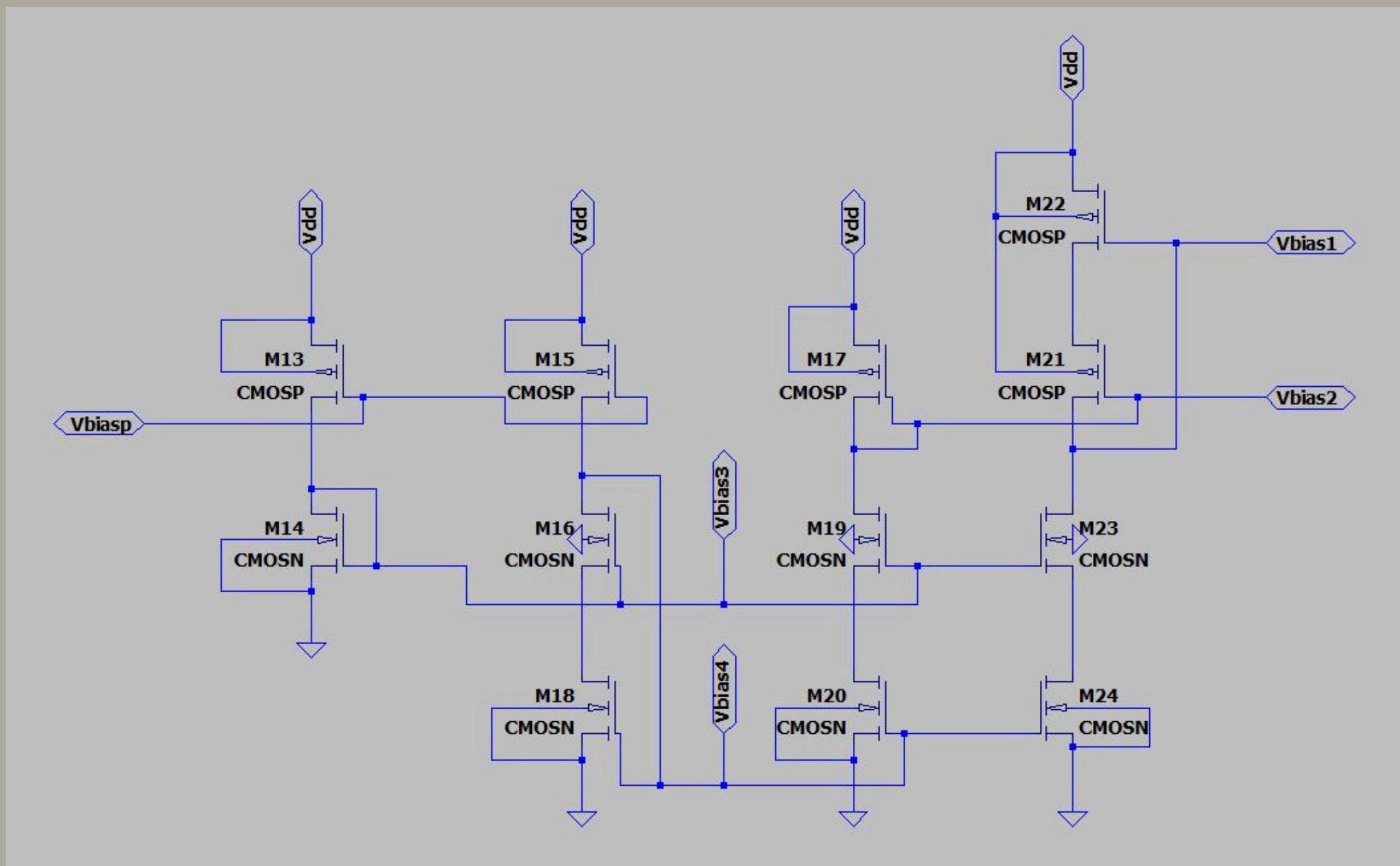
## LT Spice for 180nm

### Simulation Circuit

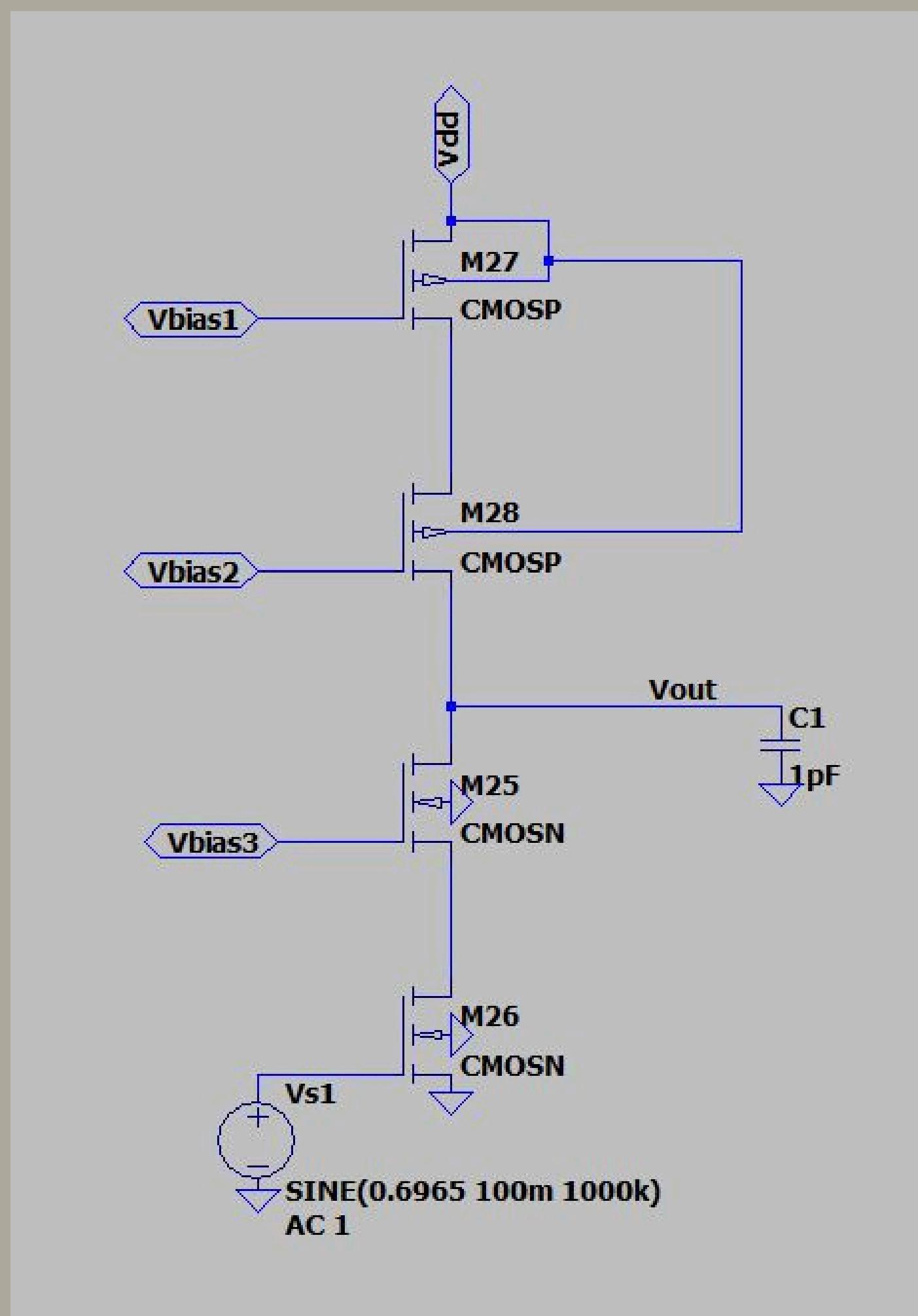
The images below display circuits created in LTSpice for a Beta Multiplier, Cascode Current Mirror, and Cascode Amplifier (180nm technology). The W/L ratios in the Beta Multiplier and Cascode Current Mirror were set based on the specified values, while for the Cascode Amplifier, this ratio was determined through calculations detailed in the following section.



Beta Multiplier



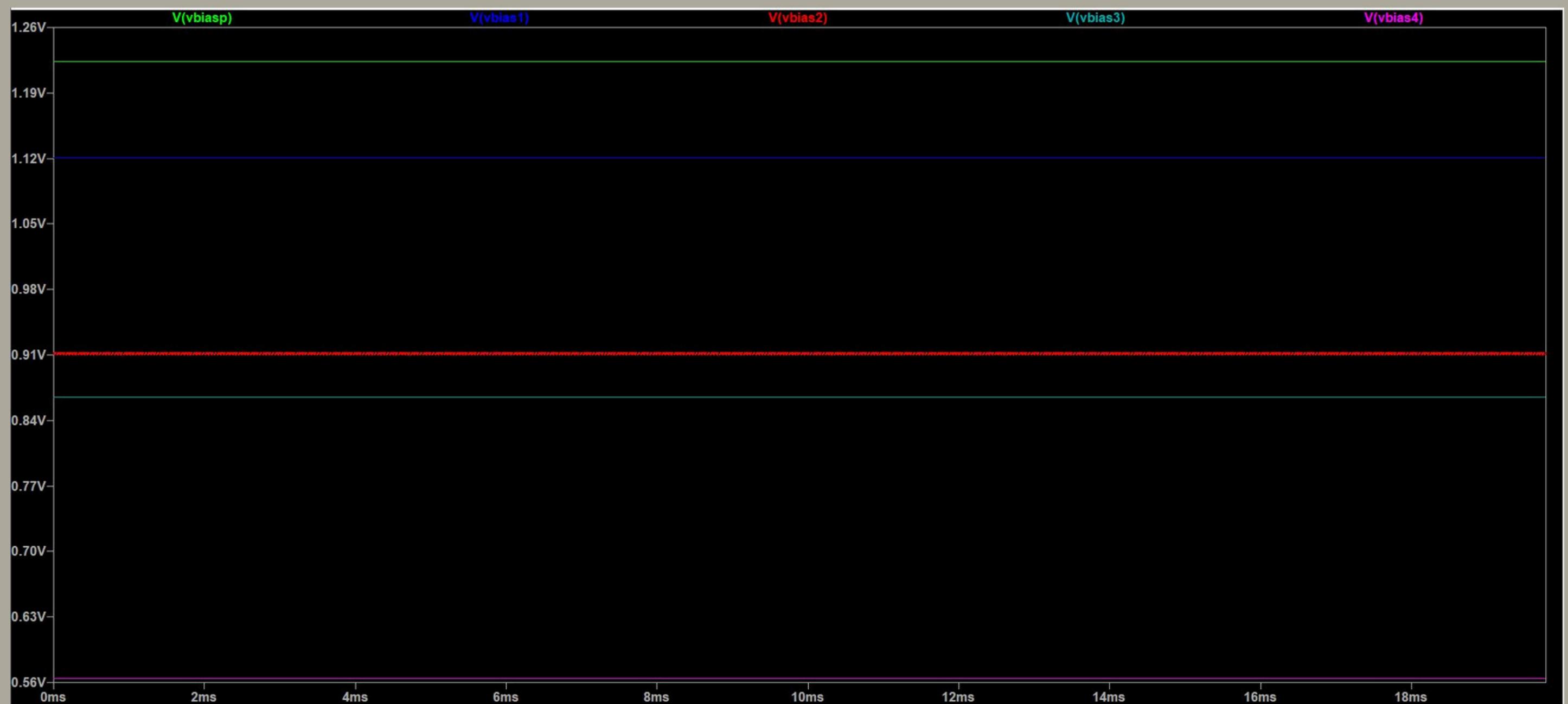
Cascode Current Mirror



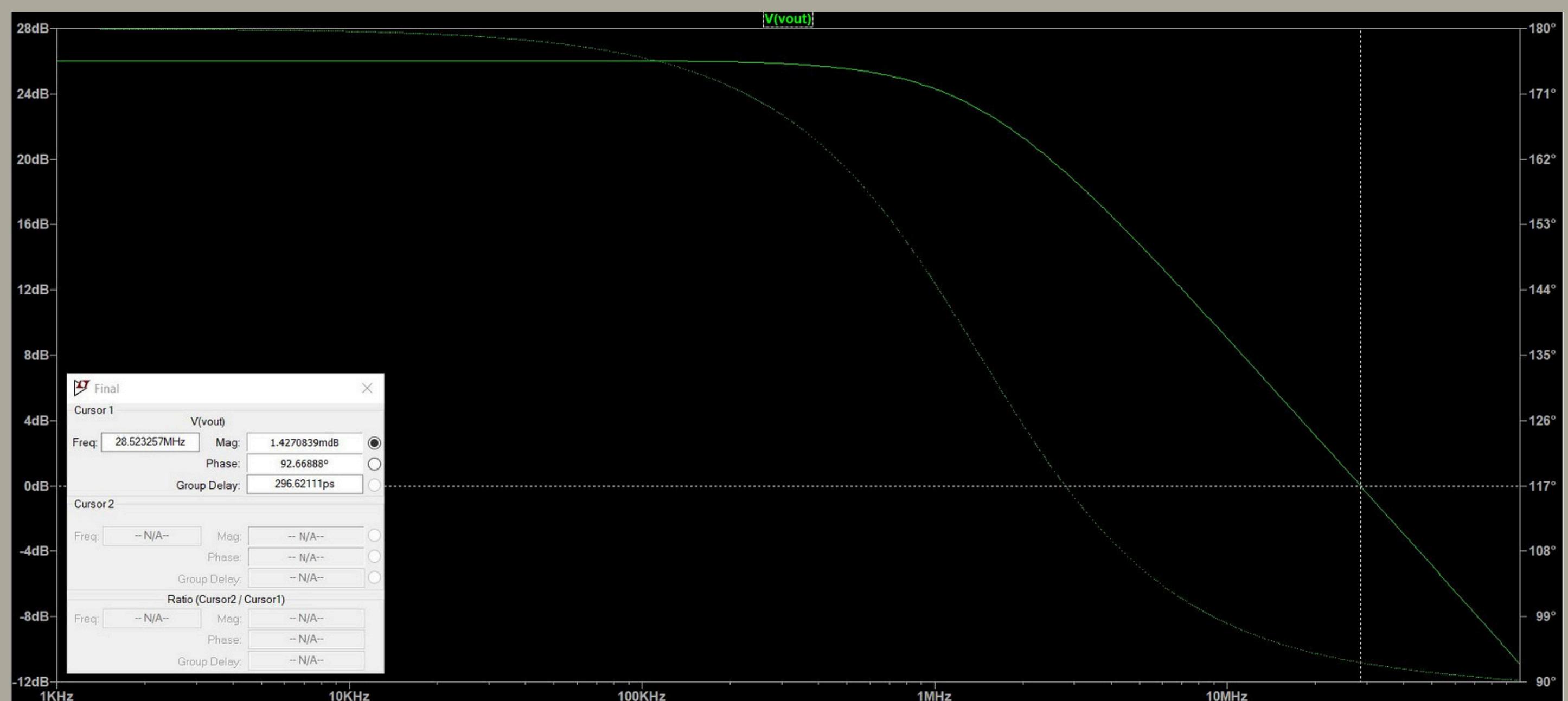
Cascode  
Amplifier

# Simulation Results

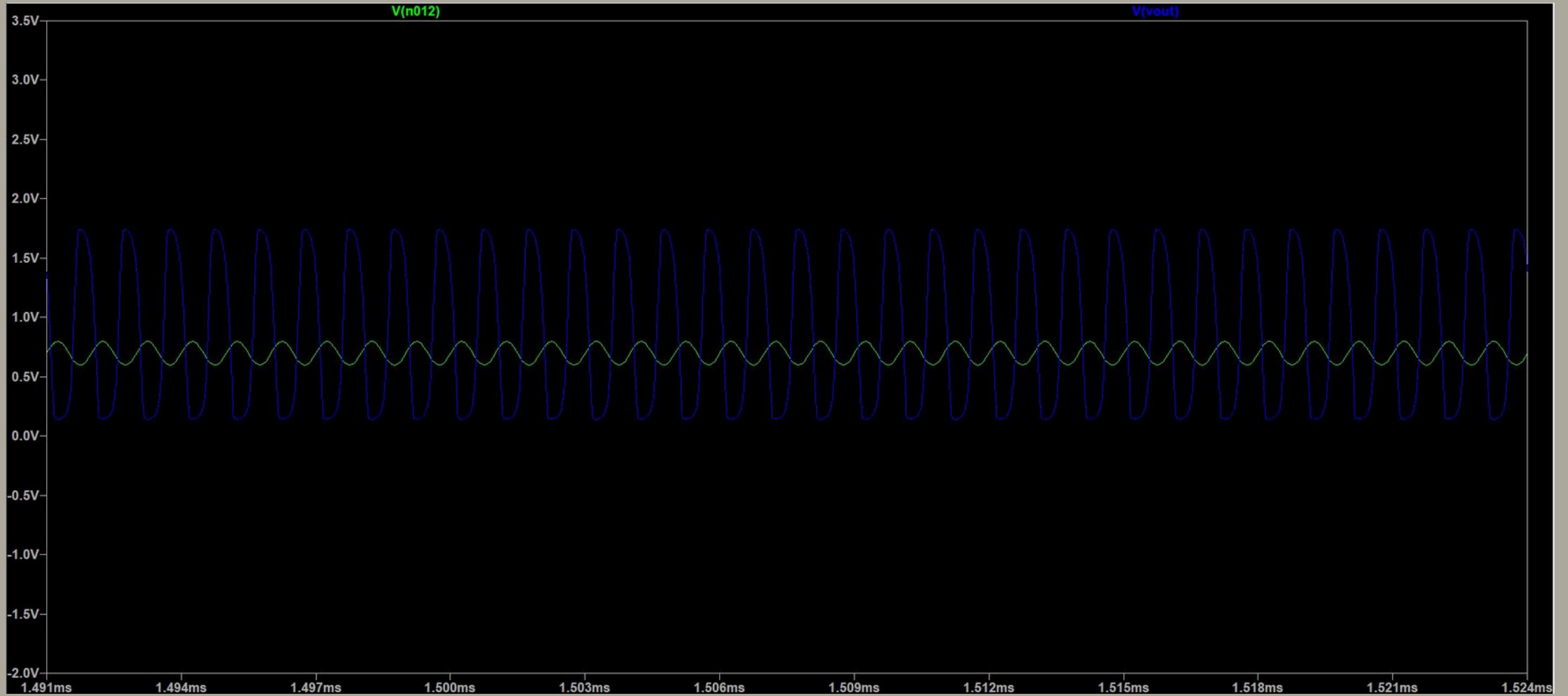
The Simulation outputs obtained were::



Bias Voltages



AC Analysis



**Voutput**

## RESULTS

QUANTITY	VALUE
Vbiasp	1.22V
Vbias1	1.12V
Vbias2	0.91V
Vbias3	0.864V
Vbias4	0.564V
Gain	26.038 dB
UGB	28.523 MHz
Power Consumed	0.064mW

## Calculations

(\*)

$$\text{Given:- } A_V = 20 \text{ V/V} \quad C_{\text{load}} = 1 \text{ pF}$$

$$V_{DD} = 1.8 \text{ V}$$

From the sheet:- (TSMC.txt) 180nm

$$M_n C_{ox} = 350.8 \mu\text{A/V}^2 \quad \lambda = 0.09$$

$$M_p C_{ox} = 71.2 \mu\text{A/V}^2$$

$$V_{TN} = 0.5 \text{ V}$$

$$V_{TP} = 0.51 \text{ V}$$

Constraints :-

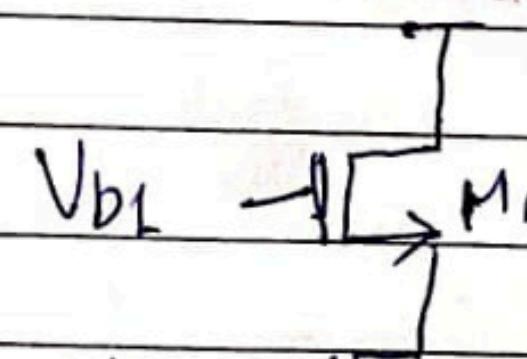
$$\text{Unity gain bandwidth (UGB)} \geq 500 \text{ kHz}$$

$$\text{Power Dissipation (P}_D \text{)} \leq 5 \text{ mW}$$

We can see the Rout of load terminal

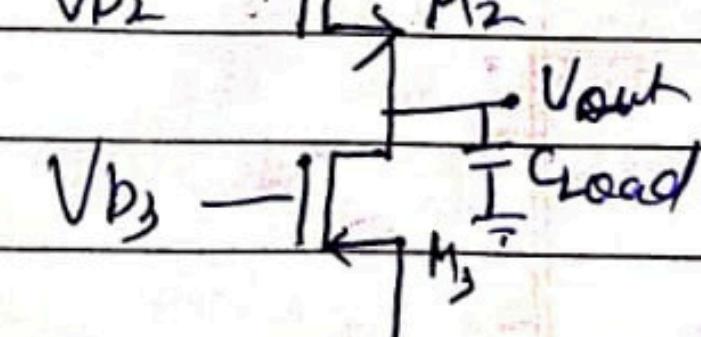
$$R_{\text{out}} \approx (g_{m3} r_{o3} r_{o4})$$

$$\approx (g_{m2} r_{o2} r_{o1})$$

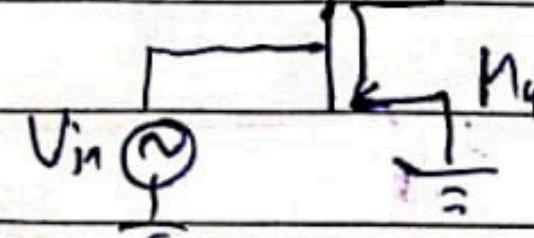


~~gm~~ = Trans

$$G_m = \text{Transconductance of circuit} \\ = g_{m4}$$



$$\therefore \text{Voltage gain (A}_V \text{)} = g_{m4} R_{\text{out}}$$



$\therefore$  We have a load capacitor at Vout node, we will name a pole in bode plot

By method of inspection, location of pole will be at frequency  $f_s$ , which is,

$$f_s = \frac{1}{2\pi \cdot \text{Cond. Rout}}$$

Assuming we want a pole at  $2.8 \text{ MHz}$ , our unity gain frequency will occur ~~at~~ after  $2.8 \text{ MHz}$

$$\therefore UGB > (2.8 \text{ MHz}) > 500 \text{ kHz}$$

$$\therefore R_{out} = \frac{1}{2\pi \times 10^{-12} \times 2.8 \times 10^6} = 56,841 \Omega$$

$$\therefore R_{out} = (g_{m_3} n_{o_3} n_{ay}) || (g_{m_2} n_{o_2} n_{o_1}) = 56,841 \Omega$$

$$A_V = g_{m_4} \cdot R_{out} \Rightarrow g_{m_4} = \frac{A_V}{R_{out}} = \frac{20}{56,841} = 0.000352 \text{ A/V}$$

We have biased gate at  $0.7V$ , hence

$$V_{ov} = V_{GS} - V_{TN} = 0.7 - 0.5 = 0.2V$$

$$\therefore g_{m_4} = \mu_n C_{ox} \left( \frac{W}{L} \right) V_{ov} = 0.000352$$

$$\left( \frac{W}{L} \right)_n = \frac{0.000352}{350.8 \times 10^{-6} \times 0.2} \approx 5$$

$$I_d = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right)_n \times (V_{ov})^2 = \frac{1}{2} \times 350.8 \times 5 \times (0.2)^2 \text{ mA}$$

$$= 35.08 \text{ mA}$$

$$\text{Power consumption} = V_{DD} \cdot I_d = 1.8 \times 35.08 = 0.064 \text{ mW}$$

$$0.064 \mu W < 5 \text{ mW}$$

∴ Power consumption doesn't exceed budget.

$$\therefore \left(\frac{W}{L}\right)_{NMOS} = \frac{5}{1}$$

∴ We have biasing circuit, gate voltage of upper PMOS is known = 1.81 V (simulation)

$$\therefore V_{SG} = 1.8 - 1.11 = 0.68 \text{ V}$$

$$\therefore V_{ov} \text{ of } M_1 = 0.68 - (0.51) = 0.18 \text{ V}$$

∴  $I_d$  is same through  $M_1, M_2, M_3, M_4$ .

$$\therefore I_d = \frac{1}{2} \times \mu_p C_{ox} \left(\frac{W}{L}\right)_{PMOS} \times (V_{ov})$$

$$\therefore \left(\frac{W}{L}\right)_{PMOS} = \frac{35.08 \times 2}{71.2 \times 0.18 \times (0.18)^2} = 24.0$$

$$\therefore \left(\frac{W}{L}\right)_{PMOS} \approx \frac{24}{1}$$

$$\therefore \left(\frac{W}{L}\right)_{NMOS} = \frac{5}{1} \quad \therefore W = 5 \times 180 = 900 \text{ nm} \\ L = 1 \times 180 = 180 \text{ nm}$$

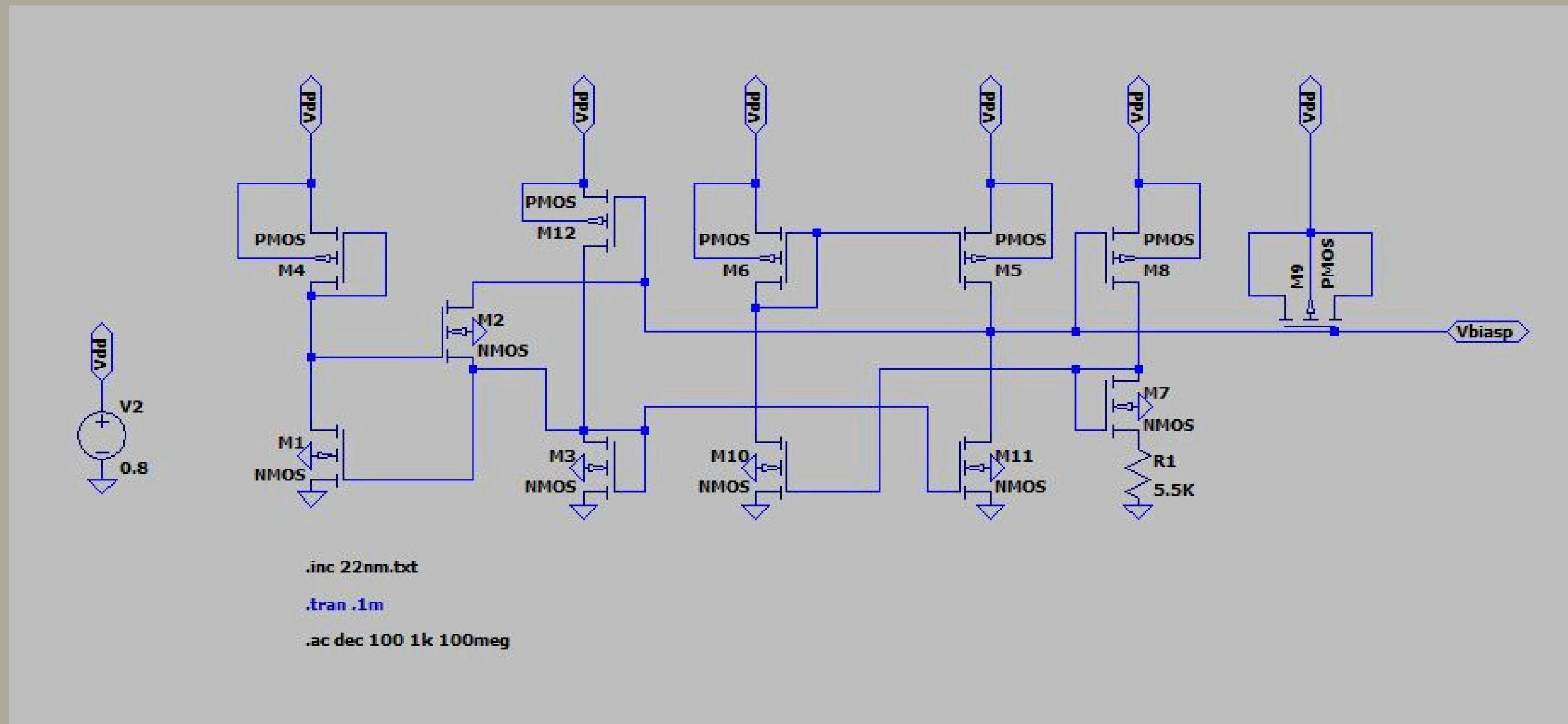
$$\left(\frac{W}{L}\right)_{PMOS} = \frac{24}{1} \quad \therefore W = 24 \times 180 = 4320 \text{ nm} \\ L = 1 \times 180 = 180 \text{ nm}$$

We got the required gain of 20 V/V (26.02 dB) and met the conditions of unity gain bandwidth (> 500KHz) and Power consumtion (<5mW).

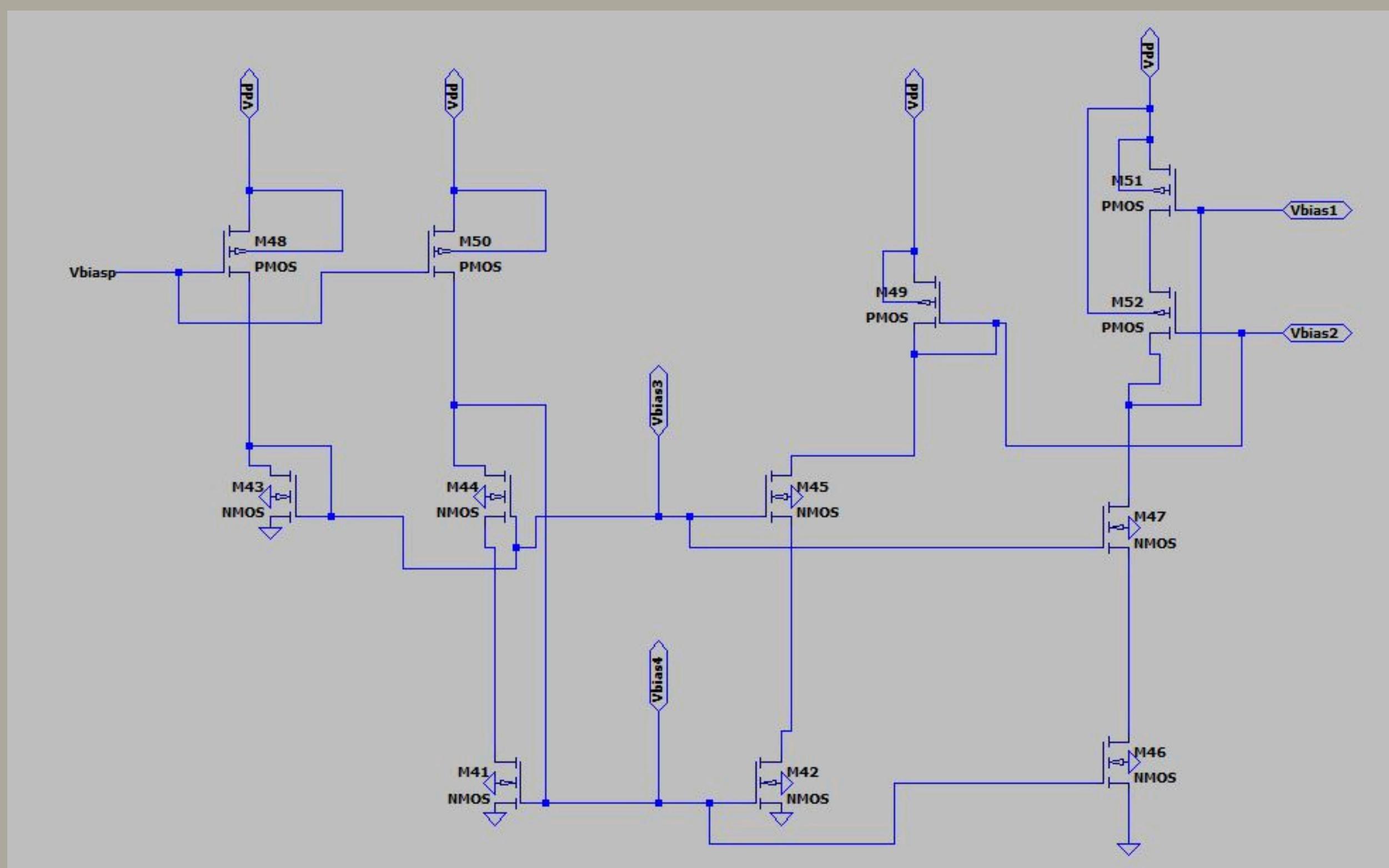
# LT Spice for 22 nm

We perform similar analysis for 22nm Technology.

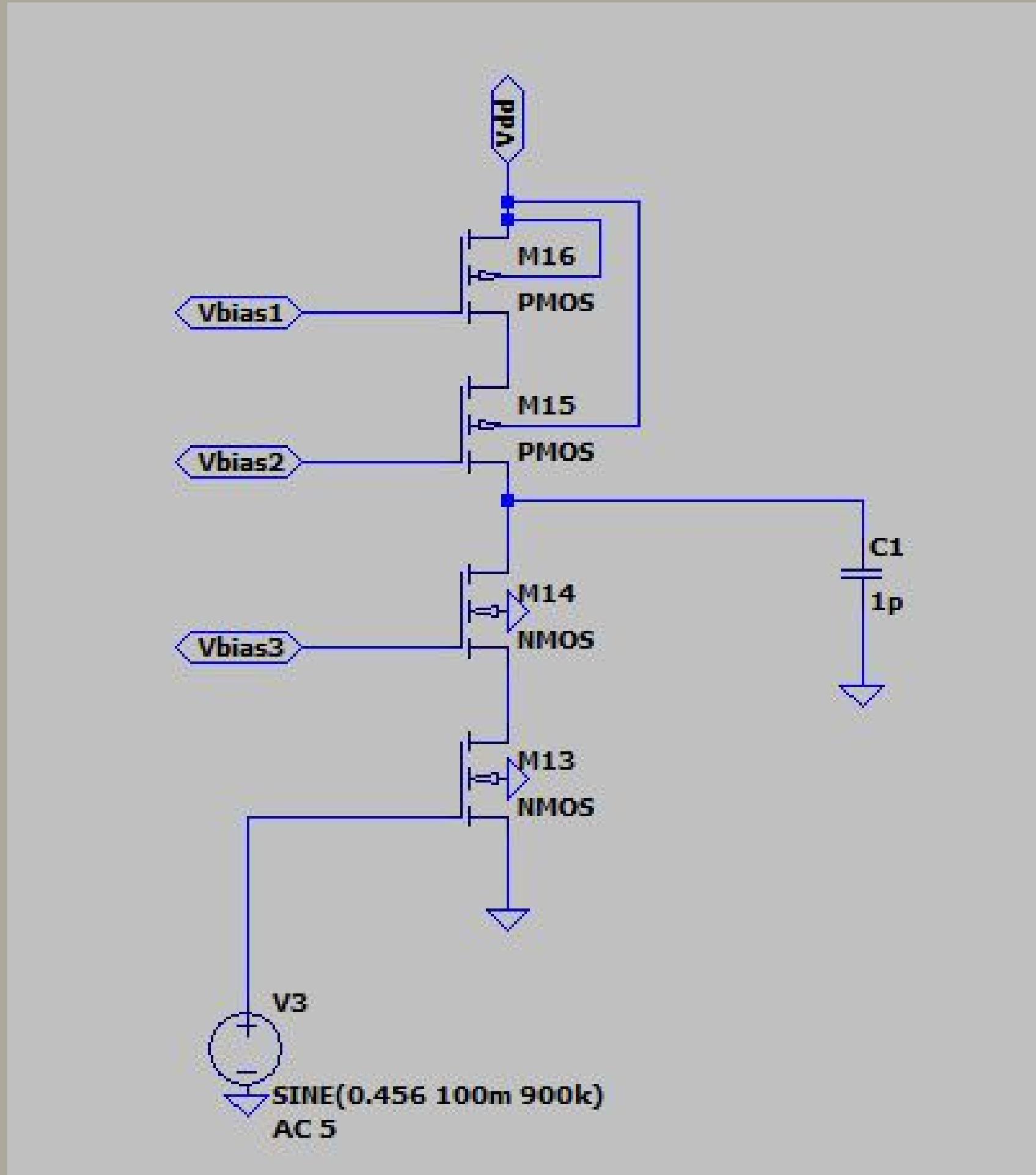
## Simulation Circuit



Beta Multiplier



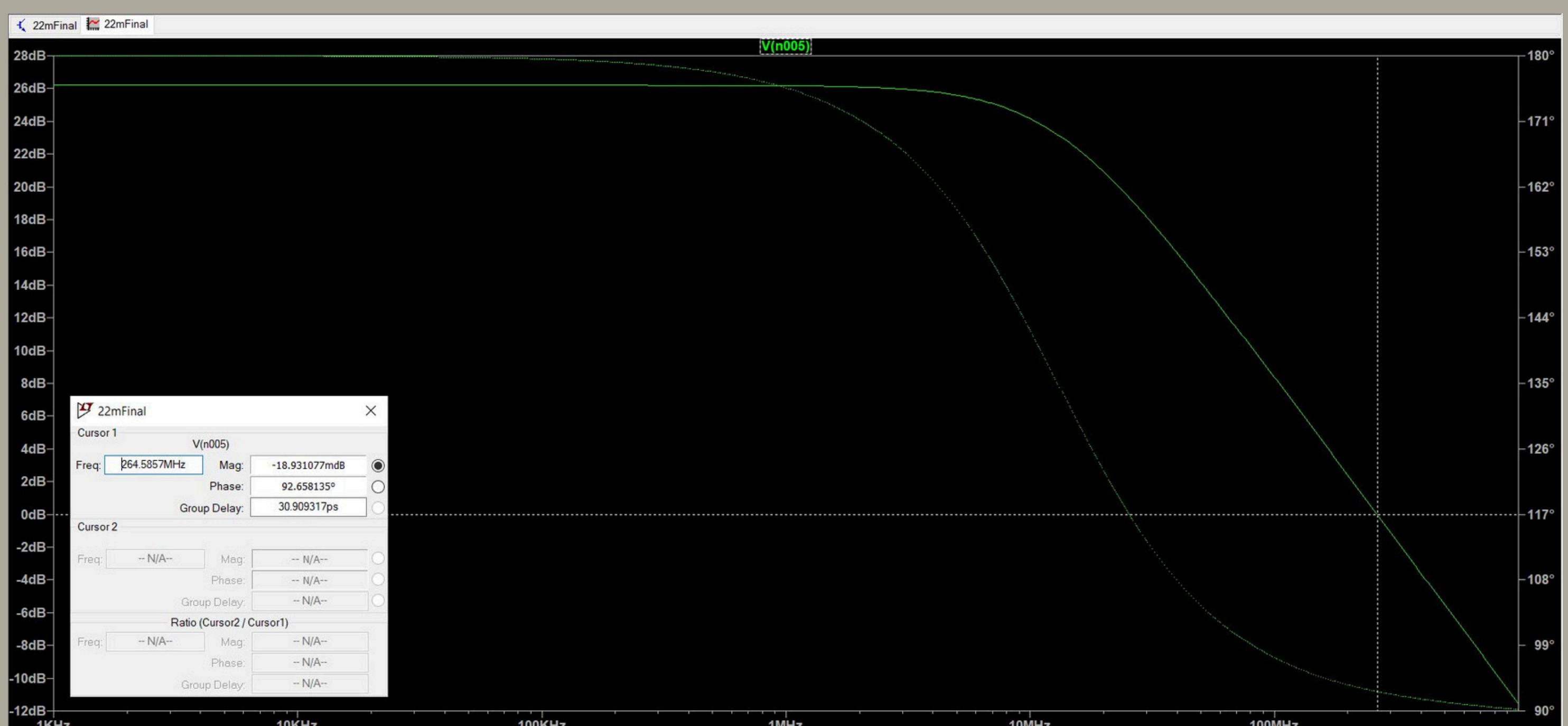
Cascode Current Mirror



Cascode Amplifier

## Simulation Results

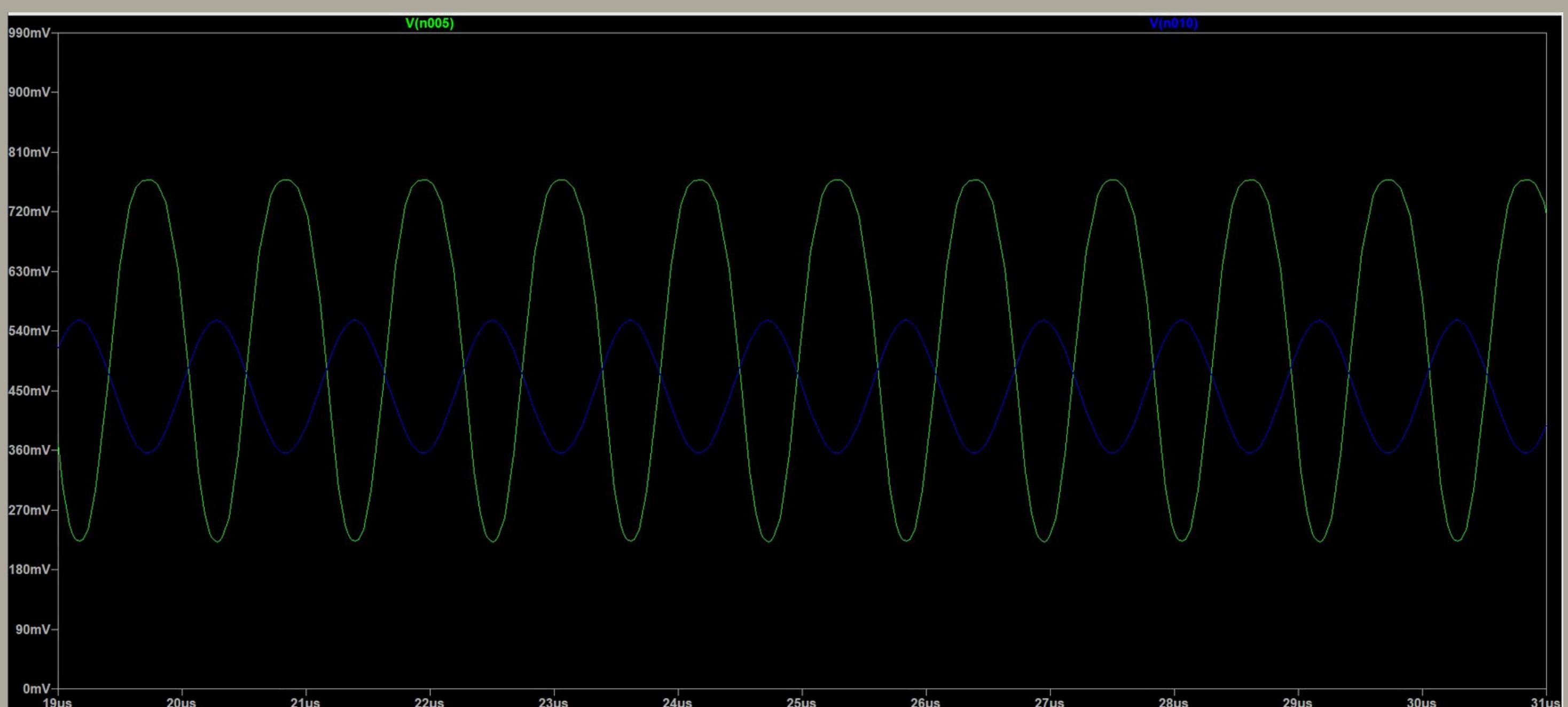
The Simulation outputs obtained were::



Bode Plot



Bias Voltages



Voutput

## RESULTS

QUANTITY	VALUE
Vbiasp	248.47 mV
Vbias1	243.05 mV
Vbias2	274.50 mV
Vbias3	604.53 mV
Vbias4	632.69 mV
Gain	26.195 dB
UGB	262.30 MHz
Power Consumed	27.2 microW

We got the required gain of 20 V/V (26.02 dB) and met the conditions of unity gain bandwidth (> 500KHz) and Power consumtion (<5mW).

## Calculations

Similarly for 22nm

ASSUMPTIONS :-

$$M_n C_{ox} = 100 \mu A/V^2$$

$$V_{THn} = -0.3V$$

$$f_s = 2.8 \text{ MHz}$$

$$M_p C_{ox} = 30 \mu A/V^2$$

$$V_{THp} = -0.3V$$

$$\therefore R_{out} = 56,841 \Omega$$

$$\text{and } g_{m,n} = 0.000352$$

$$V_{OV,n} = 0.2V$$

$$\left(\frac{W}{L}\right)_{NMOS} = \frac{g_{m,n}}{M_n C_{ox} V_{OV}} = \frac{0.000352}{10^{-6} \times 100 \times 0.2} = 17$$

$$I_d = \frac{1}{2} \times M_n C_{ox} \frac{W}{L} \cdot (V_{OV})^2$$

$$= \frac{1}{2} \times 100 \times 17 \times (0.2)^2 = 34 \mu A$$

$$\text{Power consumption} = 34 \times 0.8 = 27.2 \mu W$$

$$27.2 \mu W < 0.5mW$$

$$\left(\frac{W}{L}\right)_{NMOS} = \frac{17}{1}$$

From biasing circuit,  $U_{bias} = 243.1 \text{ mV}$

$$V_{OV} = U_{SD} - (V_{THp})$$

$$= \frac{0.8}{U_{DD}} - \frac{0.243}{U_{bias}} - 0.31 = 0.25V$$

- Current is from

$$34 \mu A = \frac{1}{2} \times 30 \times \left(\frac{W}{L}\right)_{PMOS} \times (0.25)^2$$

$$\Rightarrow \left(\frac{W}{L}\right)_{PMOS} = \frac{34 \times 2}{30 \times (0.25)^2} \approx 34$$

$$\therefore \left(\frac{W}{L}\right)_{PMOS} = \frac{34}{1}$$

For NMOS

$$W = 17 \times 22 = 374 \text{ nm}$$

$$L = 1 \times 22 = 22 \text{ nm}$$

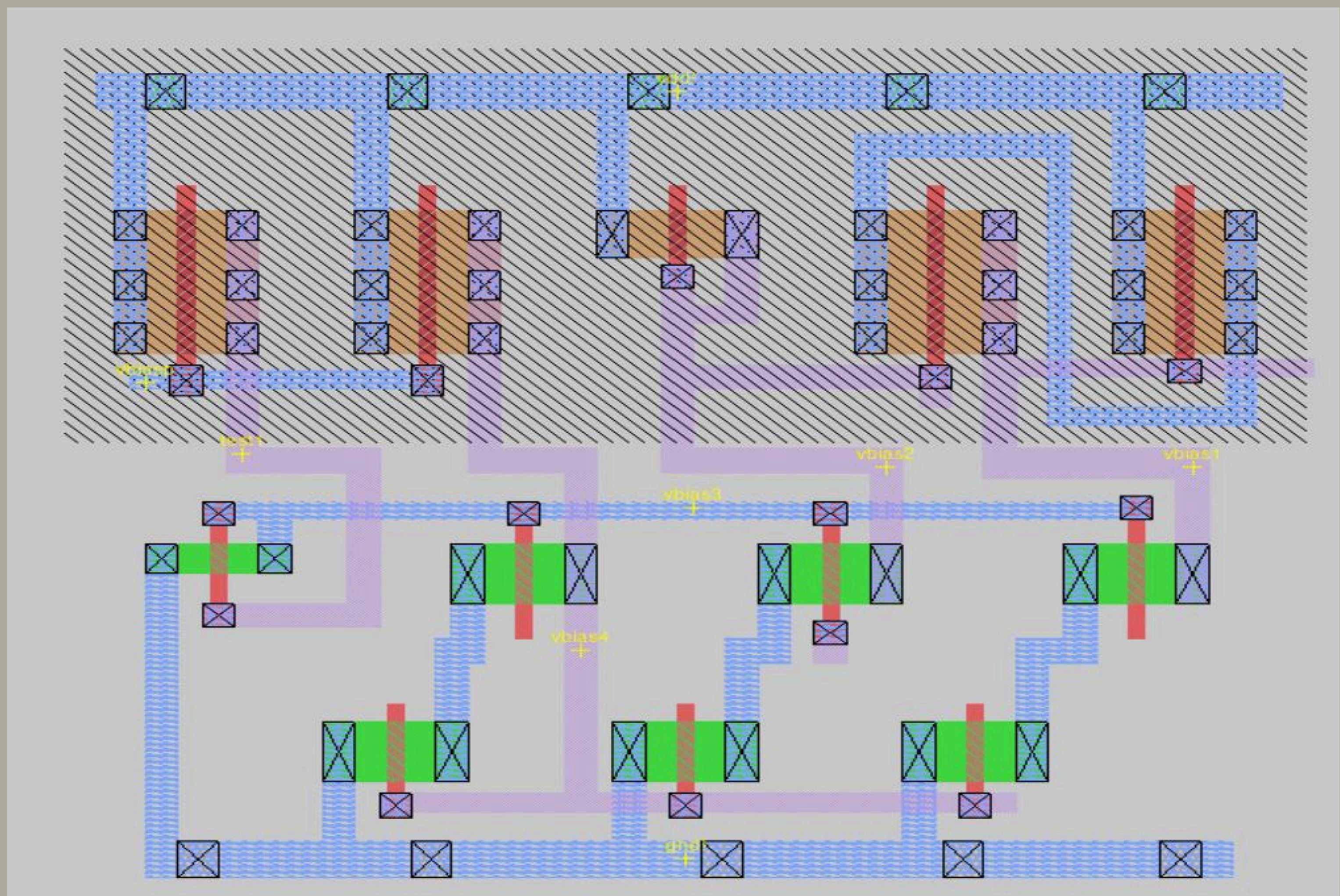
For PMOS

$$W = 34 \times 22 = 748 \text{ nm}$$

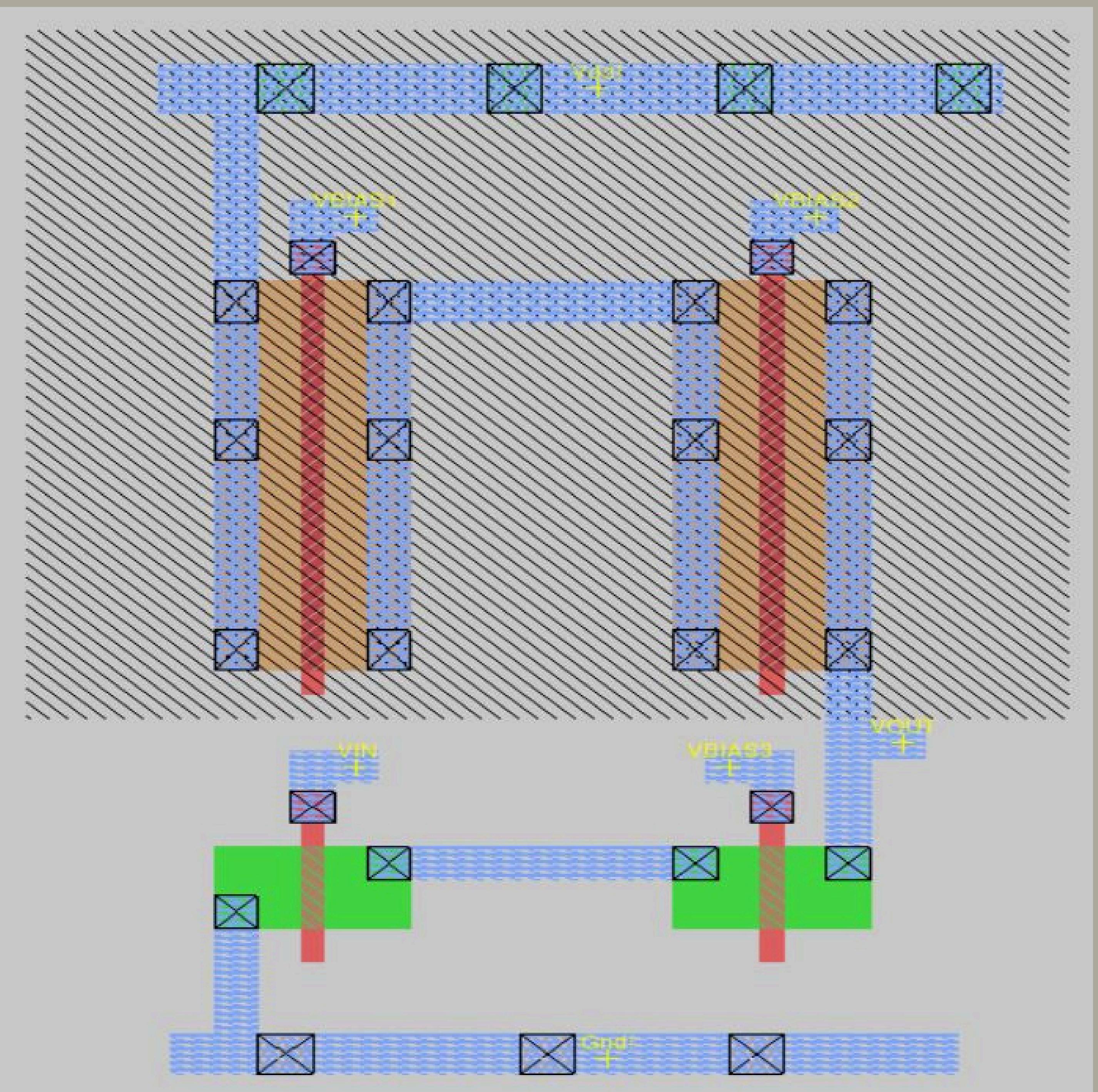
$$L = 1 \times 22 = 22 \text{ nm}$$

## Magic Layout (for 180nm Technology):

The Layout is made using the W/L values calculated earlier.

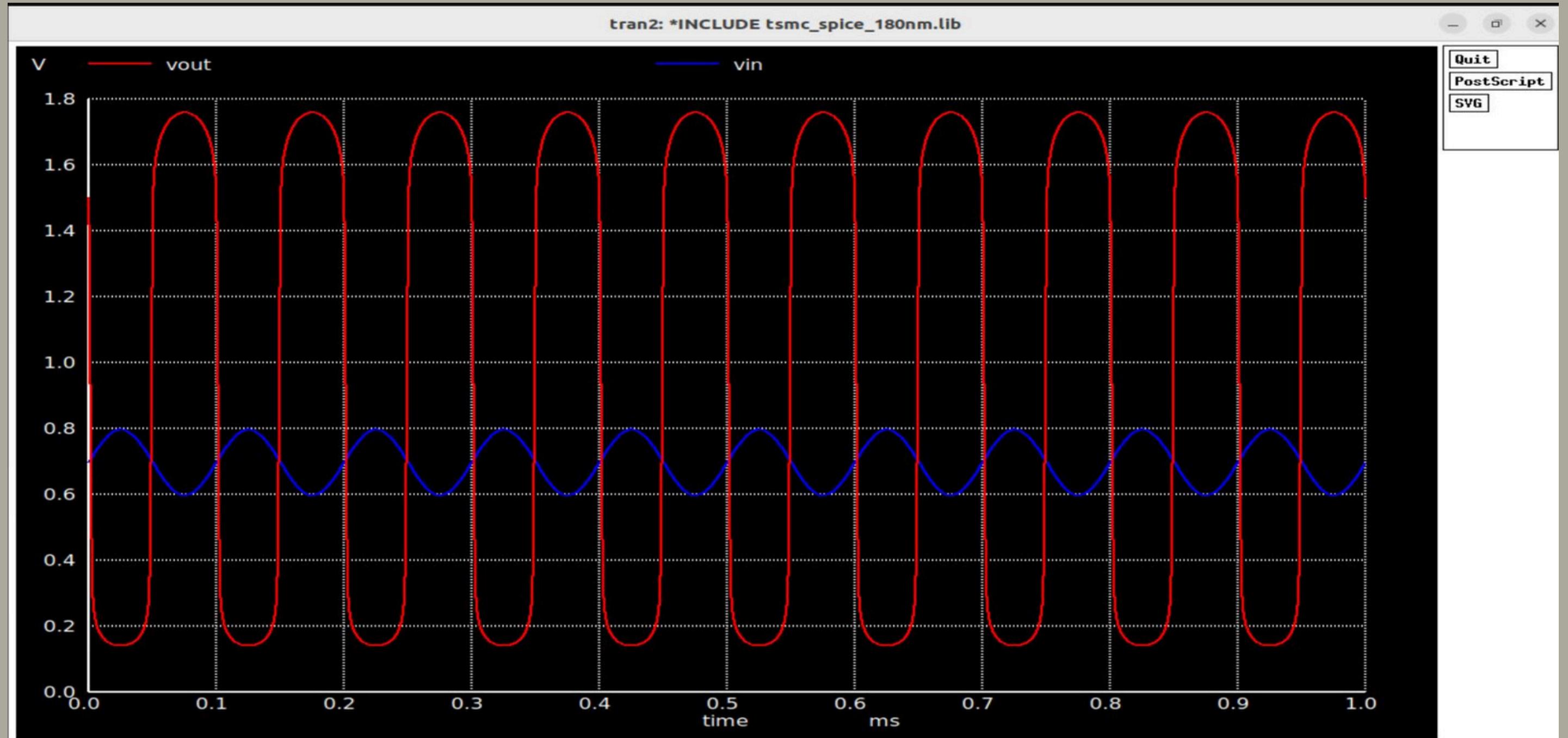


Cascode Current Mirror



Cascode Amplifier

## Result from NGSpice Simulation



Cascode Amplifier

After running the simulation in NGSpice, we got this result which shows amplification of the input signal

## **Observed Differences Between 180nm and 22nm Technology:**

- Power Consumption: The 22nm technology generally shows lower V<sub>bias</sub> values and currents than the 180nm technology, resulting in reduced power consumption.
- Bandwidth and Cut-Off Frequency: The unity gain bandwidth, and therefore the cut-off frequency, is higher for 22nm technology.
- Density and Layout: With 22nm MOSFETs being approximately eight times smaller than their 180nm counterparts, they allow for tighter packing on a layout, enabling more transistors per chip and thus improving performance. However, their smaller size complicates the layout design, which can increase production costs.

## **Conclusion:**

In LTSpice, we simulated the Beta Multiplier, Cascode Current Mirror, and Cascode Amplifier for both 180nm and 22nm technologies. The simulation results closely aligned with theoretical expectations, meeting all performance requirements. Additionally, we designed layouts for the Cascode Current Mirror and Cascode Amplifier using Magic software (for 180nm technology only). This allowed a comparative analysis of both technologies based on LTSpice simulations and Magic layout designs.