ECE M216A Project, Fall 2024

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Group-6 Performance Summary

Max f_{clk} [MHz]	**Area** [μm^2]	**Energy** [pJ]	**Hold Time Slack** [ps]
5263.158	3146.452181	0.43158044	70

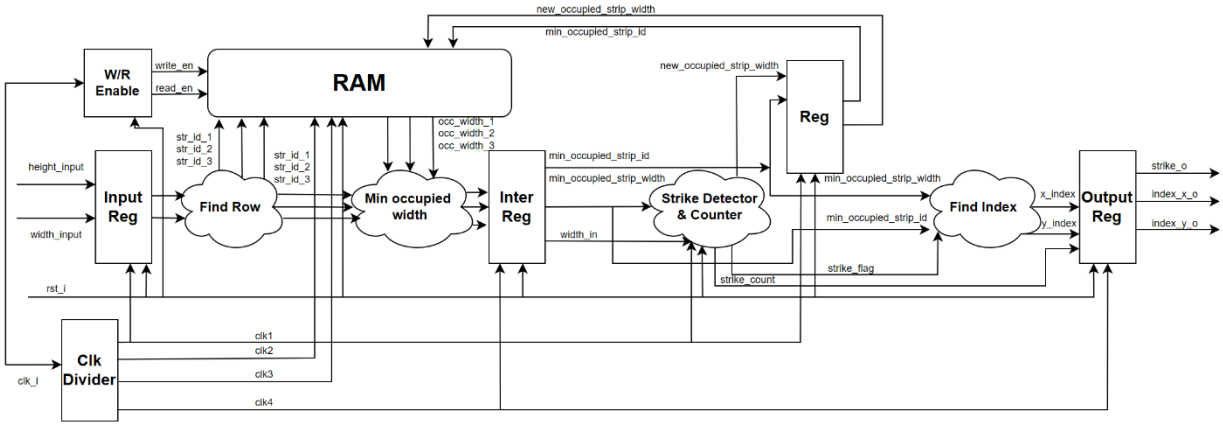

Figure. Architecture block diagram and its key building blocks.

Design Highlights:

- Pre-sorted strip IDs and preset value of 128 for strip 0 to eliminate priority and zero-input handling circuits.
- Reduced energy through clock division and clock gating, minimized the number of intermediate registers to achieve a 24.4% reduction in area and 80.8% in energy.
- Minimized synthetic metric $\frac{EA}{f}$ to 0.258 at $f_{clk} = 5.26GHz$ for optimization.