

VCU118 EVALUATION BOARD HW-U1-VCU118

(XCVU9P-2FLGA2104)

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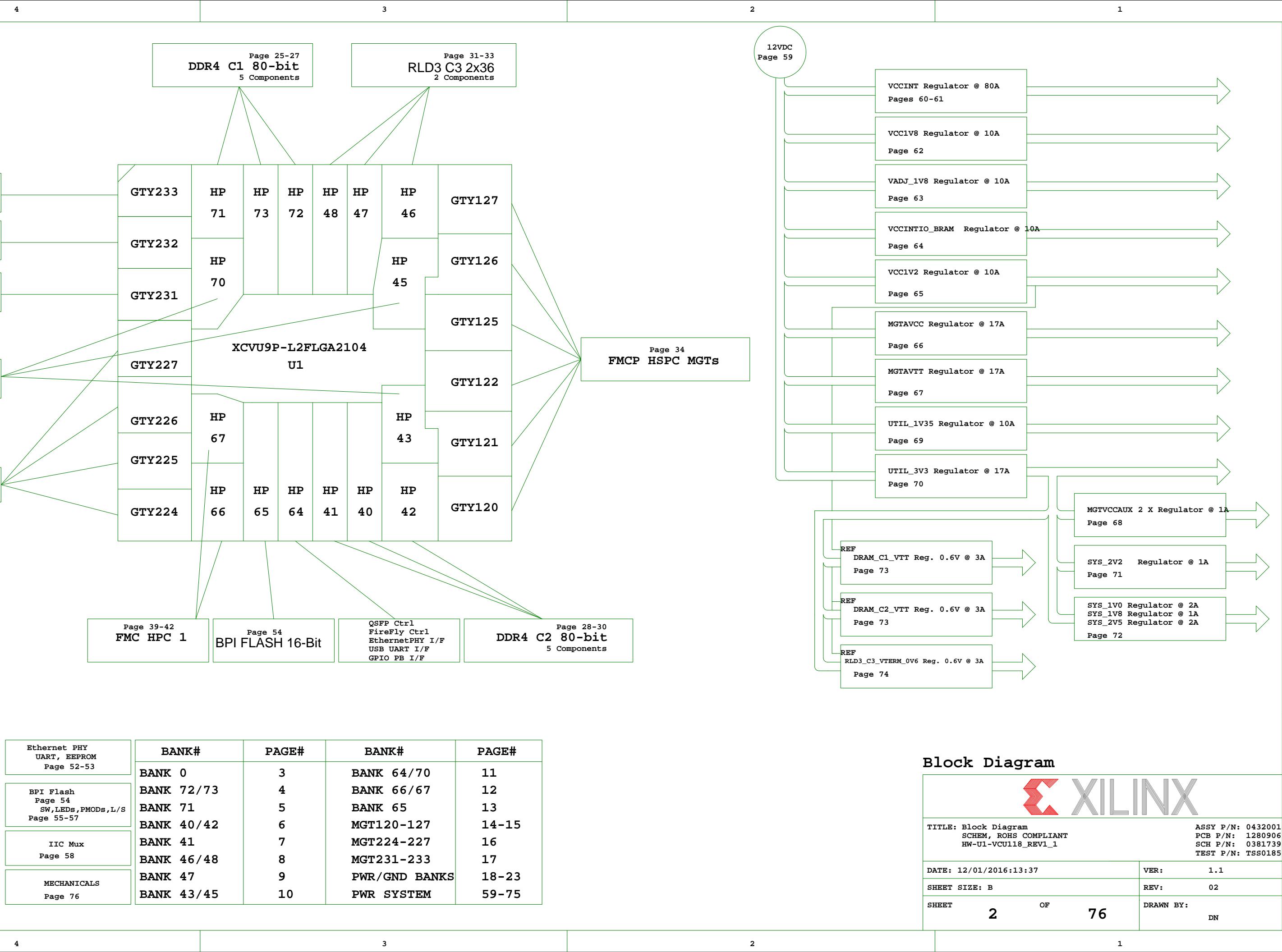
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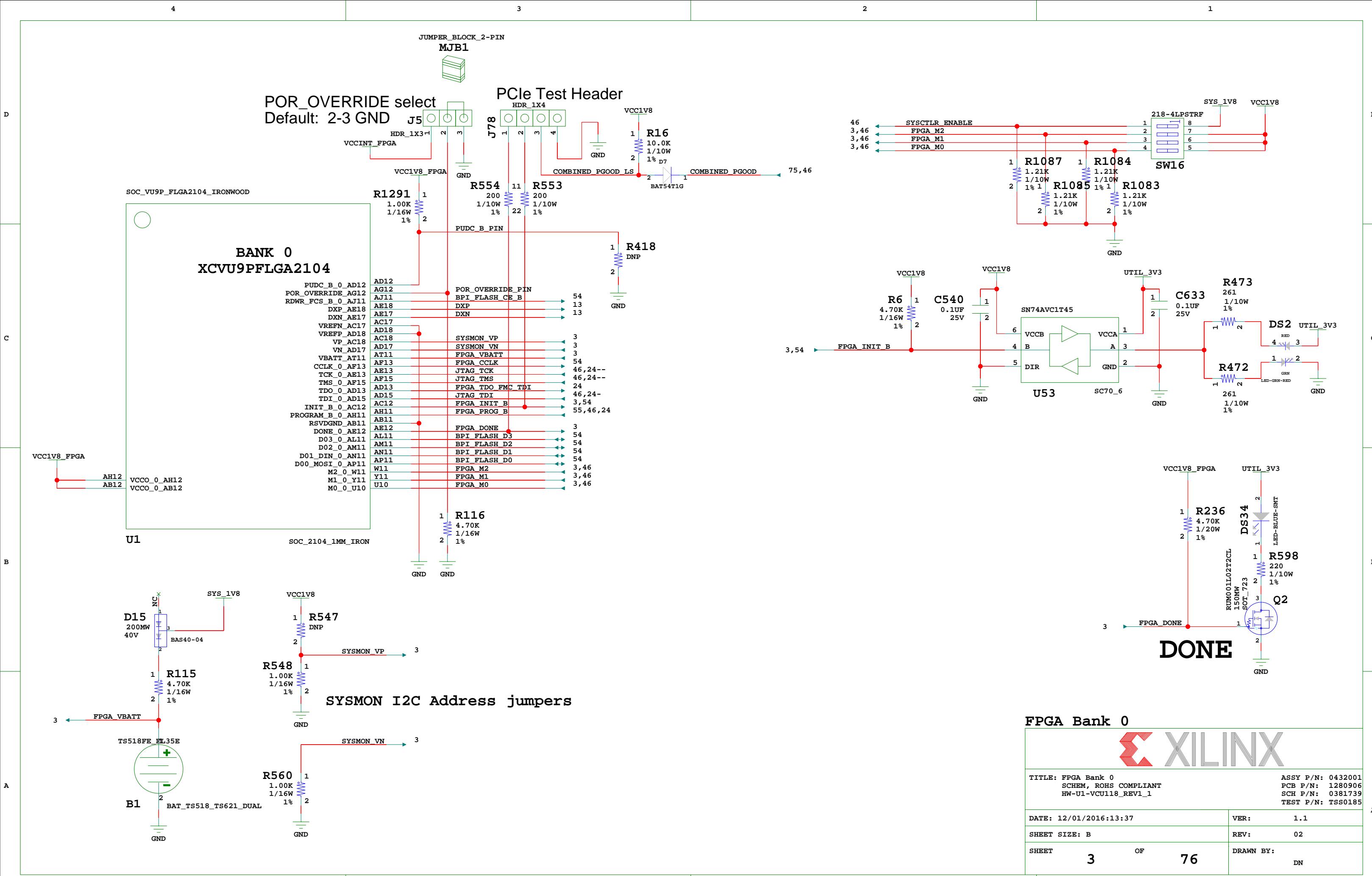
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Title Page



TITLE: Title Page SCHEM, ROHS COMPLIANT HW-U1-VCU118_REV1_1		ASSY P/N: 0432001 PCB P/N: 1280906 SCH P/N: 0381739 TEST P/N: TSS0185
DATE: 12/01/2016:13:37	VER: 1.1	
SHEET SIZE: B	REV: 02	
SHEET 1 OF 76	DRAWN BY: DN	





Bank 73 HP

SOC_VU9P_FLGA2104_IRONWOOD

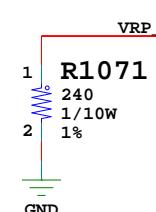
**BANK 73
XCVU9PFLGA2104**

IO_T3U_N12_73_A20
IO_L24N_T3U_N11_73_B20
IO_L24P_T3U_N10_73_C20
IO_L23N_T3U_N9_73_D19
IO_L23P_T3U_N8_73_D20
IO_L22N_T3U_N7_DBC_ADON_73_A18
IO_L22P_T3U_N6_DBC_AD0P_73_A19
IO_L21N_T3L_N5_DBN_73_C18
IO_L21P_T3L_N4_D8P_73_C19
IO_L20N_T3L_N3_AD1N_73_C17
IO_L20P_T3L_N2_AD1P_73_D17
IO_L19N_T3L_N1_DBC_AD9N_73_B17
IO_L19P_T3L_N0_DBC_AD9P_73_B18
IO_T2U_N12_73_G16
IO_L18N_T2U_N11_AD2N_73_D16
IO_L18P_T2U_N10_AD2P_73_E17
IO_L17N_T2U_N9_AD10N_73_F20
IO_L17P_T2U_N8_AD10P_73_G20
IO_L16N_T2U_N7_QBC_AD3N_73_E16
IO_L16P_T2U_N6_QBC_AD3P_73_F16
IO_L15N_T2L_N5_AD11N_73_E18
IO_L15P_T2L_N4_AD11P_73_E19
IO_L14N_T2L_N3_GC_73_F18
IO_L14P_T2L_N2_GC_73_F19
IO_L13N_T2L_N1_GC_QBC_73_G17
IO_L13P_T2L_N0_GC_QBC_73_G18
IO_T1U_N12_73_L19
IO_L12N_T1U_N11_GC_73_H18
IO_L12P_T1U_N10_GC_73_H19
IO_L11N_T1U_N9_GC_73_H17
IO_L11P_T1U_N8_GC_73_J17
IO_L10N_T1U_N7_QBC_AD4N_73_J19
IO_L10P_T1U_N6_QBC_AD4P_73_K19
IO_L9N_T1L_N5_AD12N_73_K18
IO_L9P_T1L_N4_AD12P_73_L18
IO_L8N_T1L_N3_AD5N_73_K16
IO_L8P_T1L_N2_AD5P_73_L16
IO_L7N_T1L_N1_QBC_AD13N_73_J16
IO_L7P_T1L_N0_QBC_AD13P_73_K17
IO_T0U_N12_VRP_73_T18
IO_L6N_T0U_N11_AD6N_73_M16
IO_L6P_T0U_N10_AD6P_73_N17
IO_L5N_T0U_N9_AD14N_73_N18
IO_L5P_T0U_N8_AD14P_73_N19
IO_L4N_T0U_N7_DBC_AD7N_73_P16
IO_L4P_T0U_N6_DBC_AD7P_73_P17
IO_L3N_T0L_N5_AD15N_73_M17
IO_L3P_T0L_N4_AD15P_73_M18
IO_L2N_T0L_N3_73_P19
IO_L2P_T0L_N2_73_R19
IO_L1N_T0L_N1_DBC_73_R17
IO_L1P_T0L_N0_DBC_73_R18
VREF_73_T19

A20 DDR4 C1 TEN 25-,26-,27
B20 DDR4 C1 DQ39 26
C20 DDR4 C1 DQ38 26
D19 DDR4 C1 DQ37 26
D20 DDR4 C1 DQ36 26
A18 DDR4 C1 DQS4 C 26
A19 DDR4 C1 DQS4 T 26
C18 DDR4 C1 DQ35 26
C19 DDR4 C1 DQ34 26
C17 DDR4 C1 DQ33 26
D17 DDR4 C1 DQ32 26
B17 GPIO DIP SW1 55
B18 DDR4 C1 DM4 26
G16 GPIO DIP SW2 55
D16 DDR4 C1 DQ31 25
E17 DDR4 C1 DQ30 25
F20 DDR4 C1 DQ29 25
G20 DDR4 C1 DQ28 25
E16 DDR4 C1 DQS3 C 25
F16 DDR4 C1 DQS3 T 25
E18 DDR4 C1 DQ27 25
E19 DDR4 C1 DQ26 25
F18 DDR4 C1 DQ25 25
F19 DDR4 C1 DQ24 25
G17 NC
G18 DDR4 C1 DM3 25
L19 CPU RESET 55
G19 DDR4 C1 DQ23 25
H18 DDR4 C1 DQ22 25
H19 DDR4 C1 DQ21 25
J17 DDR4 C1 DQ20 25
J19 DDR4 C1 DQS2 C 25
K19 DDR4 C1 DQS2 T 25
K18 DDR4 C1 DQ19 25
L18 DDR4 C1 DQ18 25
K16 DDR4 C1 DQ17 25
L16 DDR4 C1 DQ16 25
J16 GPIO DIP SW3 55
K17 DDR4 C1 DM2 25
T18 VRP_73 4
M16 DDR4 C1 DQ15 25
N17 DDR4 C1 DQ14 25
N18 DDR4 C1 DQ13 25
N19 DDR4 C1 DQ12 25
P16 DDR4 C1 DQS1 C 25
P17 DDR4 C1 DQS1 T 25
M17 DDR4 C1 DQ11 25
M18 DDR4 C1 DQ10 25
P19 DDR4 C1 DQ9 25
R19 DDR4 C1 DQ8 25
R17 DDR4 C1 ALERT_B 25-,26-,27
R18 DDR4 C1 DM1 25
T19 NC

VCC1V2_FPGA
A17
D18
G19
H16
L17
P18

U1 SOC_2104_1MM_IRON

**Bank 72 HP**

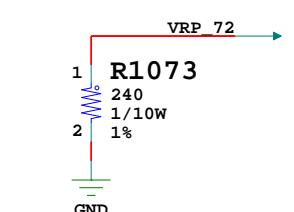
SOC_VU9P_FLGA2104_IRONWOOD

**BANK 72
XCVU9PFLGA2104**

IO_T3U_N12_72_D21
A21 DDR4 C1 DQ71 27
B21 DDR4 C1 DQ70 27
B22 DDR4 C1 DQ69 27
B23 DDR4 C1 DQ68 27
IO_L22N_T3U_N7_DBC_ADON_72_C22
IO_L22P_T3U_N6_DBC_AD0P_72_D22
IO_L21N_T3L_N5_DBN_72_C23
IO_L21P_T3L_N4_D8P_72_C24
IO_L20N_T3L_N3_AD1N_72_A23
IO_L20P_T3L_N2_AD1P_72_A24
IO_L19N_T3L_N1_DBC_AD9N_72_D24
IO_L19P_T3L_N0_DBC_AD9P_72_E24
IO_T2U_N12_72_H20
F23 DDR4 C1 DQ63 26
F24 DDR4 C1 DQ62 26
E21 DDR4 C1 DQ61 26
F21 DDR4 C1 DQ60 26
G23 DDR4 C1 DQ57_C 26
H24 DDR4 C1 DQ57_T 26
E22 DDR4 C1 DQ59 26
E23 DDR4 C1 DQ58 26
H22 DDR4 C1 DQ57 26
H23 DDR4 C1 DQ56 26
G21 NC
G22 DDR4 C1 DM7 26
IO_T1U_N12_72_J20
J22 DDR4 C1 DQ55 26
K22 DDR4 C1 DQ54 26
IO_L12P_T1U_N10_GC_72_K22
J21 DDR4 C1 DQ53 26
IO_L11N_T1U_N9_GC_72_J21
K21 DDR4 C1 DQ52 26
IO_L11P_T1U_N8_GC_72_K21
L20 DDR4 C1 DQ56_C 26
M20 DDR4 C1 DQ56_T 26
L21 DDR4 C1 DQ51 26
IO_L9N_T1L_N5_AD12N_72_L21
M21 DDR4 C1 DQ50 26
IO_L9P_T1L_N4_AD12P_72_M21
J24 DDR4 C1 DQ49 26
IO_L8N_T1L_N3_AD5N_72_J24
K24 DDR4 C1 DQ48 26
IO_L7N_T1L_N1_QBC_AD13N_72_K23
K23 NC
L23 DDR4 C1 DM6 26
IO_T0U_N12_VRP_72_T21
T21 VRP 72 4
R23 DDR4 C1 DQ47 26
T23 DDR4 C1 DQ46 26
IO_L6P_T0U_N10_AD6P_72_T23
P22 DDR4 C1 DQ45 26
IO_L5P_T0U_N8_AD14P_72_R22
R22 DDR4 C1 DQ44 26
M22 DDR4 C1 DQ55_C 26
N22 DDR4 C1 DQ55_T 26
IO_L4P_T0U_N6_DBC_AD7P_72_N22
P21 DDR4 C1 DQ43 26
IO_L3N_T0L_N5_AD15N_72_P21
R21 DDR4 C1 DQ42 26
IO_L3P_T0L_N4_AD15P_72_R21
M23 DDR4 C1 DQ41 26
IO_L2N_T0L_N3_72_M23
N23 DDR4 C1 DQ40 26
IO_L1N_T0L_N1_DBC_72_N20
N20 DDR4 C1 RESET_B 25-,26-,27
P20 DDR4 C1 DM5 26
T20 NC

VCC1V2_FPGA
B24
C21
VCCO_72_C21
F22
VCCO_72_F22
J23
VCCO_72_J23
K20
VCCO_72_K20
N21
VCCO_72_N21
T22
VCCO_72_T22

U1 SOC_2104_1MM_IRON

**FPGA Banks 73 72 C1 DDR4 Data**

TITLE: FPGA Banks 73 72 C1 DDR4 Data
SCHEM., ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:37

VER: 1.1

SHEET SIZE: B

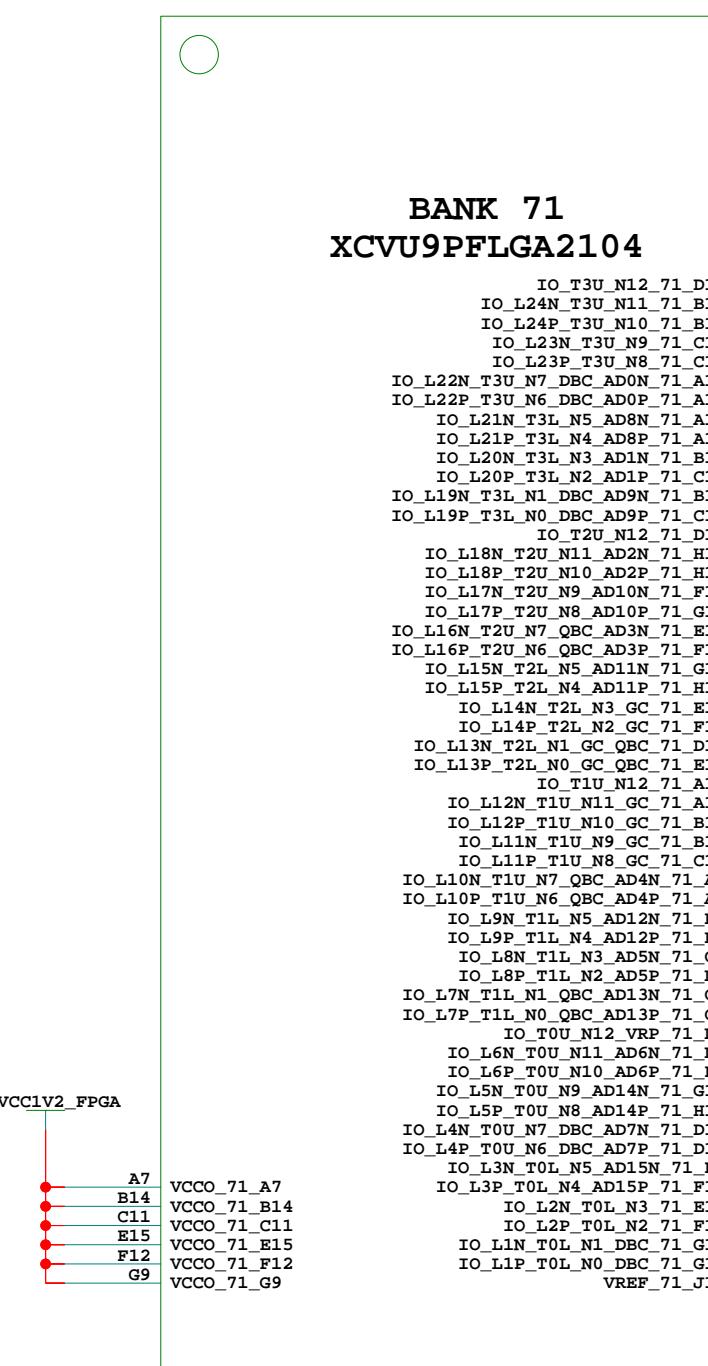
REV: 02

SHEET 4 OF 76

DRAWN BY: DN

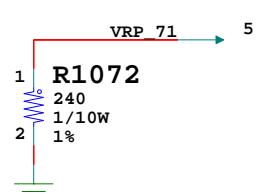
Bank 71 HP

SOC_VU9P_FLGA2104_IRONWOOD

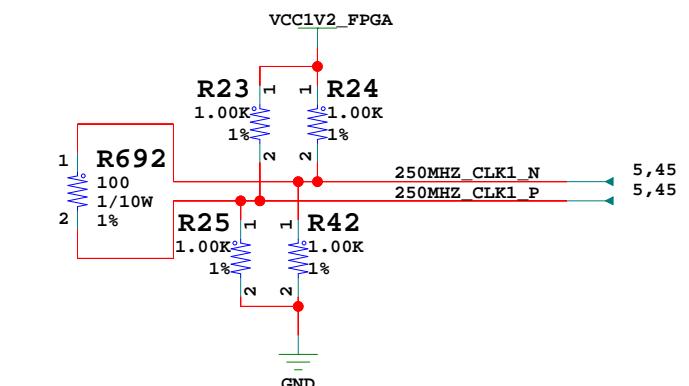


U1

SOC_2104_1MM_IRON



PCB LAYOUT DIRECTIVE:
TERMINATION RESISTOR
AND BIAS RESISTOR
NETWORK TO BE PLACED
IN "FLY-BY" CONFIGURATION



FPGA Bank 71 C1 DDR4 Addr Ctrl

TITLE: FPGA Bank 71 C1 DDR4 Addr Ctrl
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 128096
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:37

VER: 1.1

SHEET SIZE: B

REV: 02

SHEET 5 OF 76

DRAWN BY: DN

Bank 40 HP

SOC_VU9P_FLGA2104_IRONWOOD

BANK 40
XCVU9PFLGA2104

IO_T3U_N12_40_AR29	DDR4_C2_ALERT_B	28-,29-,30
IO_L24N_T3U_N11_40_AN31	DDR4_C2_DQ31	28
IO_L24P_T3U_N10_40_AN30	DDR4_C2_DQ30	28
IO_L23N_T3U_N9_40_AR30	DDR4_C2_DQ29	28
IO_L23P_T3U_N8_40_AP30	DDR4_C2_DQ28	28
IO_L22N_T3U_N7_DBC_AD0N_40_AP32	DDR4_C2_DQS3_C	28
IO_L22P_T3U_N6_DBC_AD0P_40_AP31	DDR4_C2_DQS3_T	28
IO_L21N_T3L_N5_AD8N_40_AT30	DDR4_C2_DQ27	28
IO_L21P_T3L_N4_AD8P_40_AT29	DDR4_C2_DQ26	28
IO_L20N_T3L_N3_AD1N_40_AT34	DDR4_C2_DQ25	28
IO_L20P_T3L_N2_AD1P_40_AR33	DDR4_C2_DQ24	28
IO_L19N_T3L_N1_DBC_AD9N_40_AT32	GPIO_LED0	55
IO_L19P_T3L_N0_DBC_AD9P_40_AR32	DDR4_C2_DM3	28
IO_T2U_N12_40_AV34	GPIO_LED1	55
IO_L18N_T2U_N11_AD2N_40_AV31	DDR4_C2_DQ23	28
IO_L18P_T2U_N10_AD2P_40_AV31	DDR4_C2_DQ22	28
IO_L17N_T2U_N9_AD10N_40_AV32	DDR4_C2_DQ21	28
IO_L17P_T2U_N8_AD10P_40_AT31	DDR4_C2_DQ20	28
IO_L16N_T2U_N7_QBC_AD3N_40_AV29	DDR4_C2_DQS2_C	28
IO_L16P_T2U_N6_QBC_AD3P_40_AU29	DDR4_C2_DQS2_T	28
IO_L15N_T2L_N5_AD11N_40_AU34	DDR4_C2_DQ19	28
IO_L15P_T2L_N4_AD11P_40_AU33	DDR4_C2_DQ18	28
IO_L14N_T2L_N3_GC_40_AV30	DDR4_C2_DQ17	28
IO_L14P_T2L_N2_GC_40_AV30	DDR4_C2_DQ16	28
IO_L13N_T2L_N1_GC_QBC_40_AV33	FAN_FAIL_LS_B	13
IO_L13P_T2L_N0_GC_QBC_40_AV33	DDR4_C2_DM2	28
IO_T1U_N12_40_AV30	GPIO_LED2	55
IO_L12N_T1U_N11_GC_40_AV33	DDR4_C2_DQ15	28
IO_L12P_T1U_N10_GC_40_AV32	DDR4_C2_DQ14	28
IO_L11N_T1U_N9_GC_40_AV32	DDR4_C2_DQ13	28
IO_L11P_T1U_N8_GC_40_AV31	DDR4_C2_DQ12	28
IO_L10N_T1U_N7_QBC_AD4N_40_BA34	DDR4_C2_DQS1_C	28
IO_L10P_T1U_N6_QBC_AD4P_40_AV34	DDR4_C2_DQS1_T	28
IO_L9N_T1L_N5_AD12N_40_BA31	DDR4_C2_DQ11	28
IO_L9P_T1L_N4_AD12P_40_BA30	DDR4_C2_DQ10	28
IO_L8N_T1L_N3_AD5N_40_BB33	DDR4_C2_DQ9	28
IO_L8P_T1L_N2_AD5P_40_BA32	DDR4_C2_DQ8	28
IO_L7N_T1L_N1_QBC_AD13N_40_BB32	GPIO_LED3	55
IO_L7P_T1L_N0_QBC_AD13P_40_BB31	DDR4_C2_DM1	28
IO_TOU_N12_VRP_40_BC30	VRP_40	6
IO_L6N_TOU_N11_AD6N_40_BD31	DDR4_C2_DQ7	28
IO_L6P_TOU_N10_AD6P_40_BC31	DDR4_C2_DQ6	28
IO_L5N_TOU_N9_AD14N_40_BD33	DDR4_C2_DQ5	28
IO_L5P_TOU_N8_AD14P_40_BD32	DDR4_C2_DQ4	28
IO_L4N_TOU_N7_DBC_AD7N_40_BF31	DDR4_C2_DQS0_C	28
IO_L4P_TOU_N6_DBC_AD7P_40_BF30	DDR4_C2_DQS0_T	28
IO_L3N_T0L_N5_AD15N_40_BE33	DDR4_C2_DQ3	28
IO_L3P_T0L_N4_AD15P_40_BB32	DDR4_C2_DQ2	28
IO_L2N_T0L_N3_40_BE30	DDR4_C2_DQ1	28
IO_L2P_T0L_N2_40_BD30	DDR4_C2_DQ0	28
IO_L1N_T0L_N1_DBC_40_BF32	GPIO_LED4	55
IO_L1P_T0L_N0_DBC_40_BE32	DDR4_C2_DM0	28
VREF_40_AN29	NC	

VCC1V2_FPGA

AR31	VCCO_40_AR31
AV32	VCCO_40_AV32
AW29	VCCO_40_AW29
BA33	VCCO_40_BA33
BB30	VCCO_40_BB30
BE31	VCCO_40_BE31

U1

SOC_2104_1MM_IRON

VRP_40 → 6

1 R378
240 1/10W
2 1%

GND

Bank 42 HP

SOC_VU9P_FLGA2104_IRONWOOD

BANK 42
XCVU9PFLGA2104

AR29	DDR4_C2_ALERT_B	28-,29-,30
AN31	DDR4_C2_DQ31	28
AN30	DDR4_C2_DQ30	28
AR30	DDR4_C2_DQ29	28
AP30	DDR4_C2_DQ28	28
AP32	DDR4_C2_DQS3_C	28
AP31	DDR4_C2_DQS3_T	28
AT30	DDR4_C2_DQ27	28
AT29	DDR4_C2_DQ26	28
AT34	DDR4_C2_DQ25	28
AT33	DDR4_C2_DQ24	28
AT32	GPIO_LED0	55
AR32	DDR4_C2_DM3	28
AV34	GPIO_LED1	55
AV31	DDR4_C2_DQ23	28
AU31	DDR4_C2_DQ22	28
AO32	DDR4_C2_DQ21	28
AT31	DDR4_C2_DQ20	28
AV29	DDR4_C2_DQS2_C	28
AU29	DDR4_C2_DQS2_T	28
AU34	DDR4_C2_DQ19	28
AU33	DDR4_C2_DQ18	28
AW30	DDR4_C2_DQ17	28
AV30	DDR4_C2_DQ16	28
AW33	FAN_FAIL_LS_B	13
AV33	DDR4_C2_DM2	28
AY30	GPIO_LED2	55
AY33	DDR4_C2_DQ15	28
AY32	DDR4_C2_DQ14	28
AW32	DDR4_C2_DQ13	28
AW31	DDR4_C2_DQ12	28
BA34	DDR4_C2_DQS1_C	28
AY34	DDR4_C2_DQS1_T	28
BA31	DDR4_C2_DQ11	28
BA30	DDR4_C2_DQ10	28
BB33	DDR4_C2_DQ9	28
BA32	DDR4_C2_DQ8	28
BB32	GPIO_LED3	55
BB31	DDR4_C2_DM1	28
BC30	VRP_40	6
BD31	DDR4_C2_DQ7	28
BC31	DDR4_C2_DQ6	28
BD33	DDR4_C2_DQ5	28
IO_L5N_TOU_N9_AD14N_40_BD33	DDR4_C2_DQ4	28
IO_L5P_TOU_N8_AD14P_40_BD32	DDR4_C2_DQ3	28
IO_L4N_TOU_N7_DBC_AD7N_40_BF31	DDR4_C2_DQS0_C	28
BF30	DDR4_C2_DQS0_T	28
BE33	DDR4_C2_DQ3	28
BD32	DDR4_C2_DQ2	28
BE30	DDR4_C2_DQ1	28
BD30	DDR4_C2_DQ0	28
BF32	GPIO_LED4	55
BE32	DDR4_C2_DM0	28
AN29	NC	
AU35	VCCO_42_AU35	
AW39	VCCO_42_AV39	
AY36	VCCO_42_AY36	
BB40	VCCO_42_BB40	
BC37	VCCO_42_BC37	
BD34	VCCO_42_BD34	
BF38	VCCO_42_BF38	
VREF_42_AU36	NC	

VCC1V2_FPGA

AU35	VCCO_42_AU35
AW39	VCCO_42_AV39
AY36	VCCO_42_AY36
BB40	VCCO_42_BB40
BC37	VCCO_42_BC37
BD34	VCCO_42_BD34
BF38	VCCO_42_BF38
VREF_42_AU36	NC

U1

SOC_2104_1MM_IRON

VRP_42 → 6

1 R377
240 1/10W
2 1%

GND

FPGA Banks 40 42 C2 DDR4 Data



TITLE: FPGA Banks 40 42 C2 DDR4 Data
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:37

VER: 1.1

SHEET SIZE: B

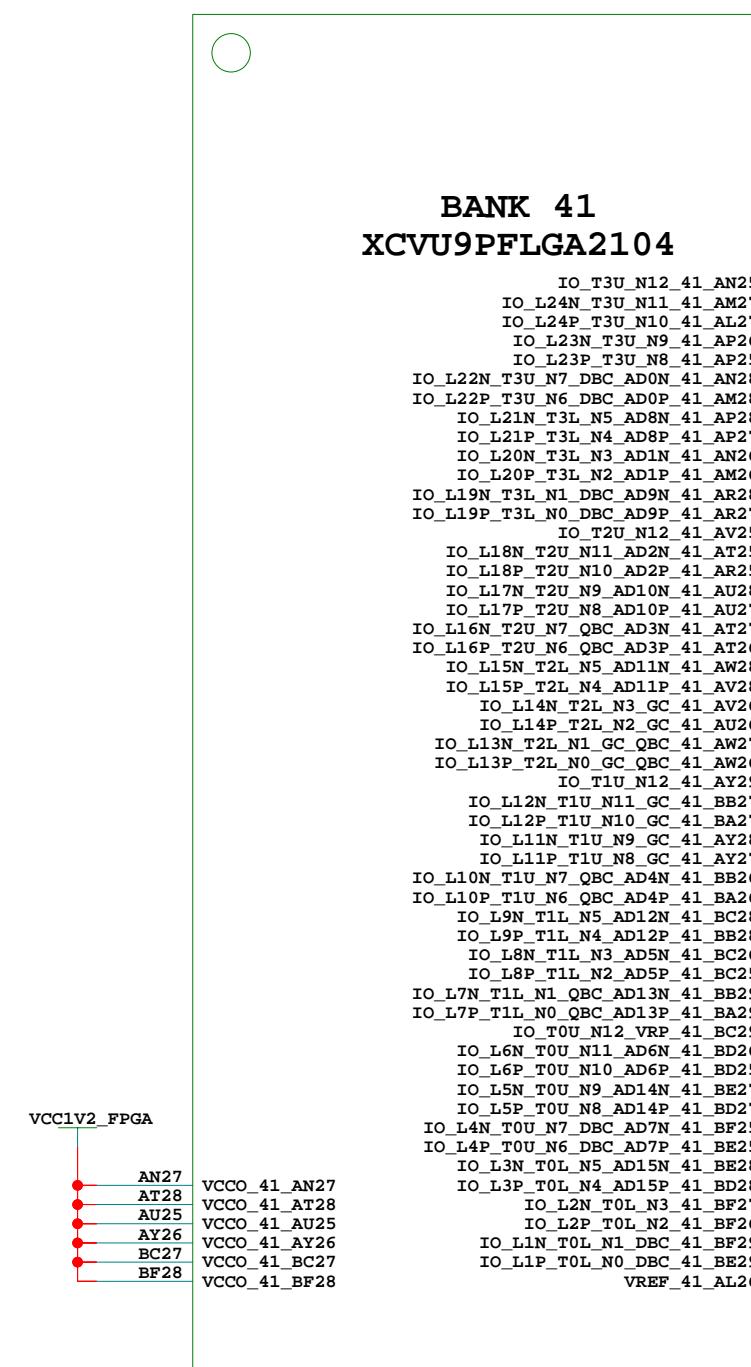
REV: 02

SHEET 6 OF 76

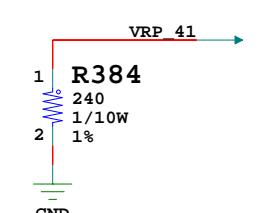
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Bank 41 HP

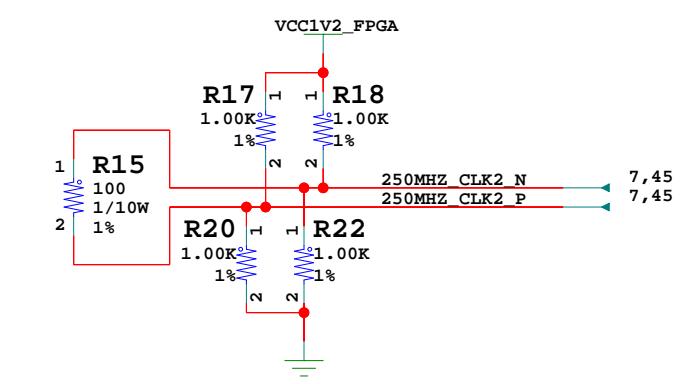
SOC_VU9P_FLGA2104_IRONWOOD



SOC_2104_1MM_IRON



PCB LAYOUT DIRECTIVE:
TERMINATION RESISTOR
AND BIAS RESISTOR
NETWORK TO BE PLACED
IN "FLY-BY" CONFIGURATION



FPGA Bank 41 C2 DDR4 Addr Ctrl



TITLE: FPGA Bank 41 C2 DDR4 Addr Ctrl
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:37

VER: 1.1

SHEET SIZE: B

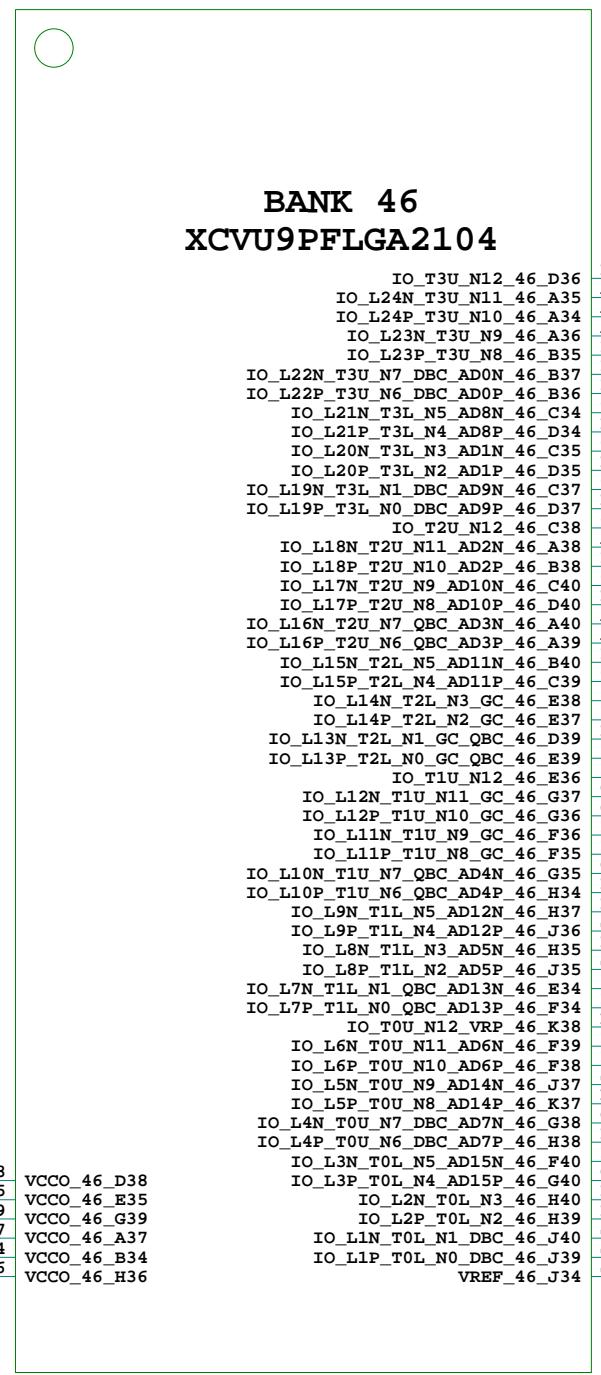
REV: 02

SHEET 7 OF 76

DRAWN BY: DN

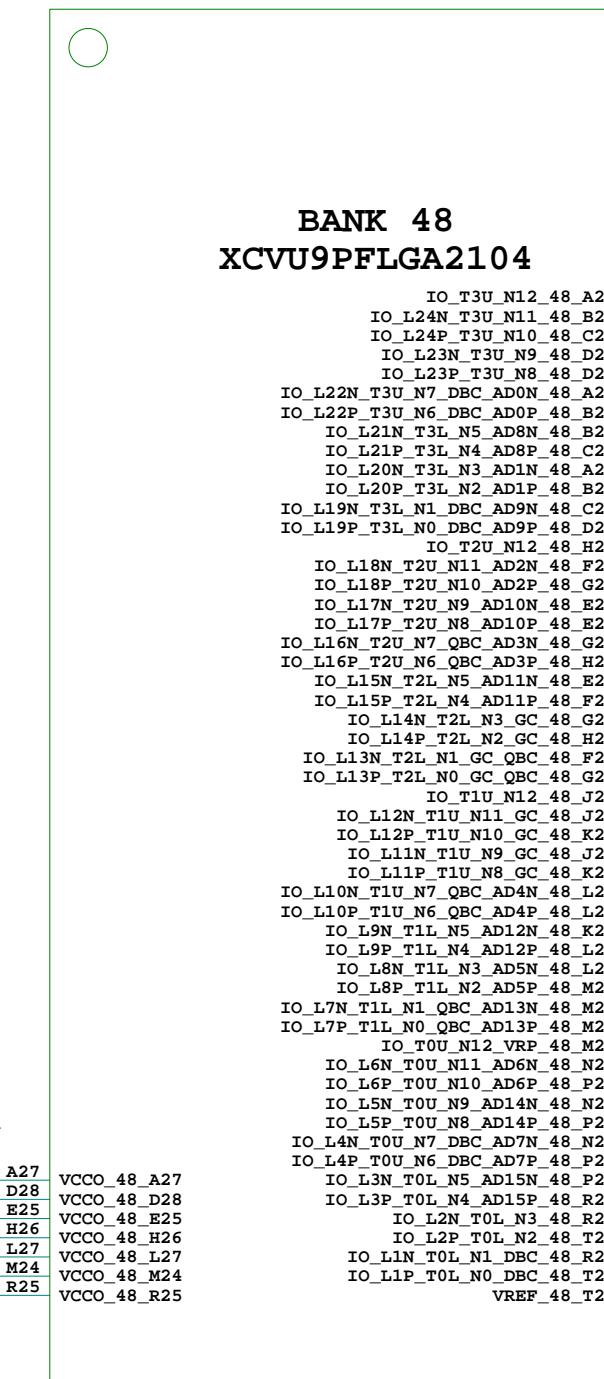
Bank 46 HP

SOC VU9P FLGA2104 IRONWOOD



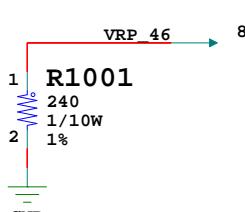
Bank 48 HF

SOC VU9P FLGA2104 IRONWOOD

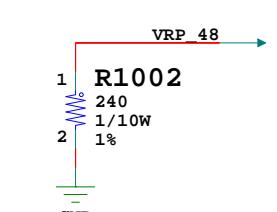


111

2021-04-12M 380



2020-01-01



FPGA Banks 46 48 C3 BL-D3 Data



**TITLE: FPGA Banks 46 48 C3 RLD3 Data
SCHEM, ROHS COMPLIANT
HW-111-VCH118 REV1.1**

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TGS0185

DATE: 12/01/2016 12:25

1 1

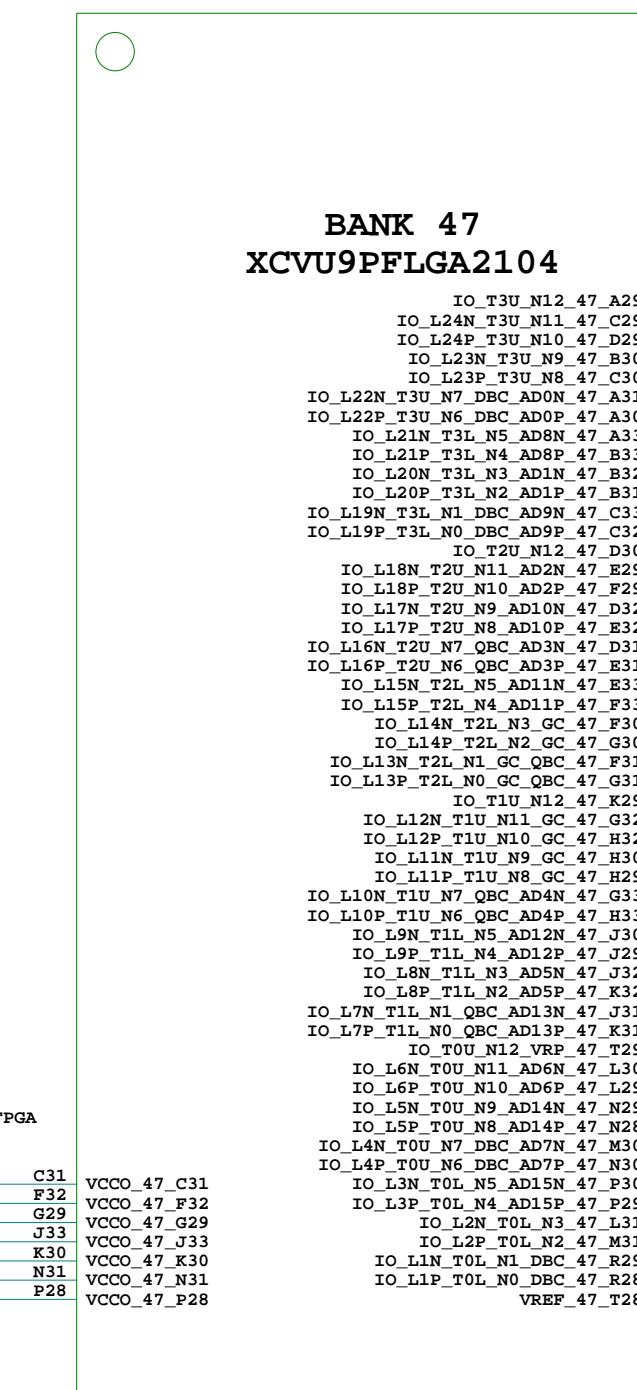
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10

SHEET 8 OF 76

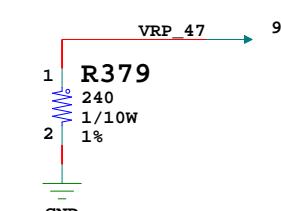
Y:

SOC_VU9P_FLGA2104_IRONWOOD



U1

SOC_2104_1MM_IRON

**FPGA Bank 47 C3 RLD3 Addr Ctrl**

TITLE: FPGA Bank 47 C3 RLD3 Addr Ctrl
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

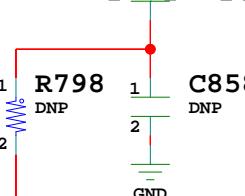
DATE: 12/01/2016:13:37	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 9 OF 76	DRAWN BY: DN

Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via

Bank 43 HP

SOC_VU9P_FLGA2104_IRONWOOD

FMCP_HSPC_VREF_A_M2C

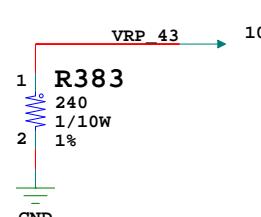


BANK 43 XCVU9PFLGA2104

IO_T3U_N12_43_AH30	NC	
AG33	FMCP_HSPC_LA15_N	36
AG32	FMCP_HSPC_LA15_P	36
IO_L24P_T3U_N10_43_AG32	FMCP_HSPC_LA14_N	34
IO_L23N_T3U_N9_43_AH31	FMCP_HSPC_LA14_P	34
IO_L23P_T3U_N8_43_AG31	FMCP_HSPC_LA16_N	35
IO_L22N_T3U_N7_DBC_AD0N_43_AH35	FMCP_HSPC_LA16_P	35
IO_L22P_T3U_N6_DBC_AD0P_43_AG34	FMCP_HSPC_LA12_N	35
IO_L21N_T3L_N5_AD8N_43_AH34	FMCP_HSPC_LA12_P	35
IO_L21P_T3L_N4_AD8P_43_AH33	FMCP_HSPC_LA13_N	34
IO_L20N_T3L_N3_AD1N_43_AJ36	FMCP_HSPC_LA13_P	34
IO_L20P_T3L_N2_AD1P_43_AJ35	FMCP_HSPC_LA09_N	34
IO_L19N_T3L_N1_DBC_AD9N_43_AK33	FMCP_HSPC_LA09_P	34
IO_L19P_T3L_N0_DBC_AD9P_43_AJ33	NC	
IO_T2U_N12_43_AM31	FMCP_HSPC_LA08_N	35
AK30	FMCP_HSPC_LA08_P	35
AK29	FMCP_HSPC_LA11_N	36
IO_L17N_T2U_N9_AD10N_43_AJ31	FMCP_HSPC_LA11_P	36
IO_L17P_T2U_N8_AD10P_43_AJ30	FMCP_HSPC_LA01_CC_N	34
IO_L16N_T2U_N7_QBC_AD3N_43_AL31	FMCP_HSPC_LA01_CC_P	34
IO_L16P_T2U_N6_QBC_AD3P_43_AL30	FMCP_HSPC_Z_PRSNT_M2C_B_LS	56
IO_L15N_T2L_N5_AD11N_43_AM29	FMCP_HSPC_Z_PRSNT_M2C_B_LS	56
IO_L15P_T2L_N4_AD11P_43_AL29	FMC_VADJ_ON_LS	56
IO_L14N_T2L_N3_GC_43_AK32	FMCP_HSPC_LA02_N	36
IO_L14P_T2L_N2_GC_43_AJ32	FMCP_HSPC_LA02_P	36
IO_L13N_T2L_N1_GC_QBC_43_AM32	FMCP_HSPC_CLK0_M2C_N	36
IO_L13P_T2L_N0_GC_QBC_43_AL32	FMCP_HSPC_CLK0_M2C_P	36
IO_T1U_N12_43_AK35	VADJ_1V8_PGOOD_LS	56
IO_L12N_T1U_N11_GC_43_AM34	FMCP_HSPC_PG_M2C_LS	56
IO_L12P_T1U_N10_GC_43_AM33	FMCP_HSPC_H_PRSNT_M2C_B_LS	56
IO_L11N_T1U_N9_GC_43_AL34	FMCP_HSPC_REFCLK_M2C_N	37
IO_L11P_T1U_N8_GC_43_AK34	FMCP_HSPC_REFCLK_M2C_P	37
IO_L10N_T1U_N7_QBC_AD4N_43_AP33	FMCP_HSPC_REFCLK_C2M_N	37
IO_L10P_T1U_N6_QBC_AD4P_43_AN33	FMCP_HSPC_REFCLK_C2M_P	37
IO_L9N_T1L_N5_AD12N_43_AN36	FMCP_HSPC_SYNC_M2C_N	37
IO_L9P_T1L_N4_AD12P_43_AM36	FMCP_HSPC_SYNC_M2C_P	37
IO_L8N_T1L_N3_AD5N_43_AN35	FMCP_HSPC_SYNC_C2M_N	37
IO_L8P_T1L_N2_AD5P_43_AN34	FMCP_HSPC_SYNC_C2M_P	37
IO_L7N_T1L_N1_QBC_AD13N_43_AL36	FMCP_HSPC_LA00_CC_N	35
IO_L7P_T1L_N0_QBC_AD13P_43_AL35	FMCP_HSPC_LA00_CC_P	35
IO_TOU_N12_VRP_43_AR34	VRP_43	10
IO_L6N_TOU_N11_AD6N_43_AT37	FMCP_HSPC_LA04_N	36
IO_L6P_TOU_N10_AD6P_43_AR37	FMCP_HSPC_LA04_P	36
IO_L5N_TOU_N9_AD14N_43_AP37	FMCP_HSPC_LA07_N	36
IO_L5P_TOU_N8_AD14P_43_AP36	FMCP_HSPC_LA07_P	36
IO_L4N_TOU_N7_DBC_AD7N_43_AT40	FMCP_HSPC_LA03_N	35
IO_L4P_TOU_N6_DBC_AD7P_43_AT39	FMCP_HSPC_LA03_P	35
IO_L3N_TOL_N5_AD15N_43_AR35	FMCP_HSPC_LA10_N	34
IO_L3P_TOL_N4_AD15P_43_AP35	FMCP_HSPC_LA10_P	34
IO_L2N_TOL_N3_43_AT36	FMCP_HSPC_LA06_N	34
IO_L2P_TOL_N2_43_AT35	FMCP_HSPC_LA06_P	34
IO_L1N_TOL_N1_DBC_43_AR38	FMCP_HSPC_LA05_N	34
IO_L1P_TOL_N0_DBC_43_AP38	FMCP_HSPC_LA05_P	34
VREF_43_AJ29	VREF_43	
VADJ_1V8_FPGA		
AH32		
VCCO_43_AH32		
AK36		
AL33		
AM30		
AP34		
AT38		

U1

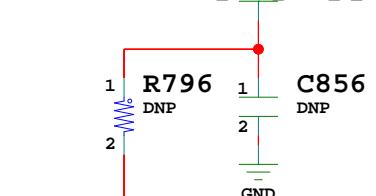
SOC_2104_1MM_IRON



Bank 45 HP

SOC_VU9P_FLGA2104_IRONWOOD

FMCP_HSPC_VREF_A_M2C

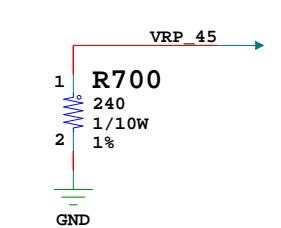


BANK 45 XCVU9PFLGA2104

IO_T3U_N12_45_K36	NC	
L35	FMCP_HSPC_LA21_N	36
M35	FMCP_HSPC_LA21_P	36
M32	FMCP_HSPC_LA20_N	35
N32	FMCP_HSPC_LA20_P	35
M33	FMCP_HSPC_LA19_N	36
N33	FMCP_HSPC_LA19_P	36
K33	FMCP_HSPC_LA32_N	36
L33	FMCP_HSPC_LA32_P	36
N35	FMCP_HSPC_LA22_N	35
N34	FMCP_HSPC_LA22_P	35
K34	FMCP_HSPC_LA33_N	35
L34	FMCP_HSPC_LA33_P	35
R36	NC	
IO_L18N_T2U_N11_AD2N_45_M38	FMCP_HSPC_LA30_N	36
N38	FMCP_HSPC_LA30_P	36
IO_L18P_T2U_N10_AD2P_45_N38	FMCP_HSPC_LA28_N	36
IO_L17N_T2U_N9_AD10N_45_L36	FMCP_HSPC_LA28_P	36
M36	FMCP_HSPC_LA31_N	35
N37	FMCP_HSPC_LA31_P	35
P37	FMCP_HSPC_CLK1_M2C_N	35
M37	FMCP_HSPC_CLK1_M2C_P	35
P36	FMCP_HSPC_LA17_CC_N	34
P35	FMCP_HSPC_LA17_CC_P	34
IO_L13N_T2L_N1_GC_QBC_45_P34	IO_L13P_T2L_N0_GC_QBC_45_R34	
IO_T1U_N12_45_V30	IO_T1U_N12_45_V30	
R33	NC	
T33	NC	
P32	USER_SMA_CLOCK_N	10,45
R32	USER_SMA_CLOCK_P	10,45
P31	USER_SMA_CLOCK_N	10,45
R31	USER_SMA_CLOCK_P	10,45
W31	NC	
Y31	NC	
U32	NC	
U31	NC	
T31	NC	
T30	NC	
Y33	VRP_45	10
IO_L6N_TOU_N11_AD6N_45_T35	FMCP_HSPC_LA24_N	36
T34	FMCP_HSPC_LA24_P	36
IO_L6P_TOU_N10_AD6P_45_T34	FMCP_HSPC_LA27_N	34
IO_L5N_TOU_N9_AD14N_45_V34	FMCP_HSPC_LA27_P	34
IO_L5P_TOU_N8_AD14P_45_V33	FMCP_HSPC_LA29_N	35
U35	FMCP_HSPC_LA29_P	35
W34	FMCP_HSPC_LA25_N	35
IO_L3N_TOL_N5_AD15N_45_W34	FMCP_HSPC_LA25_P	35
Y34	FMCP_HSPC_LA26_N	34
U33	FMCP_HSPC_LA26_P	34
IO_L2P_TOL_N2_45_V32	FMCP_HSPC_LA23_N	34
W32	FMCP_HSPC_LA23_P	34
Y32	VREF_45	
U30	VREF_45	

U1

SOC_2104_1MM_IRON



FPGA Banks 43 45 FMCP HSPC



TITLE: FPGA Banks 43 45 FMCP HSPC
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:37

VER: 1.1

SHEET SIZE: B

REV: 02

SHEET 10 OF 76

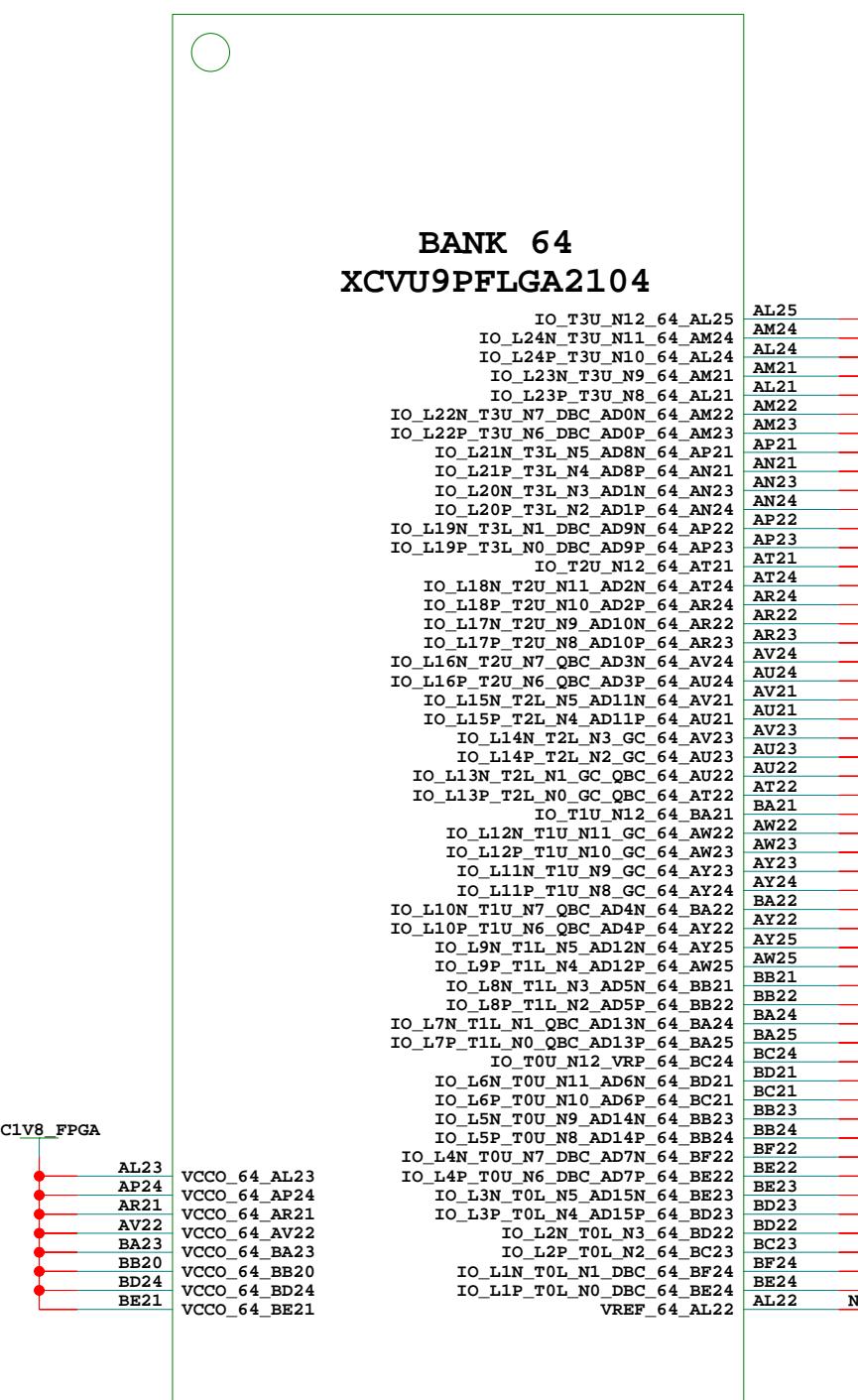
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Layout: Place resistor and capacitor for VREF

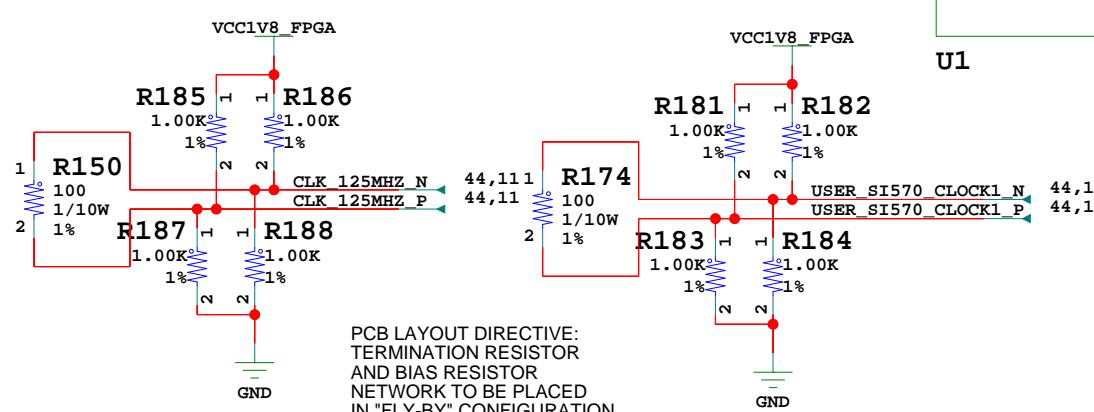
Underneath the FPGA via array
right next to the via

Bank 64 HP

SOC_VU9P_FLGA2104_IRONWOOD



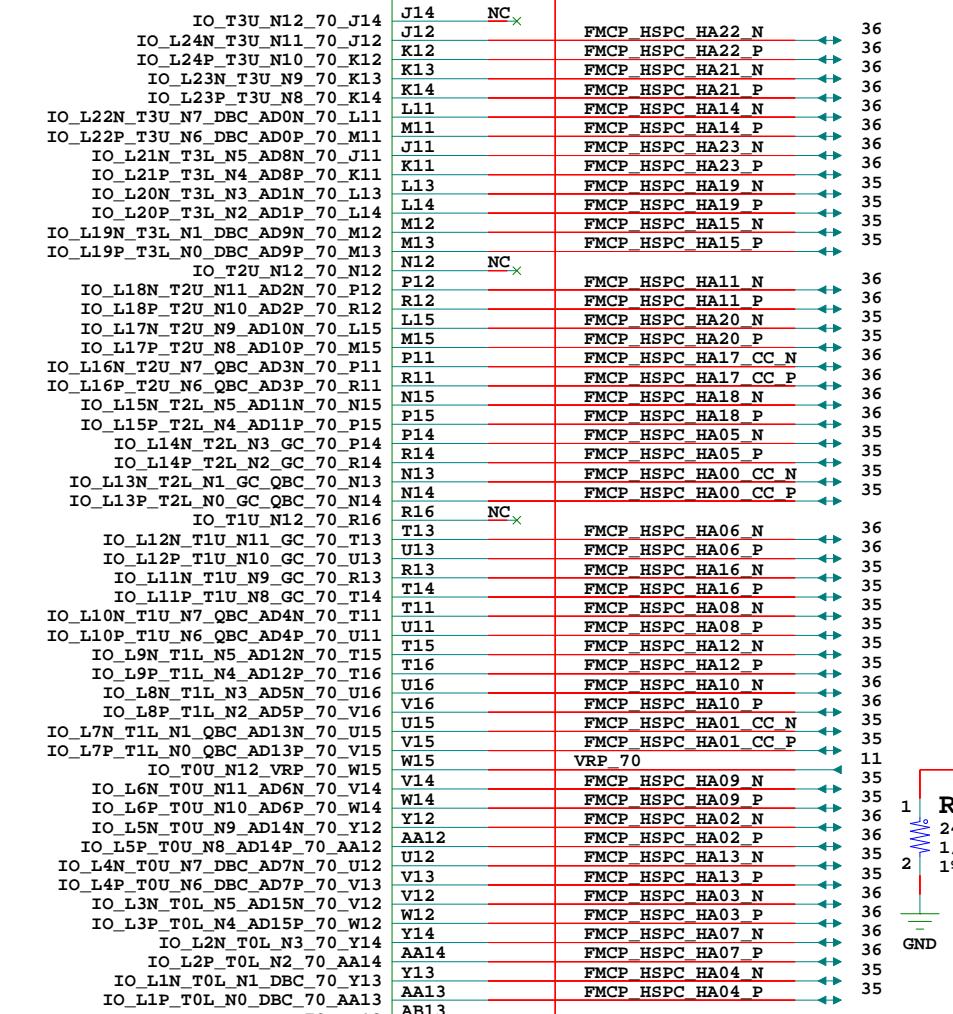
SOC_2104_1MM_IRON



Bank 70 HP

SOC_VU9P_FLGA2104_IRONWOOD

BANK 70 XCVU9PFLGA2104



SOC_2104_1MM_IRON

FPGA Banks 64 GPIO 70 FMCP HSPC

XILINX

TITLE: FPGA Banks 64 GPIO 70 FMCP HSPC
SCHEM., ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:37

VER: 1.1

SHEET SIZE: B

REV: 02

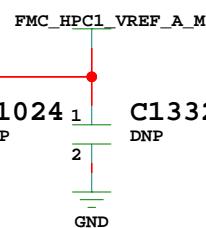
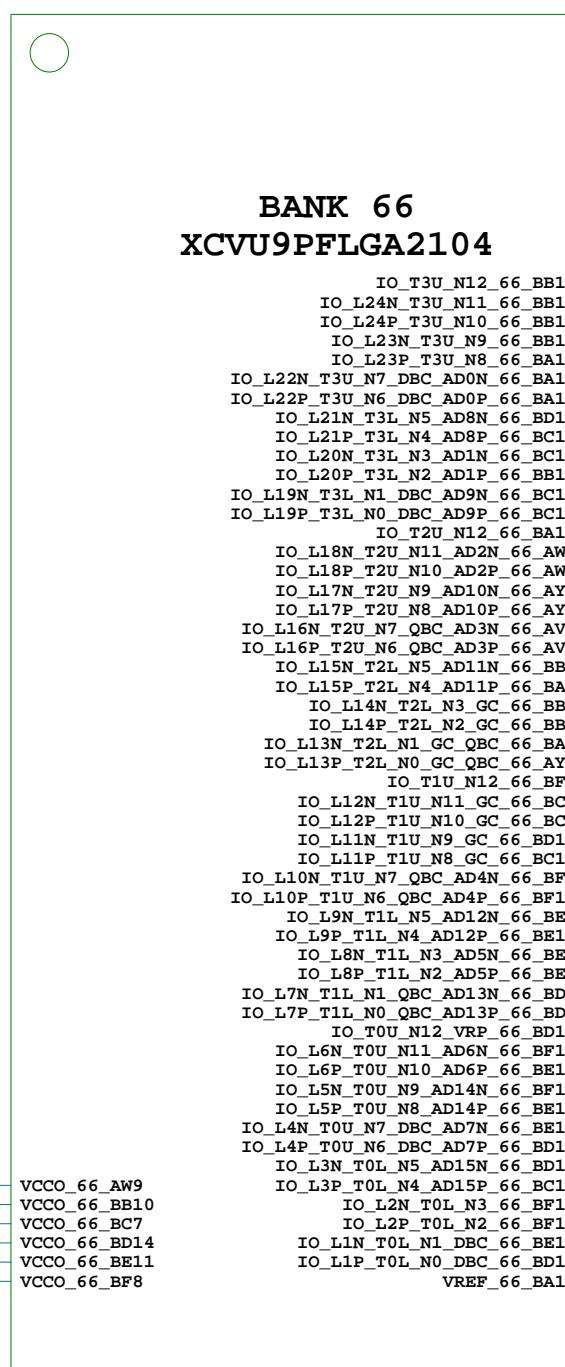
SHEET 11 OF 76

DRAWN BY: DN

Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via

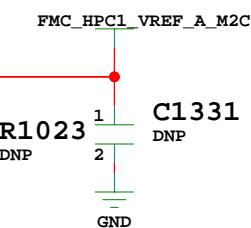
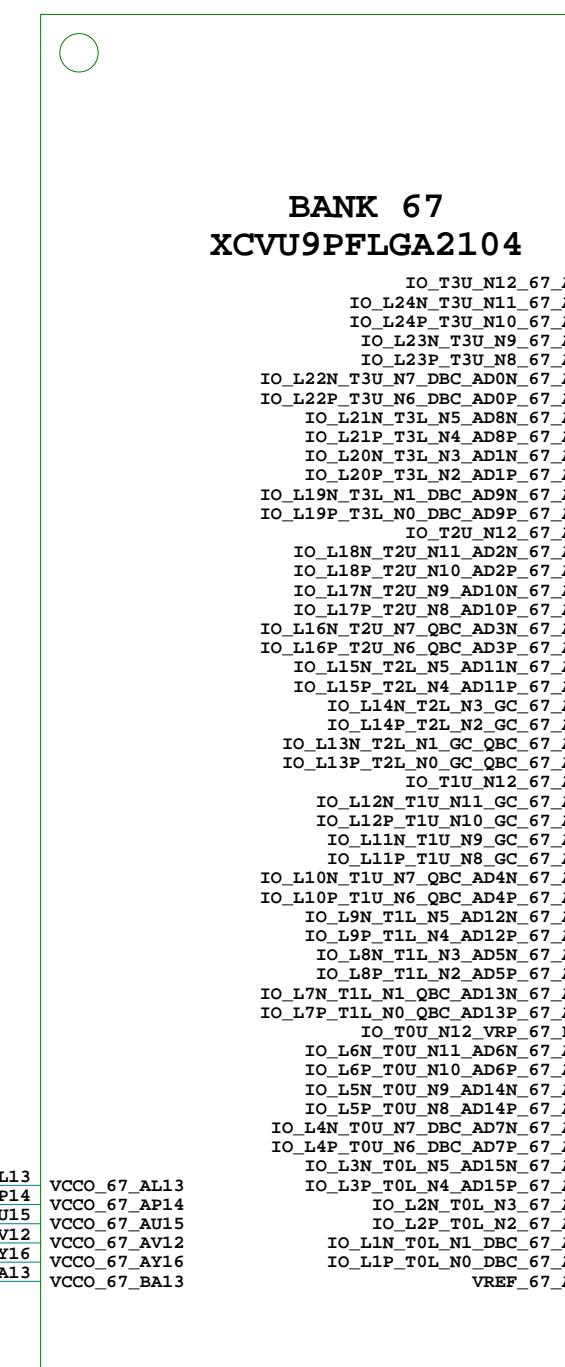
Bank 47 HP

SOC_VU9P_FLGA2104_IRONWOOD



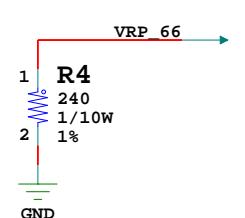
Bank 48 HP

SOC_VU9P_FLGA2104_IRONWOOD



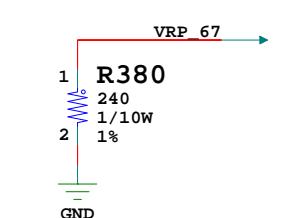
U1

SOC_2104_1MM_IRON



U1

SOC_2104_1MM_IRON



FPGA Banks 66 67 FMC HPC1



TITLE: FPGA Banks 66 67 FMC HPC1
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:37

VER: 1.1

SHEET SIZE: B

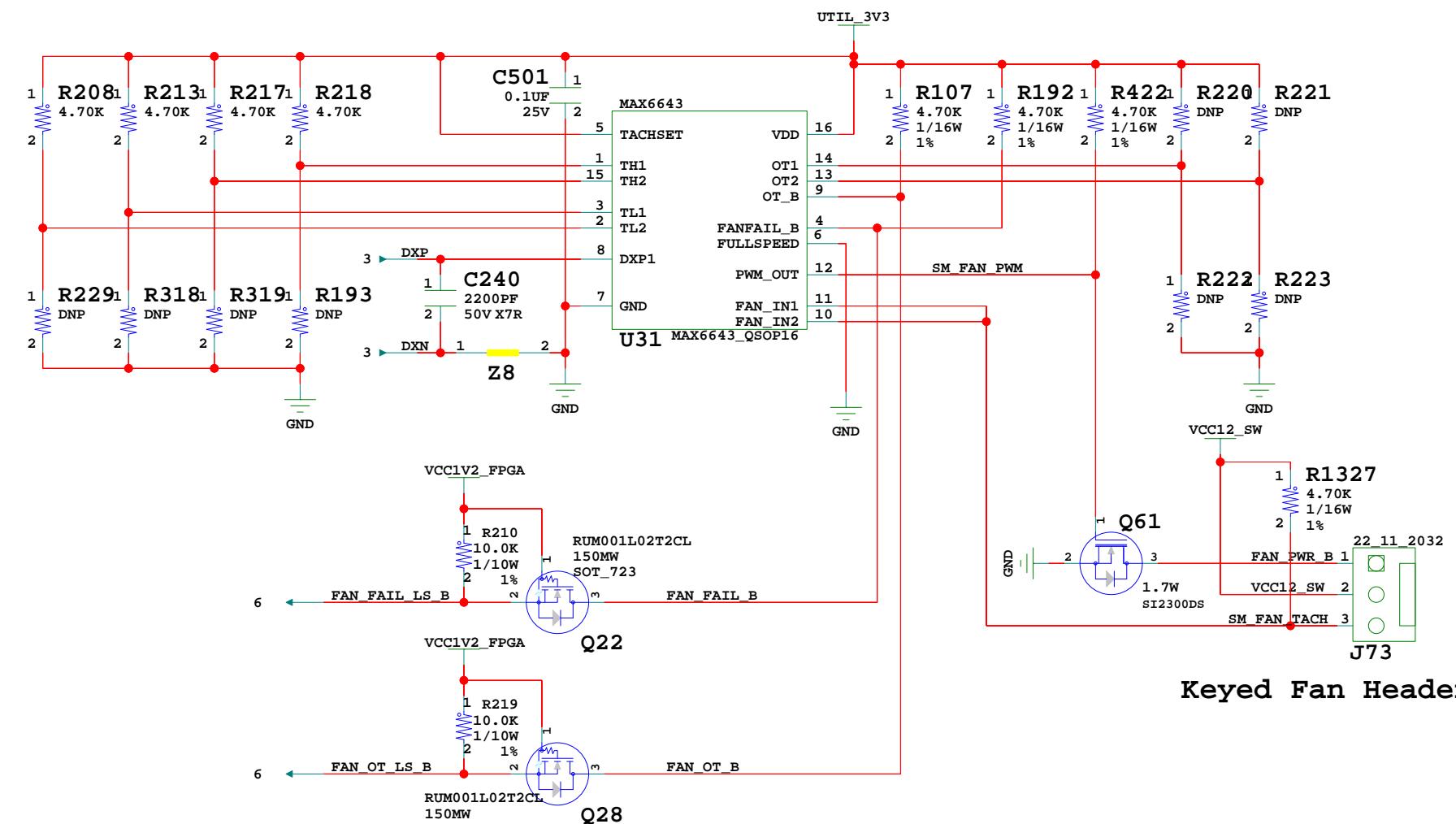
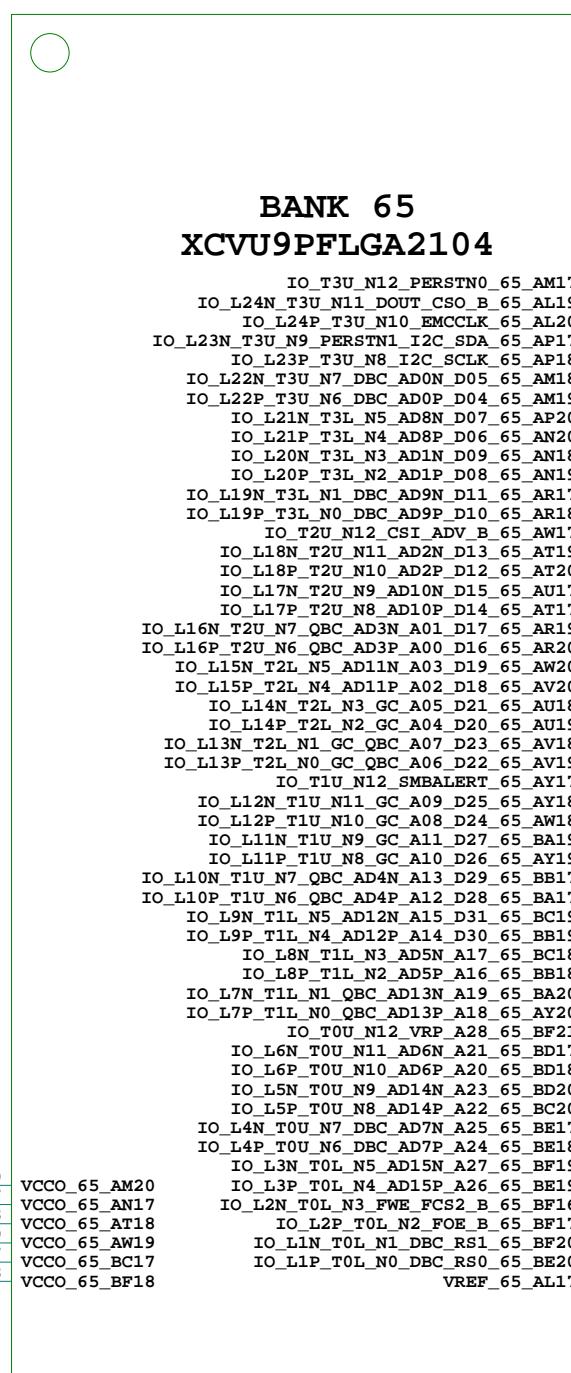
REV: 02

SHEET 12 OF 76

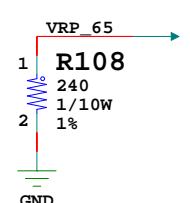
DRAWN BY: DN

Bank 65 HP

SOC_VU9P_FLGAG2104_IRONWOOD

**Keyed Fan Header**

U1 SOC_2104_1MM_IRON

**FPGA Bank 65 BPI Flash IF**

TITLE: FPGA Bank 65 BPI Flash IF
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:39	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 13 OF 76	DRAWN BY: DN

SOC_VU9P_FLGA2104_IRONWOOD

SOC_VU9P_FLGA2104_IRONWOOD

SOC_VU9P_FLGA2104_IRONWOOD

BANK 125
XCVU9PFLGA2104

MGTYTXP0_125_AC40
 MGTYTXN0_125_AC41
 MGTYRXP0_125_AC45
 MGTYRXN0_125_AC46
 MGTYTXP1_125_AA40
 MGTYTXN1_125_AA41
 MGTYRXP1_125_AB43
 MGTYRXN1_125_AB44
 MGTYTXP2_125_W40
 MGTYTXN2_125_W41
 MGTYRXP2_125_AA45
 MGTYRXN2_125_AA46
 MGTYTXP3_125_U40
 MGTYTXN3_125_U41
 MGTYRXP3_125_Y43
 MGTYRXN3_125_Y44
 MGTRCLK0P_125_AB38
 MGTRCLK0N_125_AB39
 MGTRCLK1P_125_Y38
 MGTRCLK1N_125_Y39

AC40 FMCP HSPC DP12 C2M P 37
 AC41 FMCP HSPC DP12 C2M N 37
 AC45 FMCP HSPC DP12 M2C P 37
 AC46 FMCP HSPC DP12 M2C N 37
 AA40 FMCP HSPC DP13 C2M P 37
 AA41 FMCP HSPC DP13 C2M N 37
 AB43 FMCP HSPC DP13 M2C P 37
 AB44 FMCP HSPC DP13 M2C N 37
 W40 FMCP HSPC DP14 C2M P 37
 W41 FMCP HSPC DP14 C2M N 37
 AA45 FMCP HSPC DP14 M2C P 37
 AA46 FMCP HSPC DP14 M2C N 37
 U40 FMCP HSPC DP15 C2M P 37
 U41 FMCP HSPC DP15 C2M N 37
 Y43 FMCP HSPC DP15 M2C P 37
 Y44 FMCP HSPC DP15 M2C N 37
 AB38 FMCP HSPC GBTCLK3 M2C C P 15
 AB39 FMCP HSPC GBTCLK3 M2C C N 15
 Y38 FMCP HSPC GBT1 3 P 14
 Y39 FMCP HSPC GBT1 3 N 14

SOC_2104_1MM_IRON

BANK 126
XCVU9PFLGA2104

MGTYTXP0_126_T42
 MGTYTXN0_126_T43
 MGTYRXP0_126_W45
 MGTYRXN0_126_W46
 MGTYTXP1_126_P42
 MGTYTXN1_126_F43
 MGTYRXP1_126_U45
 MGTYRXN1_126_U46
 MGTYTXP2_126_M42
 MGTYTXN2_126_M43
 MGTYRXP2_126_R45
 MGTYRXN2_126_R46
 MGTYTXP3_126_K42
 MGTYTXN3_126_K43
 MGTYRXP3_126_N45
 MGTYRXN3_126_N46
 MGTRCLK0P_126_V38
 MGTRCLK0N_126_V39
 MGTRCLK1P_126_T38
 MGTRCLK1N_126_T39
 MGTRREF_LN_L41
 MGTAVTRCAL_LN_L40

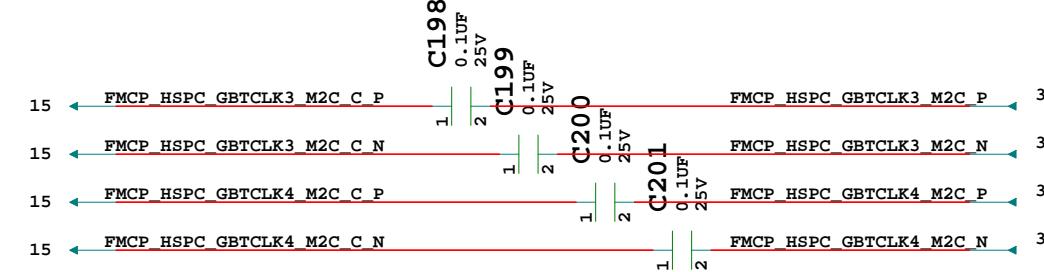
T42 FMCP HSPC DP4 C2M P 34
 W45 FMCP HSPC DP4 M2C P 34
 W46 FMCP HSPC DP4 M2C N 34
 P42 FMCP HSPC DP5 C2M P 34
 F43 FMCP HSPC DP5 C2M N 34
 U45 FMCP HSPC DP5 M2C P 34
 U46 FMCP HSPC DP5 M2C N 34
 M42 FMCP HSPC DP6 C2M P 34
 M43 FMCP HSPC DP6 C2M N 34
 R45 FMCP HSPC DP6 M2C P 34
 R46 FMCP HSPC DP6 M2C N 34
 K42 FMCP HSPC DP7 C2M P 34
 K43 FMCP HSPC DP7 C2M N 34
 N45 FMCP HSPC DP7 M2C P 34
 N46 FMCP HSPC DP7 M2C N 34
 V38 FMCP HSPC GBT0 1 P 14
 V39 FMCP HSPC GBT0 1 N 14
 T38 FMCP HSPC GBT1 1 P 14
 T39 FMCP HSPC GBT1 1 N 14
 L41 MGTRREF_126
 L40

SOC_2104_1MM_IRON

BANK 127
XCVU9PFLGA2104

MGTYTXP0_127_H42
 MGTYTXN0_127_H43
 MGTYRXP0_127_L45
 MGTYRXN0_127_L46
 MGTYTXP1_127_F42
 MGTYTXN1_127_F43
 MGTYRXP1_127_J45
 MGTYRXN1_127_J46
 D42 FMCP HSPC DP16 C2M P 37
 D43 FMCP HSPC DP18 C2M N 37
 MGTYTXN2_127_D43
 MGTYRXP2_127_G45
 MGTYRXN2_127_G46
 MGTYTXP3_127_B42
 MGTYTXN3_127_B43
 MGTYRXP3_127_E45
 MGTYRXN3_127_E46
 R40 FMCP HSPC GBTCLK4 M2C C P 15
 R41 FMCP HSPC GBTCLK4 M2C C N 15
 N40 FMCP HSPC GBT1 4 P 14
 N41 FMCP HSPC GBT1 4 N 14

SOC_2104_1MM_IRON

**FPGA Banks 125 126 127**

 TITLE: FPGA Banks 125 126 127
 SCHEM, ROHS COMPLIANT
 HW-U1-VCU118_REV1_1

 ASSY P/N: 0432001
 PCB P/N: 1280906
 SCH P/N: 0381739
 TEST P/N: TSS0185

DATE: 12/01/2016:13:37

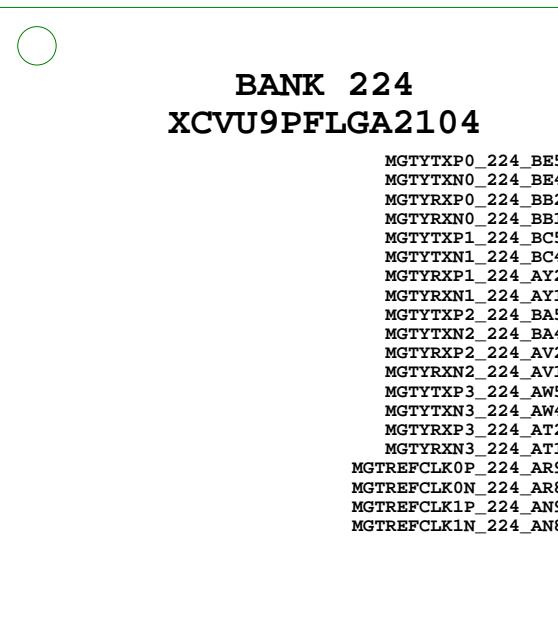
VER: 1.1

SHEET SIZE: B

REV: 02

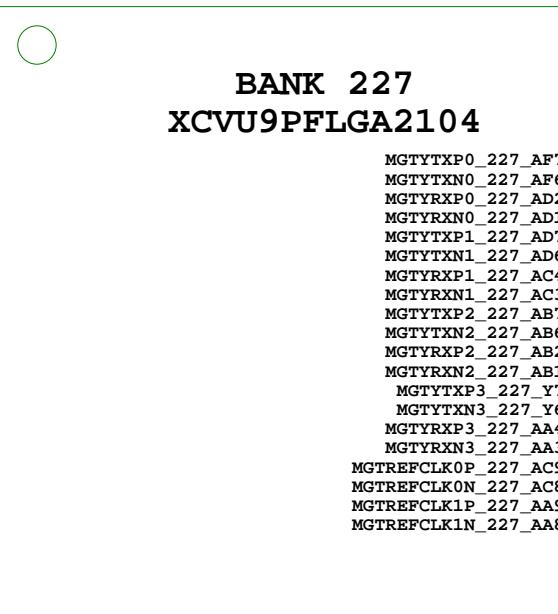
SHEET 15 OF 76 DRAWN BY: DN

SOC_VU9P_FLGA2104_IRONWOOD



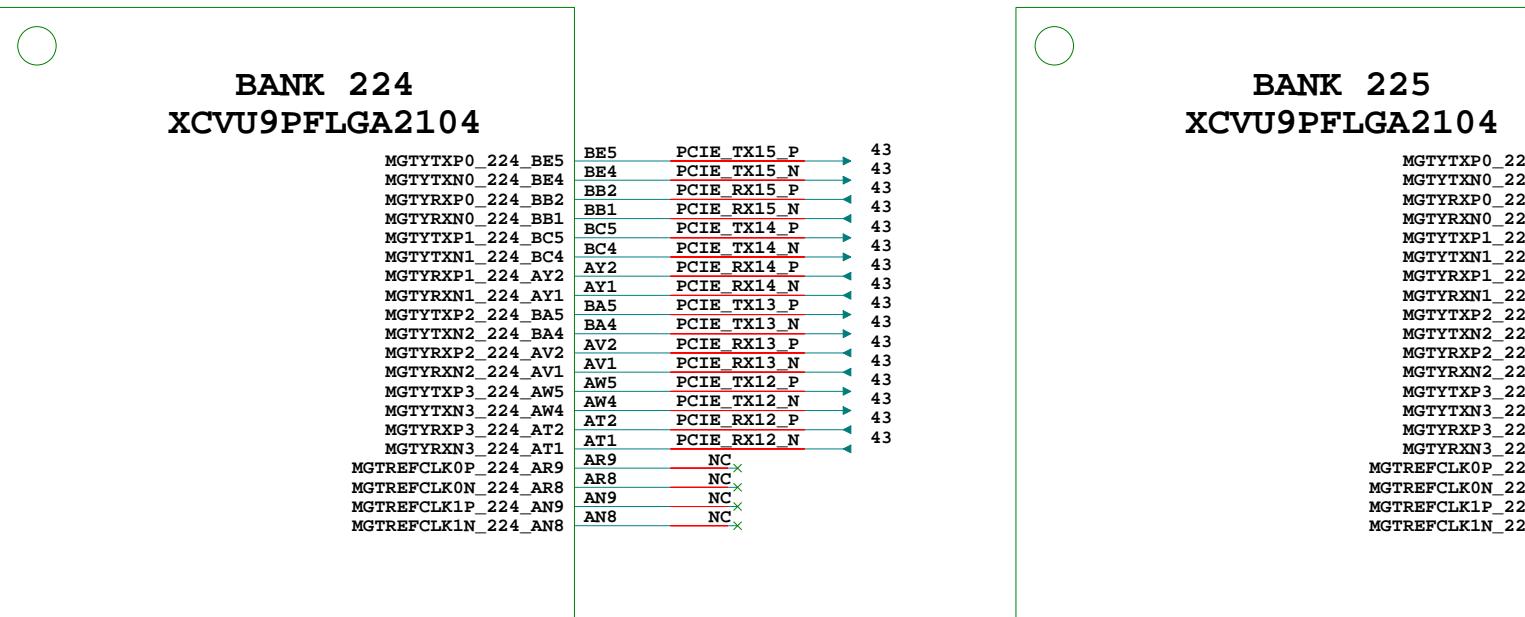
U1 SOC_2104_1MM_IRON

SOC_VU9P_FLGA2104_IRONWOOD



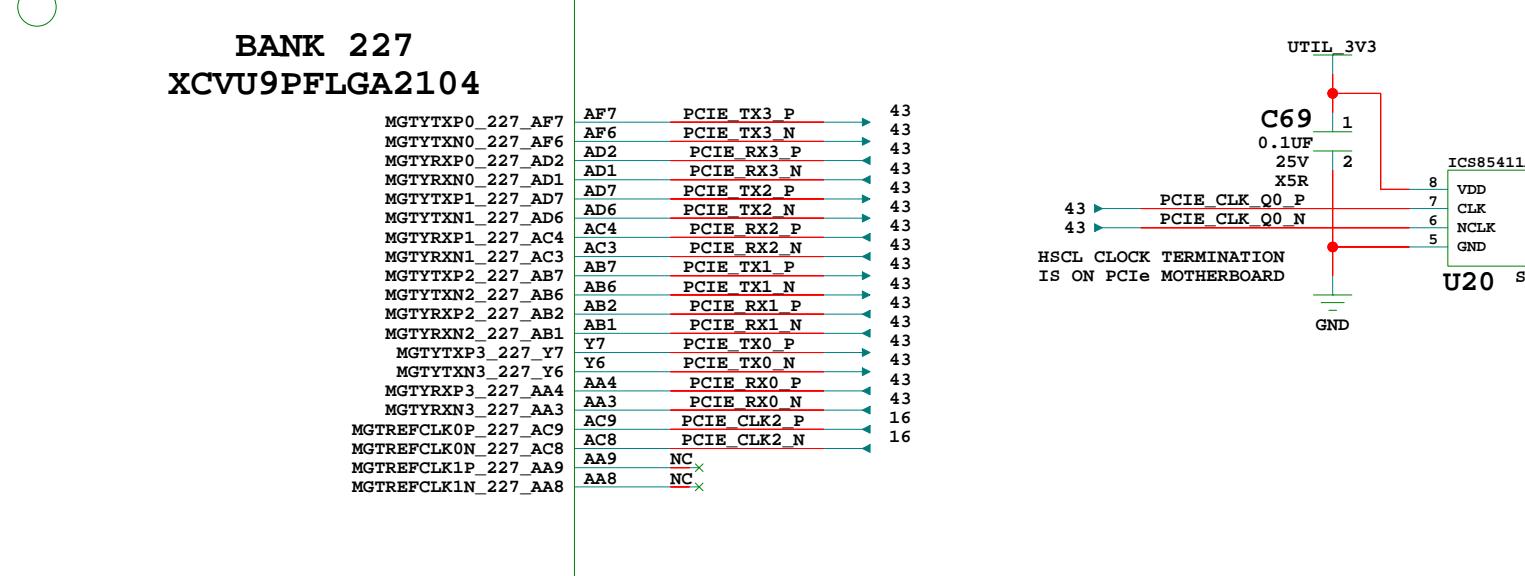
U1 SOC_2104_1MM_IRON

SOC_VU9P_FLGA2104_IRONWOOD



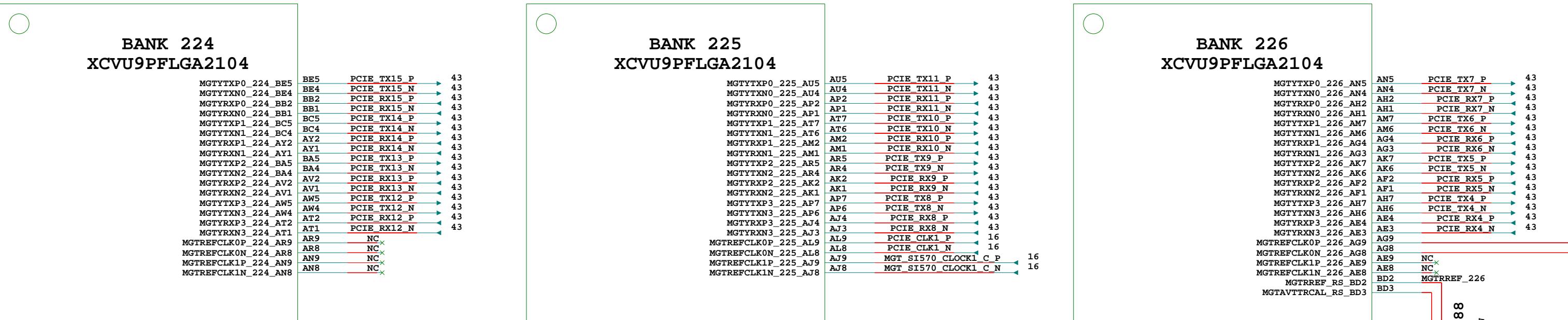
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SOC_VU9P_FLGA2104_IRONWOOD

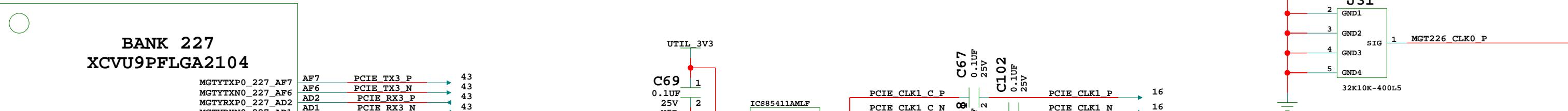


U1 SOC_2104_1MM_IRON

SOC_VU9P_FLGA2104_IRONWOOD

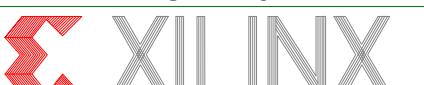


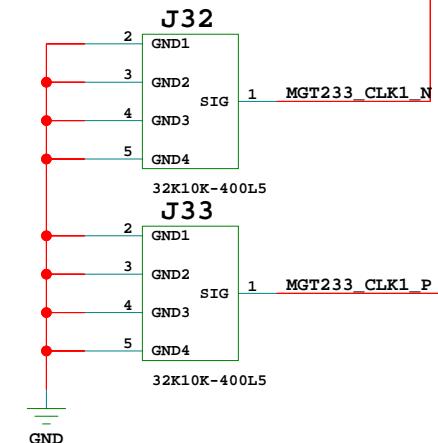
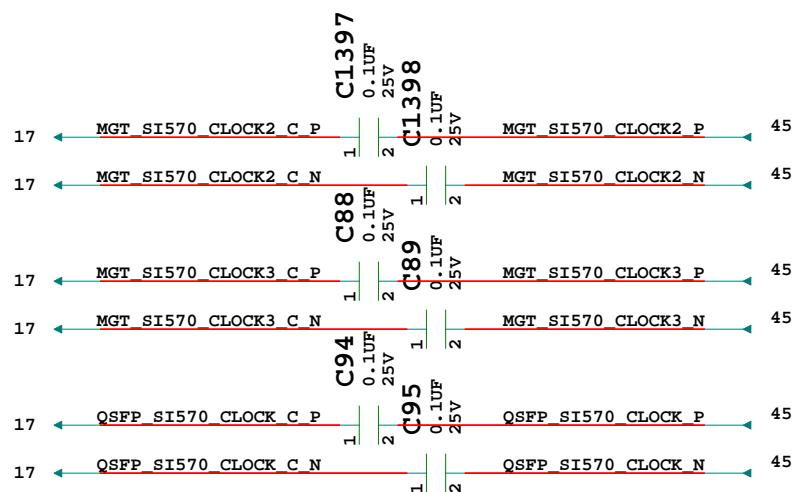
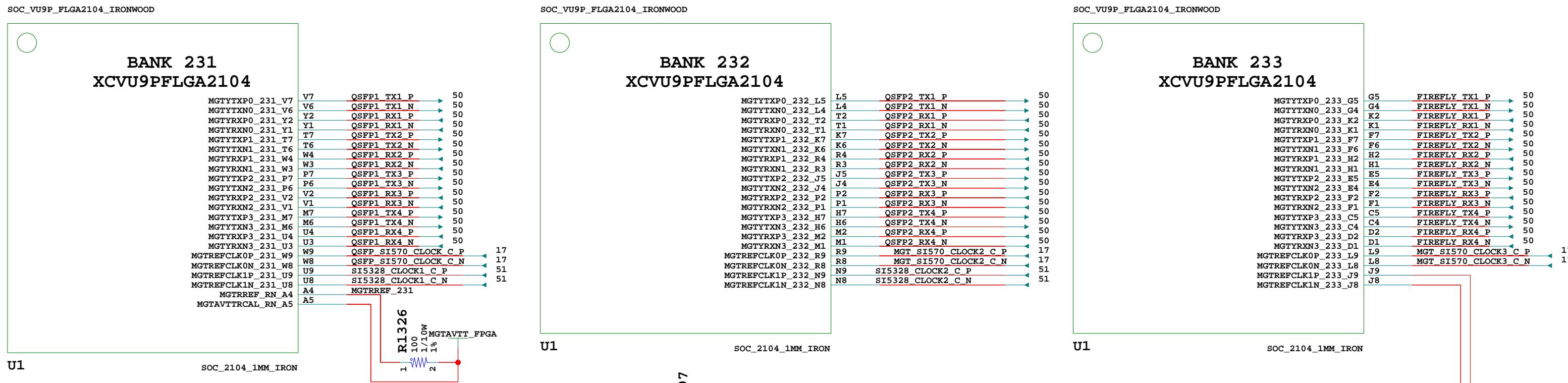
U1 SOC_2104_1MM_IRON



U1 SOC_2104_1MM_IRON

FPGA Banks 224 225 226 227

	
TITLE: FPGA Banks 224 225 226 227 SCHEM, ROHS COMPLIANT HW-U1-VCU118_REV1_1	ASSY P/N: 0432001 PCB P/N: 1280906 SCH P/N: 0381739 TEST P/N: TSS0185
DATE: 12/01/2016:13:37	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 16 OF 76	DRAWN BY: DN



FPGA Banks 231 232 233



**TITLE: FPGA Banks 231 232 233
SCHEM, ROHS COMPLIANT
HW-U1-VCU118 REV1 1**

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016 13:37

1 1

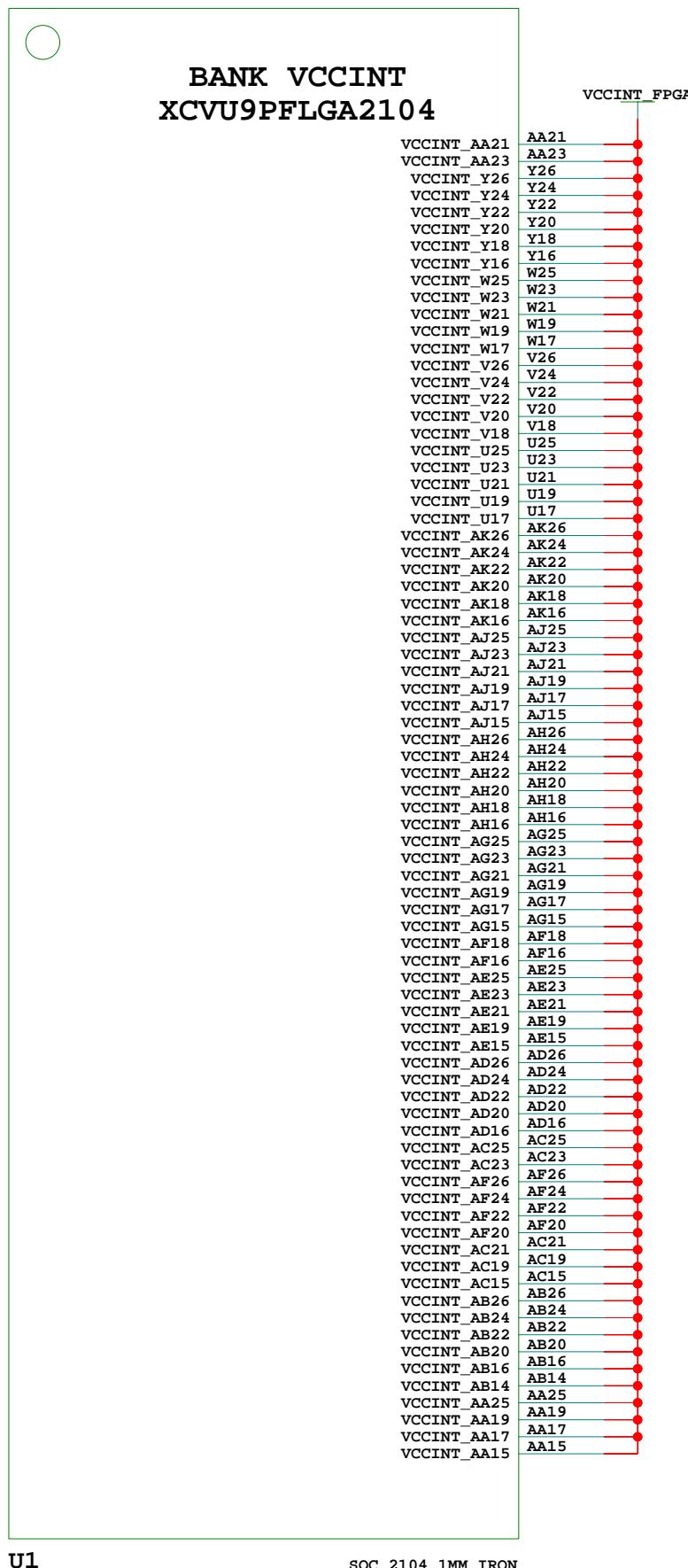
SHEET SIZE: B

03

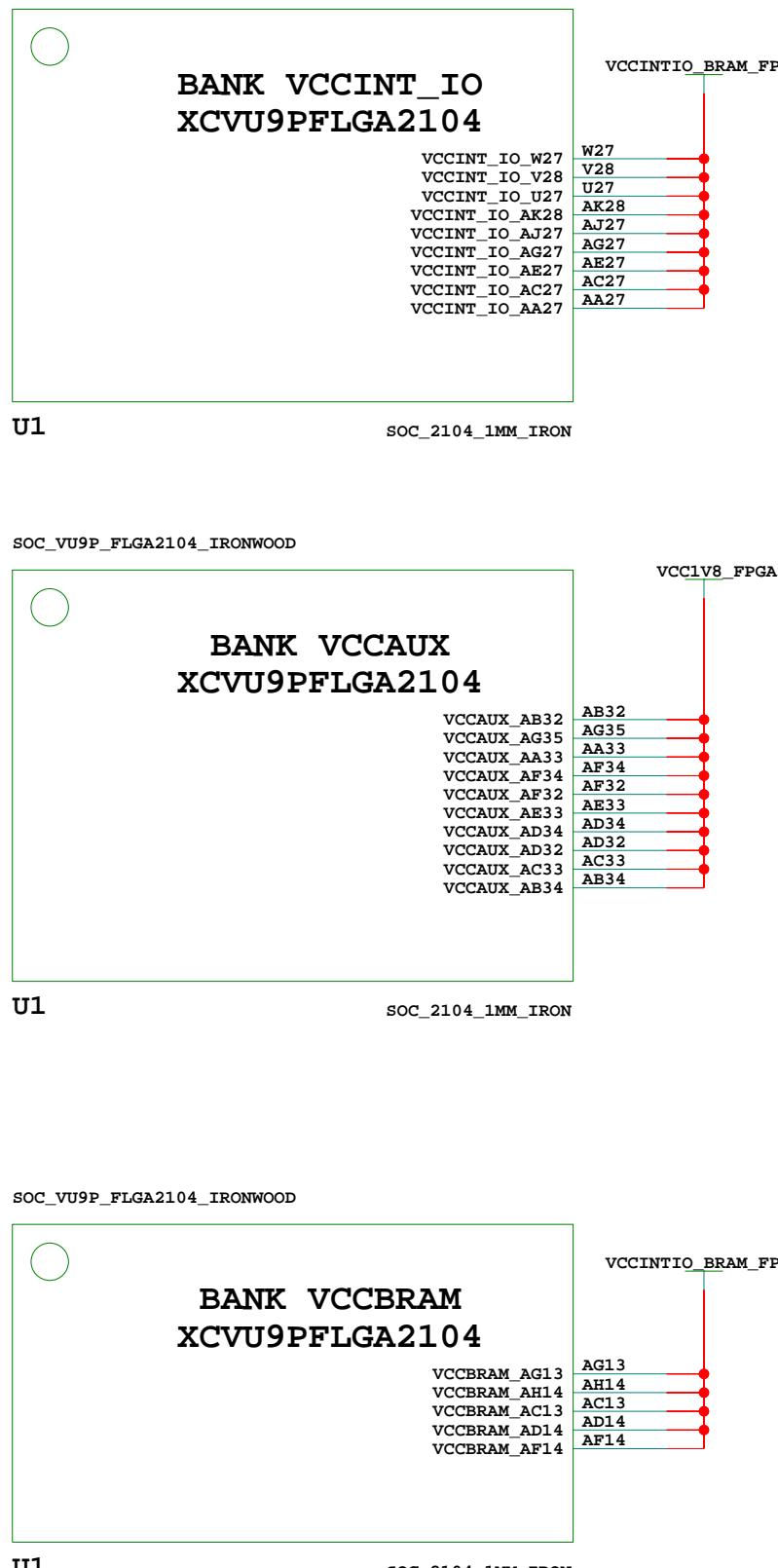
SHEET 17 OF 76

DN

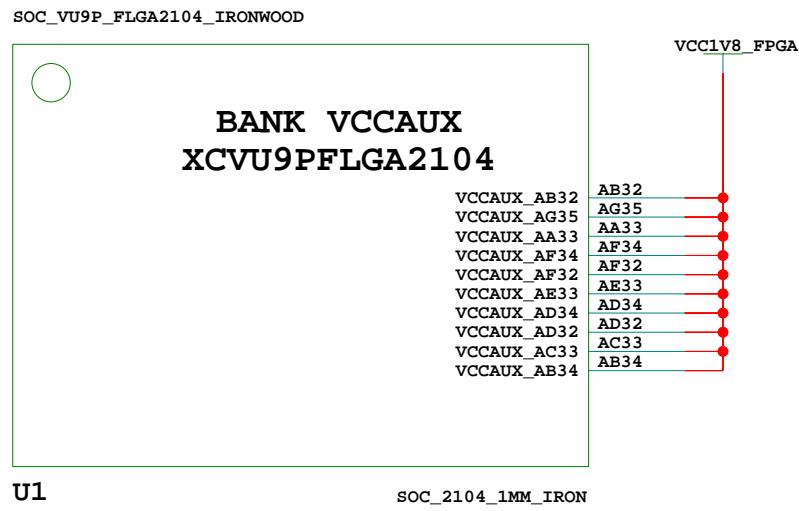
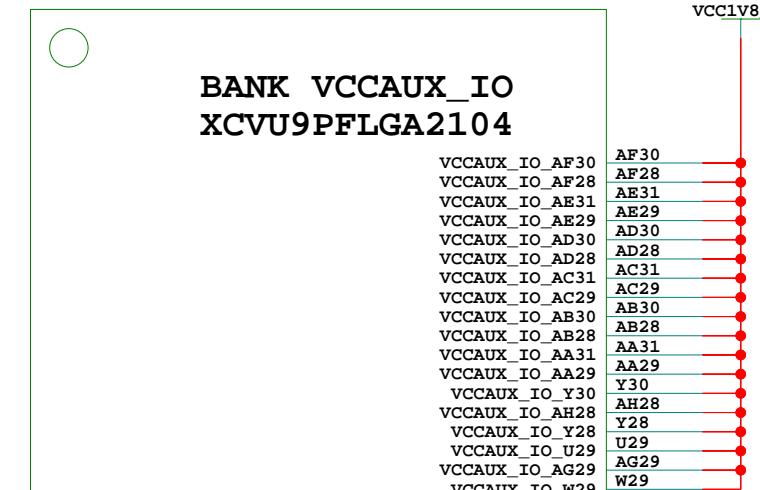
SOC_VU9P_FLGA2104_IRONWOOD



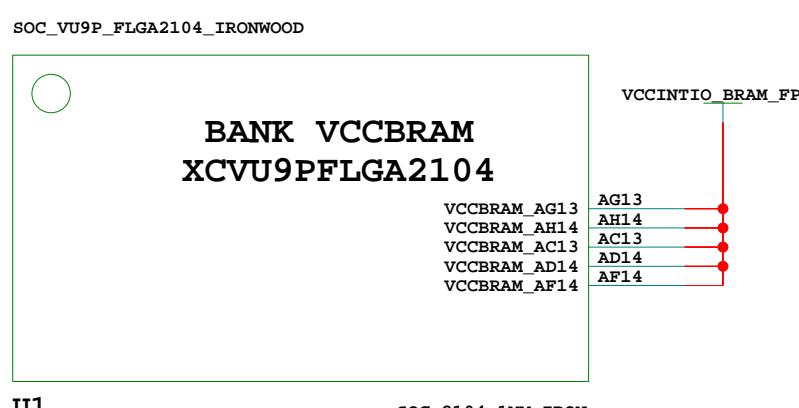
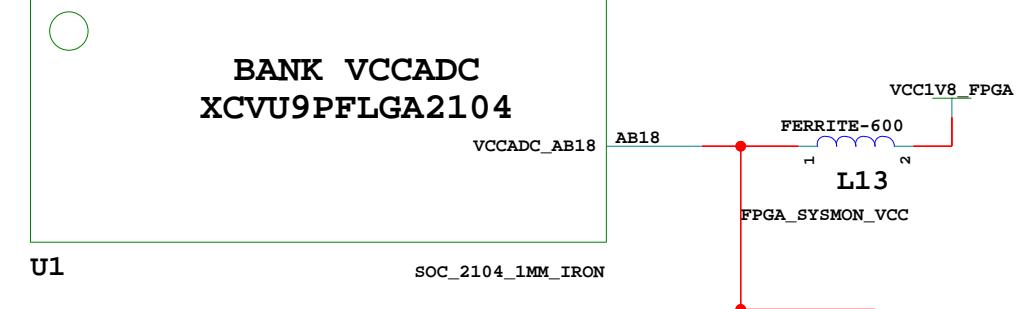
SOC_VU9P_FLGA2104_IRONWOOD



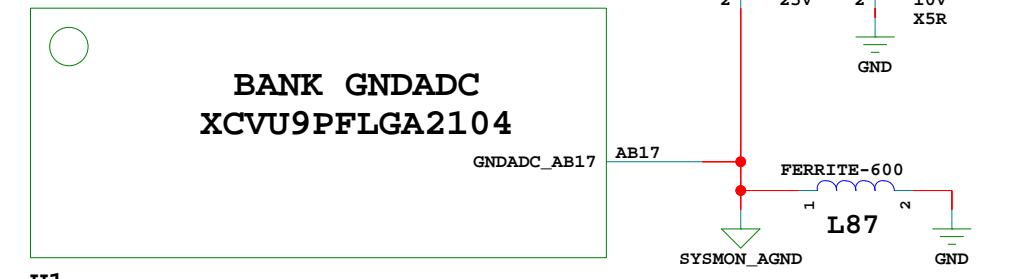
SOC_VU9P_FLGA2104_IRONWOOD



SOC_VU9P_FLGA2104_IRONWOOD



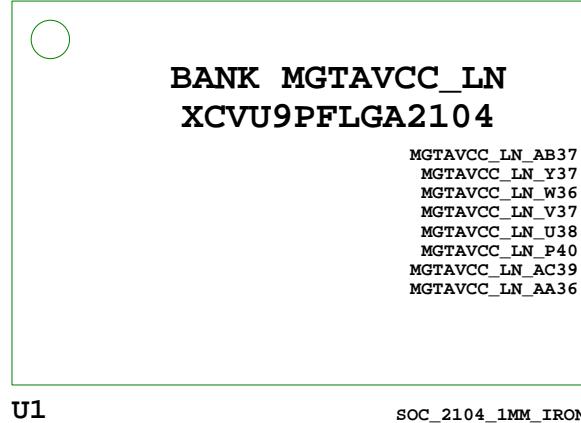
SOC_VU9P_FLGA2104_IRONWOOD

**FPGA Power 1**
XILINX

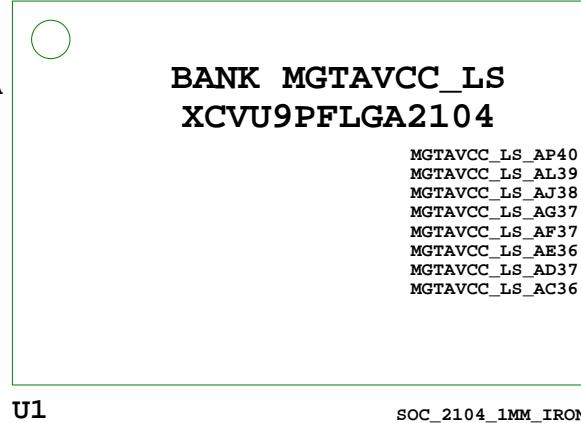
TITLE: FPGA Power 1
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

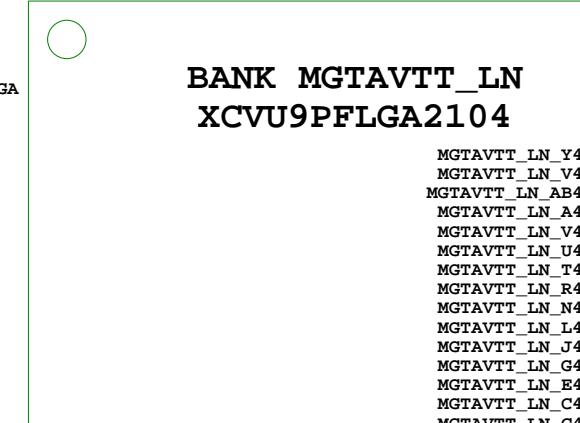
DATE: 12/01/2016:13:37	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 18 OF 76	DRAWN BY: DN



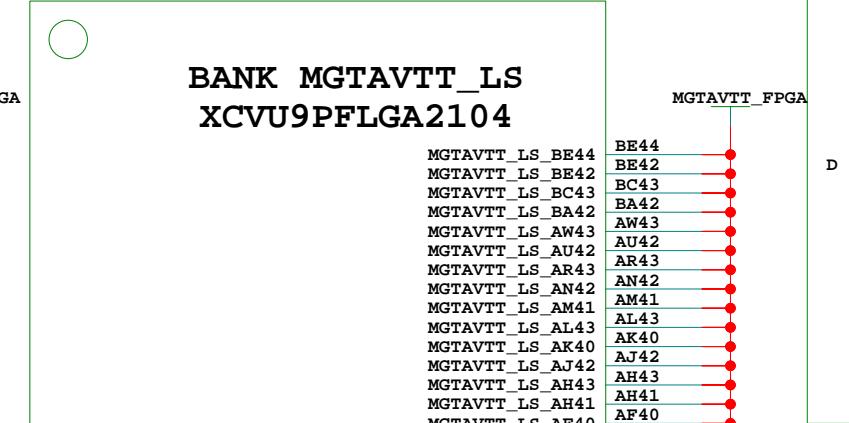
U1 SOC_2104_1MM_IRON



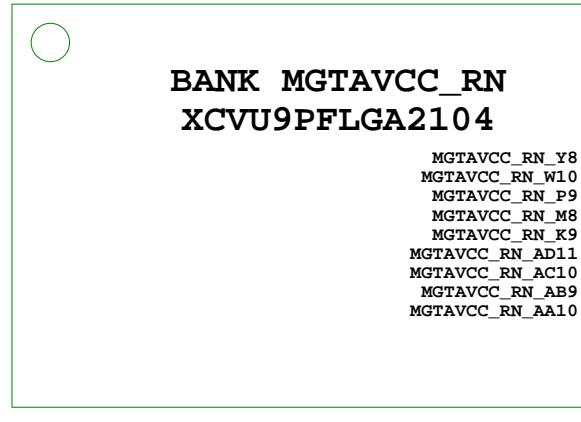
U1 SOC_2104_1MM_IRON



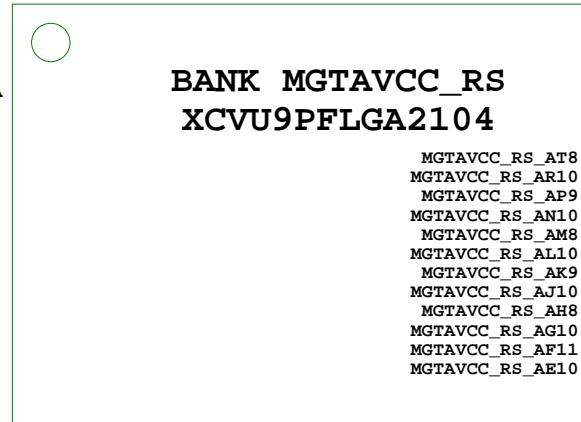
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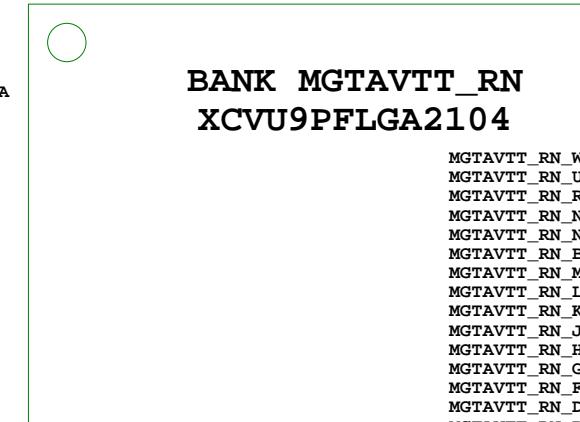
U1 SOC_2104_1MM_IRON



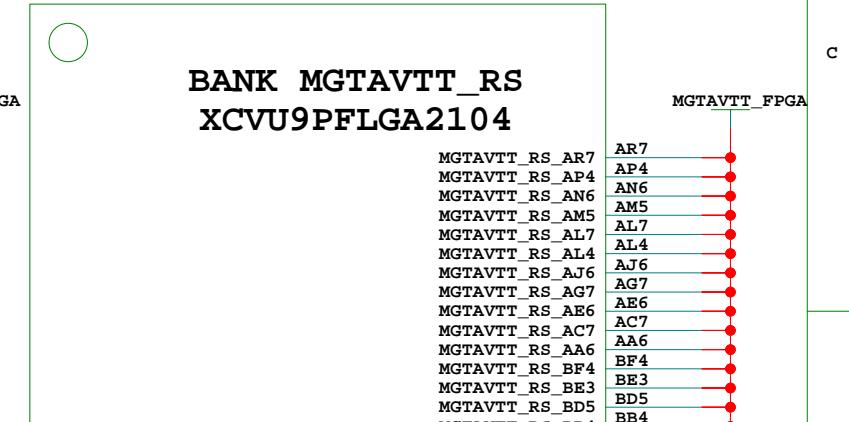
U1 SOC_2104_1MM_IRON



U1 SOC_2104_1MM_IRON



U1 SOC_2104_1MM_IRON



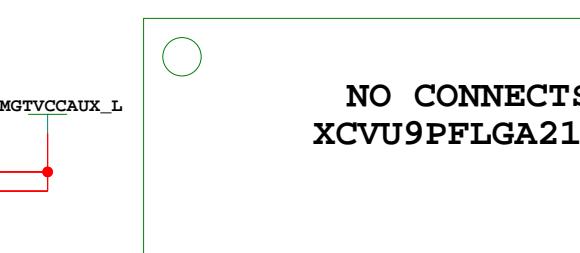
U1 SOC_2104_1MM_IRON



U1 SOC_2104_1MM_IRON



U1 SOC_2104_1MM_IRON



U1 SOC_2104_1MM_IRON



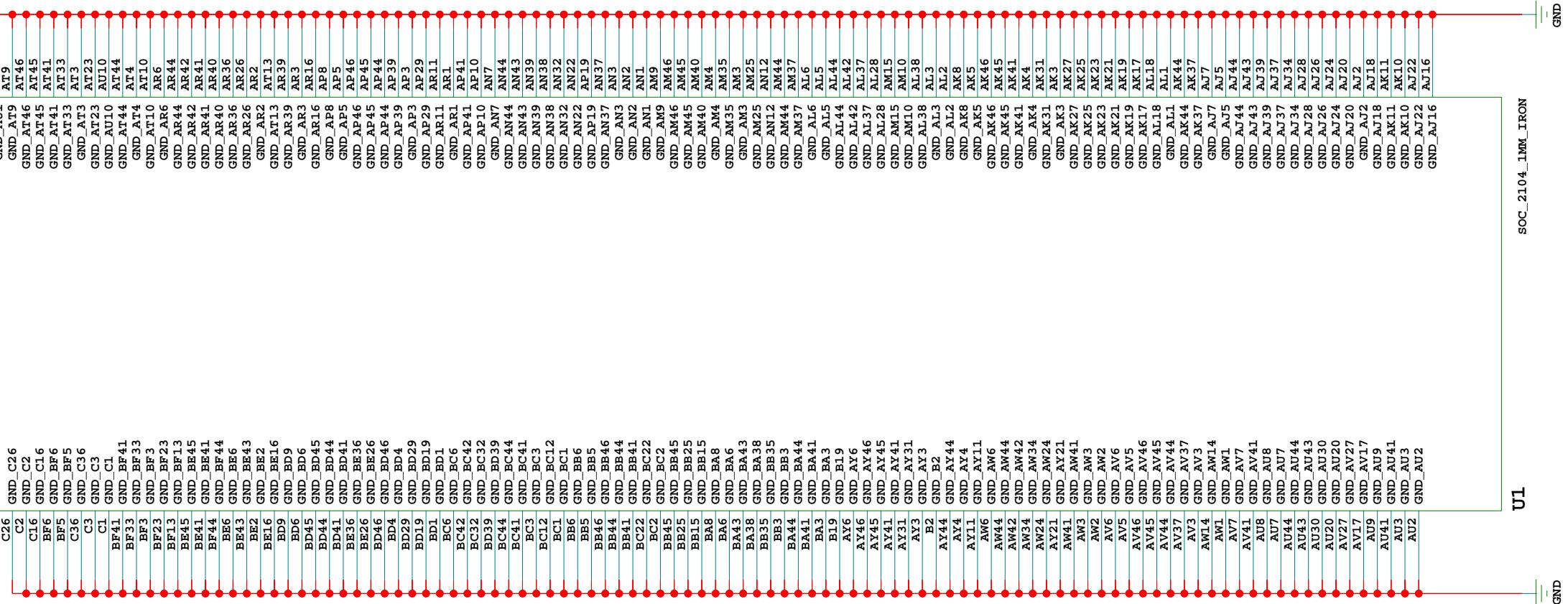
U1 SOC_2104_1MM_IRON



U1 SOC_2104_1MM_IRON

TITLE: FPGA Power 2		ASSY P/N: 0432001
SCHEM, ROHS COMPLIANT		PCB P/N: 1280906
HW-U1-VCU118_REV1_1		SCH P/N: 0381739
TEST P/N: TSS0185		TEST P/N: TSS0185
DATE: 12/01/2016:13:37		VER: 1.1
SHEET SIZE: B		REV: 02
SHEET 19 OF 76		DRAWN BY: DN

**BANK GND3
XCVU9PFLGA2104**



FPGA GND 3

 XILINX

**TITLE: FPGA GND 3
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1**

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:37

1.1

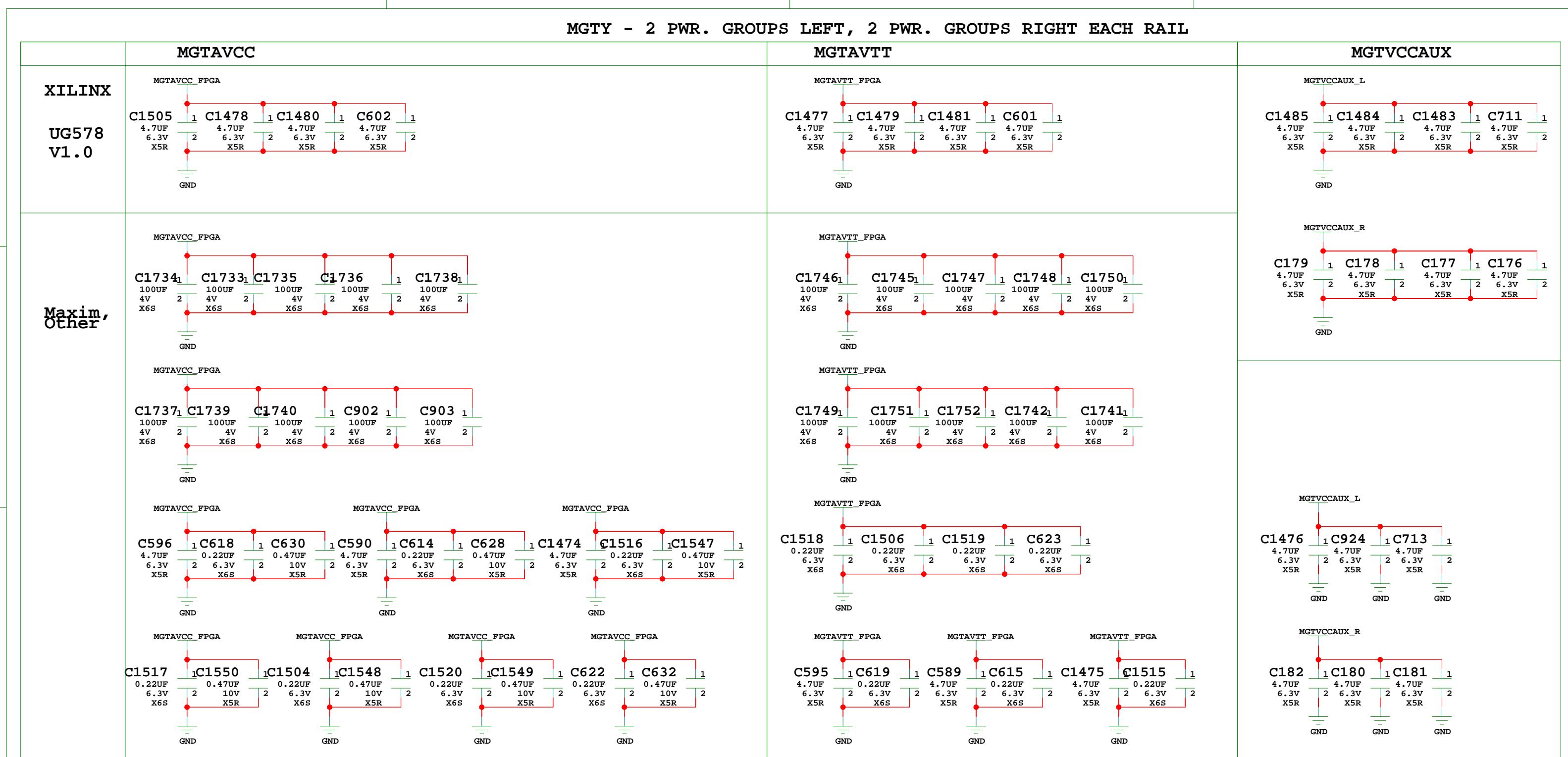
SHEET SIZE: B

02

SHEET 21 OF 76

DN

	4	3	2	1		
XILINX UG583 V1.7	<p>VCCINT</p>	<p>VCCAUX/AUX_IO</p>	<p>VCCINT_IO/VCCBRAM</p>	<p>VCCINT_FPGA VCC1V8_FPGA VCCINTIO_BRAM_FPGA</p>		
Maxim, Other				<p>VADJ_1V8_FPGA VCC1V2_FPGA UTIL_1V35 UTIL_3V3</p>		
XILINX UG583 V1.7	<p>VCCO_40 / VCCO_41 / VCCO_42</p>	<p>VCCO_46 / VCCO_47 / VCCO_48</p>	<p>VCCO_71 / VCCO_72 / VCCO_73</p>	<p>VCCO_64 / VCCO_65</p>	<p>VCCO_0</p>	<p>VCCO_40 1.2V VCCO_41 1.2V VCCO_42 1.2V VCCO_46 1.2V VCCO_47 1.2V VCCO_48 1.2V VCCO_71 1.2V VCCO_72 1.2V VCCO_73 1.2V VCCO_64 1.8V VCCO_65 1.8V VCCO_0 1.8V</p>
Maxim, Other			<p>VCCO_43 1.8V(Vadj) VCCO_45 1.8V(Vadj) VCCO_66 1.8V(Vadj) VCCO_67 1.8V(Vadj) VCCO_70 1.8V(Vadj)</p>	<p>FPGA Decoupling 1</p> <p>TITLE: FPGA Decoupling 1 SCHEM, ROHS COMPLIANT HW-U1-VCU118_REV1_1</p> <p>ASSY P/N: 0432001 PCB P/N: 1280906 SCH P/N: 0381739 TEST P/N: TSS0185</p> <p>DATE: 12/01/2016:13:37 VER: 1.1</p> <p>SHEET SIZE: B REV: 02</p> <p>SHEET 22 OF 76 DRAWN BY: DN</p>		
Maxim, Other			<p>VCCO_43 1.8V(Vadj) VCCO_45 1.8V(Vadj) VCCO_66 1.8V(Vadj) VCCO_67 1.8V(Vadj) VCCO_70 1.8V(Vadj)</p>			



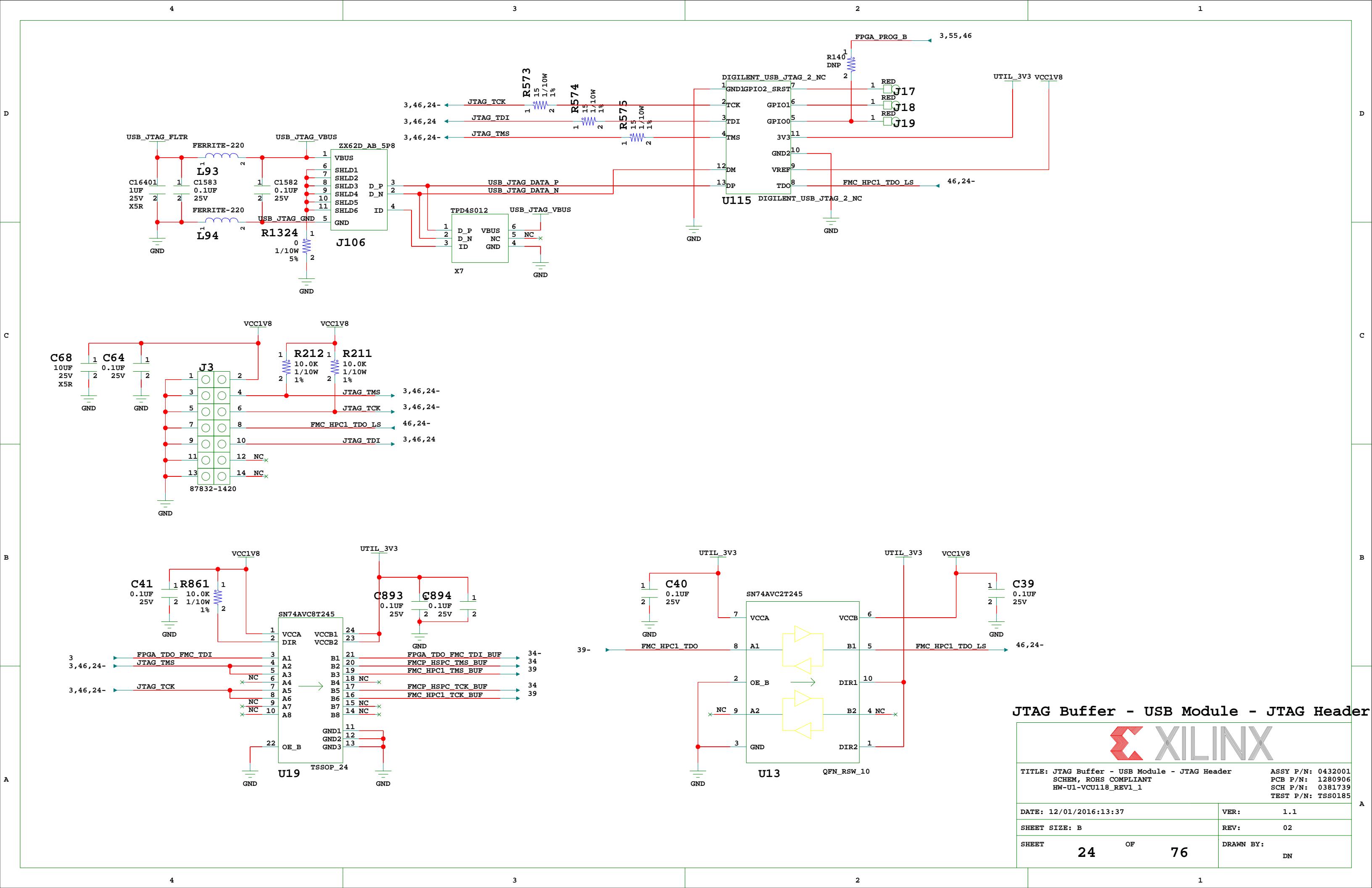
FPGA Decoupling 2

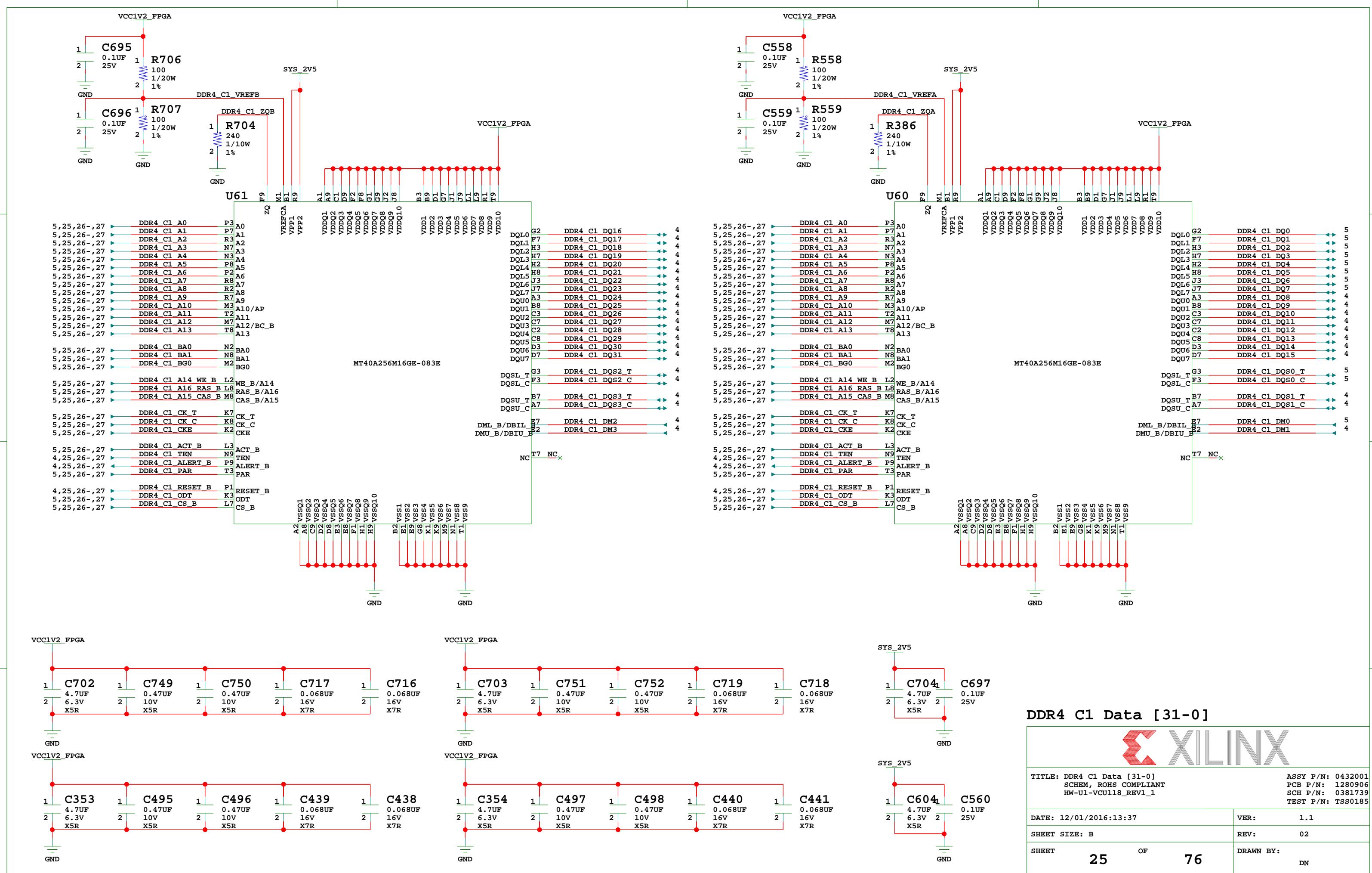


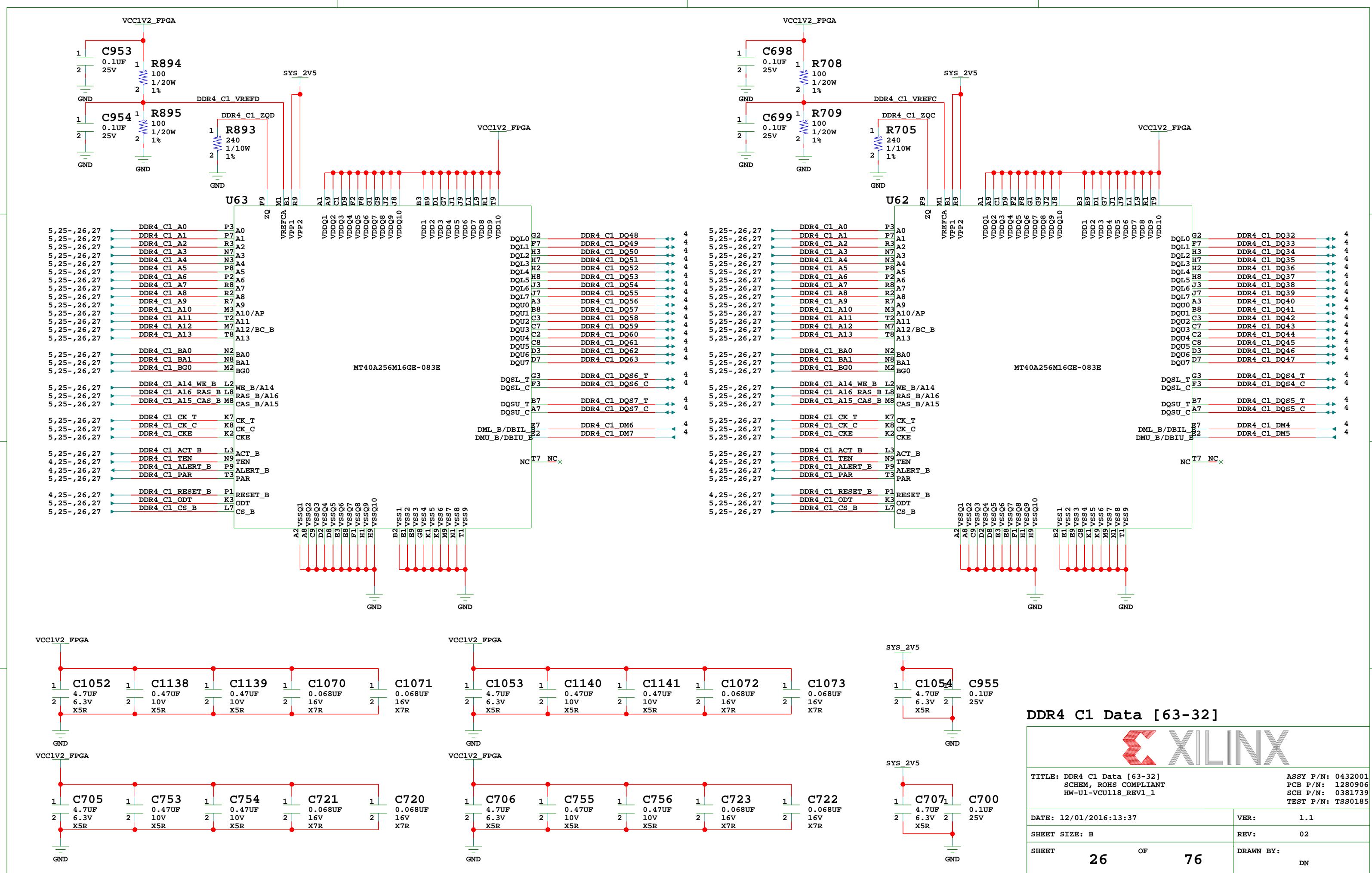
TITLE: FPGA Decoupling 2
 SCHEM, ROHS COMPLIANT
 HW-U1-VCU118_REV1_1

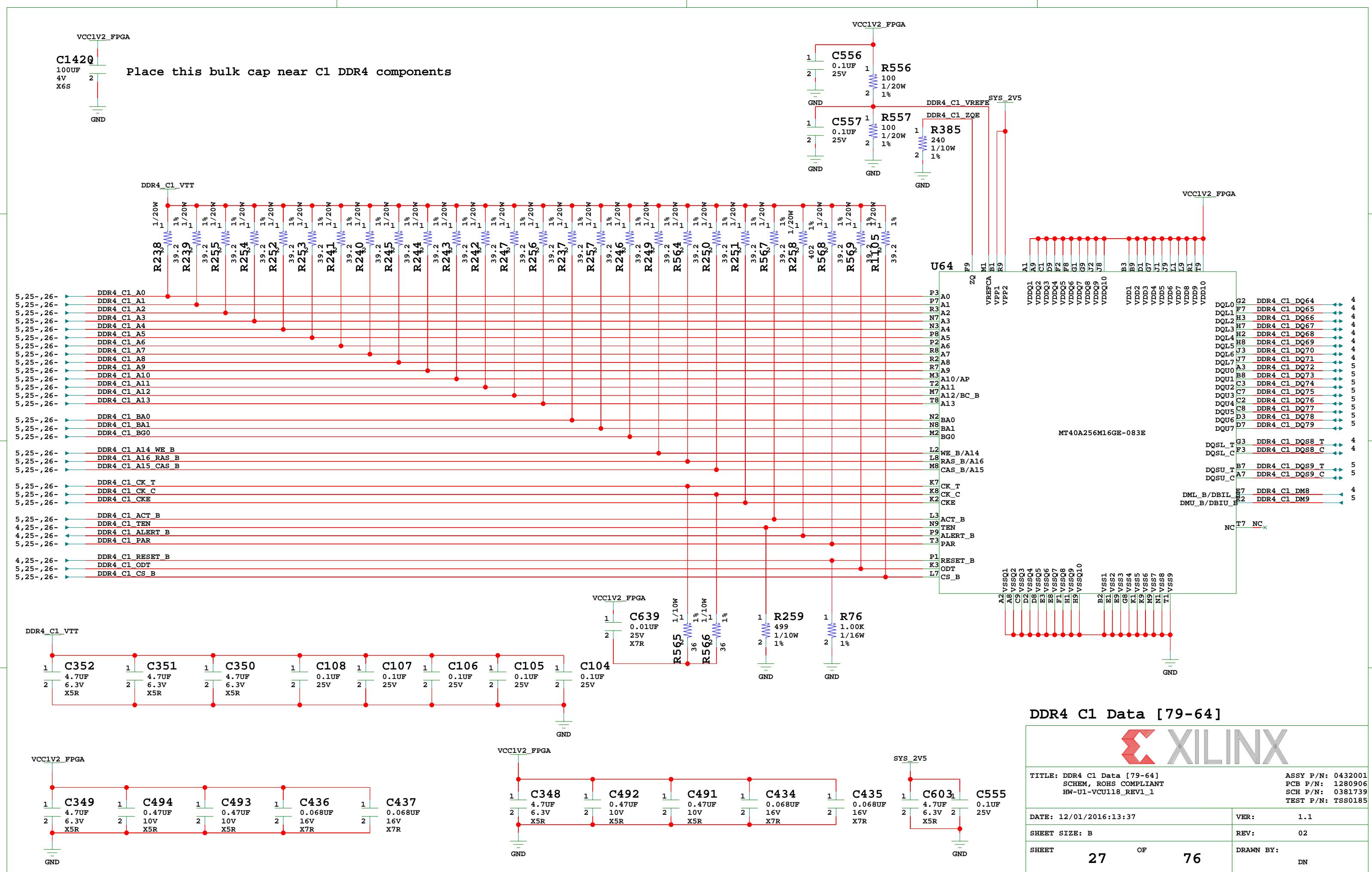
ASSY P/N: 0432001
 PCB P/N: 1280906
 SCH P/N: 0381739
 TEST P/N: TSS0185

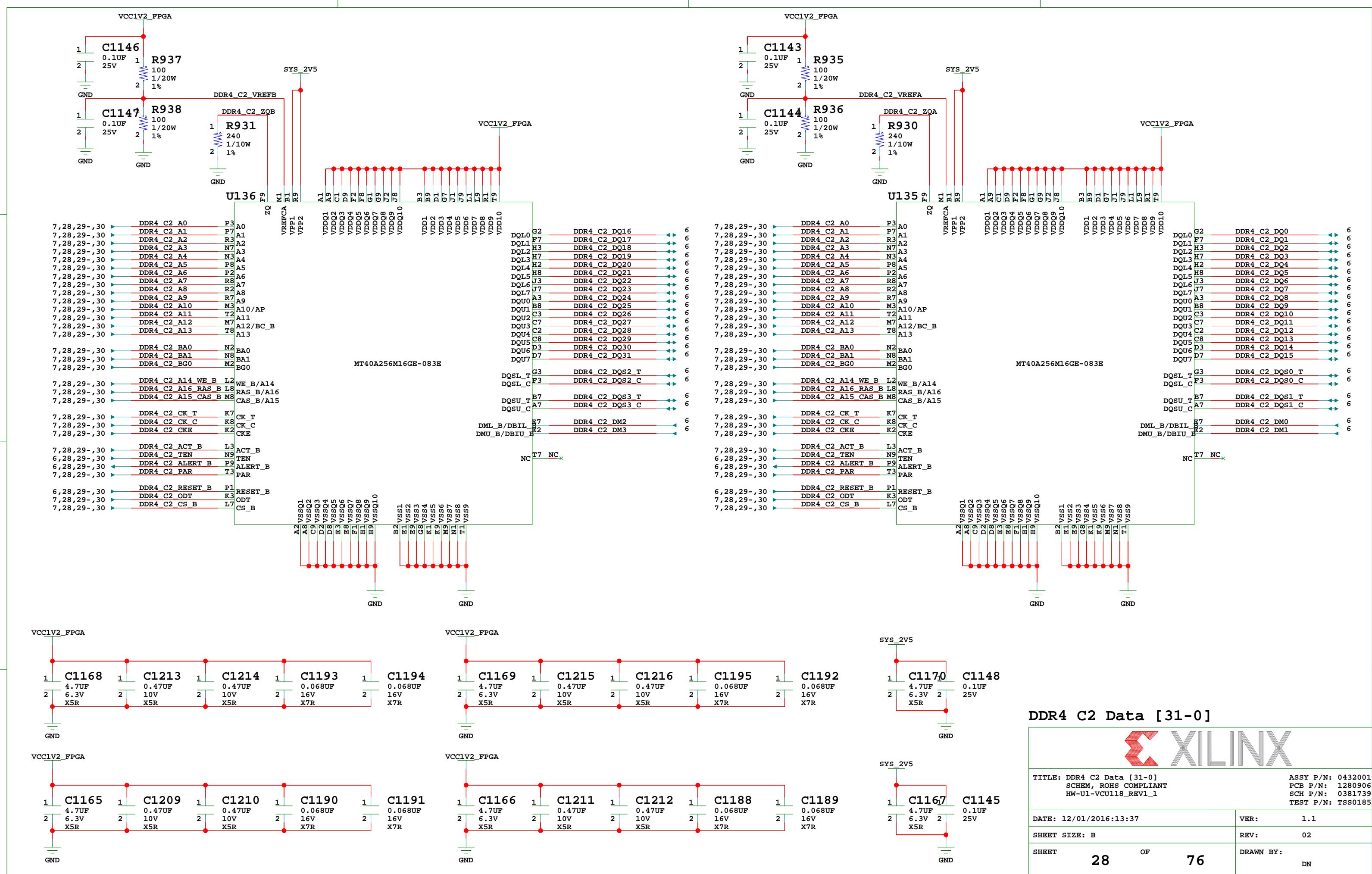
DATE: 12/01/2016:13:37	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 23 OF 76	DRAWN BY: DN

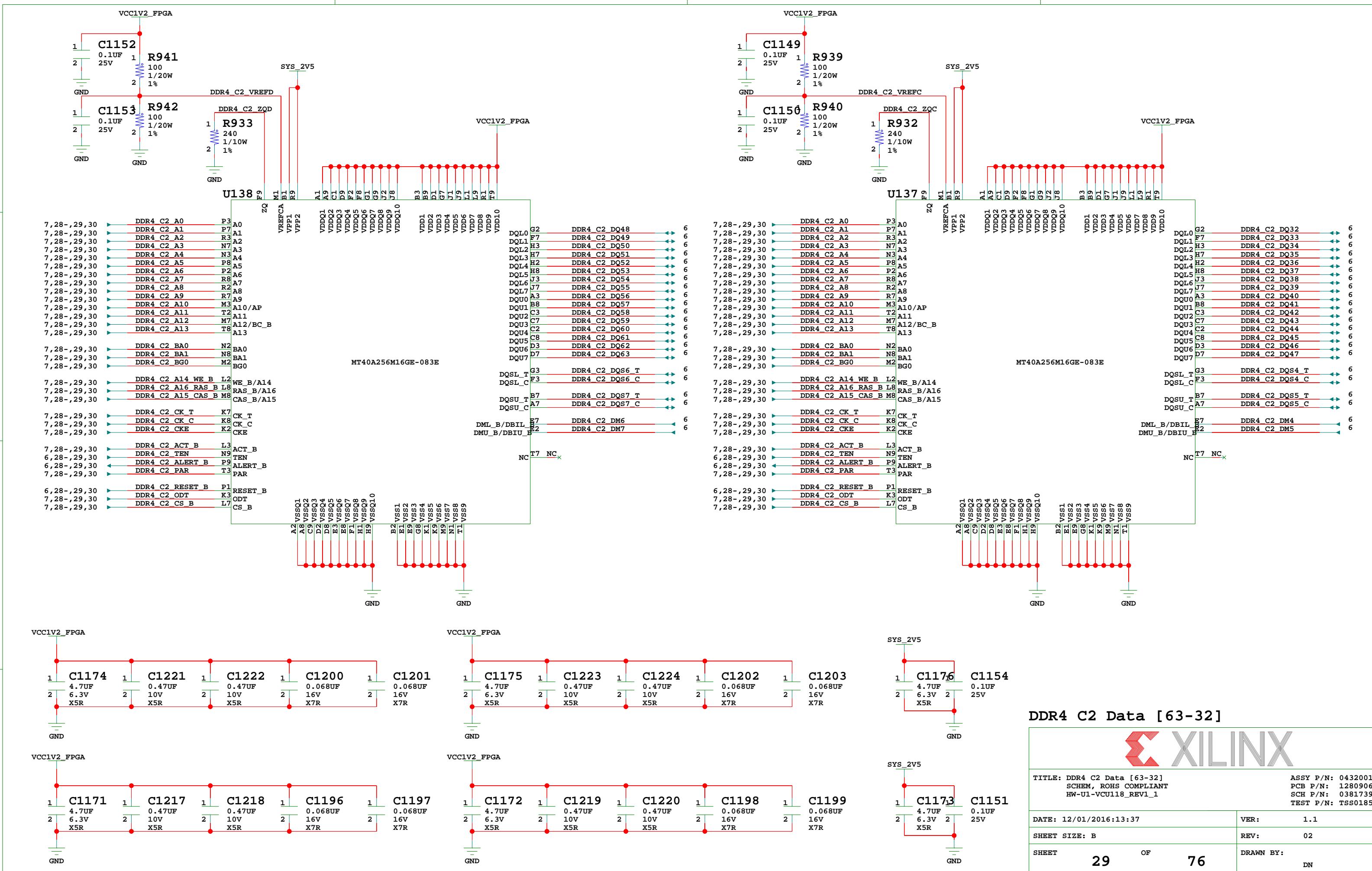












DDR4 C2 Data [63-32]



TITLE: DDR4 C2 Data [63-32]
SCHEM., ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:37

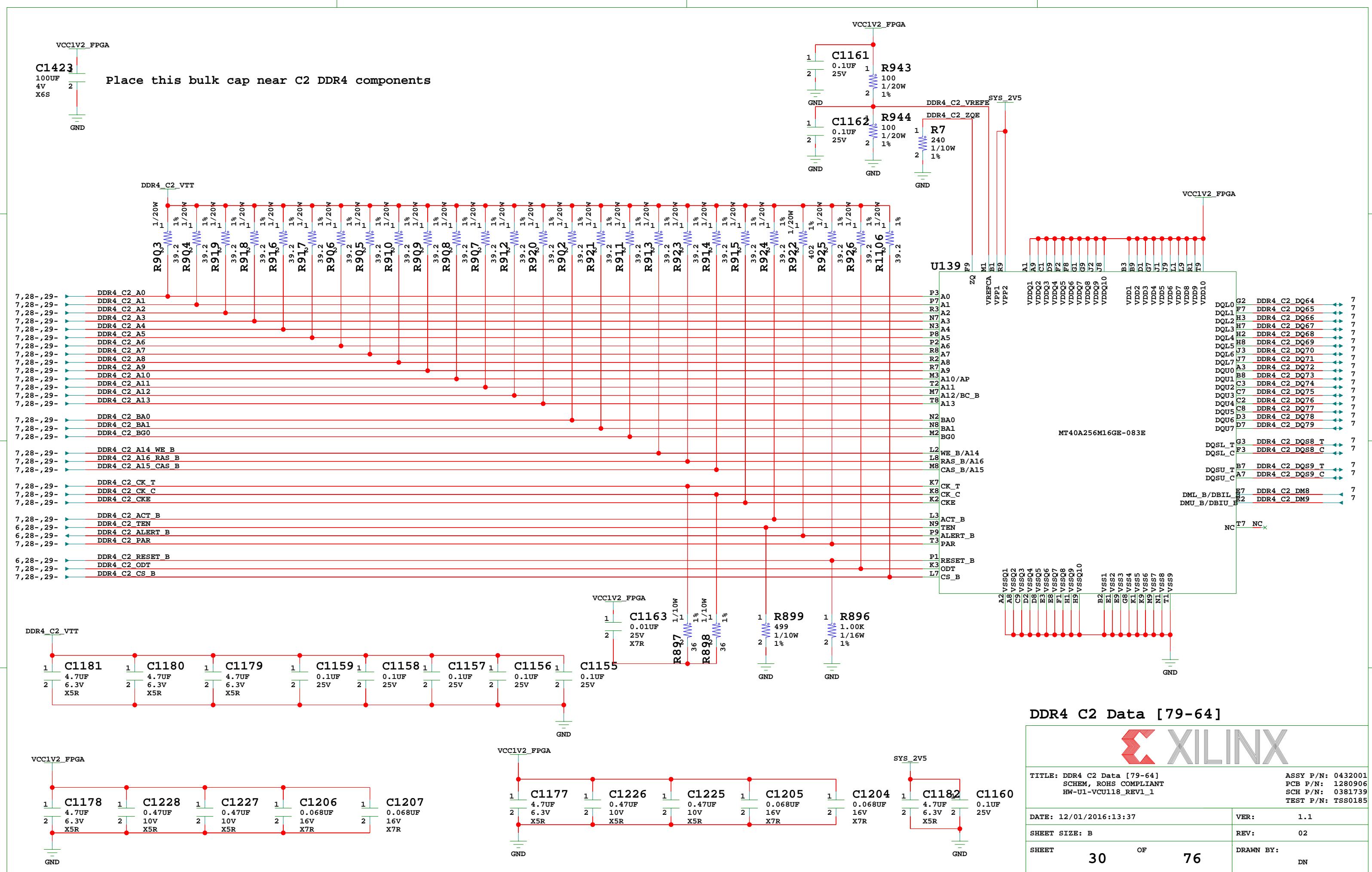
VER: 1.1

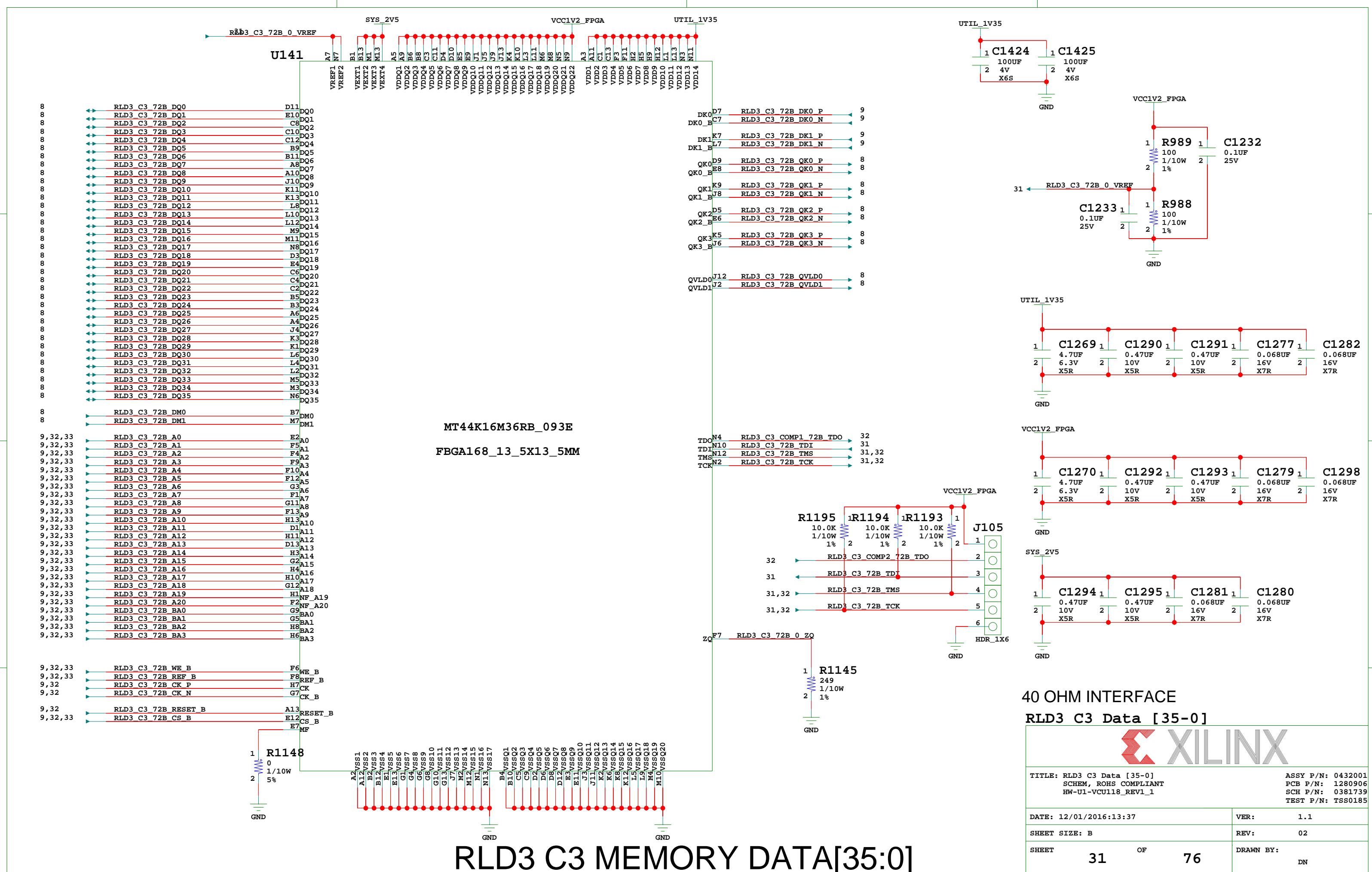
SHEET SIZE: B

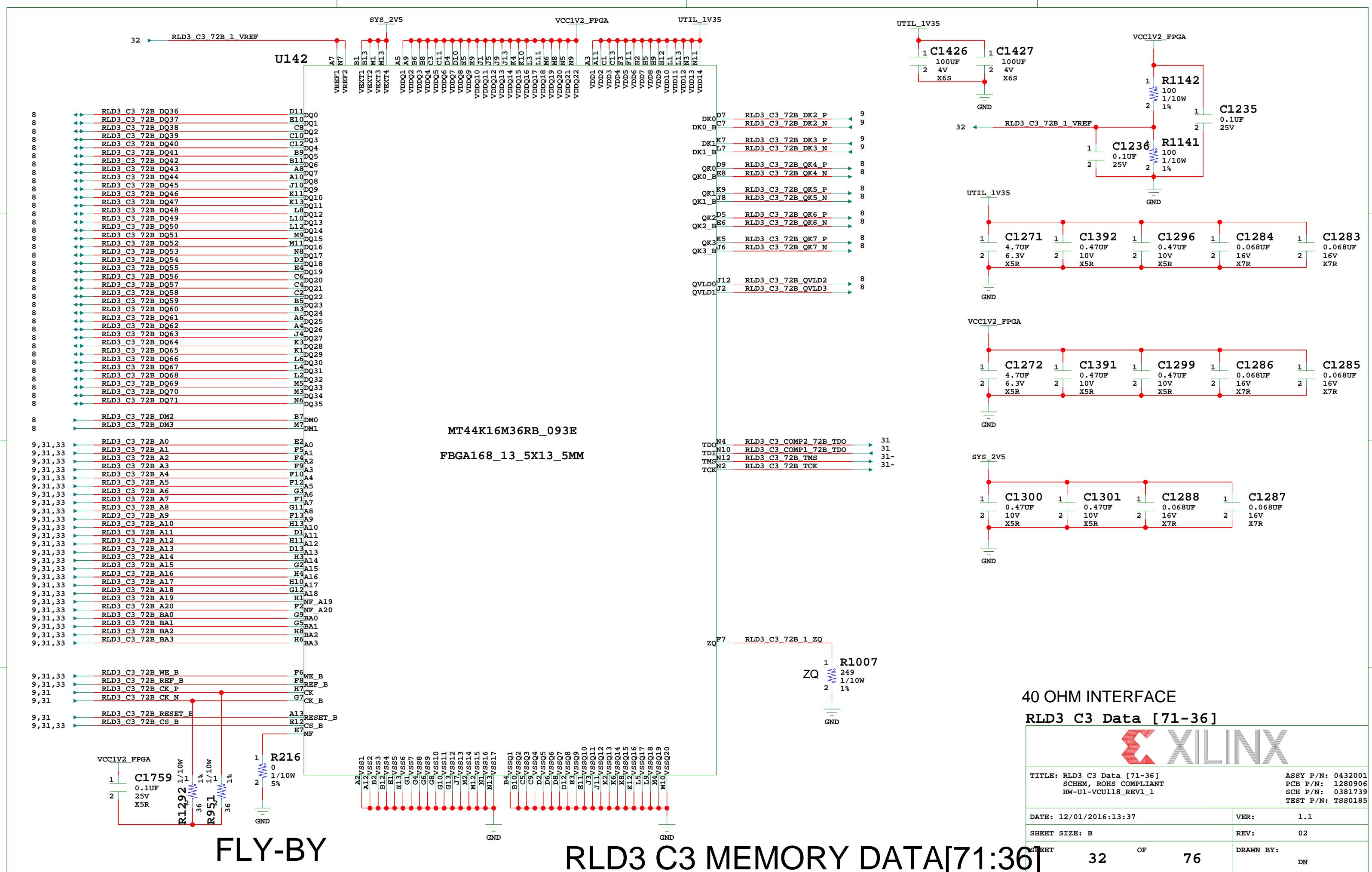
REV: 02

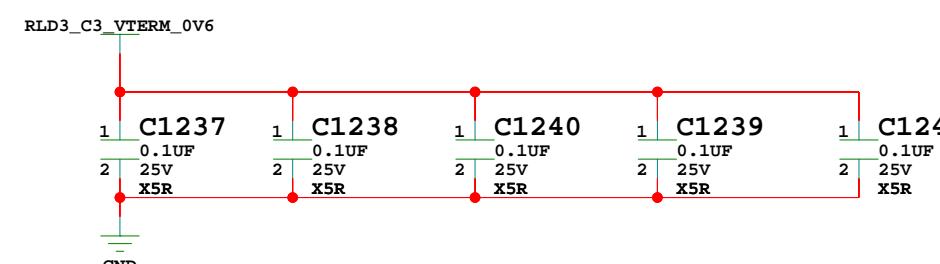
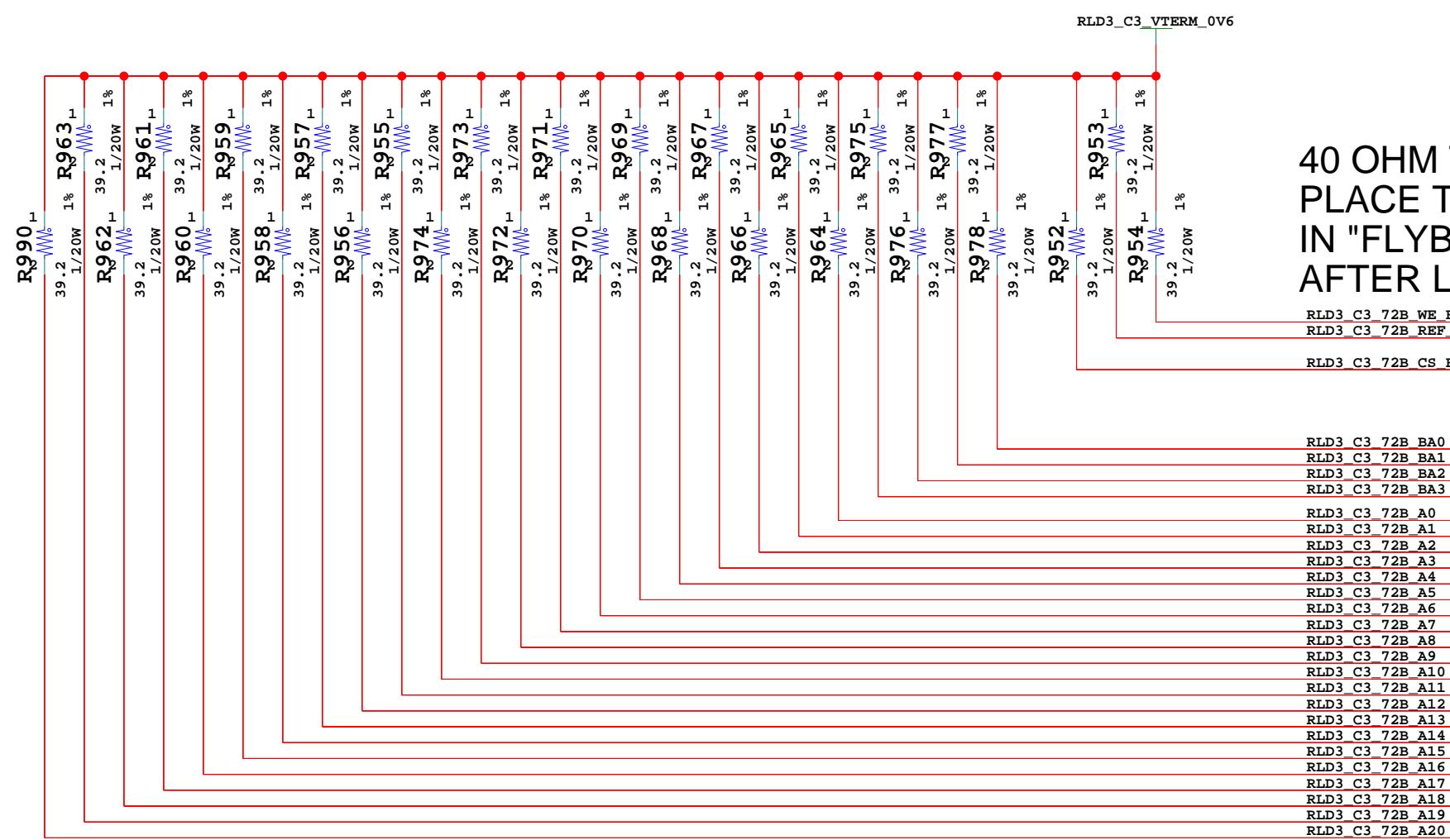
SHEET 29 OF 76

DRAWN BY: DN

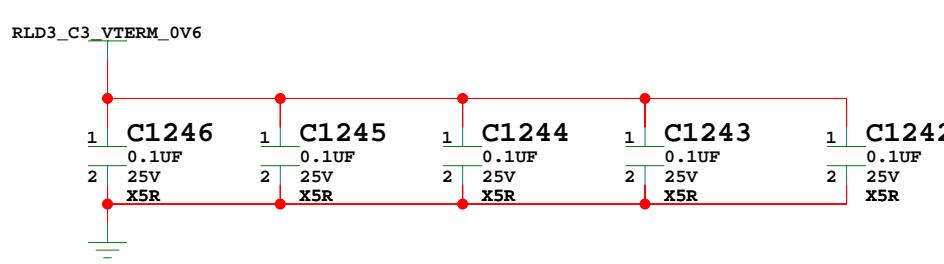








RLD3 C3 72-BIT RTERM DECOUPLING



40 OHM INTERFACE RLD3 C3 Termination/Decoupling



TITLE: RLD3 C3 Termination/Decoupling
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:37

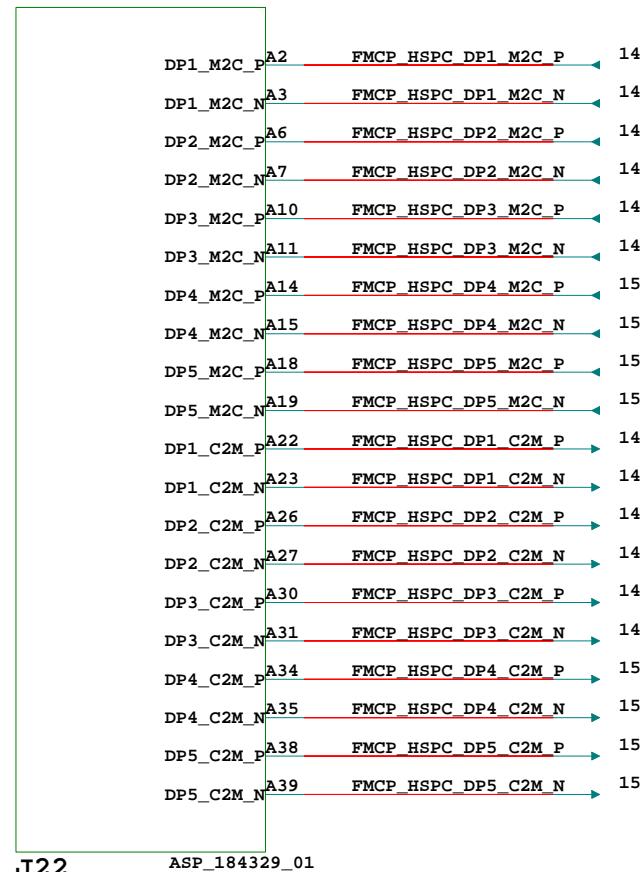
VER: 1.1

SHEET SIZE: B

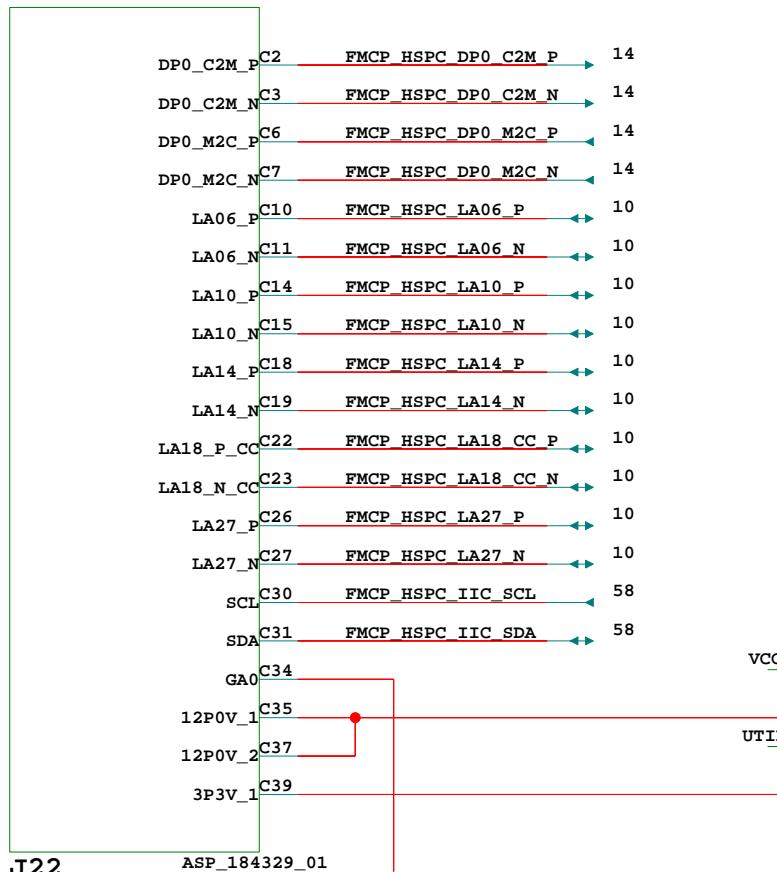
REV: 02

SHEET 33 OF 76

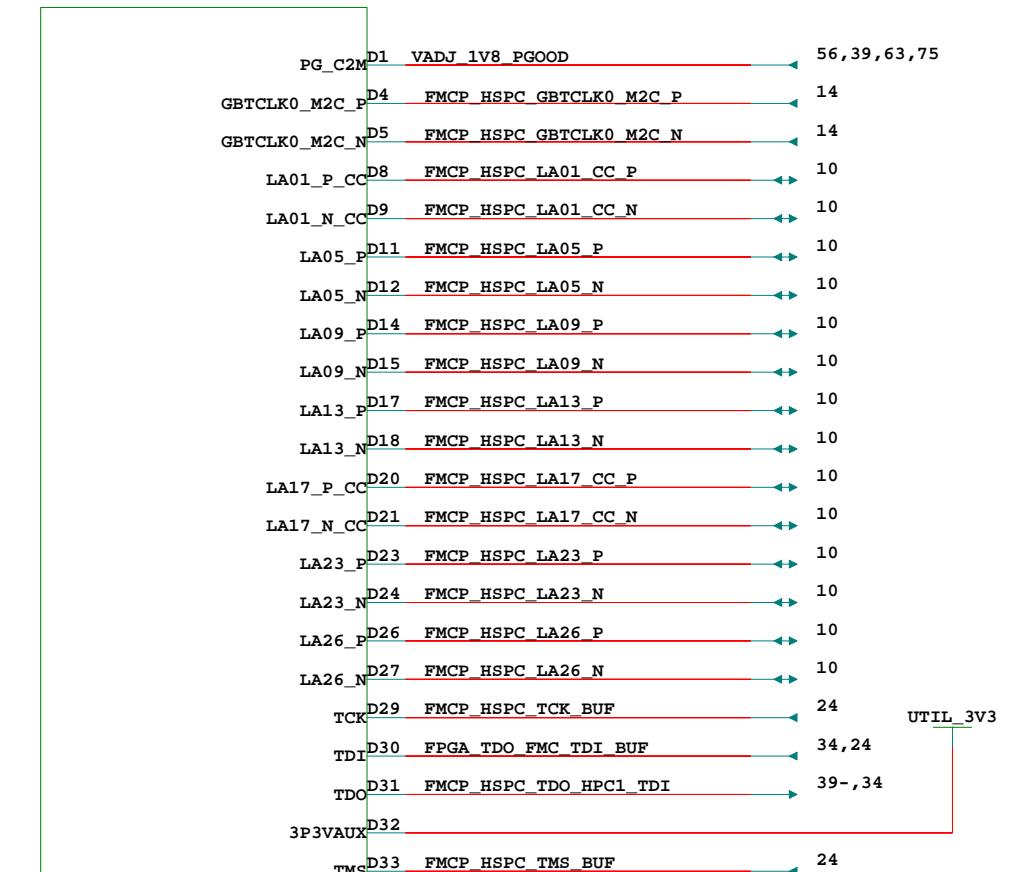
DRAWN BY: DN



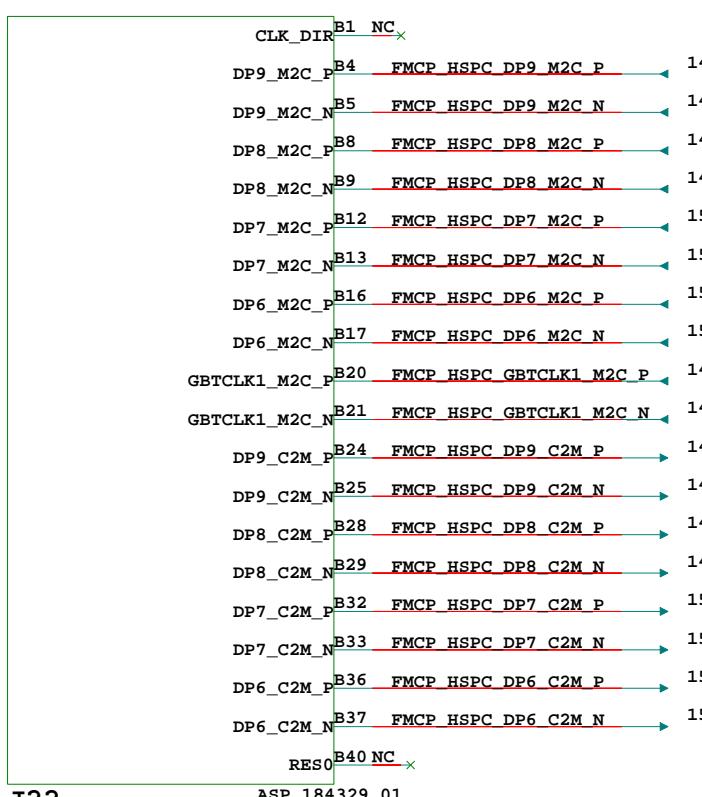
J22 ASP_184329_01



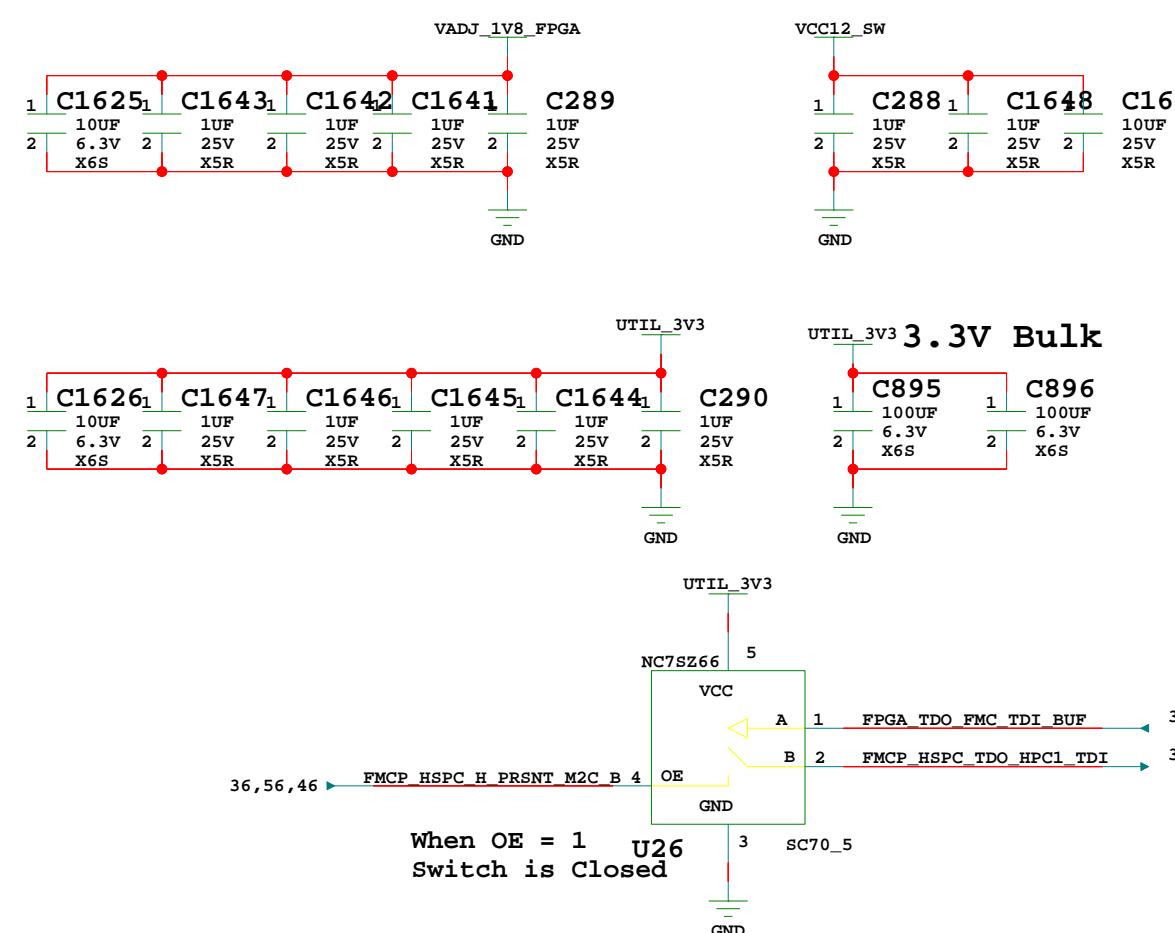
J22 ASP_184329_01



J22 ASP_184329_01



J22 ASP_184329_01



ANSI/VITA 57.4 - Draft OCT 2015 FMCP HSPC Header Rows A B C D



TITLE: FMCP HSPC Header Rows A B C D
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:37

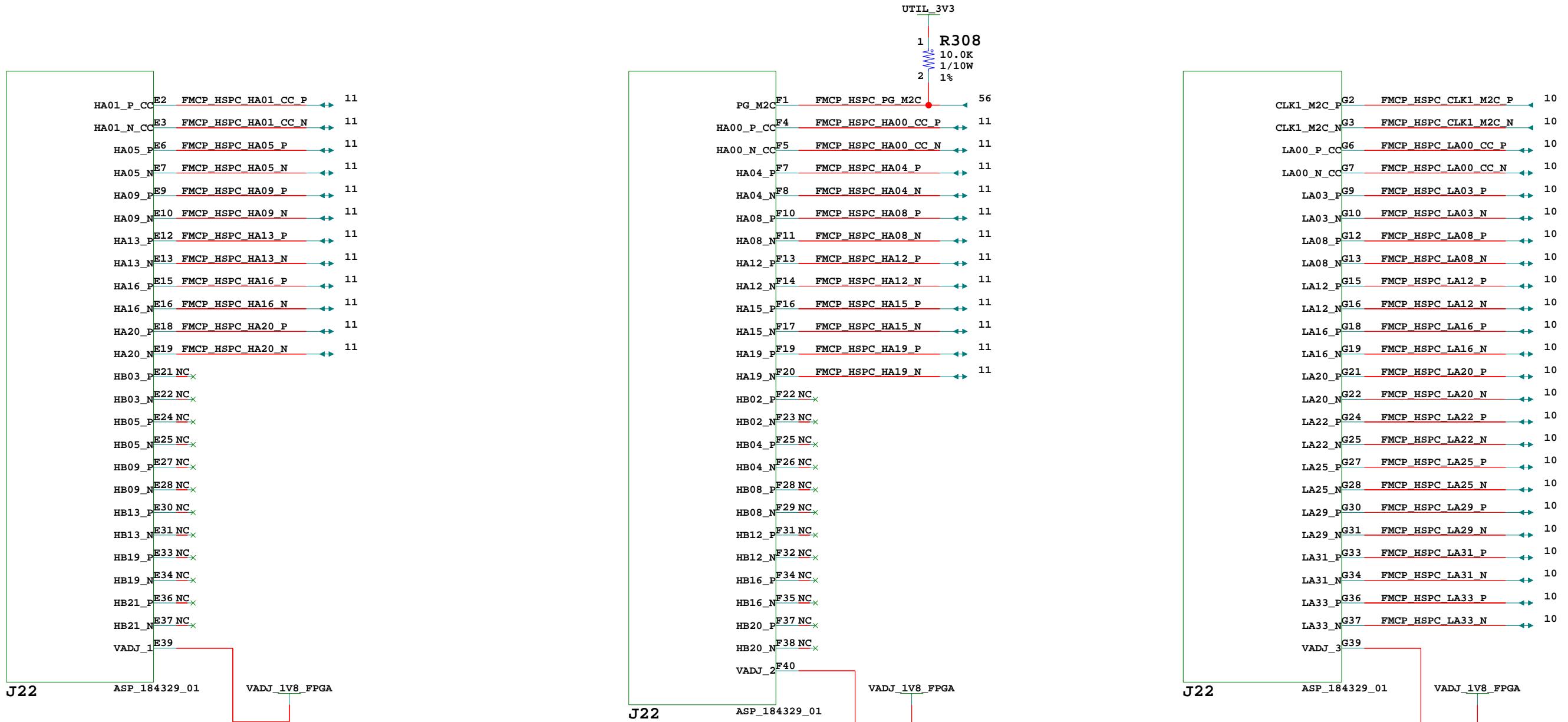
VER: 1.1

SHEET SIZE: B

REV: 02

SHEET 34 OF 76

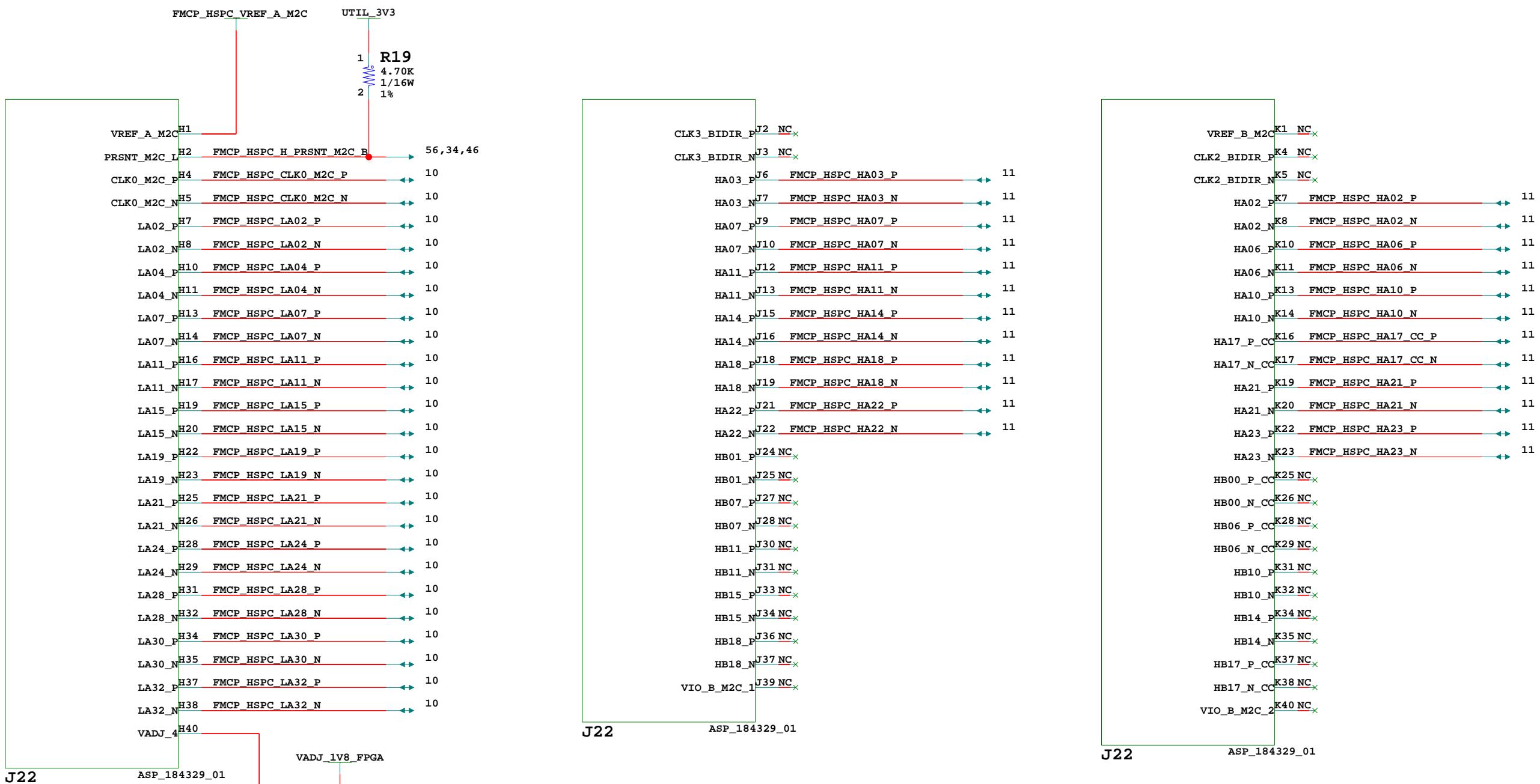
DRAWN BY: DN



ANSI/VITA 57.4 - Draft OCT 2015
FMCP HSPC Header Rows E F G



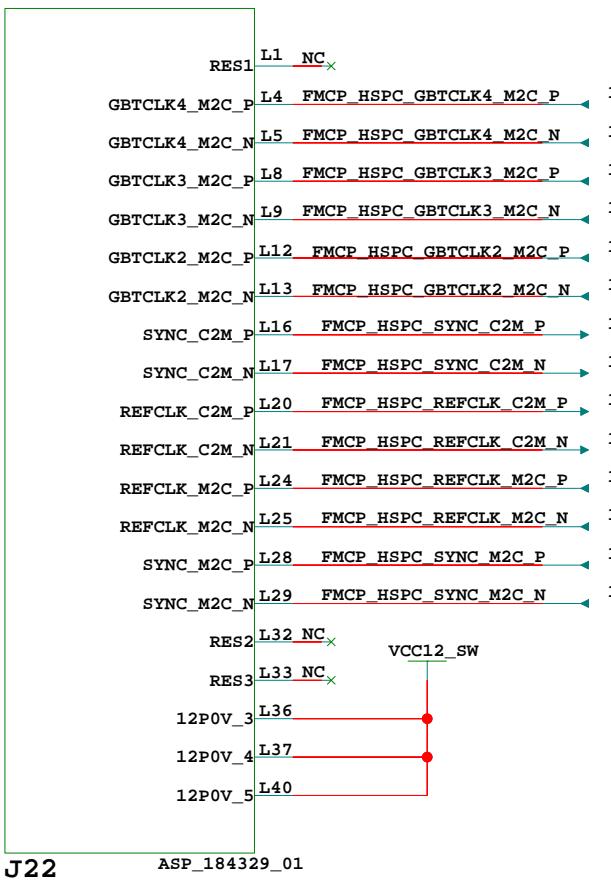
TITLE: FMCP HSPC Header Rows E F G SCHEM, ROHS COMPLIANT HW-U1-VCU118_REV1_1	ASSY P/N: 0432001 PCB P/N: 1280906 SCH P/N: 0381739 TEST P/N: TSS0185
DATE: 12/01/2016:13:37	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 35 OF 76	DRAWN BY: DN



ANSI/VITA 57.4 - Draft OCT 2015
FMCP HSPC Header Rows H J K

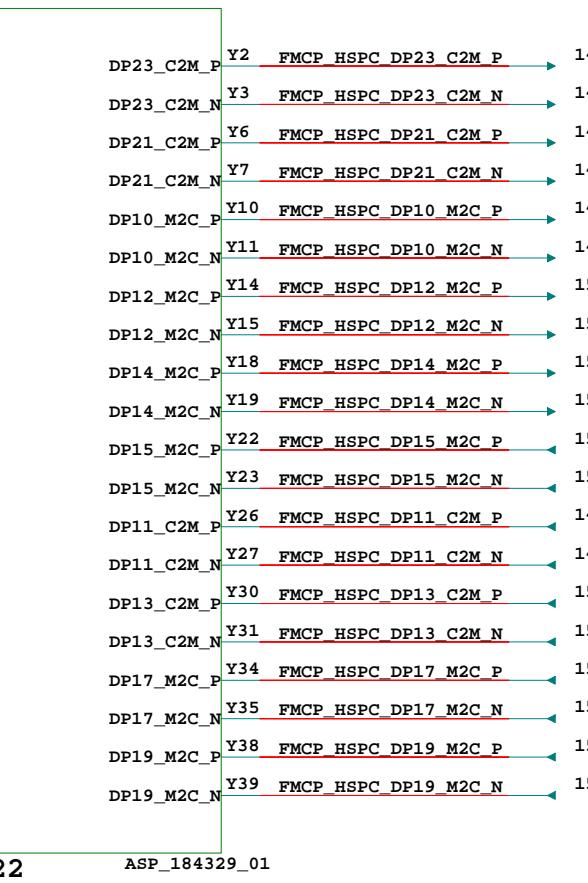


TITLE: FMCP HSPC Header Rows H J K SCHEM, ROHS COMPLIANT HW-U1-VCU118_REV1_1		ASSY P/N: 0432001 PCB P/N: 1280906 SCH P/N: 0381739 TEST P/N: TSS0185
DATE: 12/01/2016:13:37	VER: 1.1	
SHEET SIZE: B	REV: 02	
SHEET 36 OF 76	DRAWN BY: DN	



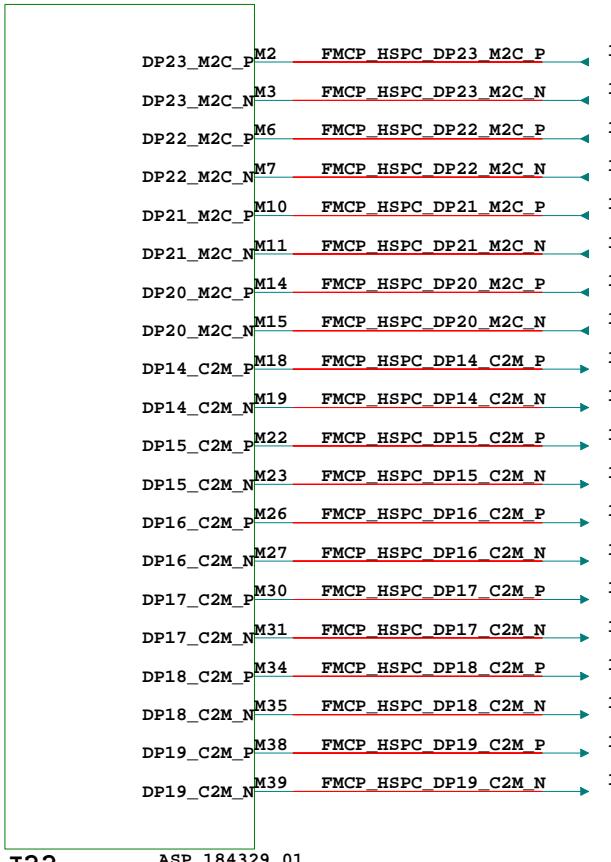
J22

ASP_184329_01



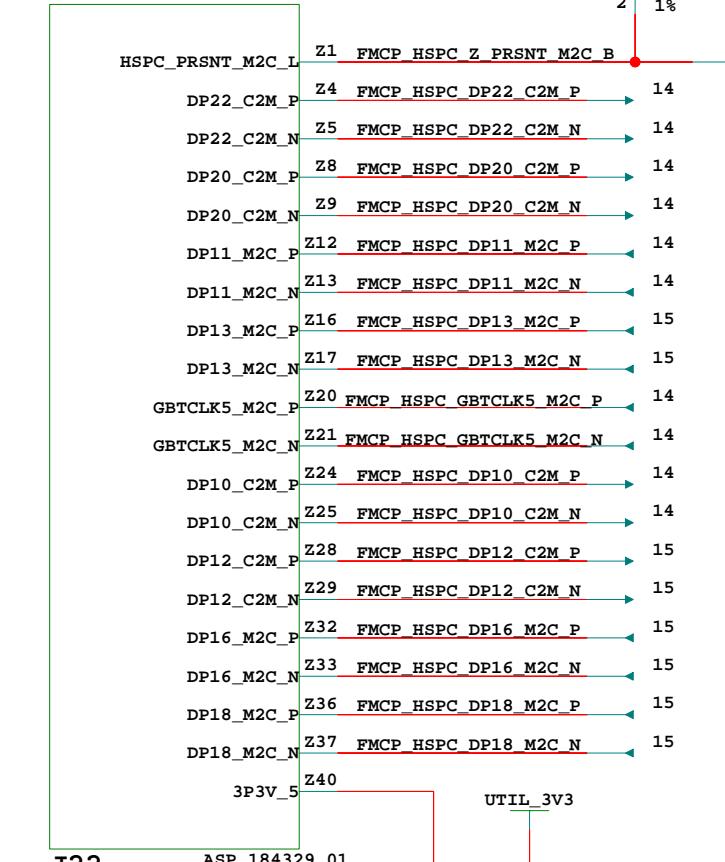
J22

ASP_184329_01



J22

ASP_184329_01



J22

ASP_184329_01

UTIL_3V3

R934

1 4.70K
2 1/16W
1%
1%

ANSI/VITA 57.4 - Draft OCT 2015
FMCP HSPC Header Rows L M Y Z

 XILINX

TITLE: FMCP HSPC Header Rows L M Y Z
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:37

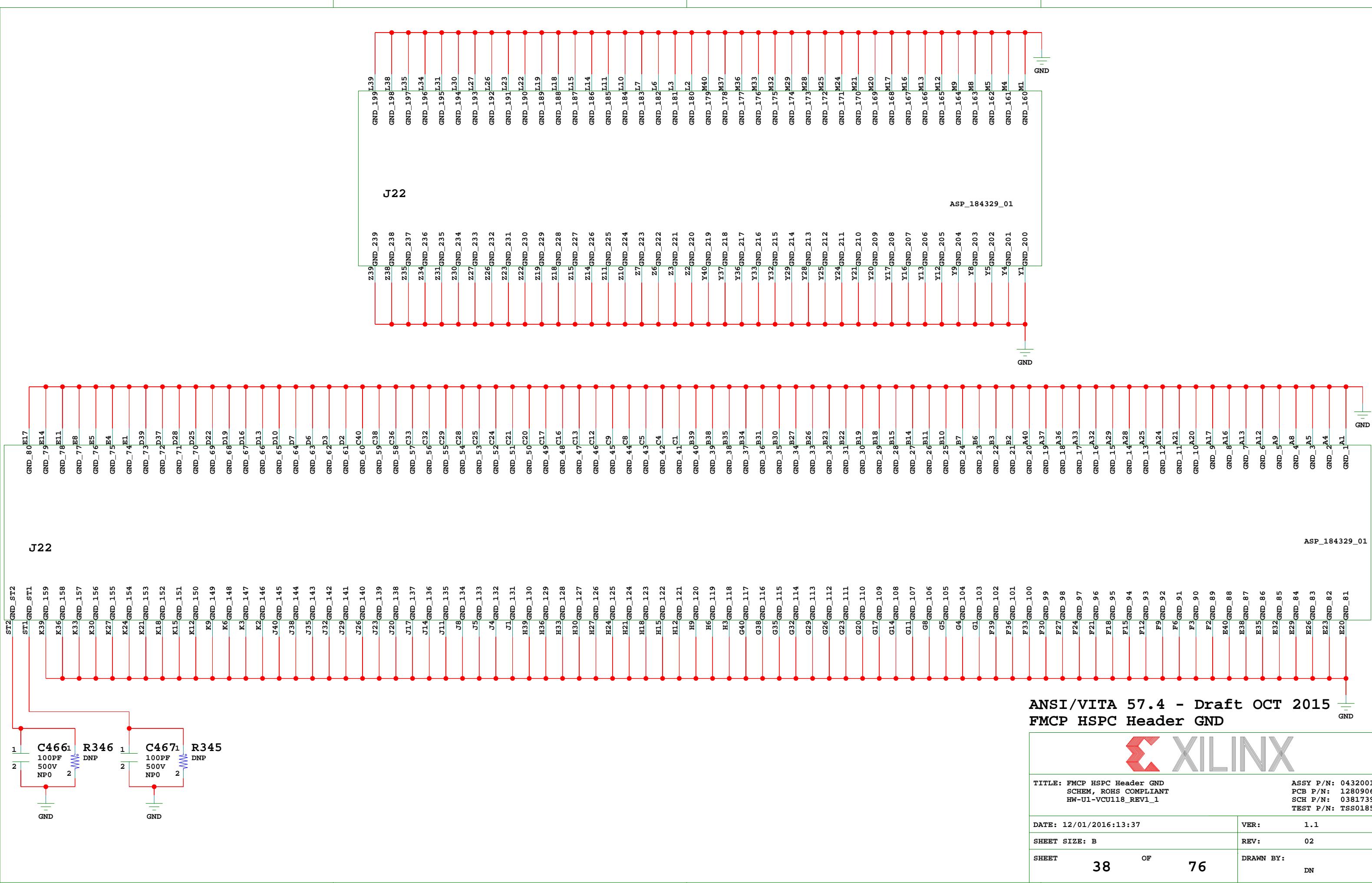
VER: 1.1

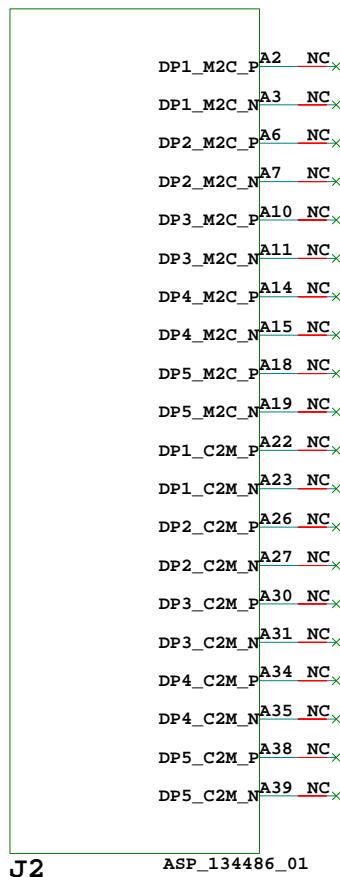
SHEET SIZE: B

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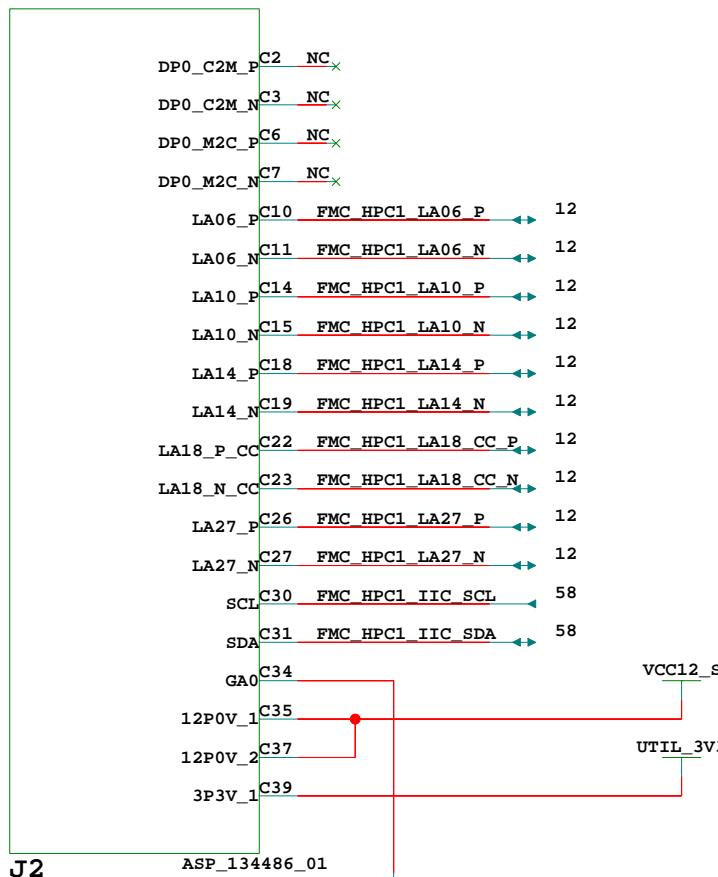
SHEET 37 OF 76

DRAWN BY: DN

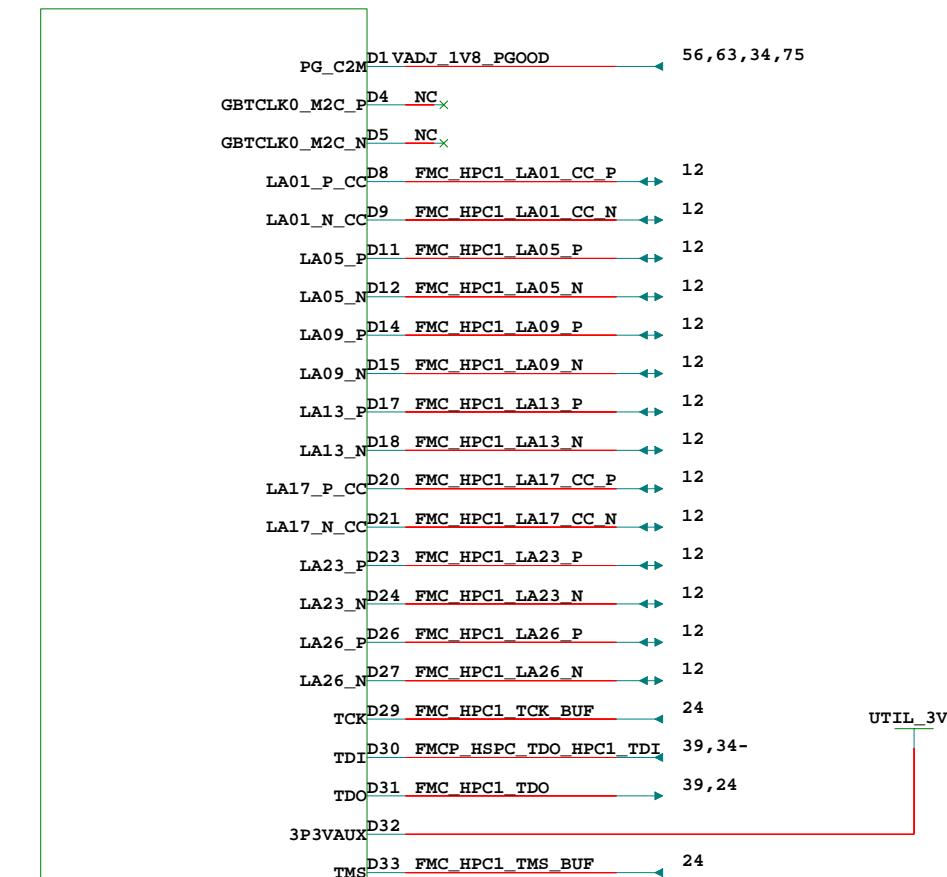




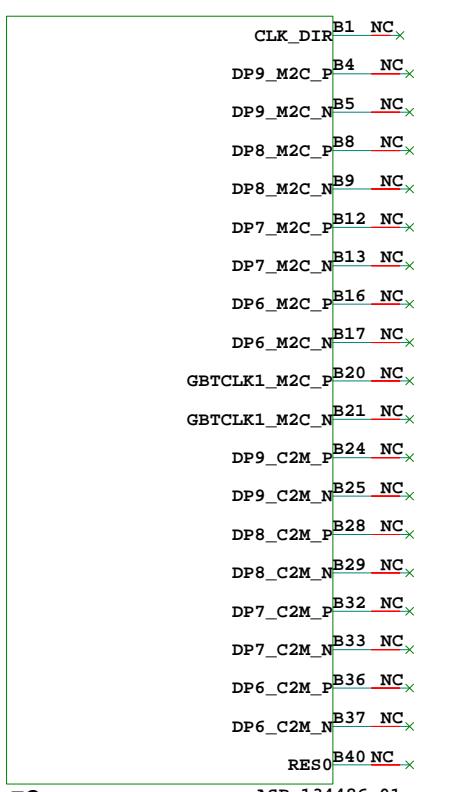
J2 ASP_134486_01



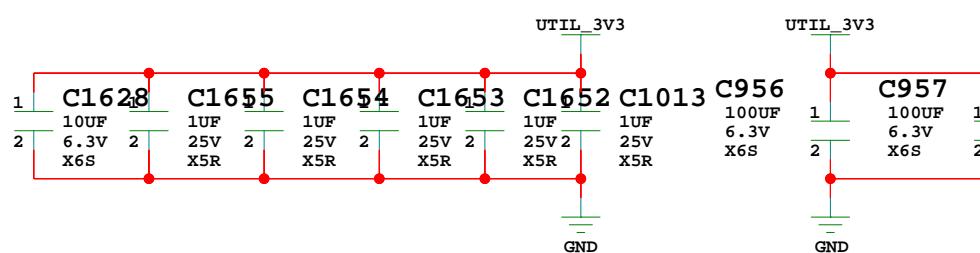
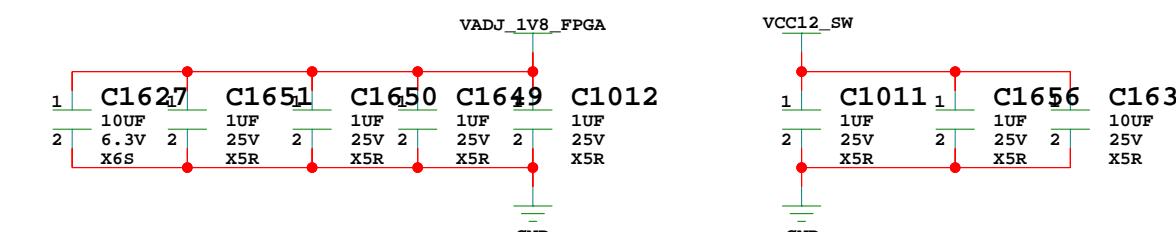
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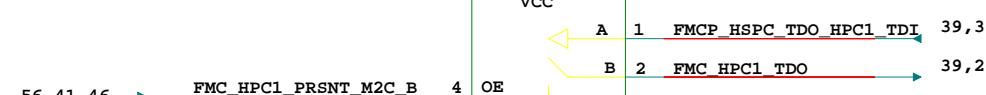
J2 ASP_134486_01



J2 ASP_134486_01



3.3V Bulk



When OE = 1 U132
Switch is Closed

ANSI/VITA 57.1 - Revised 2010
FMC HPC1 Header Rows A B C D

TITLE: FMC HPC1 Header Rows A B C D
SCHEM., ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:37

VER: 1.1

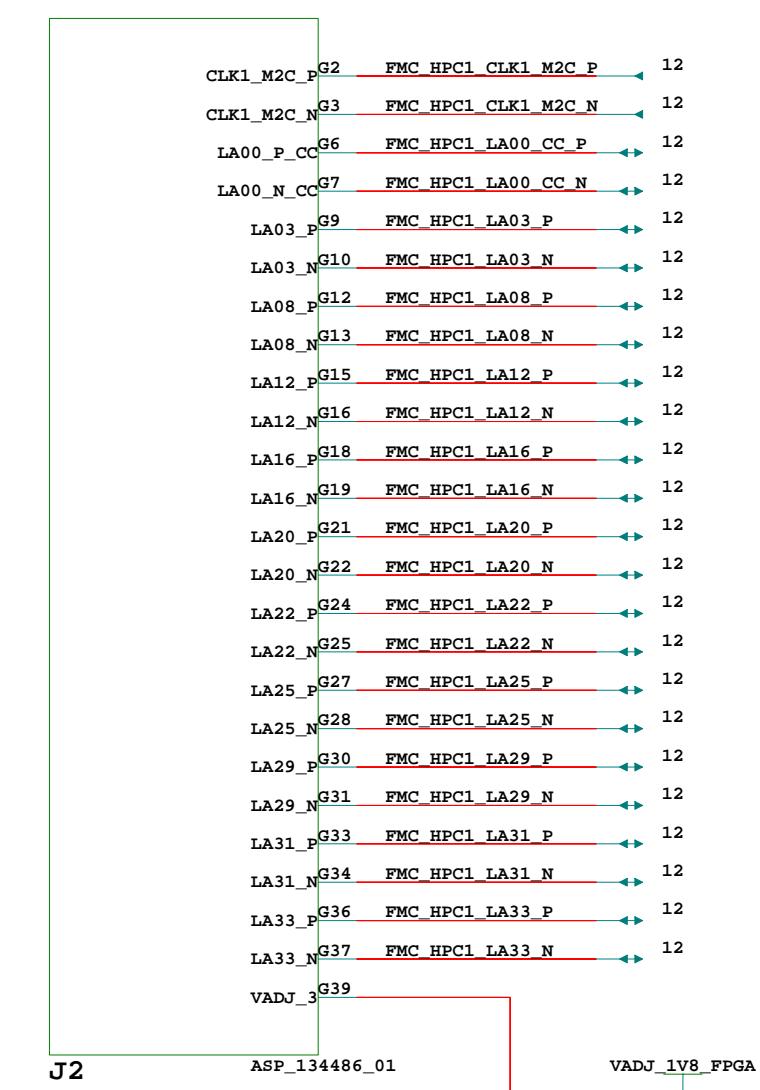
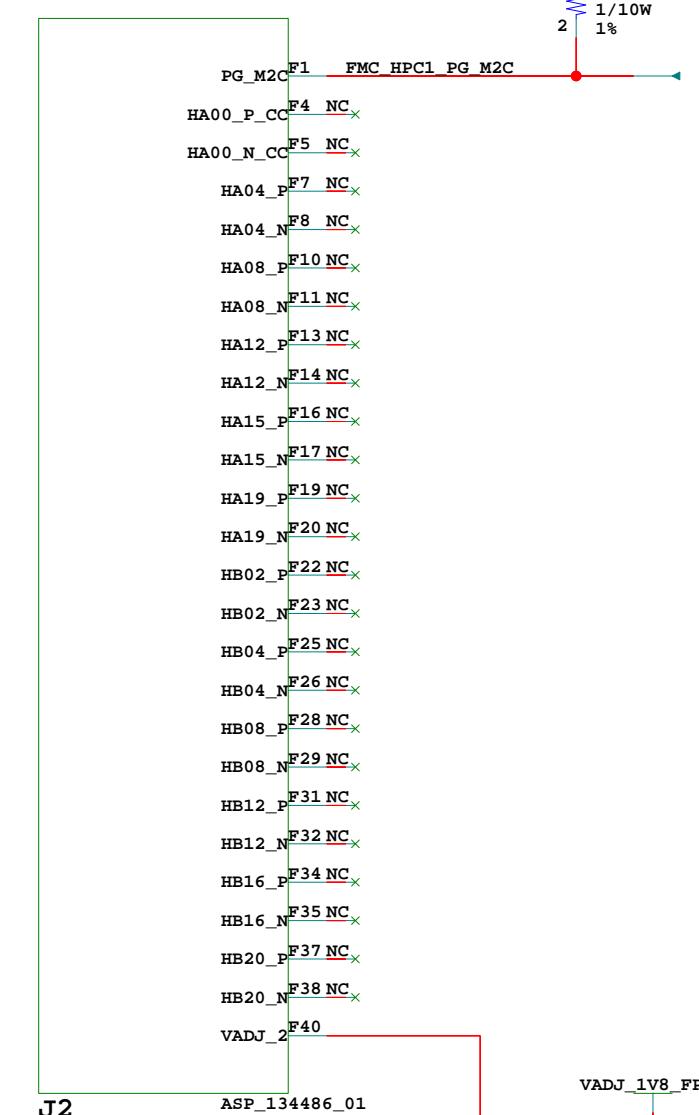
SHEET SIZE: B

REV: 02

SHEET 39 OF 76

DRAWN BY:

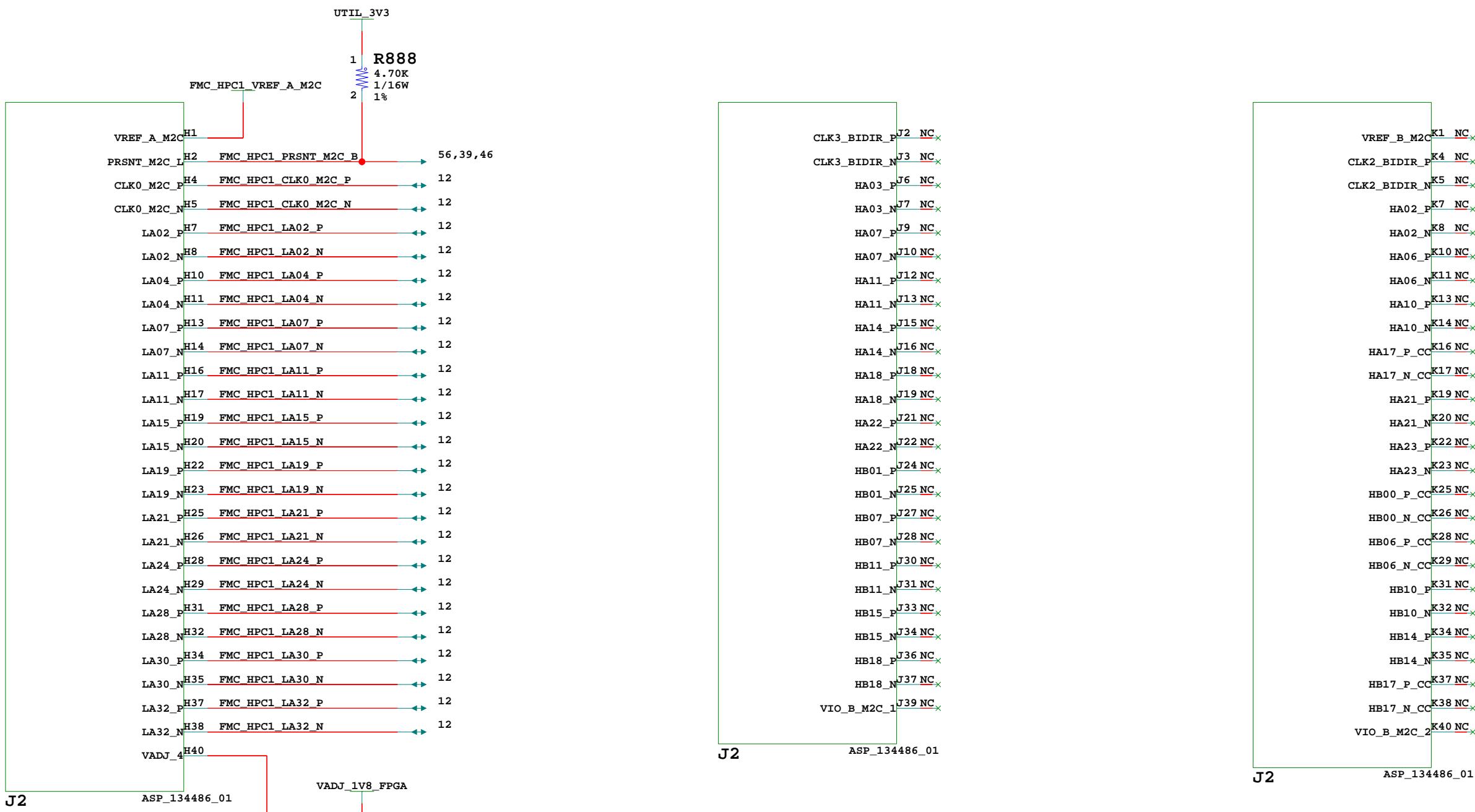
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ANSI/VITA 57.1 - Revised 2010
FMC HPC1 Header Rows E F G



TITLE: FMC HPC1 Header Rows E F G SCHEM, ROHS COMPLIANT HW-U1-VCU118_REV1_1	ASSY P/N: 0432001 PCB P/N: 1280906 SCH P/N: 0381739 TEST P/N: TSS0185
DATE: 12/01/2016:13:37	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 40 OF 76	DRAWN BY: DN



ANSI/VITA 57.1 - Revised 2010
FMC HPC1 Header Rows H J K



**TITLE: FMC HPC1 Header Rows H J K
SCHEM, ROHS COMPLIANT
HW-U1-VCU118 REV1 1**

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 13/01/2016 13:37

1 1

SUMMARY

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SHEET

Page 10

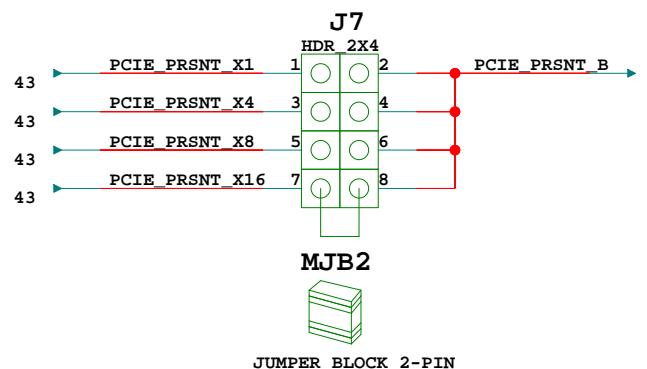
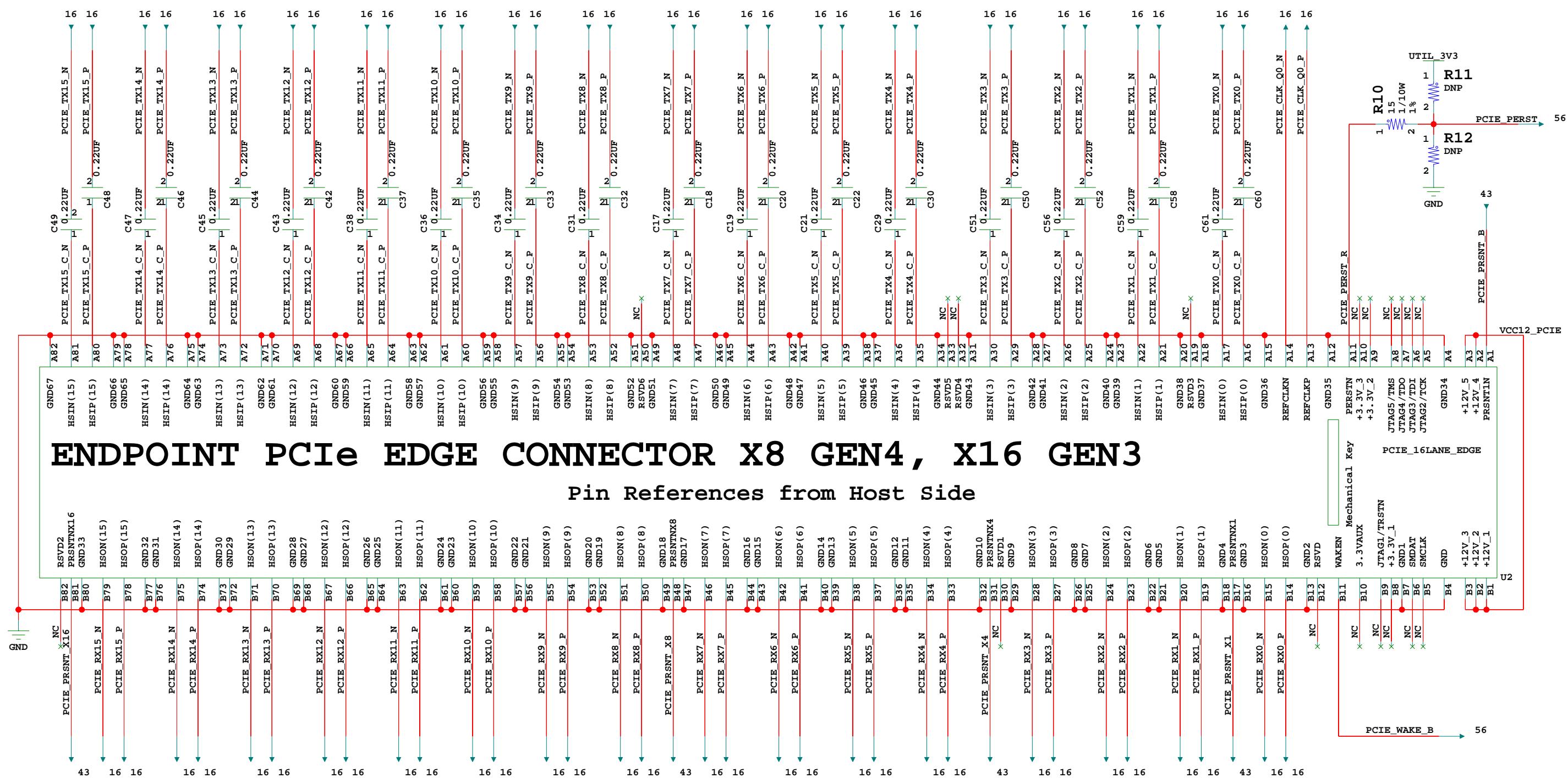
41

DN



ENDPOINT PCIe EDGE CONNECTOR X8 GEN4, X16 GEN3

Pin References from Host Side



PCIe x16 Endpoint Edge Connector



**TITLE: PCIe x16 Endpoint Edge Connector
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1**

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:37

1.1

SHEET SIZE: B

02

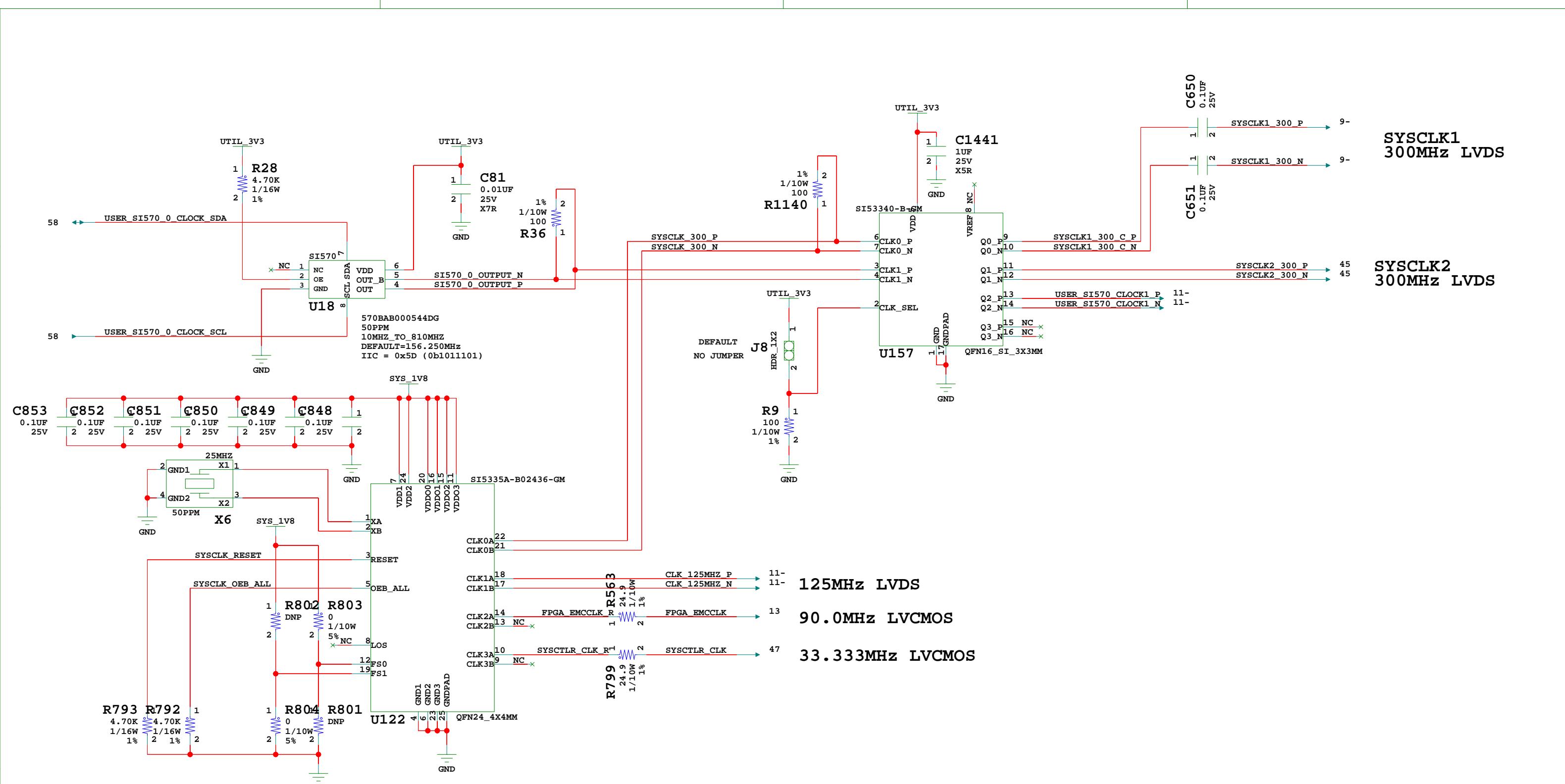
SHEET 43 OF 76

1. *What is the primary purpose of the study?* (e.g., to evaluate the effectiveness of a new treatment, to describe a population, to compare two groups).

Figure 1. A schematic diagram of the experimental setup.

111

1



EMCCLK and System Clocks



**TITLE: EMCCLK and System Clocks
SCHEM, ROHS COMPLIANT
HW-U1-VCU118 REV1 1**

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 13/01/2016 13:37

1 1

SWEET SENSE B

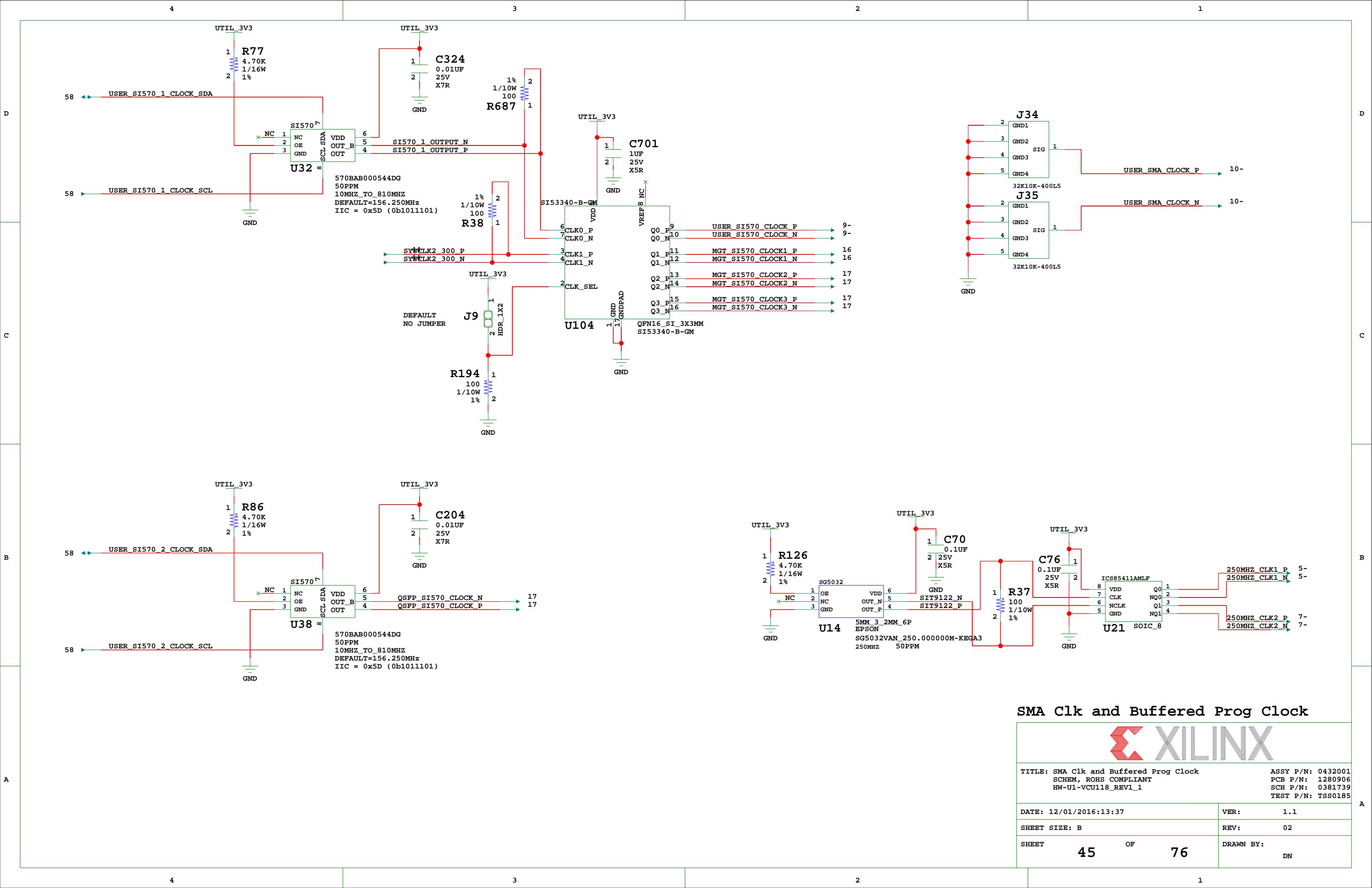
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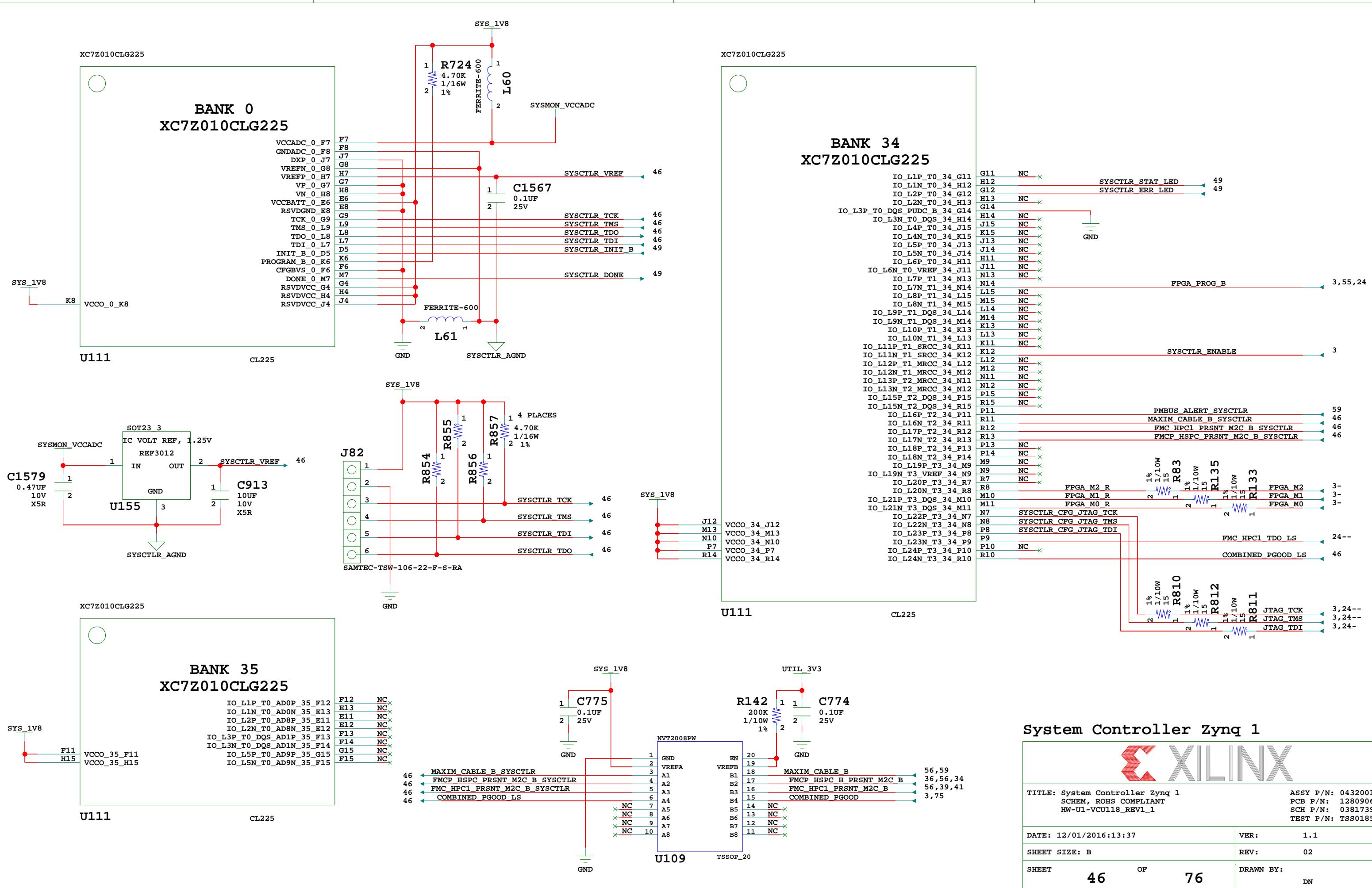
QUESTION

1000

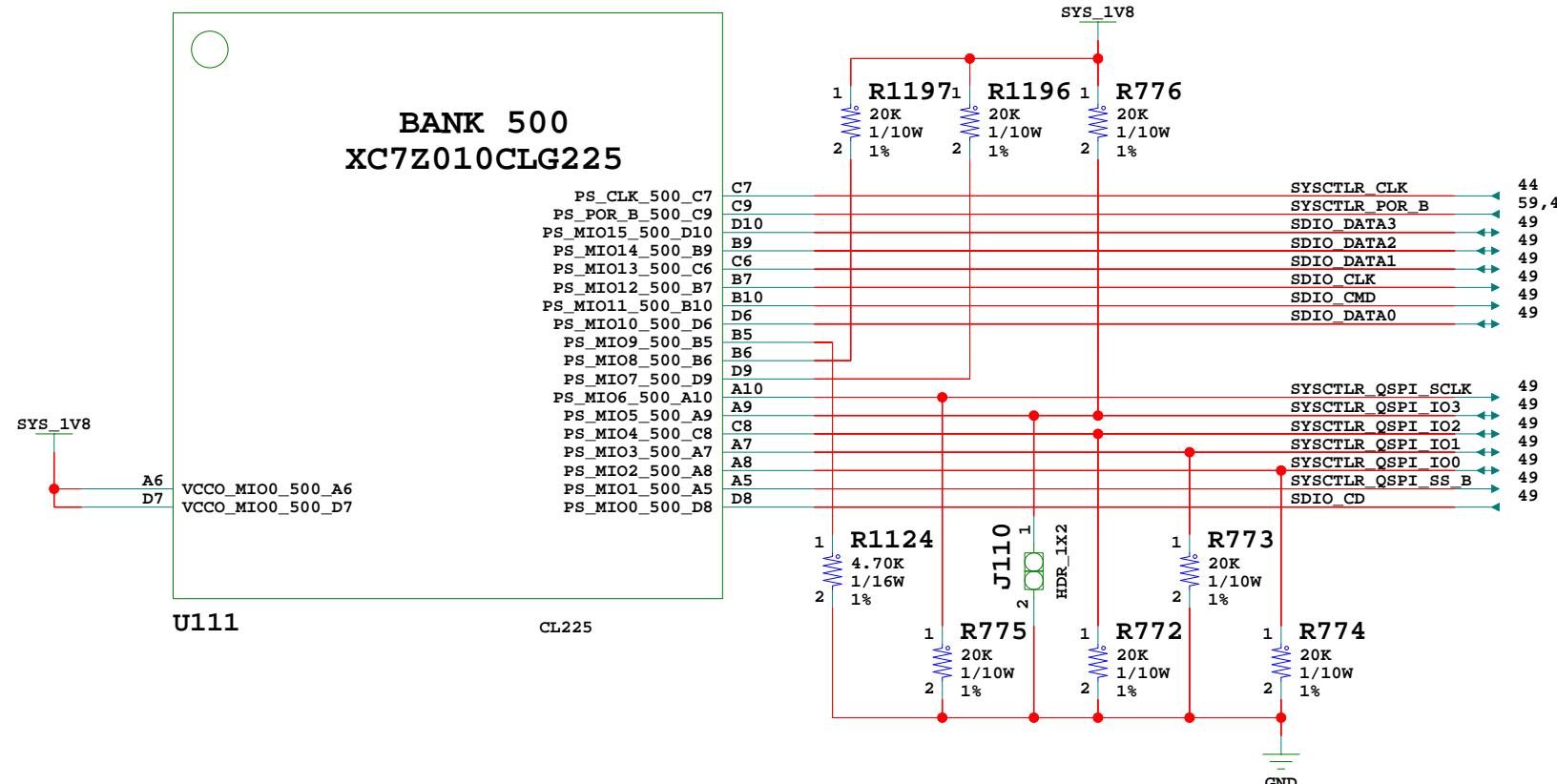
44 OF 76

76

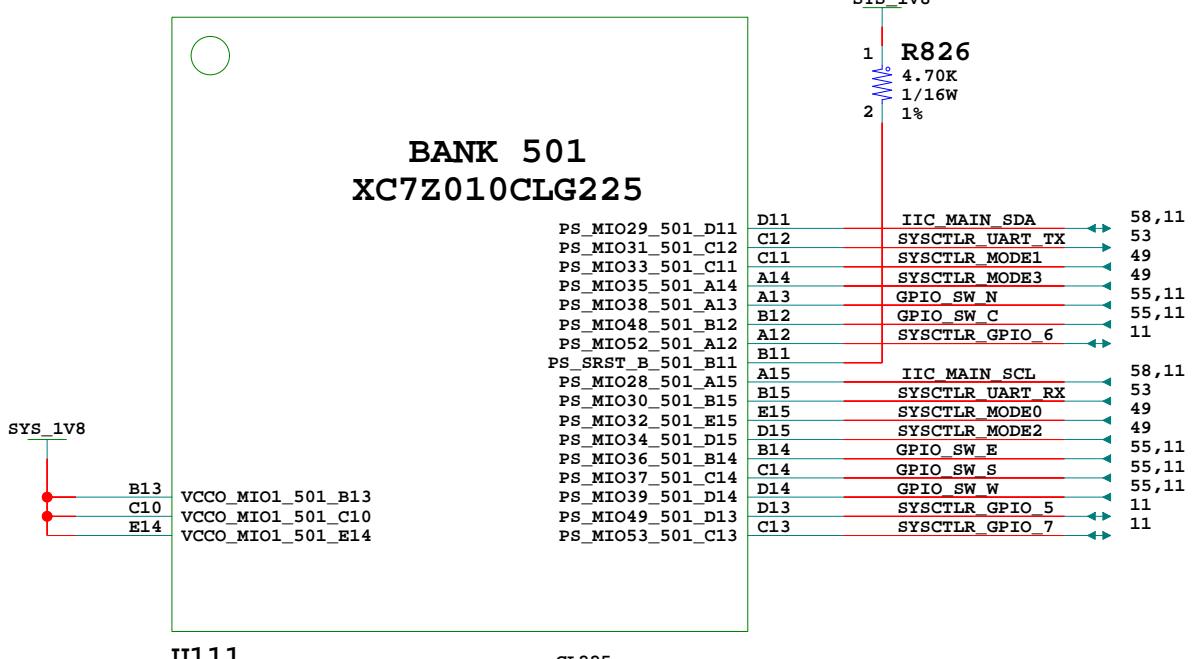




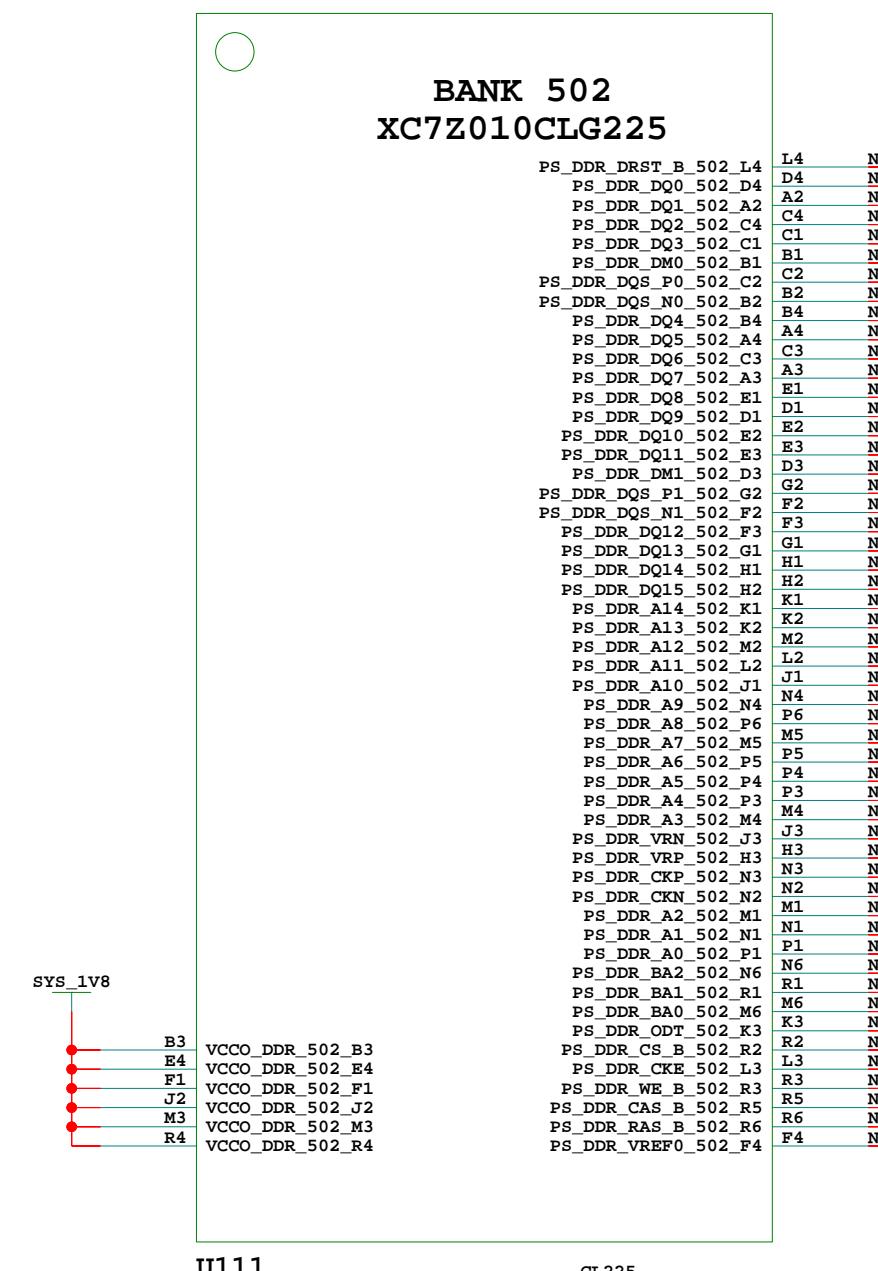
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XC7Z010CLG225



XC7Z010CLG225



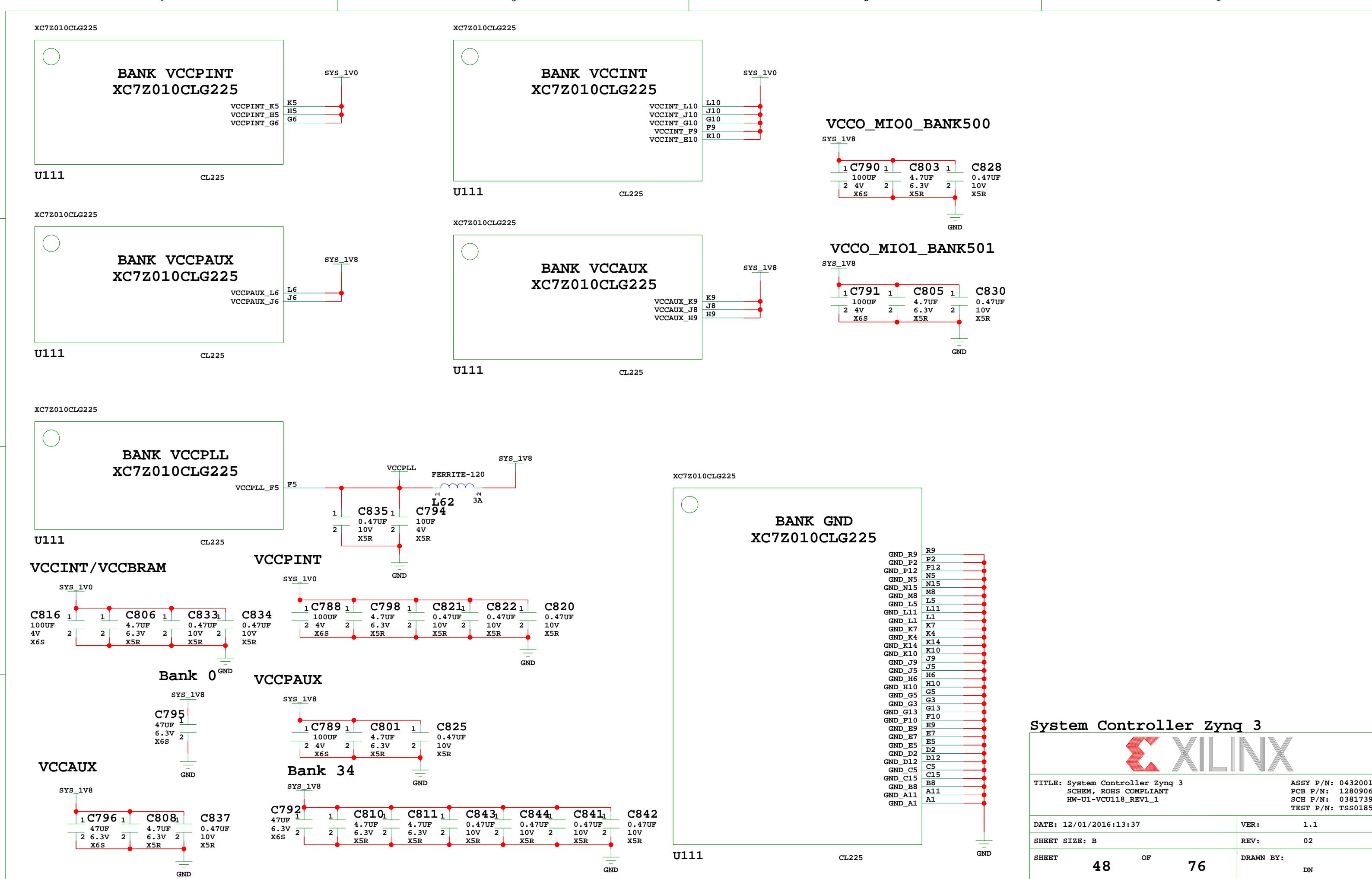
System Controller Zynq 2

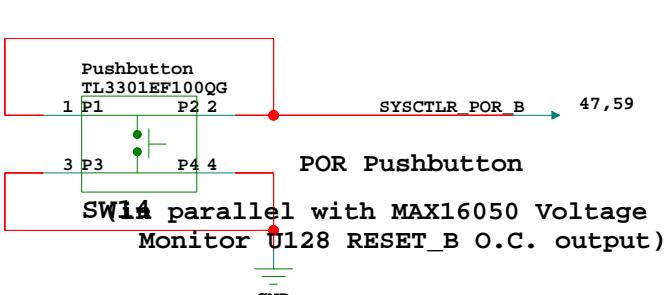
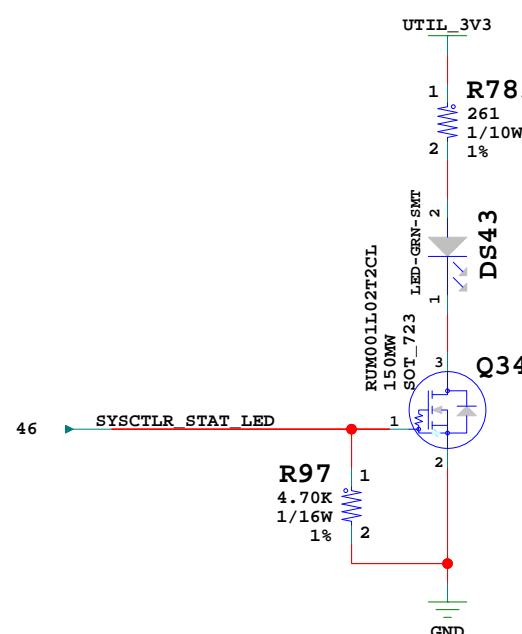
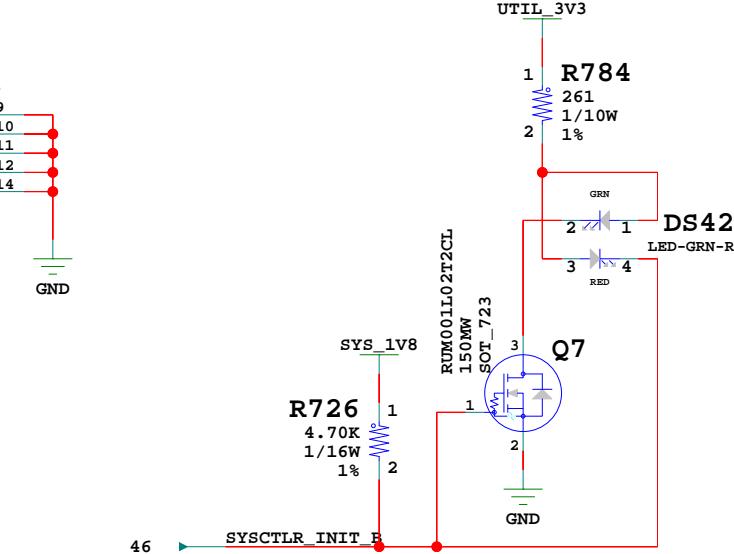
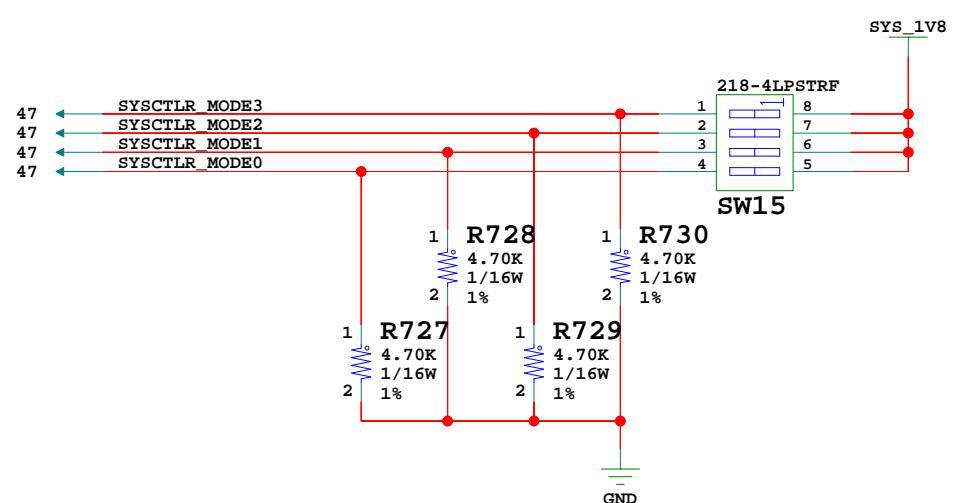
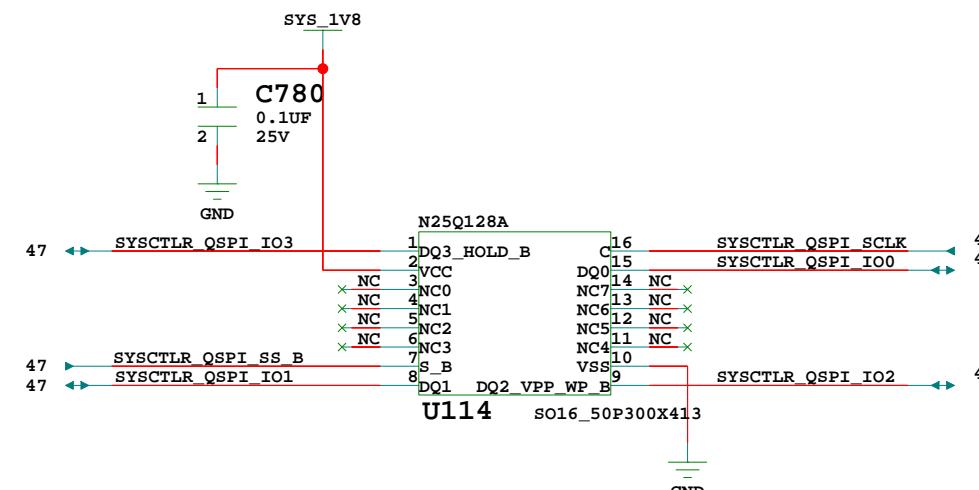
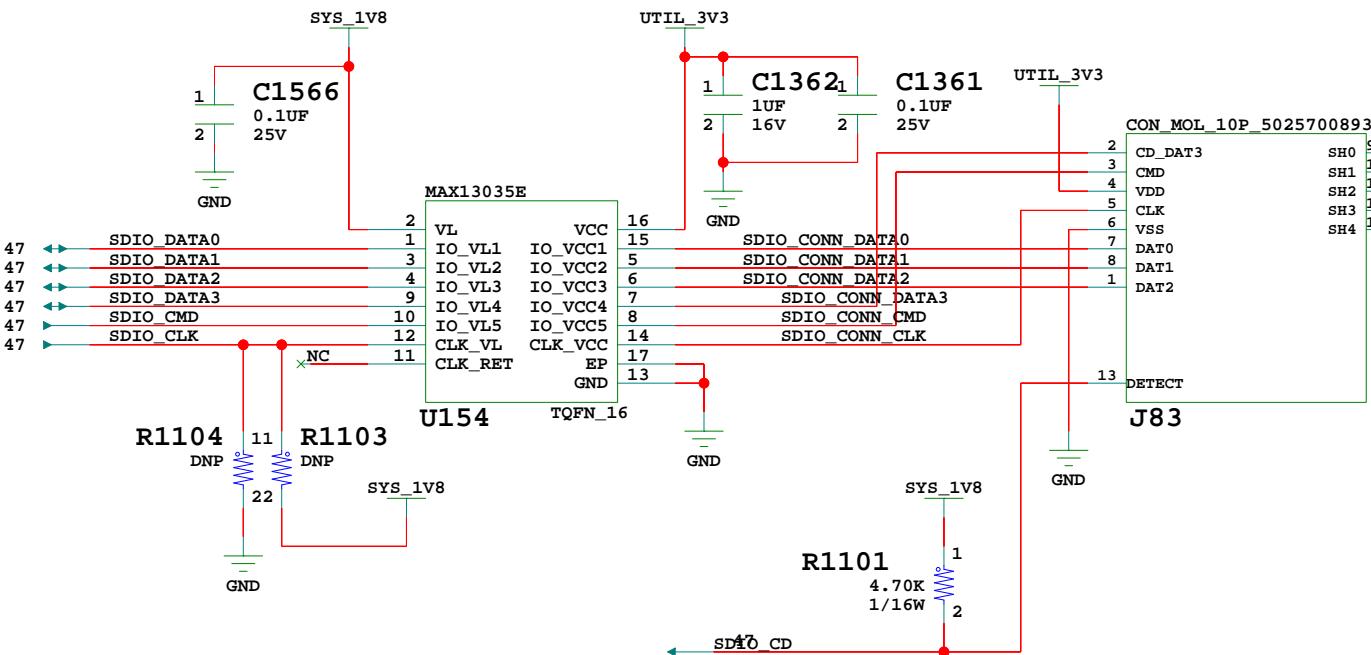


TITLE: System Controller Zynq 2
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:37	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 47 OF 76	DRAWN BY: DN





System Controller Zynq 4

**TITLE: System Controller Zynq 4
SCHEM, ROHS COMPLIANT
HW-111-VCH118 REV1.1**

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016 13:37

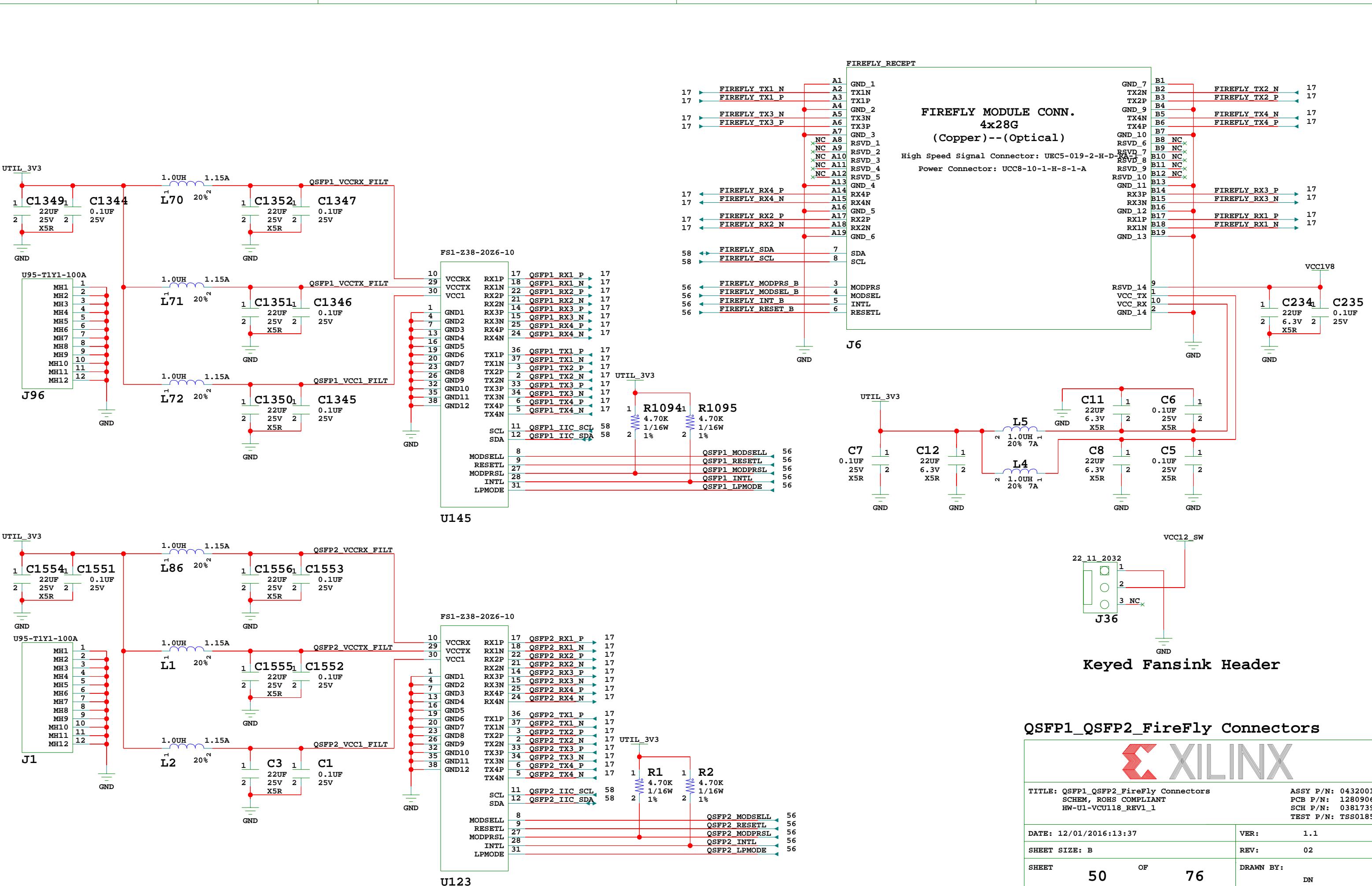
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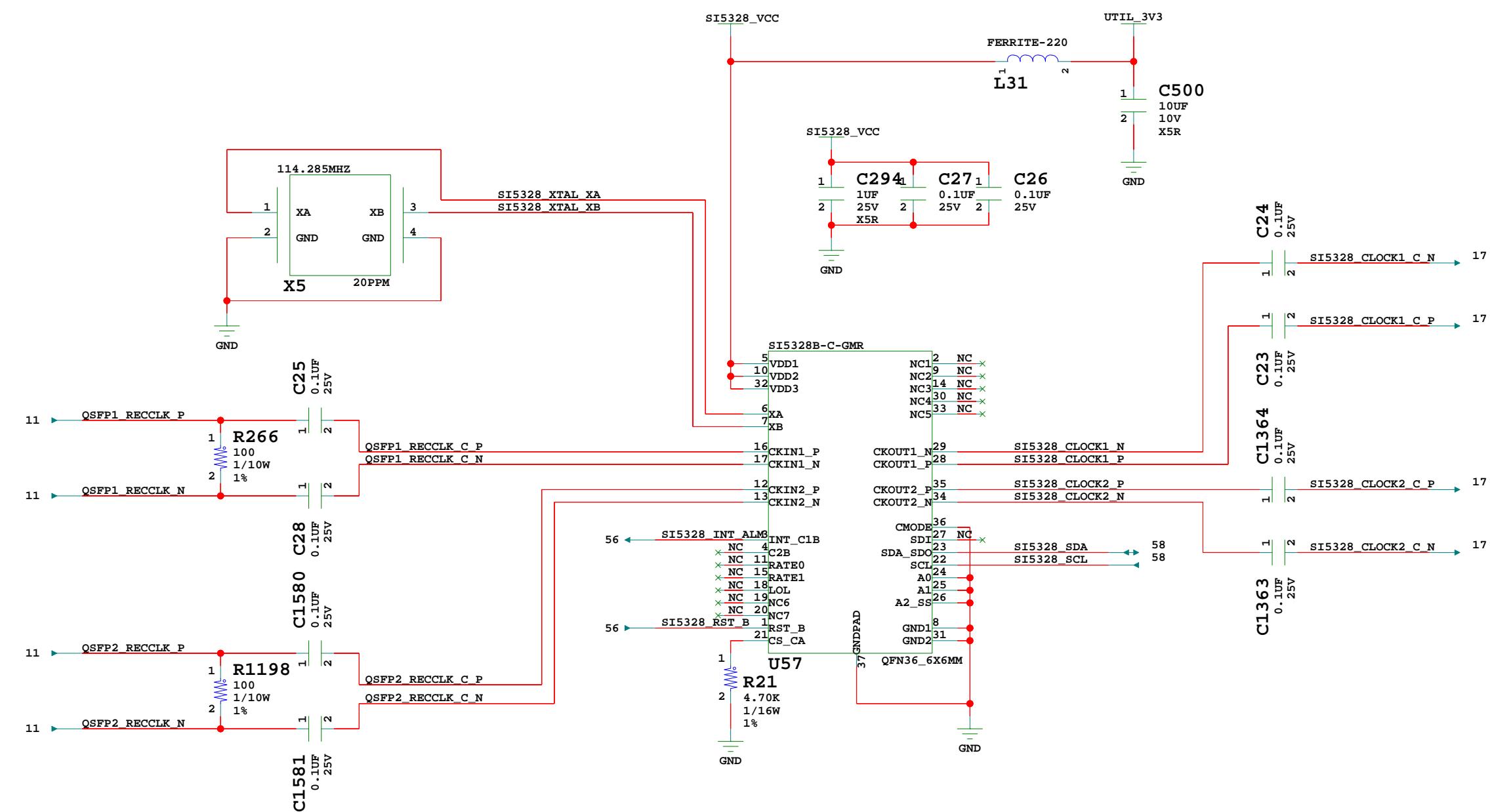
SHEET OF

1 1

03

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QSFP+ 5328 Jitter Recovery

 XILINX

**TITLE: QSFP+ 5328 Jitter Recovery
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1**

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 13/01/2016:13:37

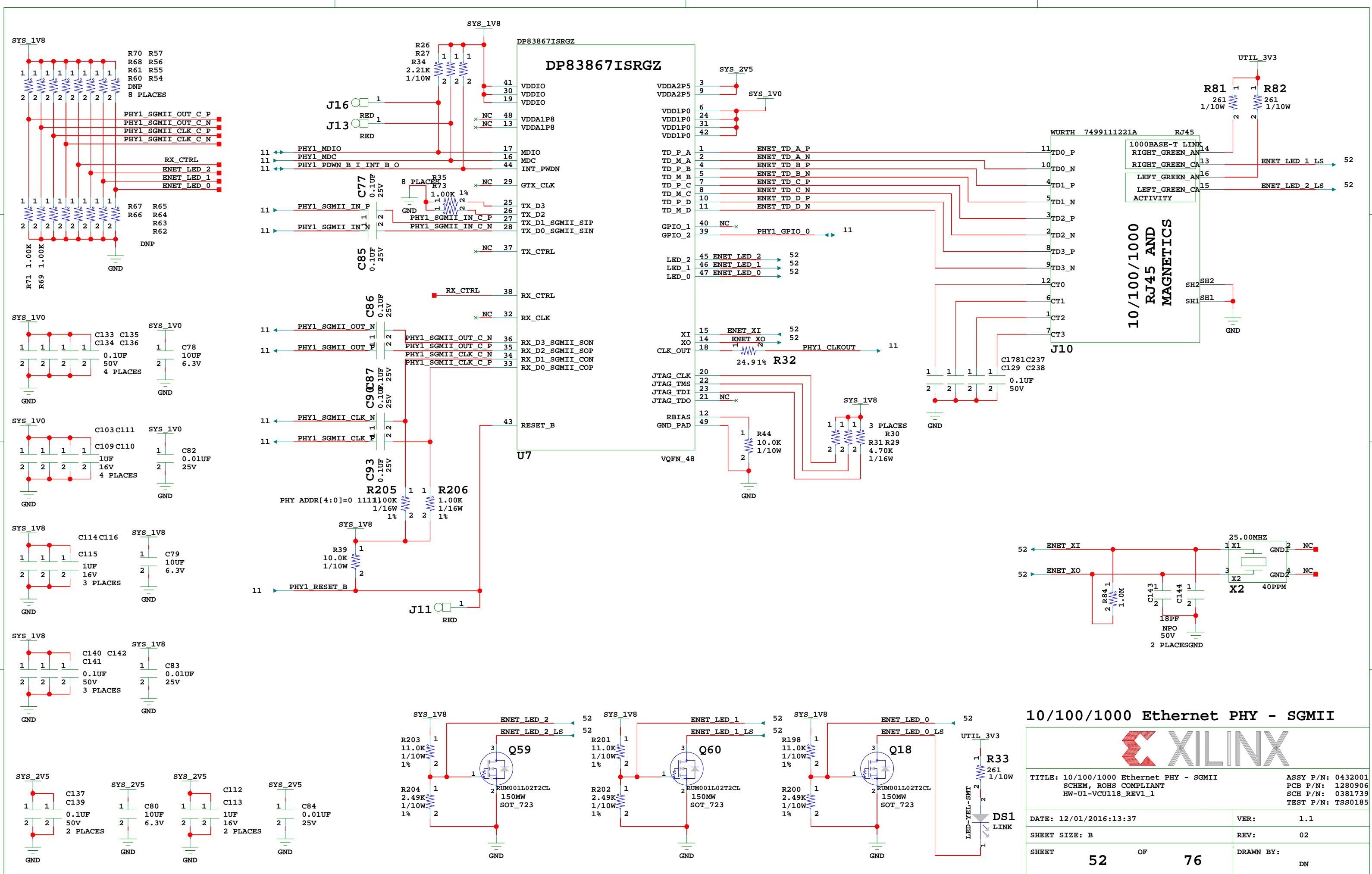
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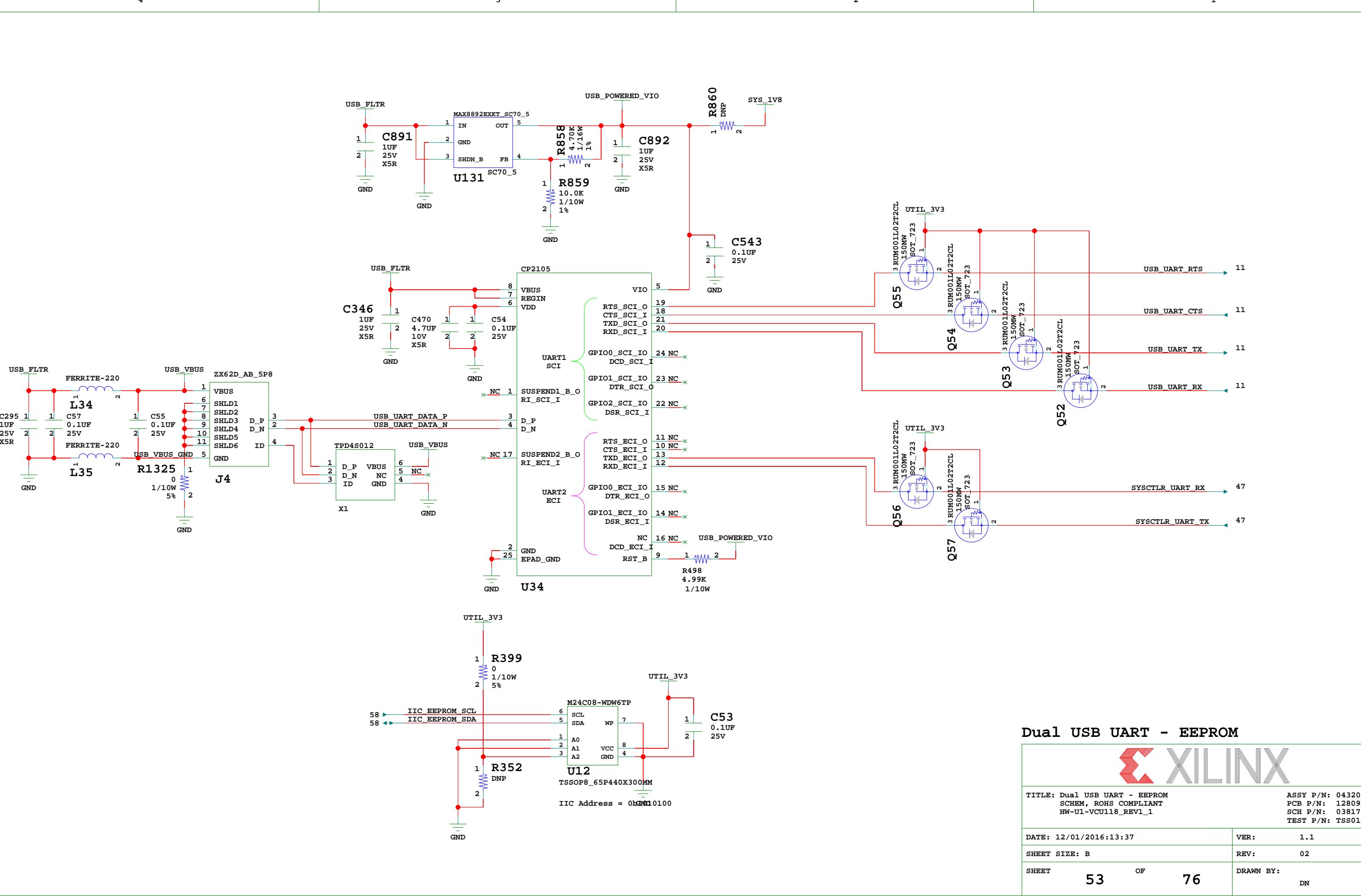
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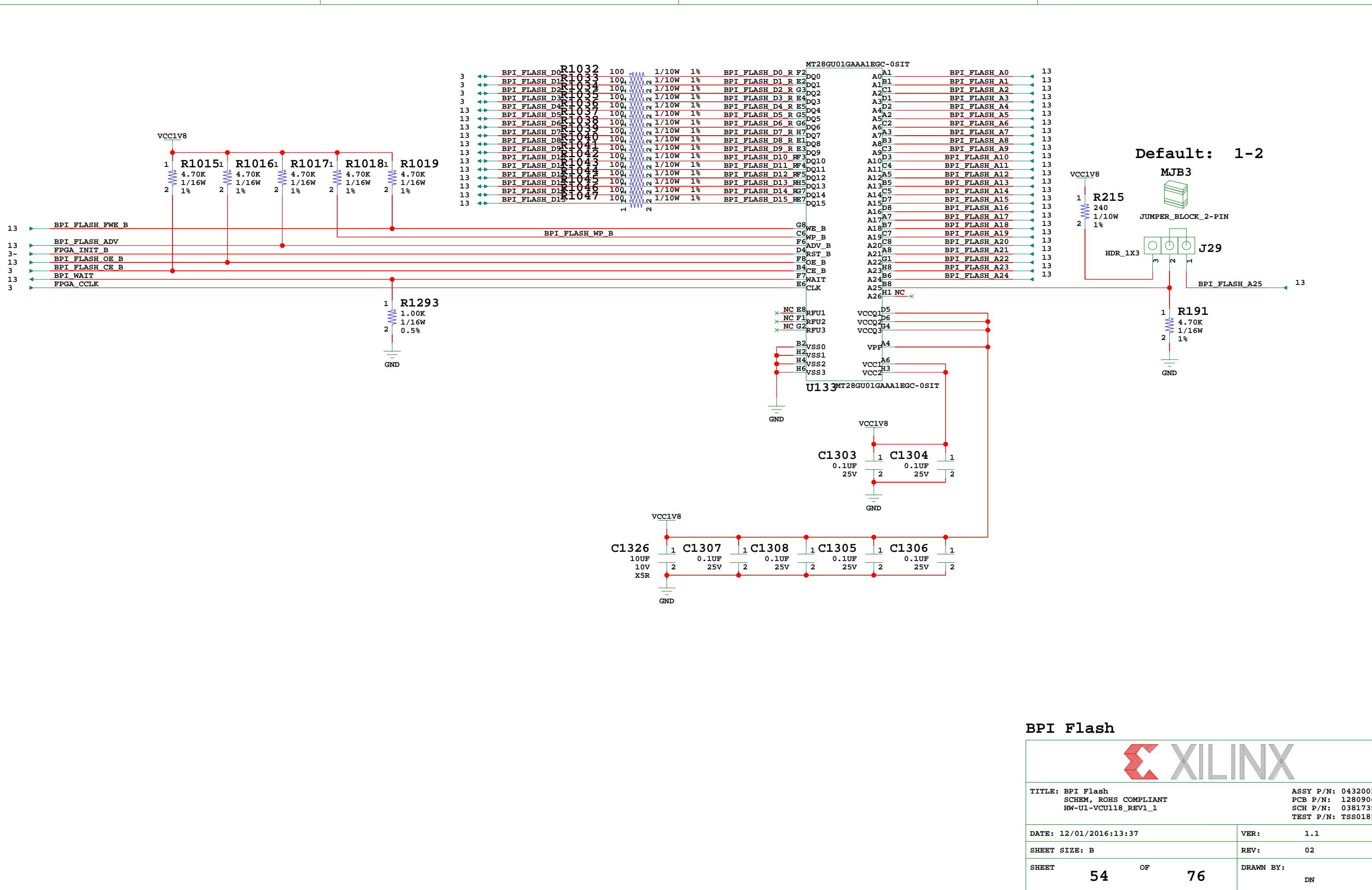
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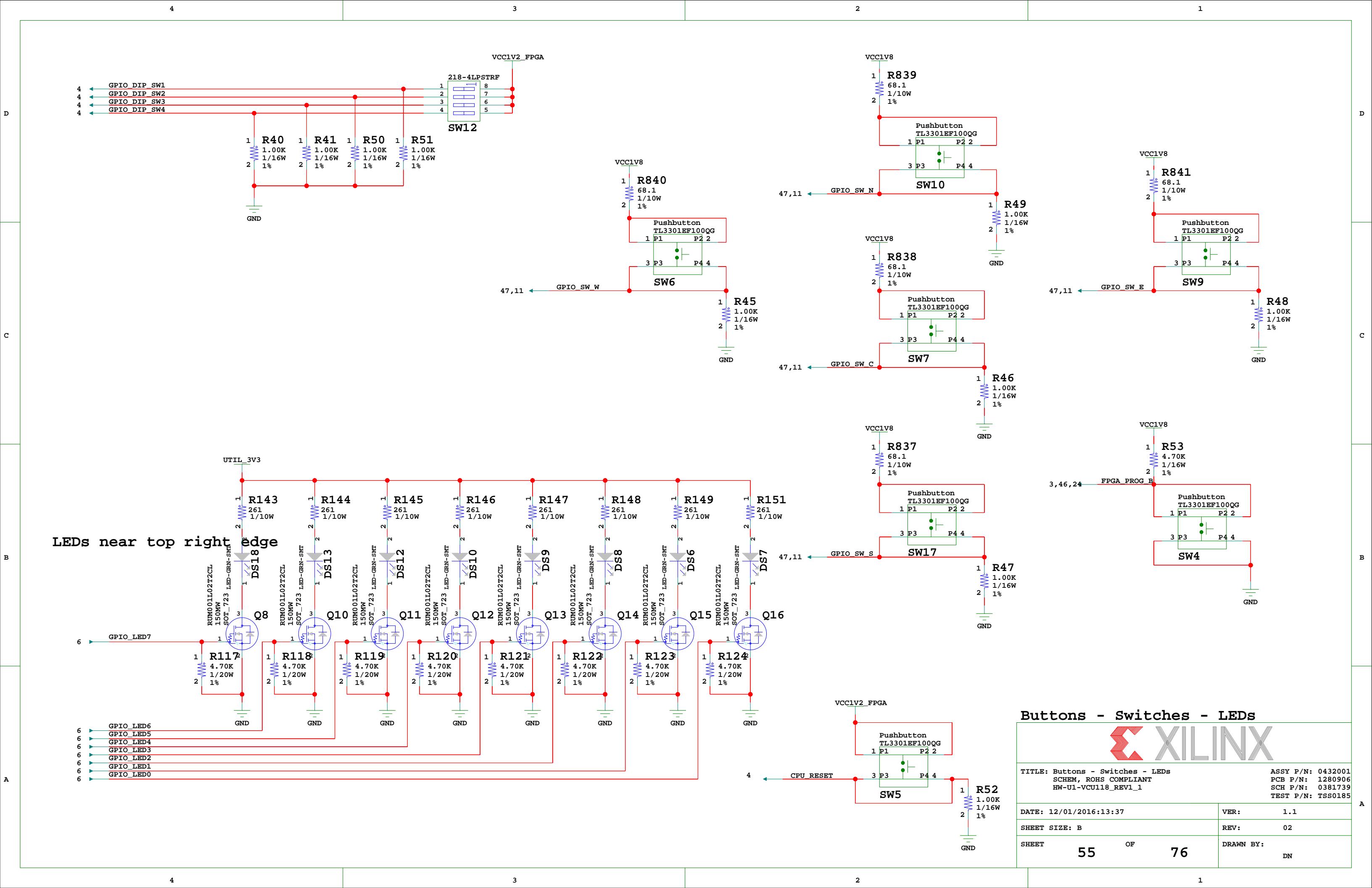
SHEET 51 OF 76

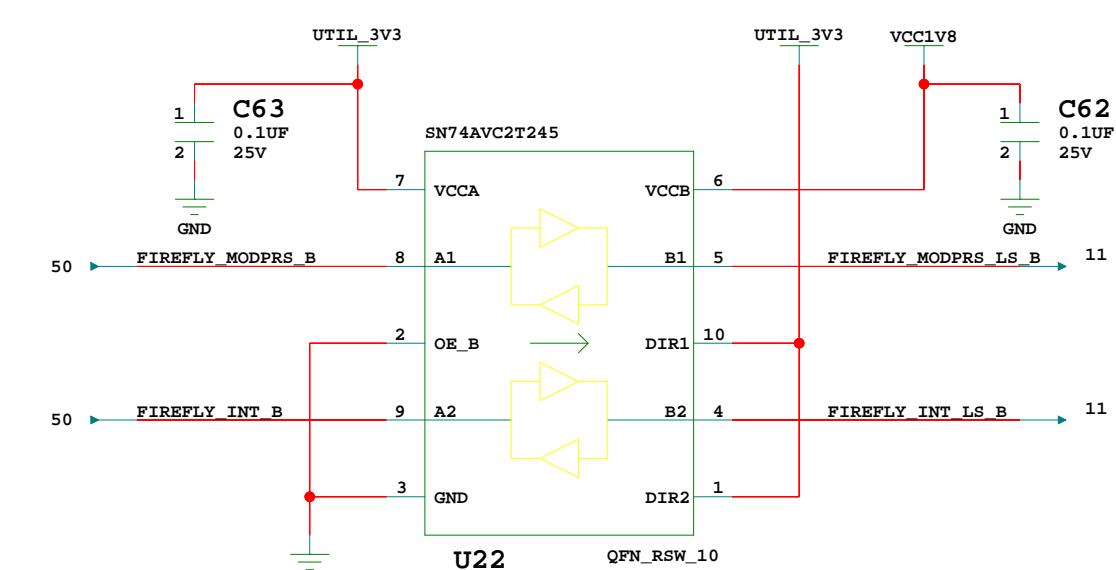
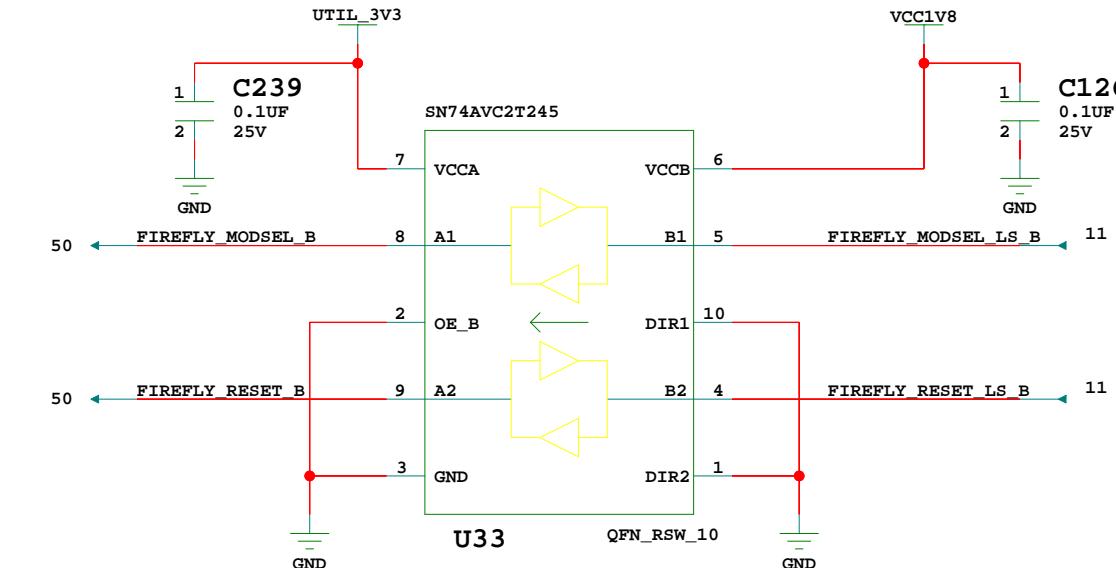
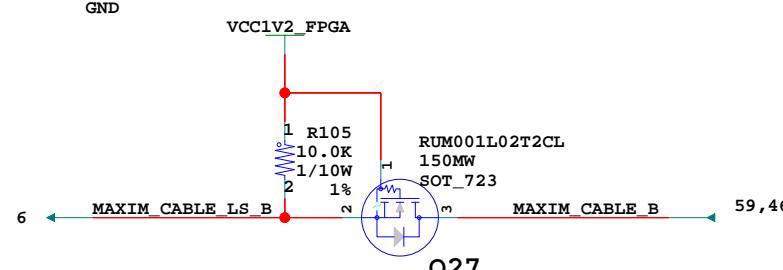
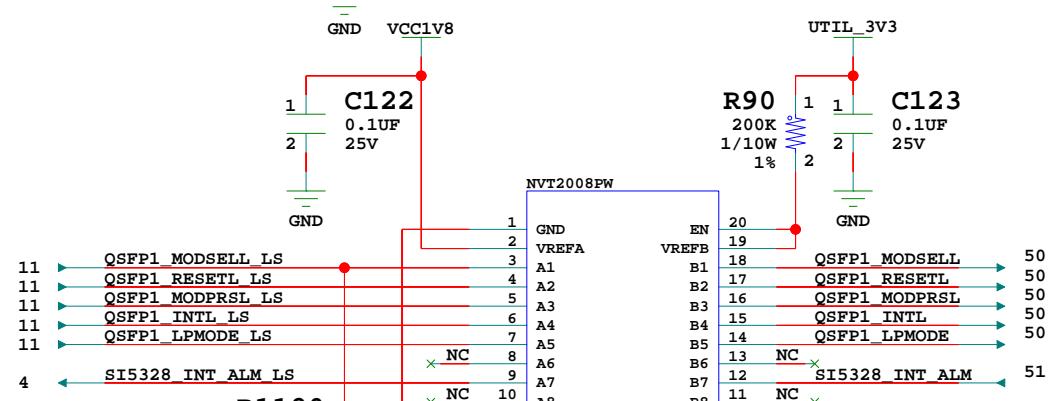
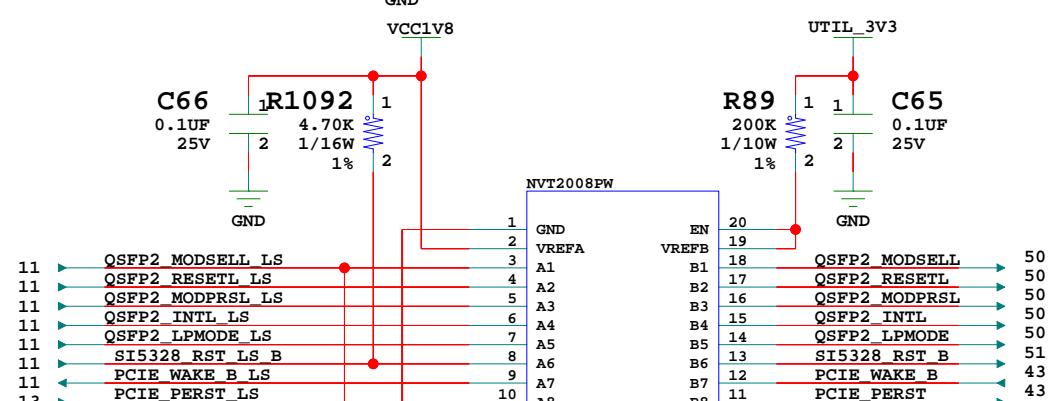
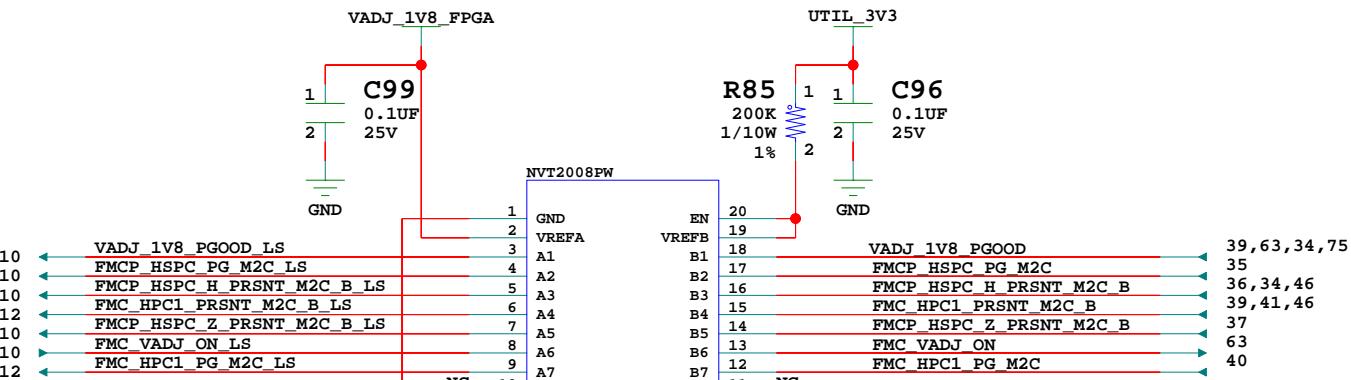
1. **What is the primary purpose of the study?**











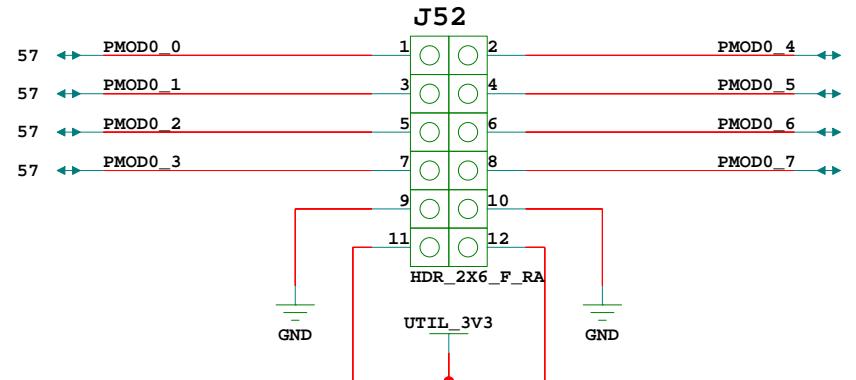
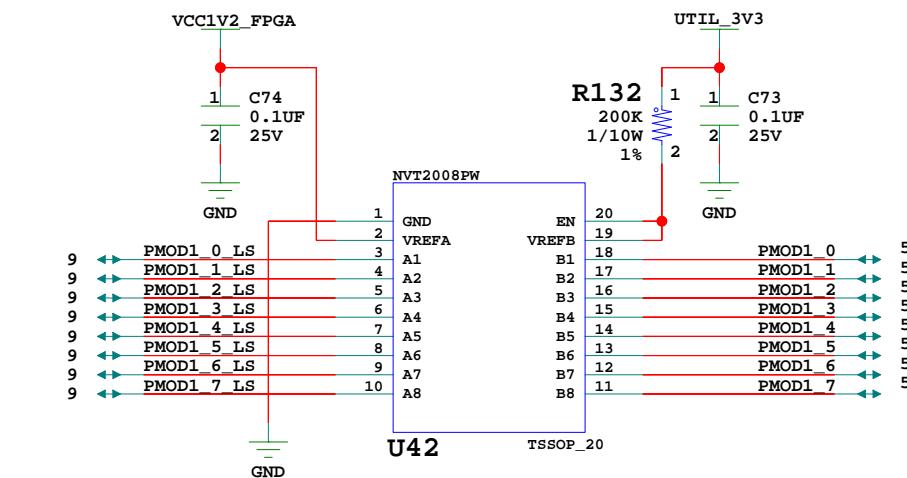
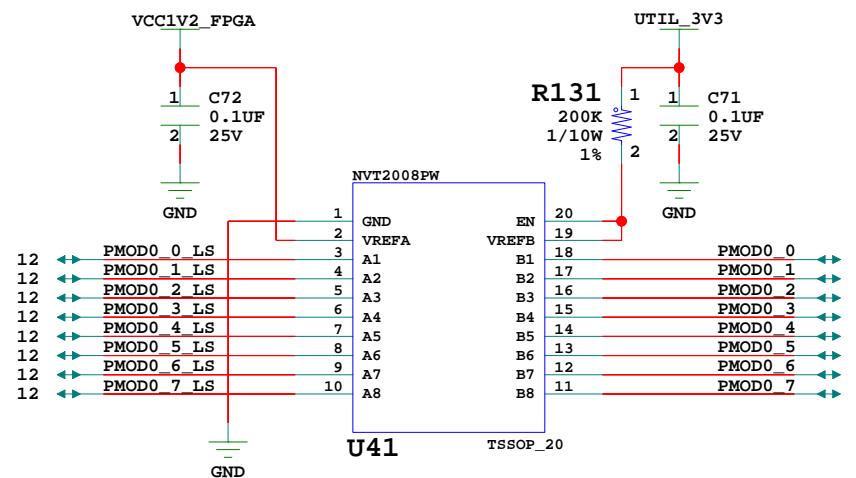
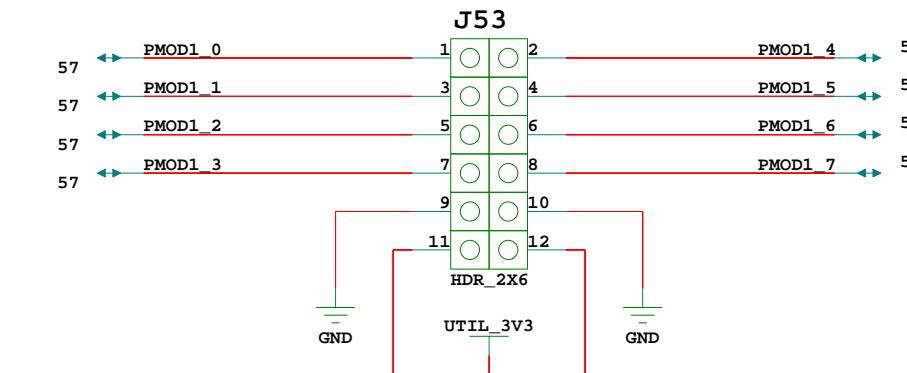
Level Shifters



TITLE: Level Shifters
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:37	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 56 OF 76	DRAWN BY: DN

PMOD Rt-Angle Female Receptacle**PMOD Male Pin Header****PMODs and Level Shifters**

TITLE: PMODs and Level Shifters
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:39

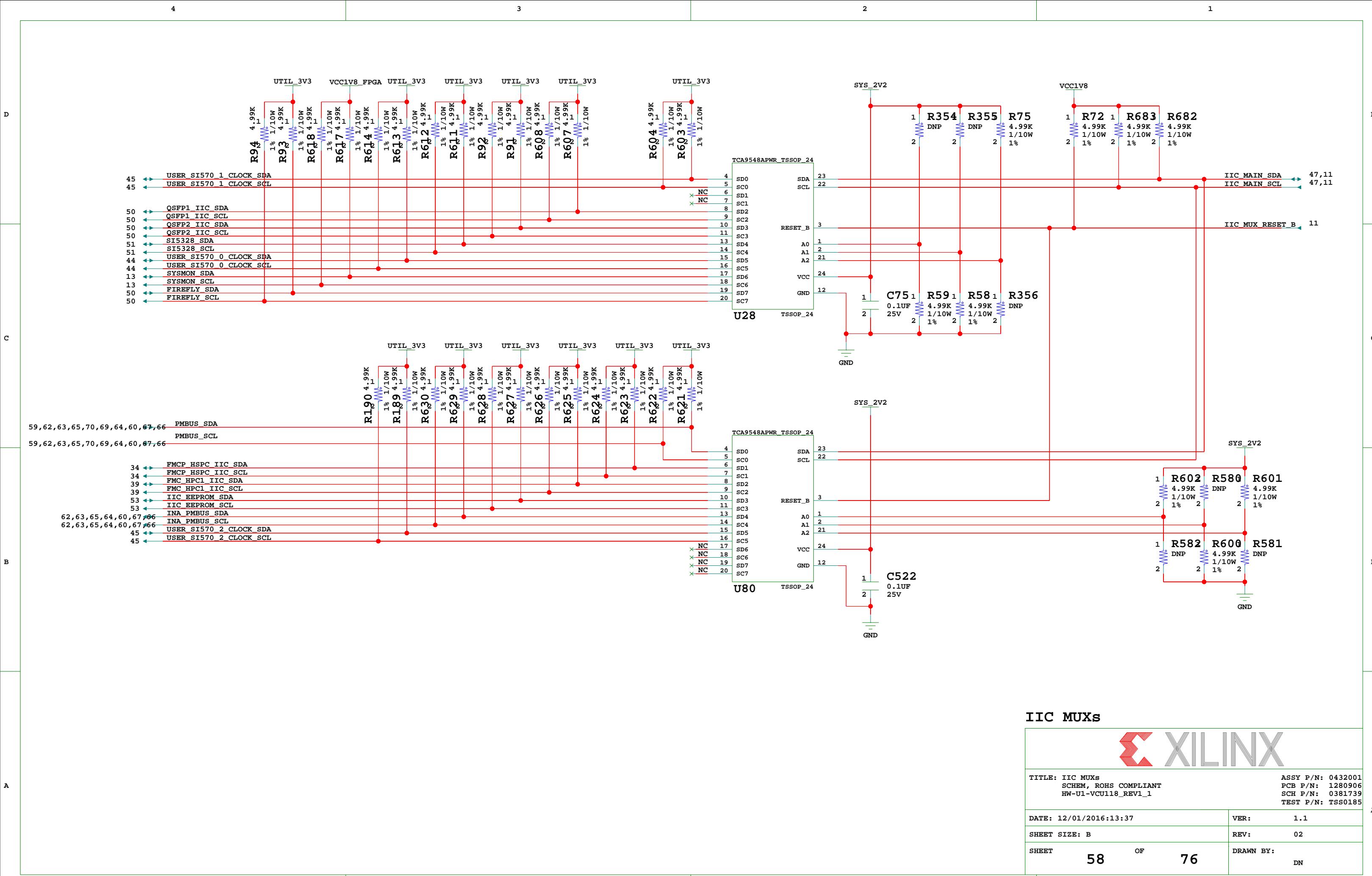
VER: 1.1

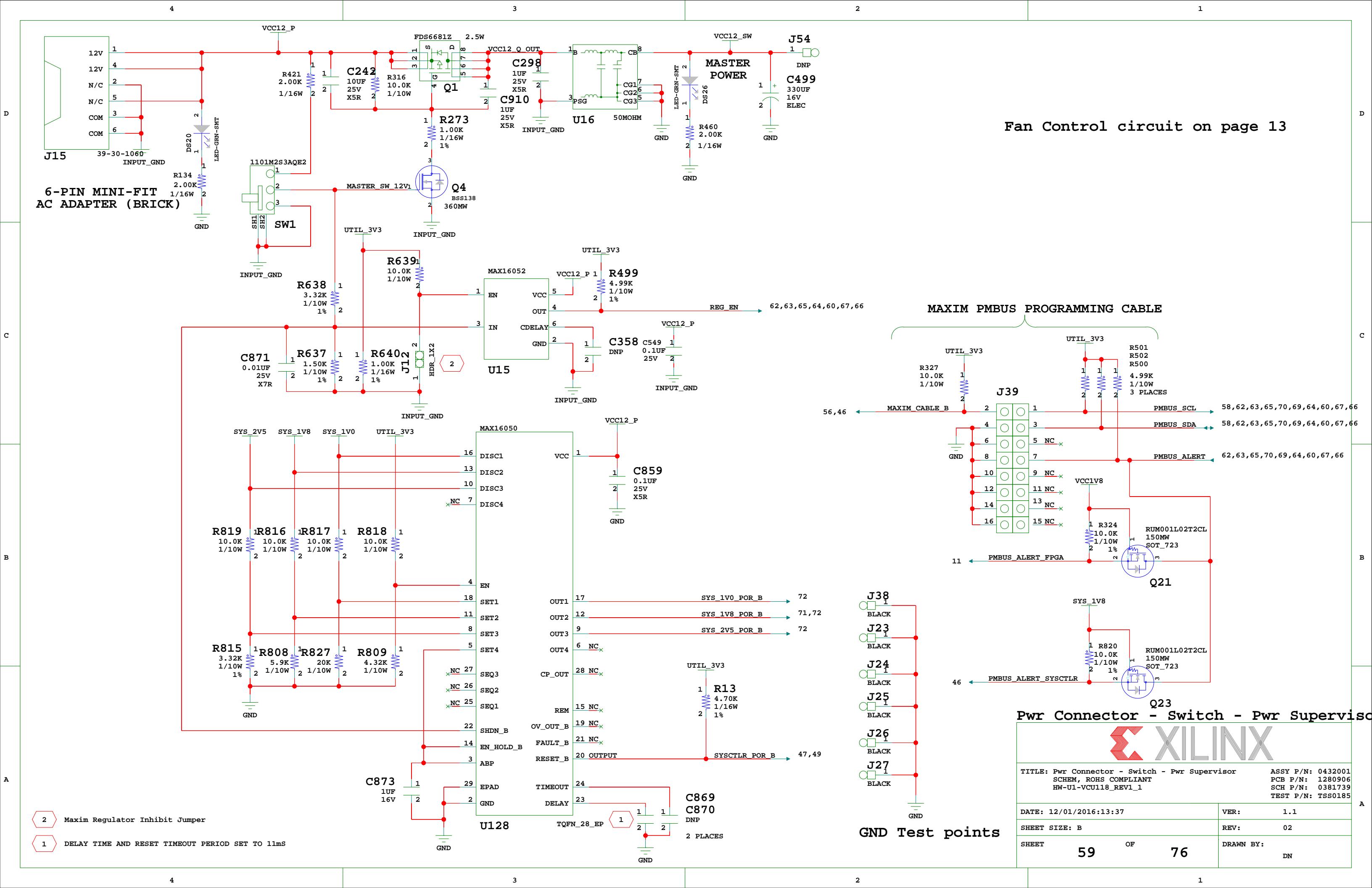
SHEET SIZE: B

REV: 02

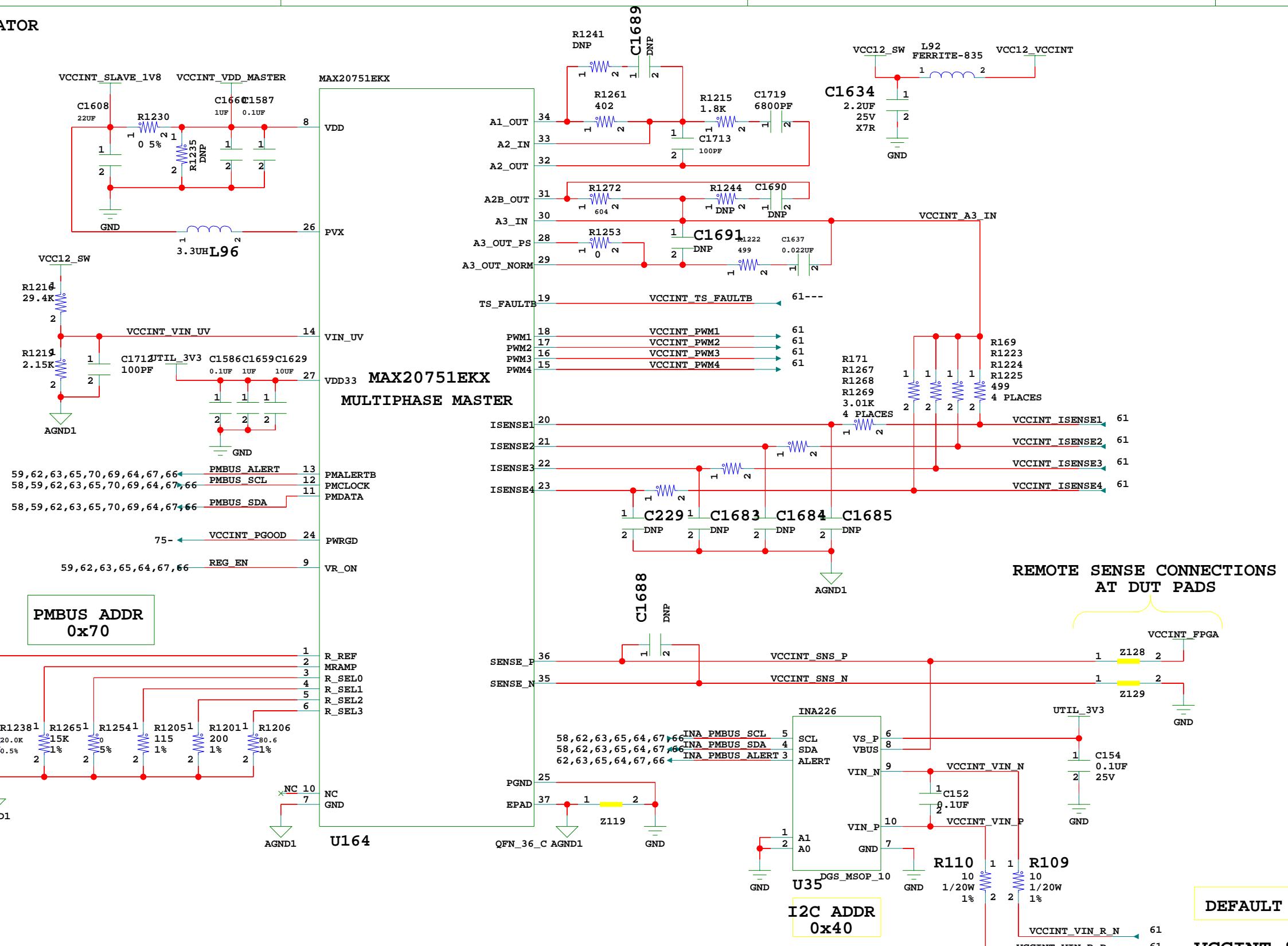
SHEET 57 OF 76

DRAWN BY: DN





VCCINT REGULATOR



DEFAULT = 0.72VDC

VCCINT 80A Regulator Master

The image shows three stylized letters: 'E', 'XII', and 'INX'. The 'E' is composed of red diagonal lines. The 'XII' is composed of grey vertical and diagonal lines. The 'INX' is composed of grey vertical lines.

**TITLE: VCCINT 80A Regulator Master
SCHEM, ROHS COMPLIANT
HW-U1-VCU118 REV1 1**

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 13/01/2016:13:37

1 1

SHEET SIZE: B

03

SHEET **OF**

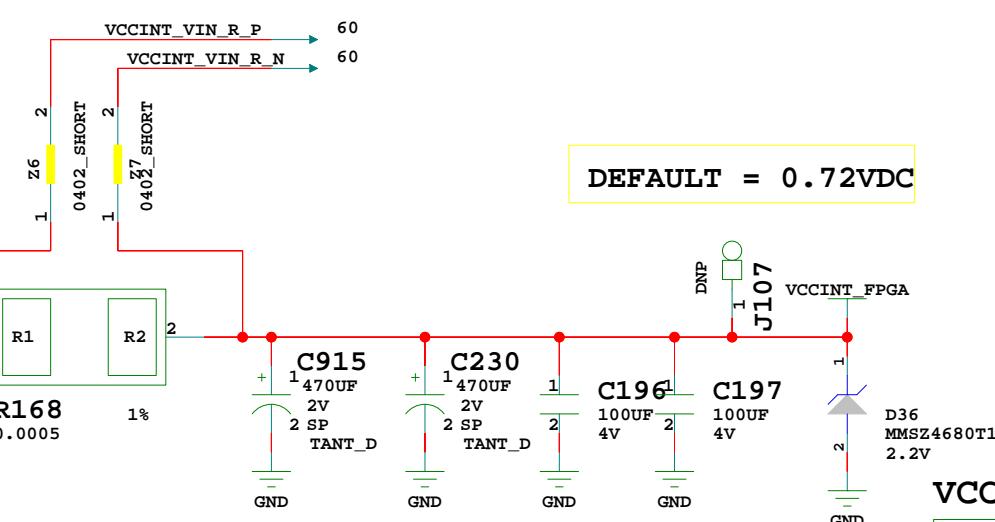
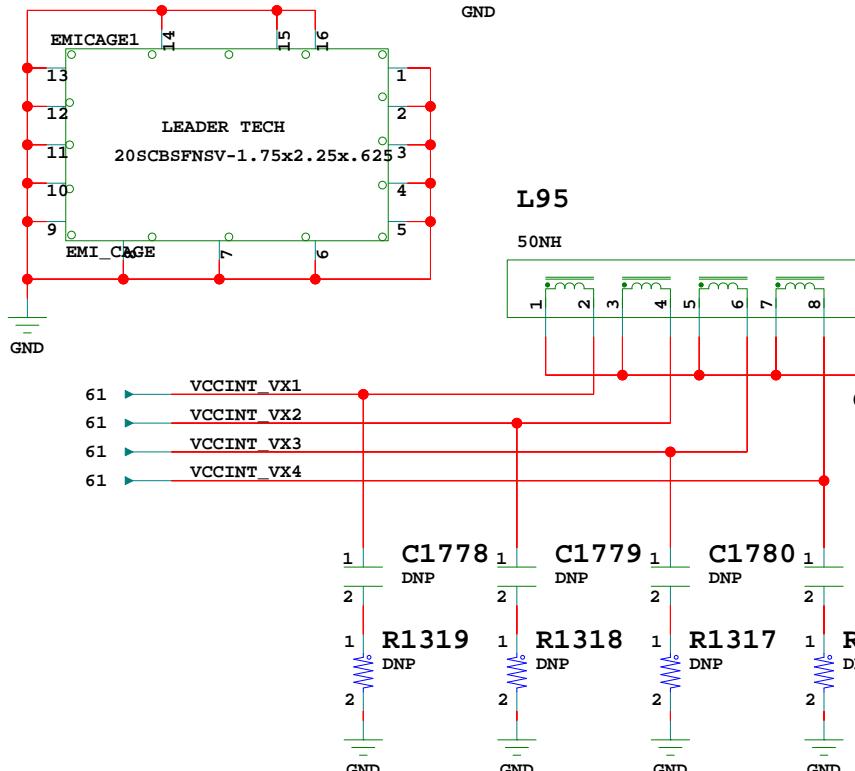
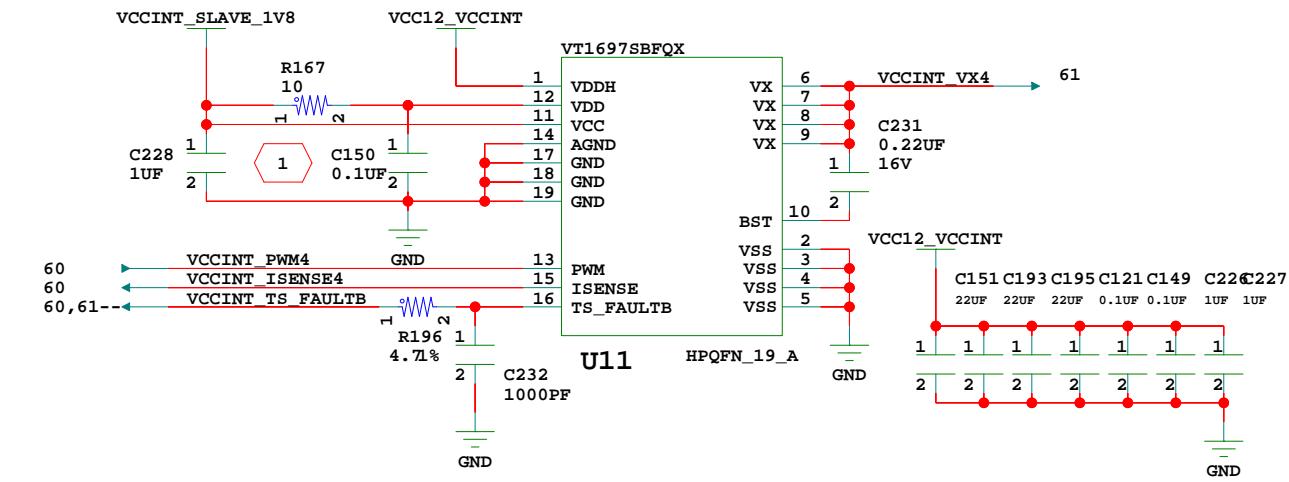
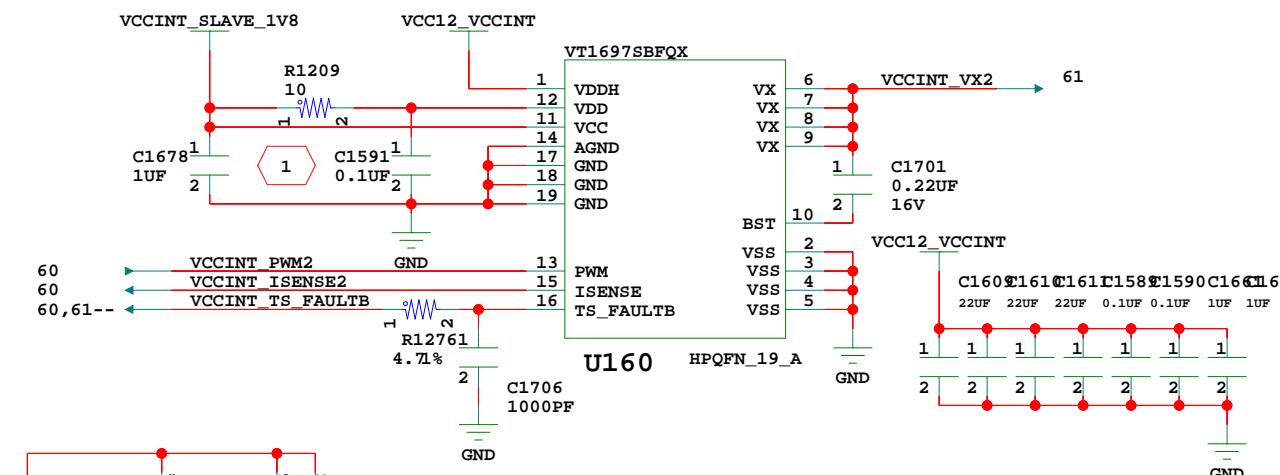
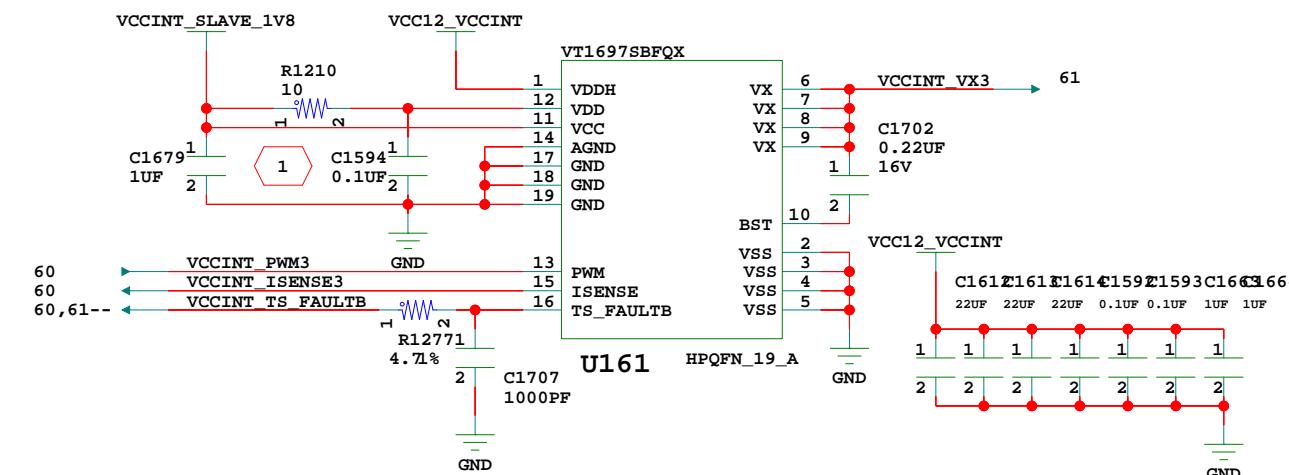
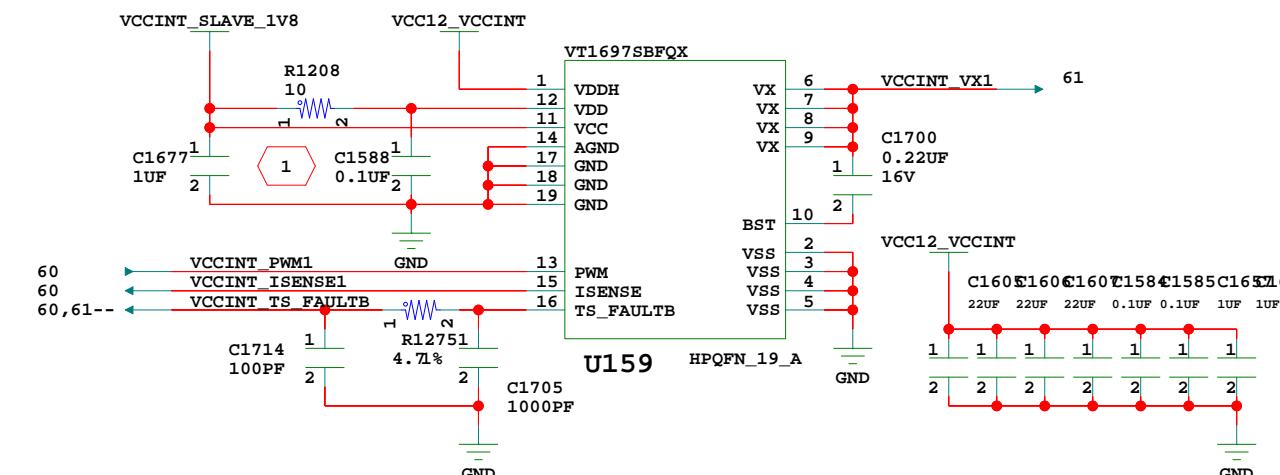
ANSWER

60

DN

1

10 of 10 | Page | [Report a Problem](#) | [Feedback](#) | [Help](#) | [About](#) | [Contact Us](#) | [Privacy Policy](#) | [Terms of Use](#) | [Sitemap](#)

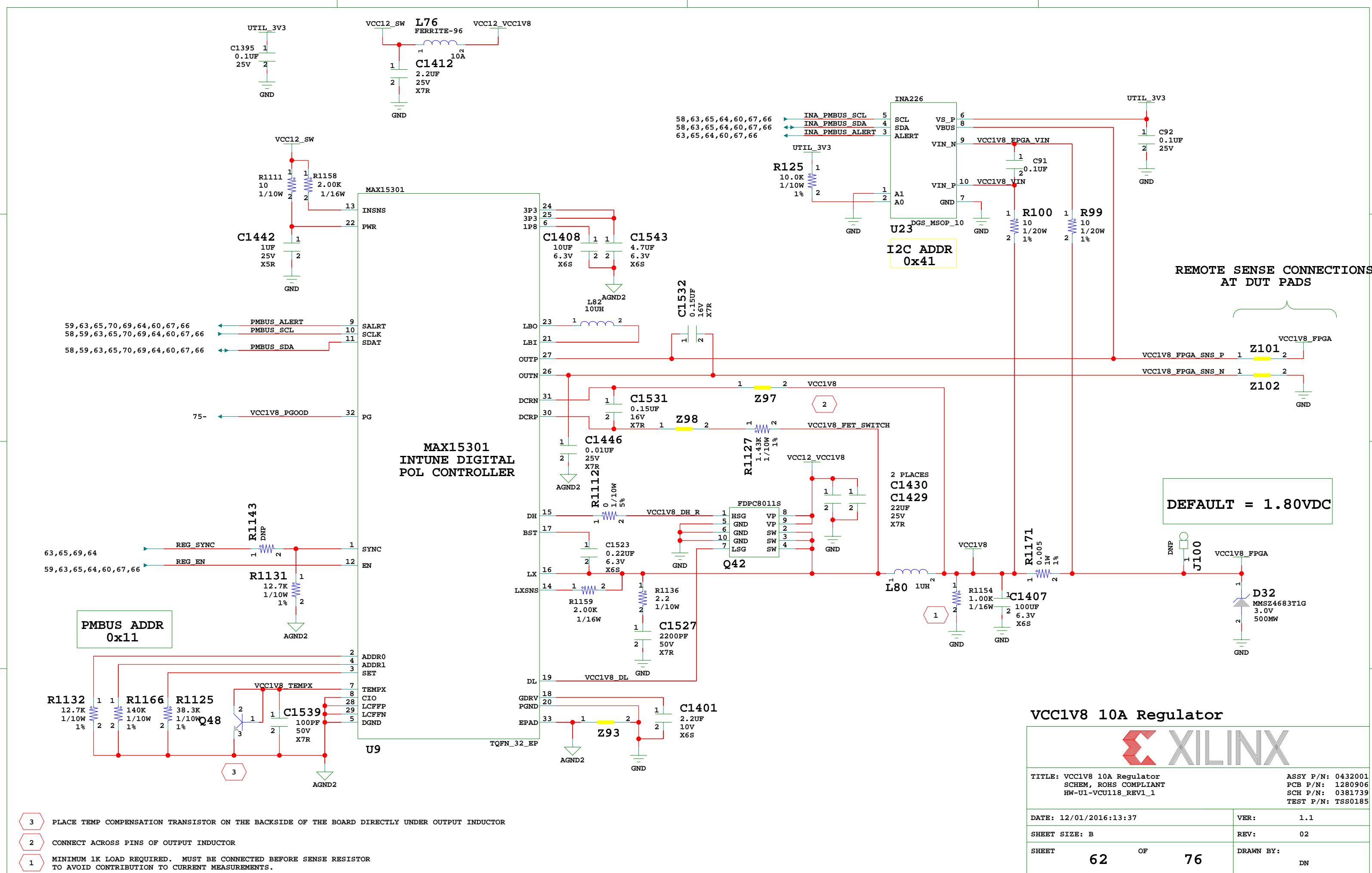


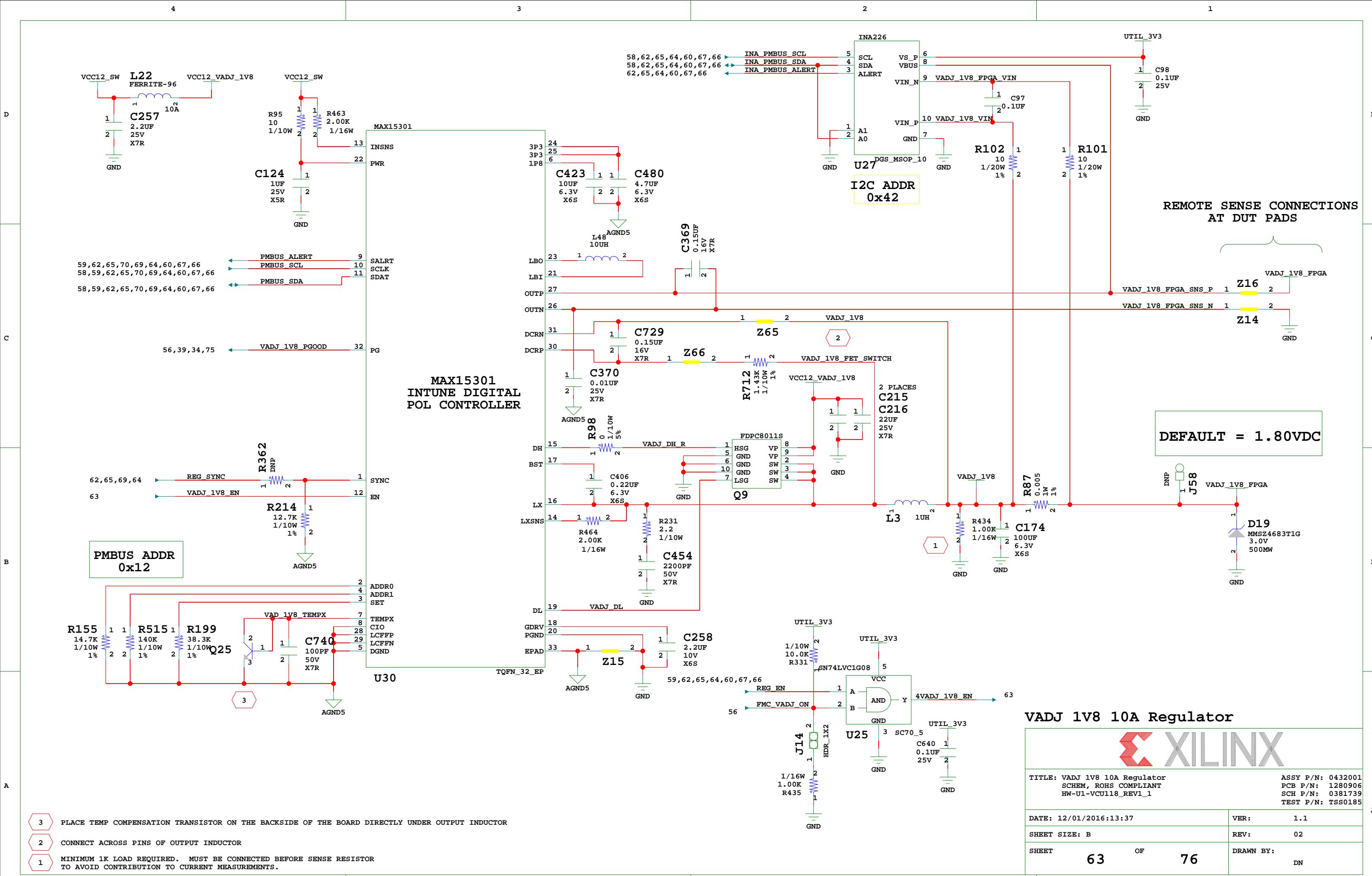
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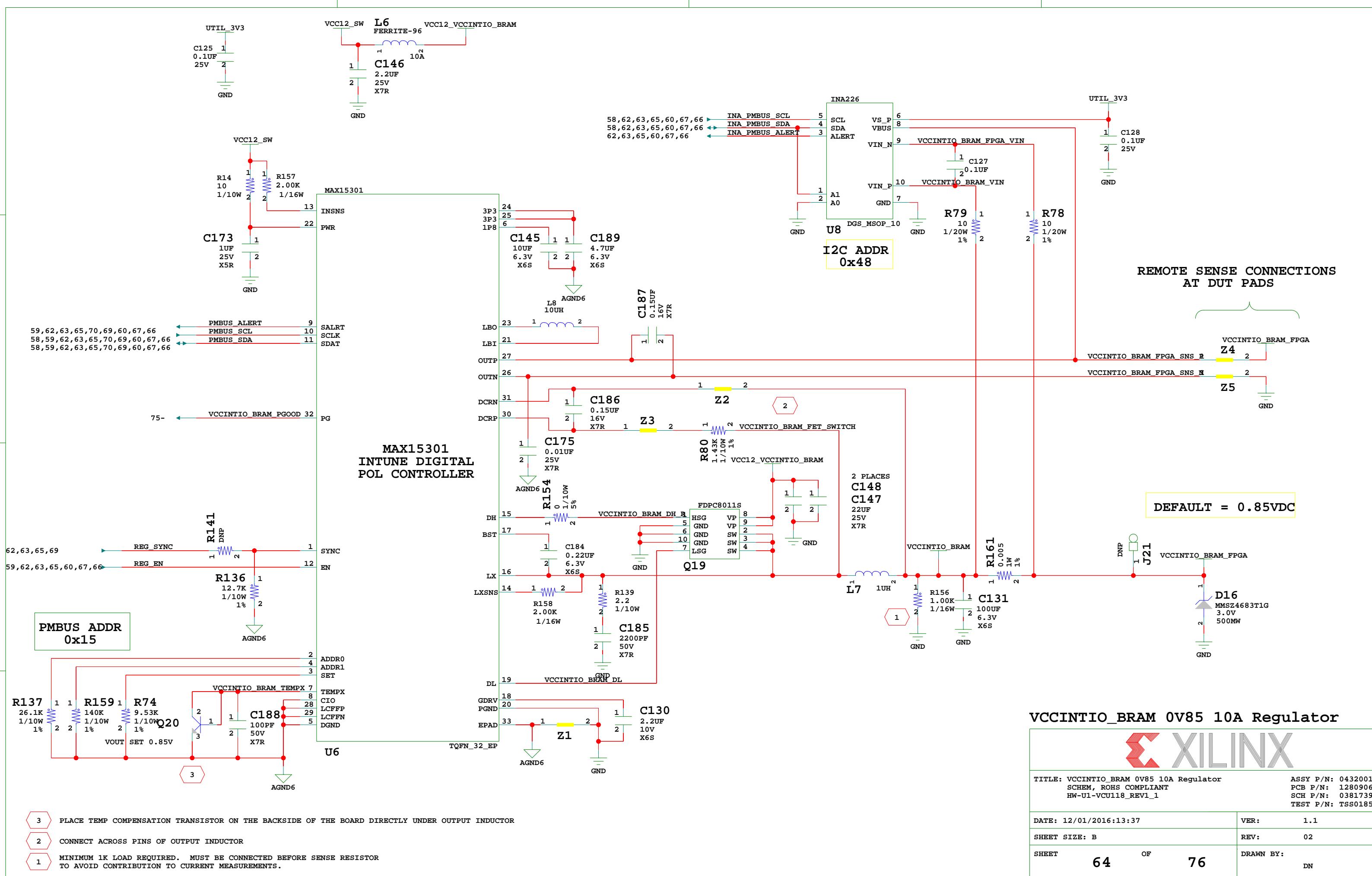
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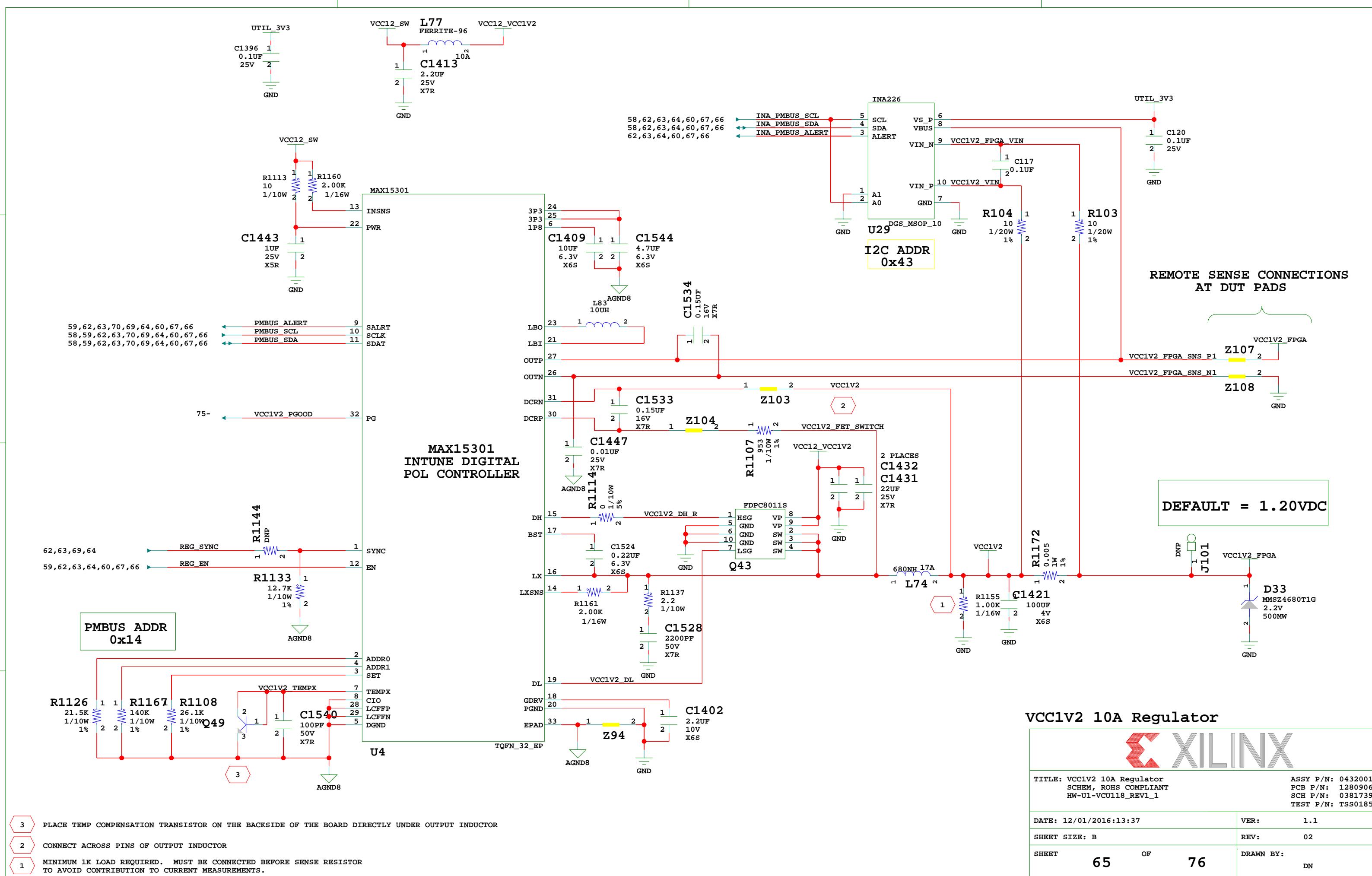
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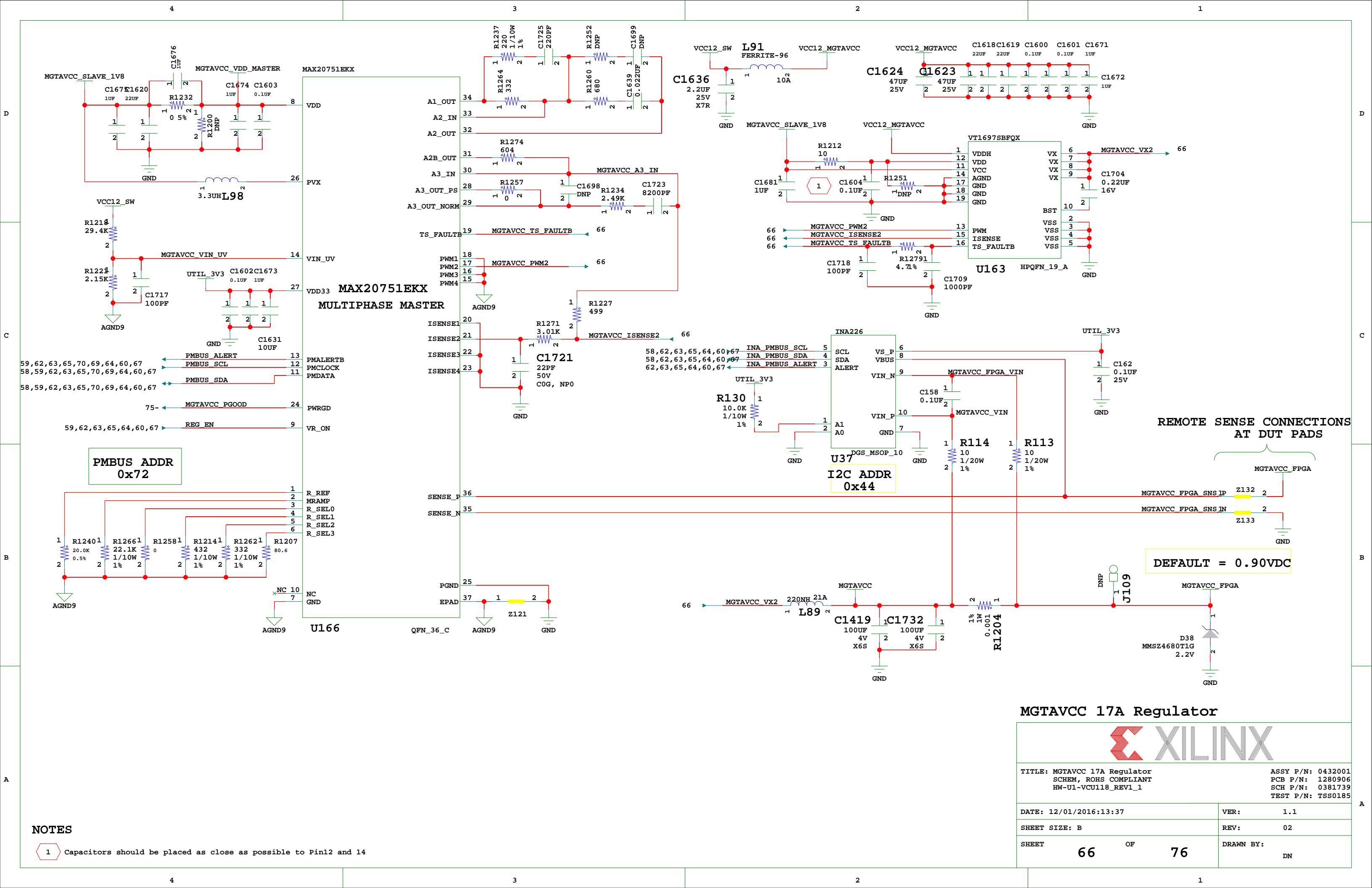
TITLE: VCCINT 80A Regulator Slave	ASSY P/N: 0432001
SCHEM, ROHS COMPLIANT	PCB P/N: 1280906
HW-U1-VCU118_REV1_1	SCH P/N: 0381739
	TEST P/N: TSS0185
DATE: 12/01/2016:13:37	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 61 OF 76	DRAWN BY: DN

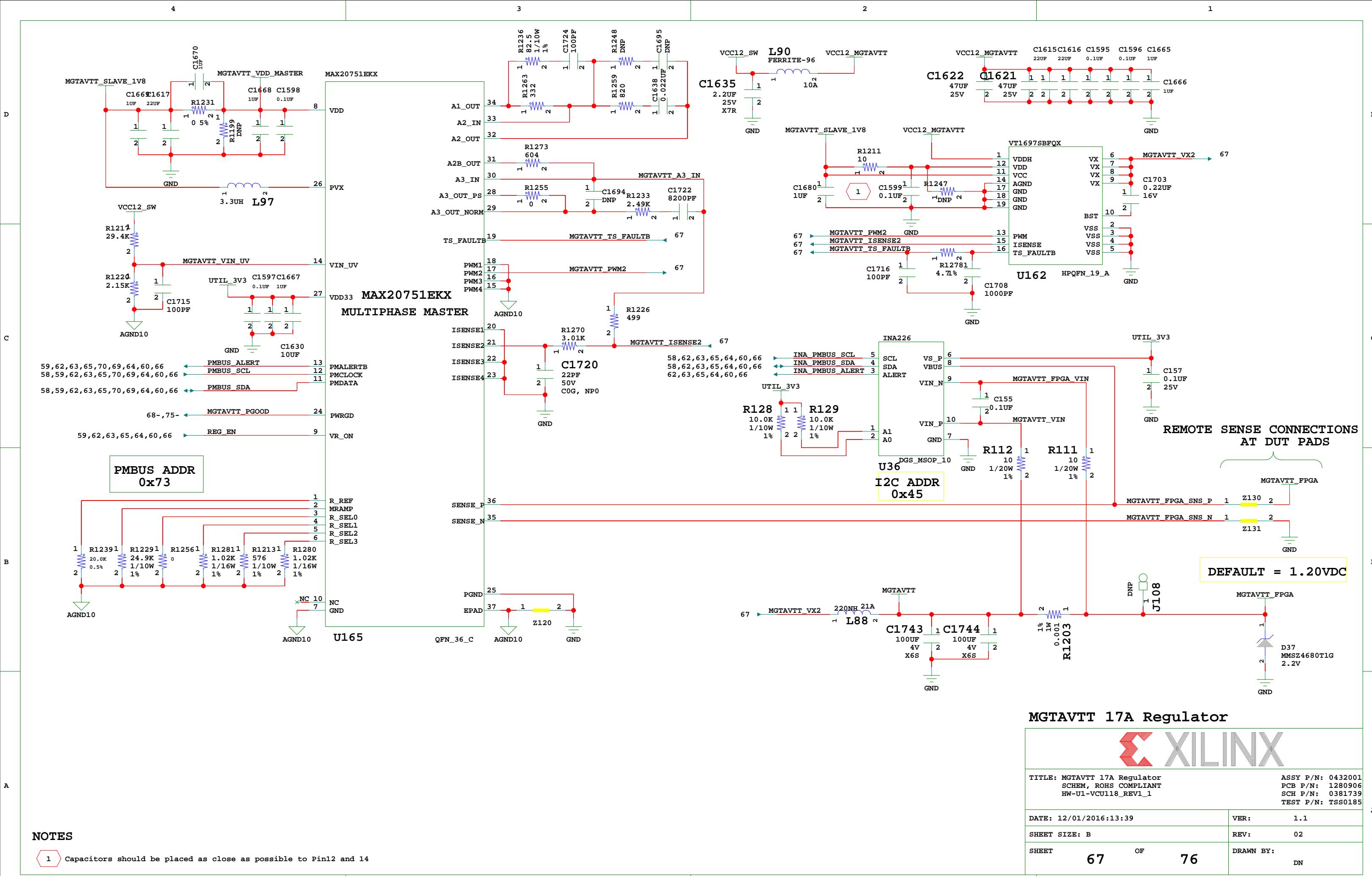


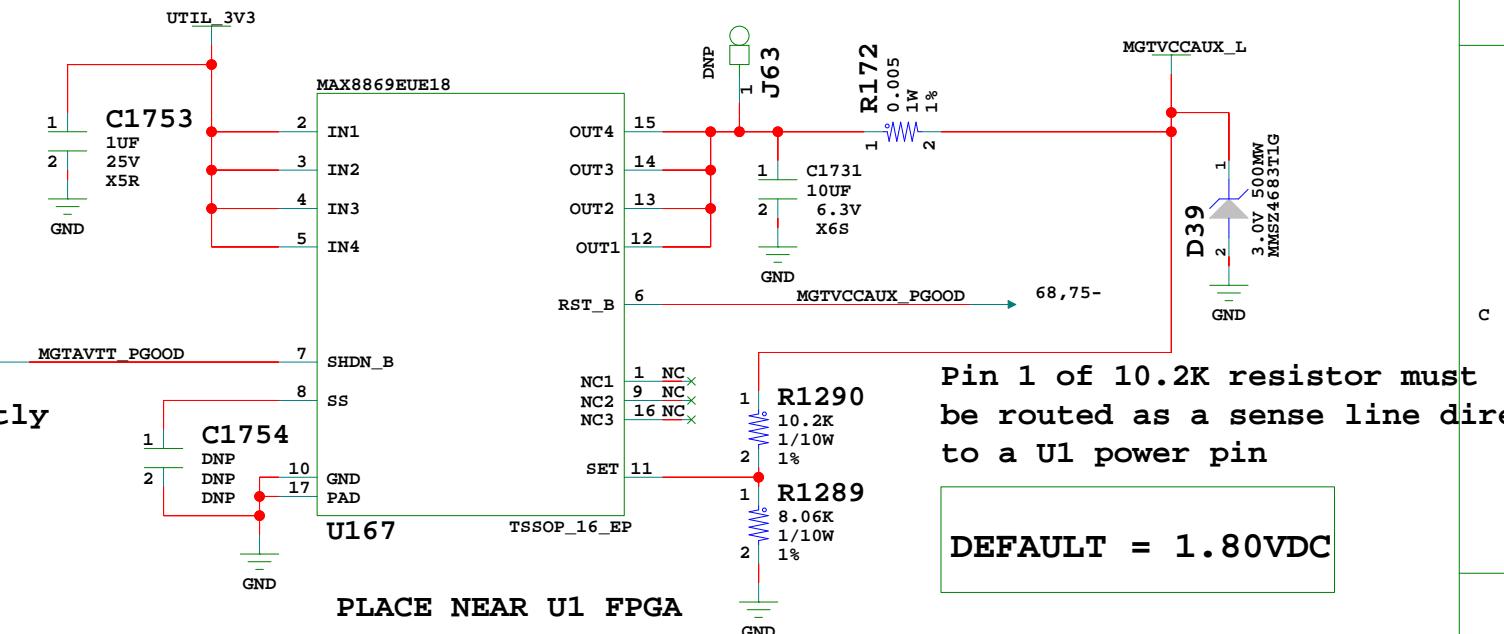
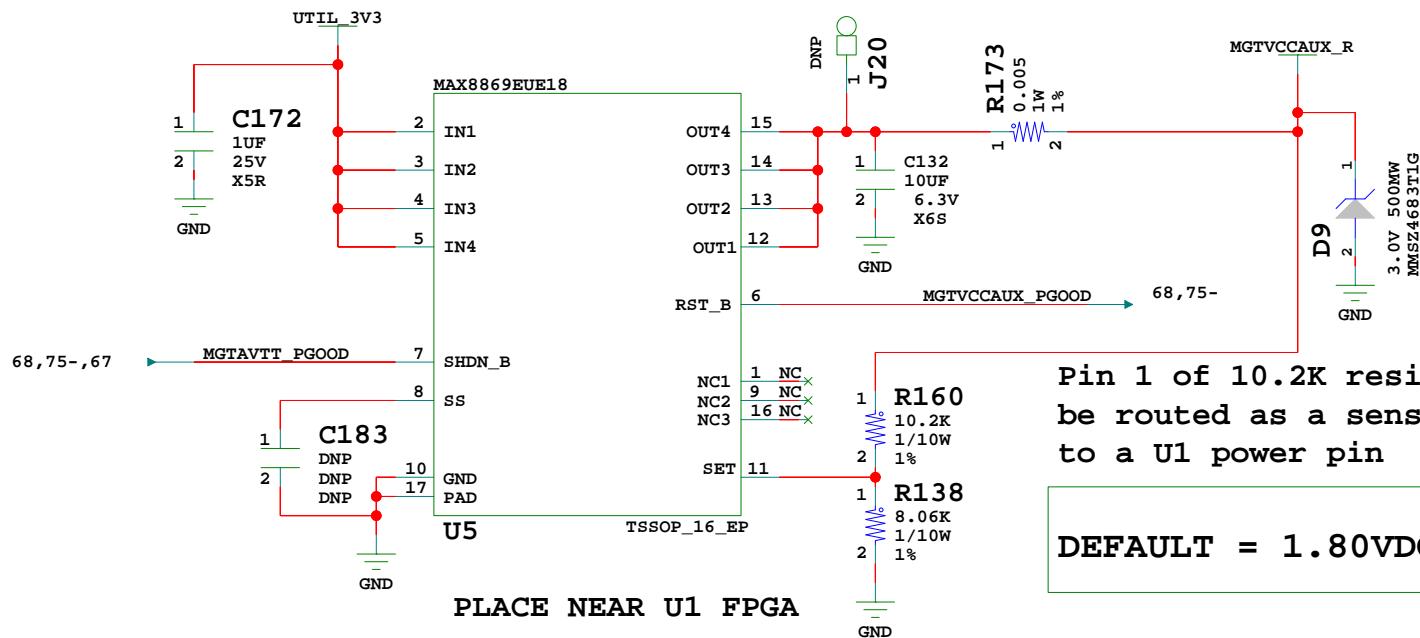












MGTVCCAUX 1A Regulator



TITLE: MGTVCCAUX 1A Regulator
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:37

VER: 1.1

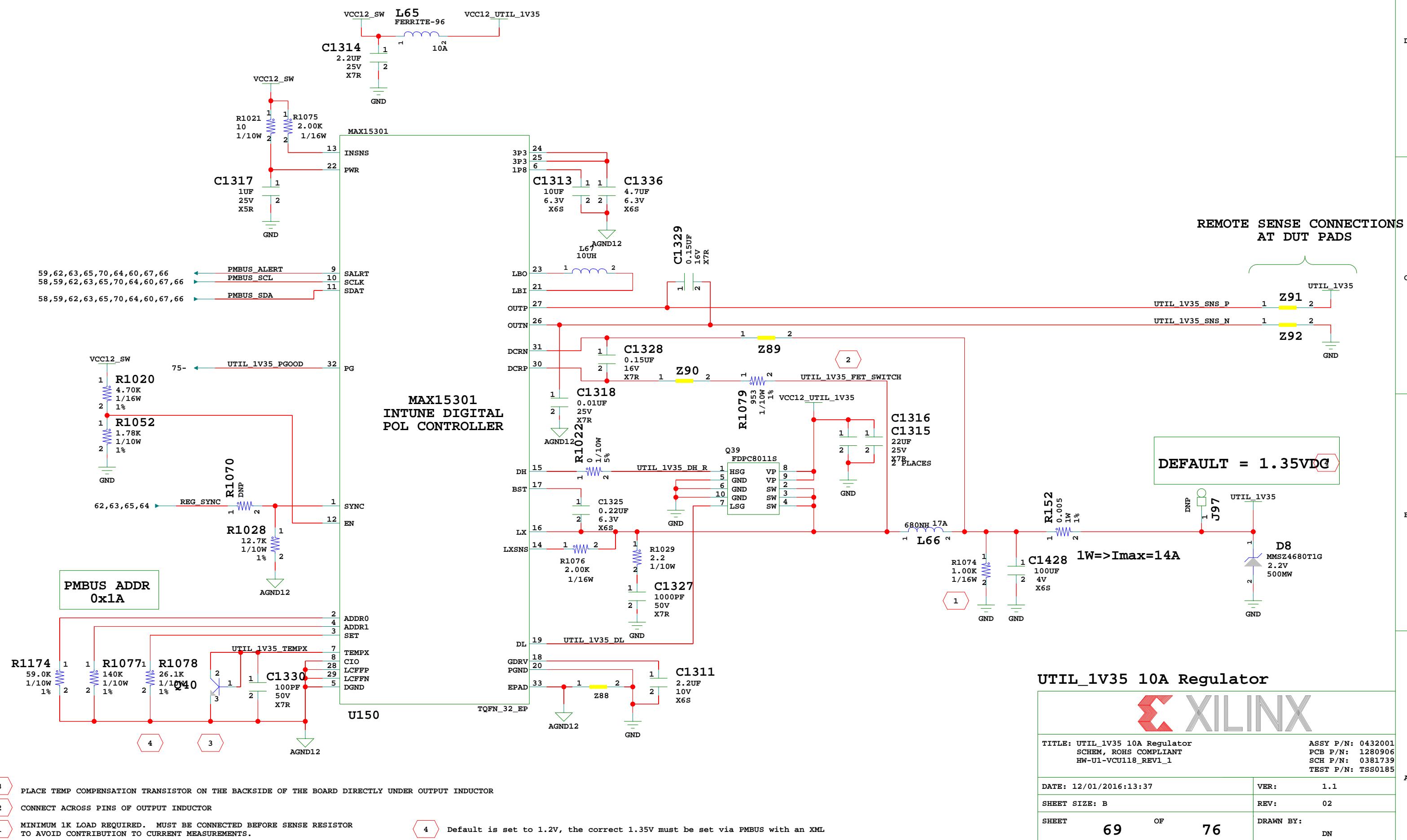
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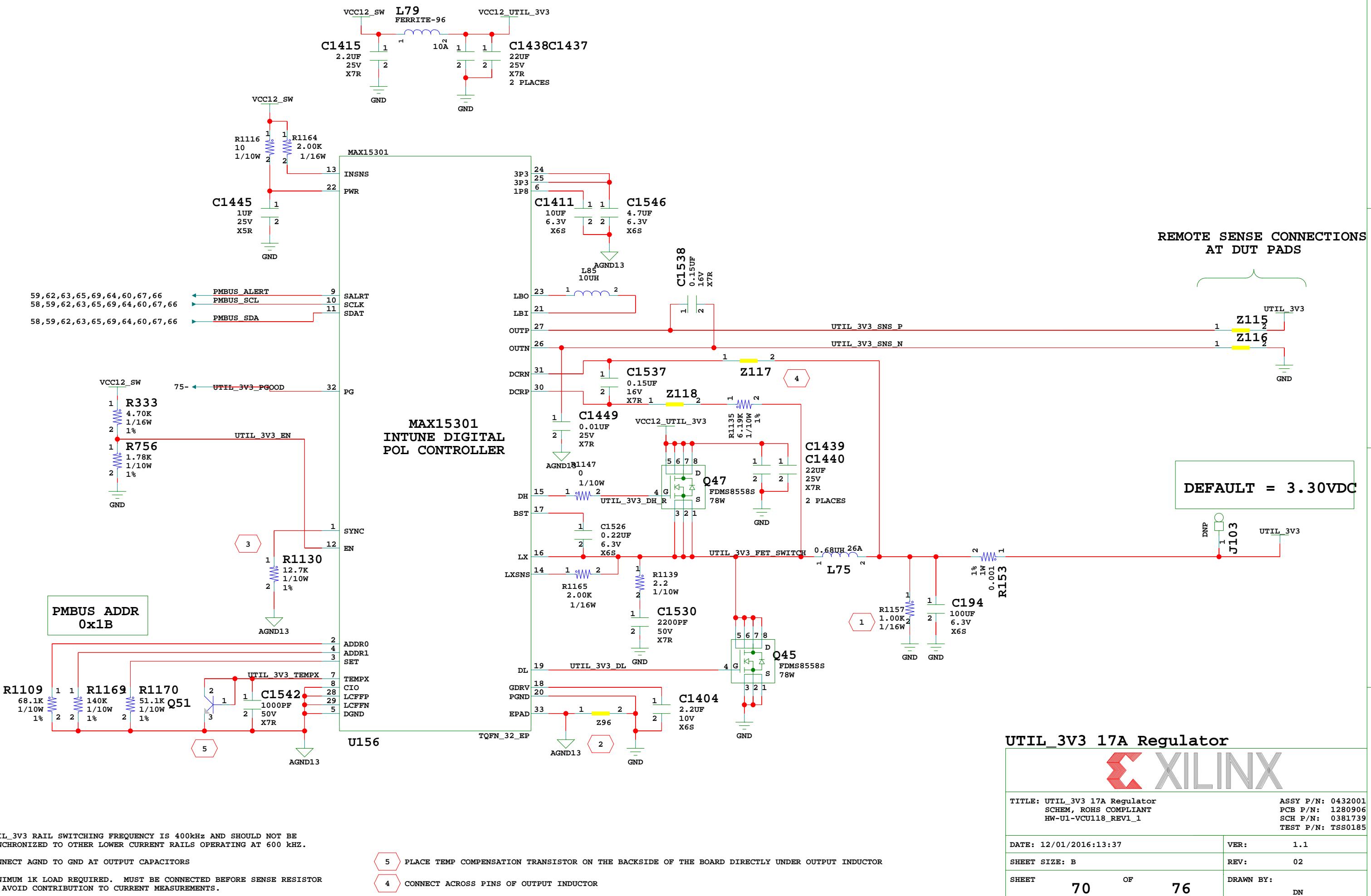
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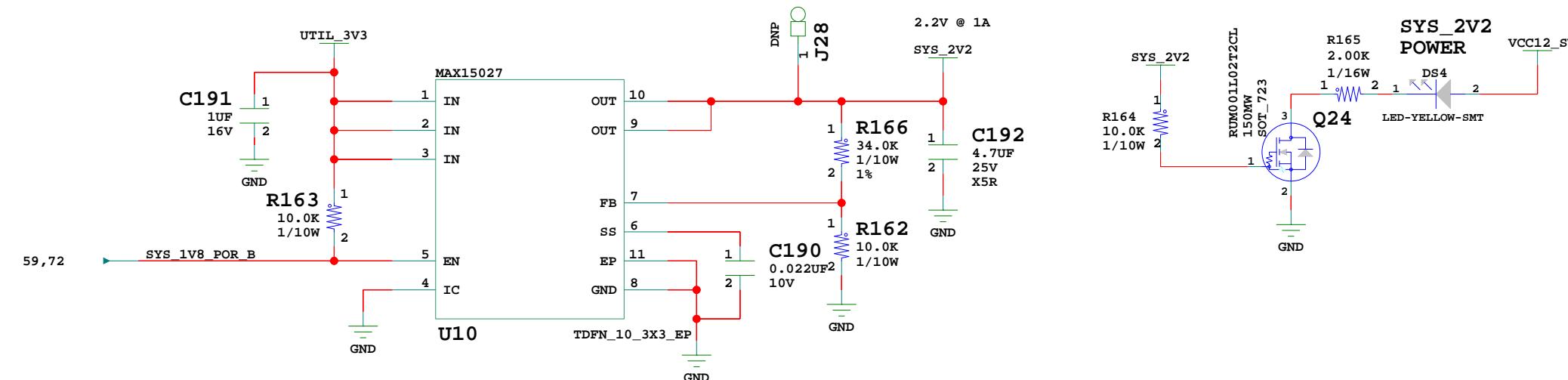
SHEET 68 OF 76

DRAWN BY:

DN







SYS_ 2V2 Regulator



**TITLE: SYS_ 2V2 Regulator
SCHEM, ROHS COMPLIANT
HW-U1-VCU118 REV1 1**

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016 13:37

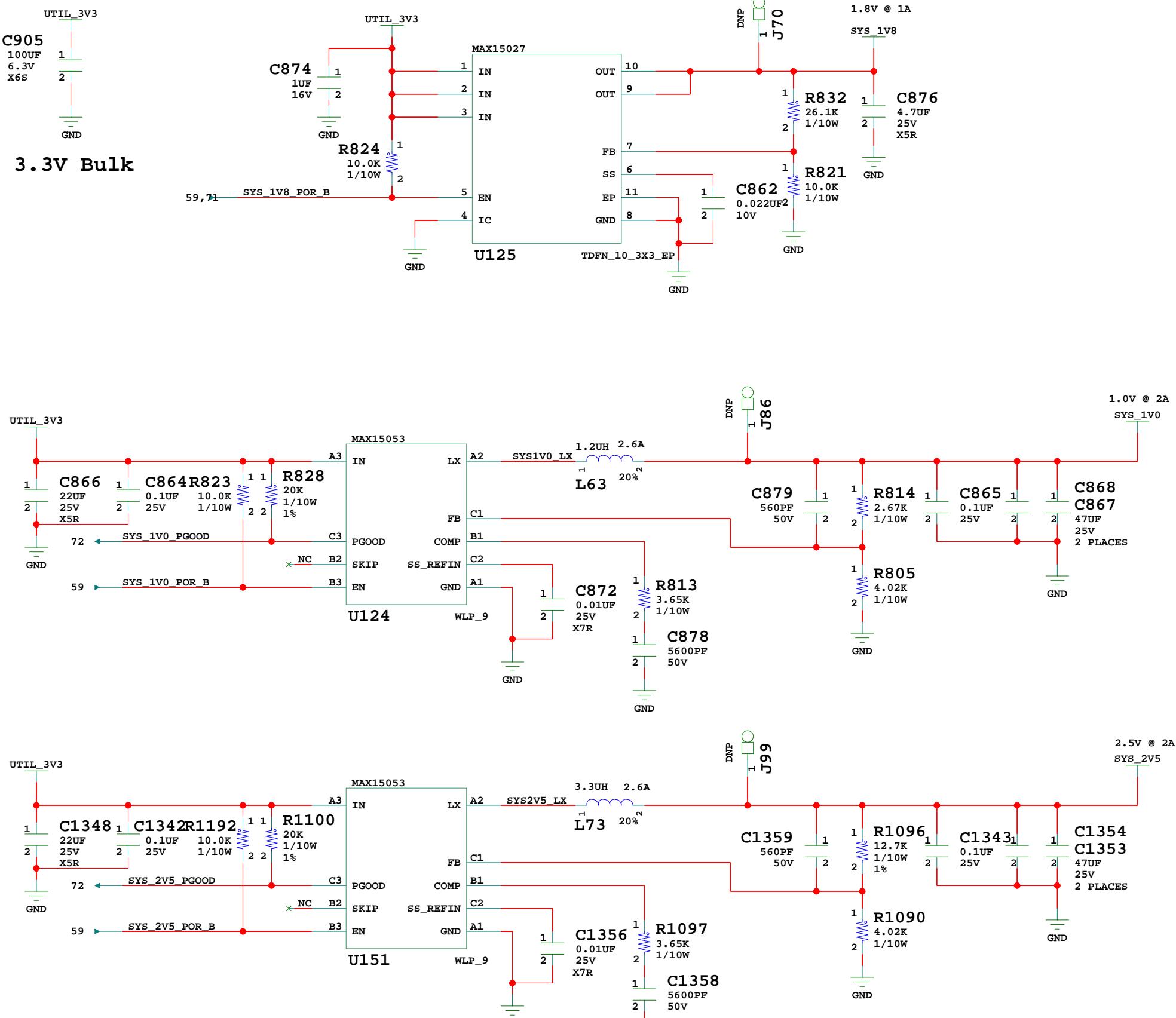
VERB: 1 1

SHEET SIZE: B

REV. 1

SHEET 71 OF 76

DRAWN BY:



SYS 2V5 SYS 1V8 SYS 1V0 Regulators

**TITLE: SYS_2V5 SYS_1V8 SYS_1V0 Regulators
SCHEM, ROHS COMPLIANT
HW-U1-VCU118 REV1 1**

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

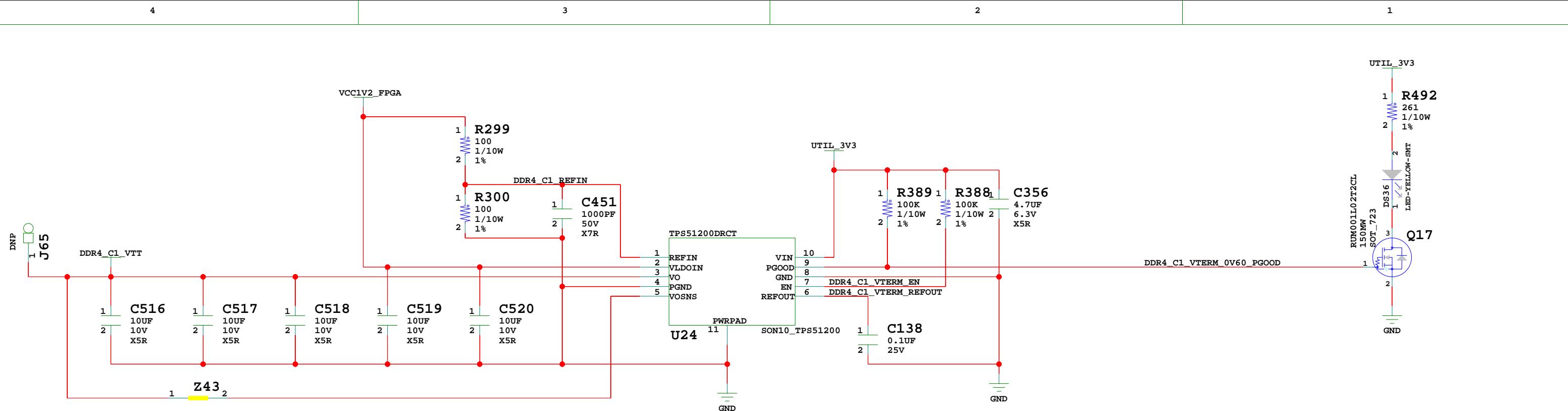
DATE: 13/01/2016 13:37

SHEET SIZE: B

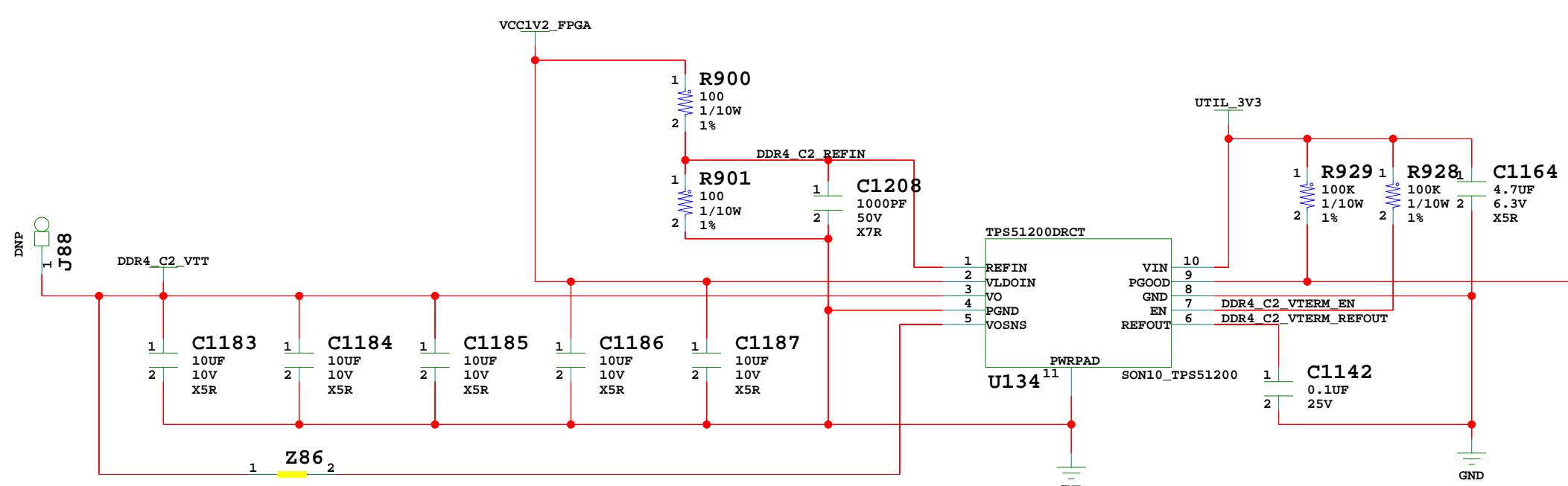
SHEET **OF** **DRAWN BY:**

72 76

1



Place sense near DDR4 C1 components



Place sense near DDR4 C2 components

DDR4 Termination Supplies

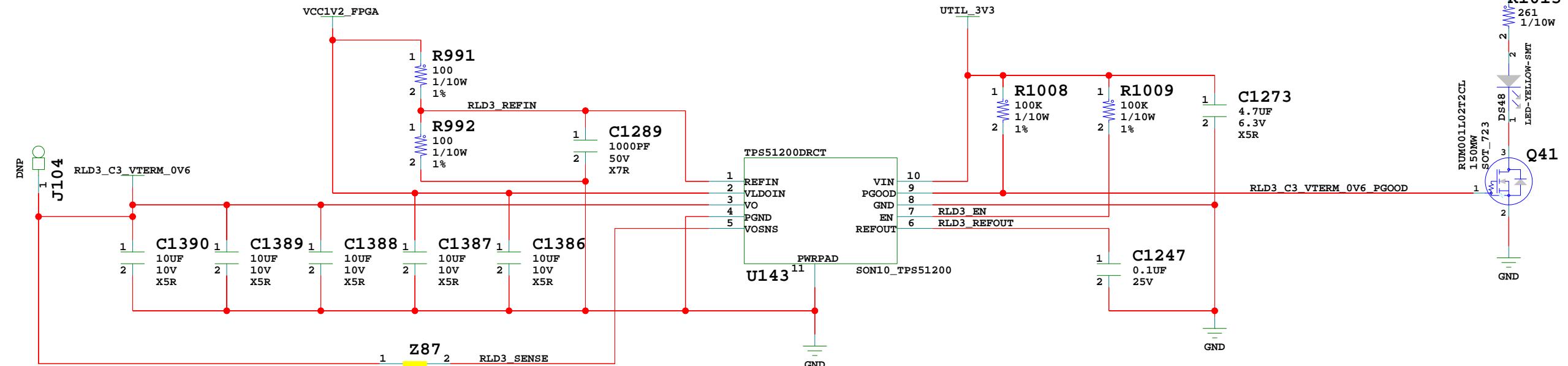


TITLE: DDR4 Termination Supplies
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:37	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 73 OF 76	DRAWN BY: DN

RLD3 C3 IF COMP. MEM. HP BANKs TERM. REGULATOR, 0.6V @ 3A



Place sense near RLD3 C3 components

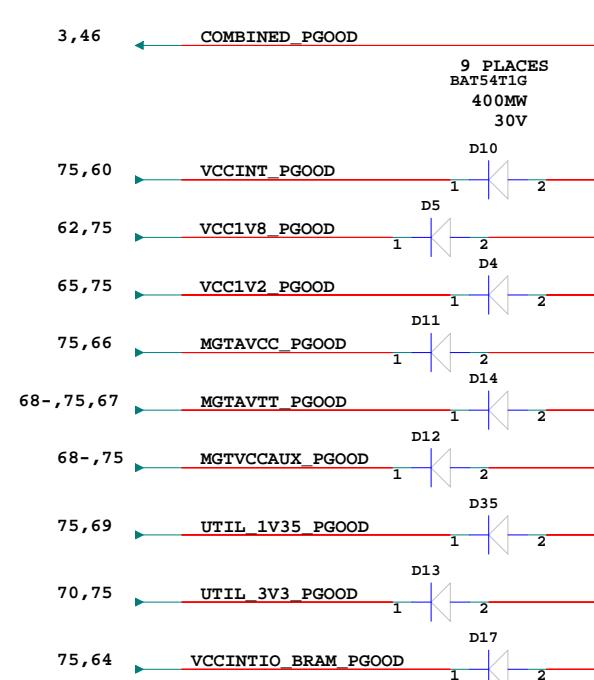
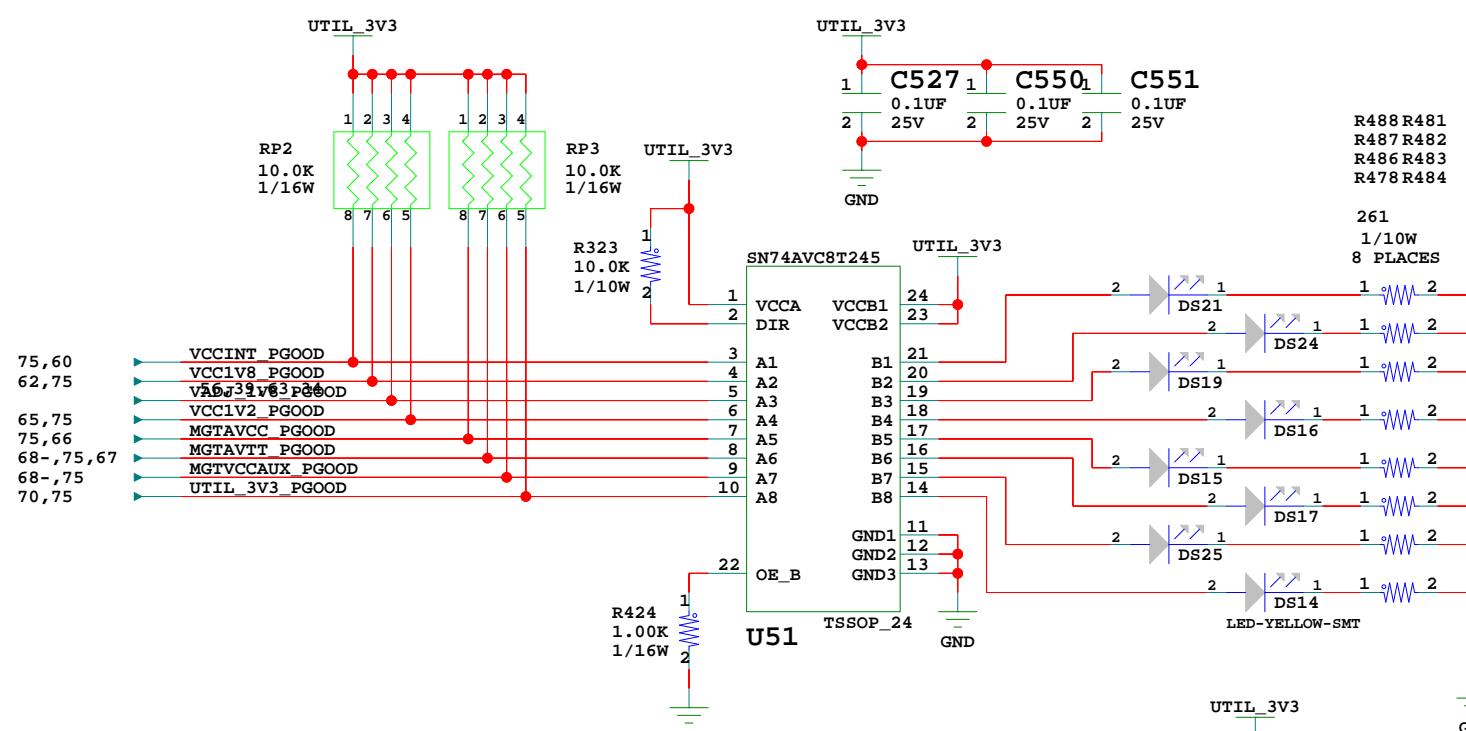
RLD3 Termination Supply



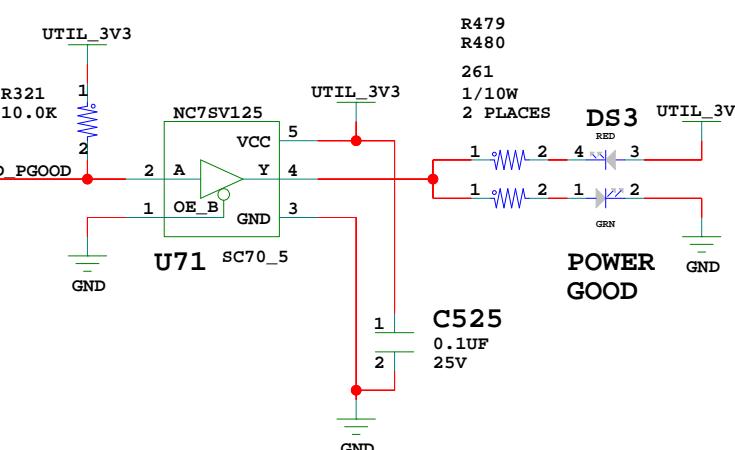
TITLE: RLD3 Termination Supply SCHEM, ROHS COMPLIANT HW-U1-VCU118_REV1_1		ASSY P/N: 0432001 PCB P/N: 1280906 SCH P/N: 0381739 TEST P/N: TSS0185
DATE: 12/01/2016:13:37	VER: 1.1	
SHEET SIZE: B	REV: 02	
SHEET 74 OF 76	DRAWN BY: DN	

DS19 must be labeled VADJ Power Good

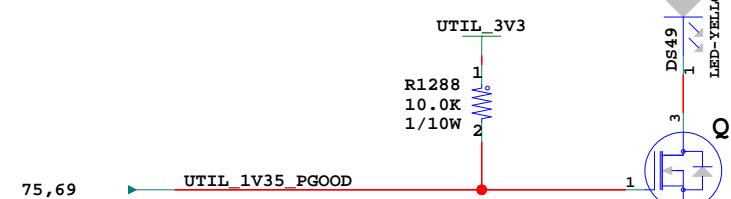
Place LEDs near top right corner of board



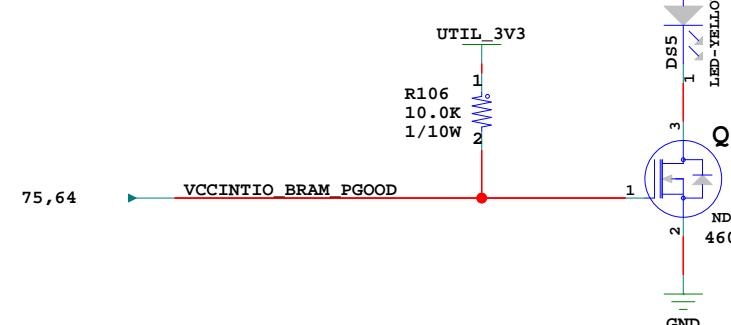
VADJ not included in POWER_GOOD logic



1V35 Power Good



VCCINTIO_BRAM Power Good



Power Status LEDs



TITLE: Power Status LEDs
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:37

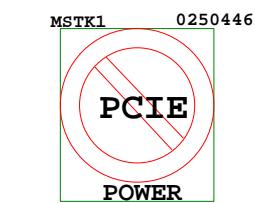
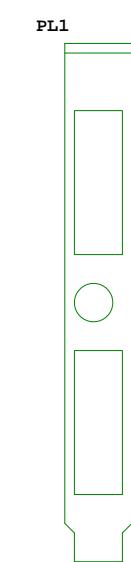
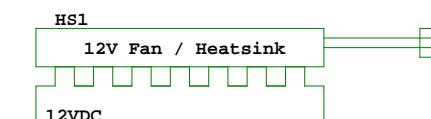
VER: 1.1

SHEET SIZE: B

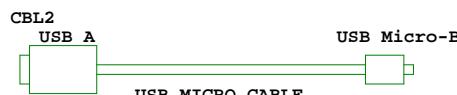
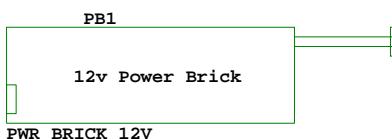
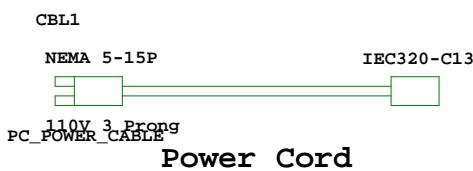
REV: 02

SHEET 75 OF 76

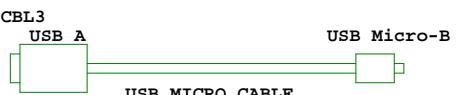
DRAWN BY: DN



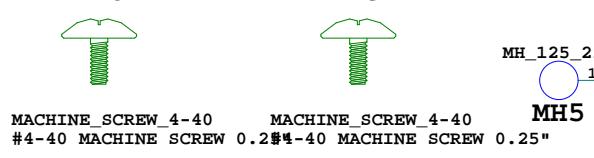
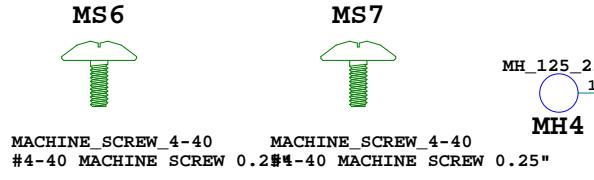
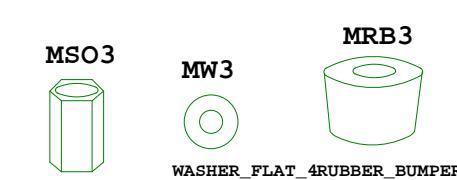
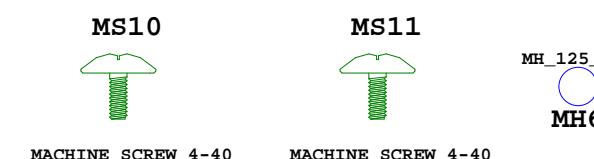
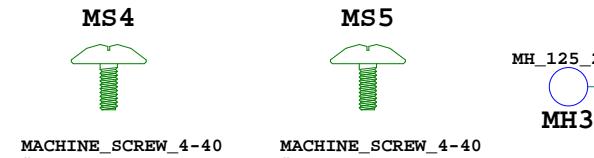
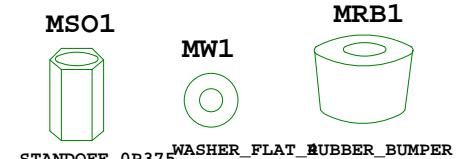
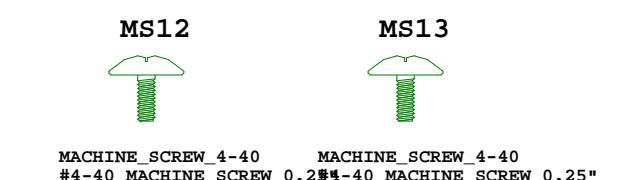
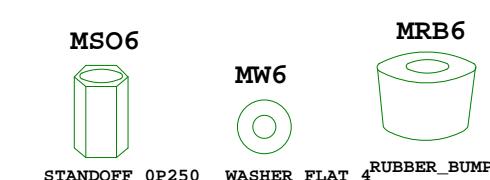
PCIE_POWER_STICKER



USB Micro-B Cable



USB Micro-B Cable



NOTE: The two standoffs above are shorter and must be connected to MH4 and MH5 to level the board properly

Mechanical Components



TITLE: Mechanical Components
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1

ASSY P/N: 0432001
PCB P/N: 1280906
SCH P/N: 0381739
TEST P/N: TSS0185

DATE: 12/01/2016:13:37

VER: 1.1

SHEET SIZE: B

REV: 02

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DRAWN BY: DN