Christopher Kniss

Curriculum Vitae

EDUCATION & APPOINTMENTS

Ph.D. in Electrical Engineering (Direct Ph.D. Program) University of Massachusetts Amherst Advisor: Dr. Rod Kim Research Assistantship **Status:** Accepted — Fall 2025 start

B.E. in Computer Engineering (with Highest Honors) Concentration: Electronics & Embedded Systems Minor: Physics Stevens Institute of Technology, Hoboken, NJ Cumulative GPA: 3.959 **Status:** Completed — May 2025

AWARDS & HONORS

- **Dean's List** — Stevens Institute of Technology
- **Edwin A. Stevens Scholarship** — Stevens Institute of Technology
- **Provost's Office Undergraduate Research Fund** — Stevens Institute of Technology

PROFESSIONAL MEMBERSHIPS

- **Tau Beta Pi** — Alpha Chapter
- **IEEE Eta Kappa Nu (HKN)**

WORK EXPERIENCE

NIST SURF Program Intern National Institute of Standards and Technology, Gaithersburg, MD — May 2025–August 2025

- Designed and developed PCBs in Altium Designer for cryogenic chamber mounting applications
- Characterized S-parameters and RF performance using vector network analyzers and oscilloscopes in cryogenic environments
- Operated probing stations and signal generators for precision measurements at temperatures from 10 K to 300 K
- Presented research findings at NIST SURF Colloquium to multidisciplinary audience of 50+ attendees

Undergraduate Research Assistant, SINE Lab Stevens Institute of Technology (Provost's Office of Undergraduate Research) — Jan 2024–May 2025

- Investigated economic trade-offs in RFIC design, fabrication, and implementation through ∼15 hours/week lab work
- Designed and simulated analog folding amplifier achieving 100 MHz operational bandwidth in Cadence
- Applied device physics principles to optimize transistor sizing and debug circuit performance
- Led weekly progress meetings and delegated tasks to 3 peers, accelerating project timeline by 2 weeks

Teaching Assistant, Electronic Circuits Course Stevens Institute of Technology — Sep–Dec 2023

- Designed and delivered weekly recitations covering circuit analysis and design for class of 44 students
- Maintained consistent attendance of 20–30 students (45–68% of class) through engaging problem-solving sessions
- Graded assignments and proctored exams, providing detailed feedback to support student learning

PUBLICATIONS

Temperature-Compensated Multi-Level CMOS Modulators Operating from 10 K to 300 K for Cryogenic Interconnects *Christopher Kniss, Abhishek Sharma, Ratanak Phon, Gregory Shimonov,*

Eran Socher, Pragya R. Shrestha, Karthick Ramu, Jason P. Campbell, Amin Pourvali Kakhki, Richard Al Hadi, Rod Kim IEEE Journal of Microwaves (JMW), October 2025

Summary:

- Designed and fabricated current-steering 2-bit modulator in 65 nm bulk CMOS achieving 13 Gb/s at 10 K with 1.18 pJ/b energy efficiency
- Implemented temperature compensation circuitry enabling operation across 10 K to 300 K range with 15.4 mW power consumption
- Demonstrated 150 GHz transmitter in 28 nm CMOS using same modulator scheme for high-performance computing applications
- Established contactless cryogenic-to-room-temperature connections achieving 8 Gb/s data rate
- Addressed thermal load vs. frequency-dependent attenuation trade-off in scalable quantum computing interconnects

Funding: Defense Advanced Research Projects Agency (DARPA) Grant D22AP00139

Ceramic Fiber Interconnects Beyond 1000° C Enabled by Automatic Gain Compensated Millimeter-Wave CMOS Transceivers *Abhishek Sharma, Christopher Kniss, Ratanak Phon, Rod Kim* 2025 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1–5, May 2025

Summary:

- Characterized S-parameters of hollow-core alumina fiber waveguides at temperatures up to 1100°C using vector network analyzer across 50–75 GHz range
- Quantified transmission stability, achieving <0.5 dB variation after 1 hour at 1100°C despite non-linear temperature dependence
- Integrated 57 GHz CMOS transceiver with automatic gain control loop to compensate for temperature-induced transmission variations
- Demonstrated high-speed communication link achieving 5 Gb/s at 1100°C for aerospace and geothermal applications

RESEARCH ACTIVITY

Analog Folding Amplifier Operational up to 100 MHz Stevens Institute of Technology — May 2024–Present

- Designed and simulated folding amplifier topology in Cadence achieving 100 MHz bandwidth with low distortion
- Applied device physics analysis to optimize transistor sizing and debug non-ideal circuit behavior
- Presented research findings via poster presentation to faculty and peers at Stevens Institute of Technology

High-Temperature Alumina Fiber Waveguide Stevens Institute of Technology — Sep–Dec 2023

- Conducted extreme temperature experiments characterizing waveguide performance up to 1100°C
- Measured S-parameters using vector network analyzer to quantify transmission loss and stability
- Demonstrated experimental setup and results at iCNS Launch Event to multidisciplinary audience

TECHNICAL PROJECTS

High-Performance Computing Server Design University of Massachusetts Amherst — September 2025

- Designed and optimized component selection for $42K lab server supporting 3 concurrent HFSS and Cadence users
- Configured system architecture to enable large-scale electromagnetic and circuit simulations

- Increased lab productivity by eliminating computational bottlenecks in simulation workflows

CONFERENCES & PRESENTATIONS

Inaugural Riccio College of Engineering Innovation Day University of Massachusetts Amherst — November 17, 2025

- Presented poster on temperature-compensated cryogenic CMOS modulators during student networking session

NIST SURF Colloquium National Institute of Standards and Technology, Gaithersburg, MD — July 2025

- Delivered oral presentation on cryogenic PCB design and lab instrumentation to 50+ researchers
- Communicated technical findings to broad scientific audience spanning multiple disciplines

Folding Amplifier Poster Presentation Stevens Institute of Technology, Hoboken, NJ — Spring 2025

- Presented analog folding amplifier design achieving 100 MHz operation to faculty and peer reviewers

iCNS Launch Event Demonstration Stevens Institute of Technology, Hoboken, NJ — Fall 2023

- Demonstrated alumina waveguide characterization at 1100°C with live VNA measurements

COURSEWORK

Graduate Core (UMass Amherst):

- **E&C-ENG 606 Electromagnetic Field Theory**: Electromagnetic fields in dielectric and lossy media, transmission lines, antennas and resonators treated with concepts of duality, image theory, reciprocity, and integral equations; boundary and initial value problems for frequently encountered symmetries

Undergraduate Core (Stevens):

- **Senior Design Project**: Speaker Spine — brand-agnostic smart home audio system (team of 6)
- **Electronics Design**: Intro. VLSI Design, Electronic Circuits, Design of Dynamical Systems, Digital System Design
- **Device Physics**: Electromagnetism, Gen. Chem. II, Thermodynamics, Design with Materials, Quantum Mechanics w.E.A.
- **Embedded Systems**: Digital & Comp. Sys. Architecture, Real-Time & Embedded Sys., Microprocessor Systems, Computational Data Structures and Algorithms, Information Sys. Engineering I

SKILLS

- **Software:** Cadence, Git, Altium Designer, Renesas E2 Studio, MATLAB, Vivado, Arduino, SolidWorks, MS Office
- **Programming:** C and C++ (Experienced), Linux CLI, VHDL, x86 and ARMv8 Assembly, Java (Proficient)