

# Christopher Kniss

*Curriculum Vitae*

## EDUCATION & APPOINTMENTS

---

**Ph.D. in Electrical Engineering (Direct Ph.D. Program)** University of Massachusetts Amherst

Advisor: Dr. Rod Kim

Research Assistantship

**Status:** Accepted — Fall 2025 start

**B.E. in Computer Engineering (with Highest Honors)** Concentration: Electronics & Embedded Systems

Minor: Physics

Stevens Institute of Technology, Hoboken, NJ

Cumulative GPA: 3.959

**Status:** Completed — May 2025

## AWARDS & HONORS

---

- **Dean's List** — Stevens Institute of Technology
- **Edwin A. Stevens Scholarship** — Stevens Institute of Technology
- **Provost's Office Undergraduate Research Fund** — Stevens Institute of Technology

## PROFESSIONAL MEMBERSHIPS

---

- **Tau Beta Pi** — Alpha Chapter
- **IEEE Eta Kappa Nu (HKN)**

## WORK EXPERIENCE

---

**Teaching Assistant, Electronic Circuits Course** Stevens Institute of Technology — Sep–Dec 2023

- Hosted optional recitations, graded, and proctored exams for a class of 44 students.
- Crafted practice problems and planned recitations that reviewed important course content.
- Optional attendance was consistently 20–30 students.

**Status:** Completed — Dec 2023

**Undergraduate Research Assistant, SINE Lab (Provost's Office of Undergraduate Research)**

Stevens Institute of Technology — Jan 2024–May 2025

- Contributed ~15 hours/week in-person lab work and weekly meetings.
- Studied economic implications in RFIC design, fabrication, and implementation.

**Status:** Completed — May 2025

**NIST SURF Program Intern** Gaithersburg Campus, Maryland — May 2025–August 2025

- Developed PCBs in Altium Designer to be mounted in cryogenic chambers.
- Gained experience with probing stations, VNAs, oscilloscopes, and signal generators.
- Enhanced lab skills for use in cryogenic and non-cryogenic environments.
- **Related Presentation:** NIST SURF Colloquium — July 2025

**Status:** Completed — August 2025

## RESEARCH ACTIVITY

---

**Analog Folding Amplifier Operational up to 100 MHz** — May 2024–Present

- Practiced poster presentation skills.
- Designed amplifier prototype and simulated in Cadence.
- Improved independent study, circuit design, and project management skills.
- Applied device physics to debugging and transistor sizing.
- Frequent meetings with Dr. Rod Kim; delegated tasks to peers for progress acceleration.
- **Related Presentation:** Poster Presentation — Spring 2025, Stevens Institute of Technology

**Status:** Ongoing — since May 2024

### High-Temperature Alumina Fiber Waveguide — Sep–Dec 2023

- Conducted extreme temperature experiments up to 1100°C.
- Characterized S-parameters using a vector network analyzer.
- Performed lab demos and presentations of the project.
- **Related Presentation:** iCNS Launch Event Demo — Fall 2023

**Status:** Completed — Dec 2023

## TECHNICAL PROJECTS

---

### High-Performance Computing Server Design

- Designed and optimized component selection for a \$42K lab server
- Configured to support **3 concurrent users** running HFSS and Cadence workflows
- Increased lab productivity and enabled large-scale simulations

**Status:** Completed — Week of Sept 8, 2025

## PUBLICATIONS

---

**Temperature-Compensated Multi-Level CMOS Modulators Operating from 10 K to 300 K for Cryogenic Interconnects** *Christopher Kniss, Abhishek Sharma, Ratanak Phon, Gregory Shimonov, Eran Socher, Pragya R. Shrestha, Karthick Ramu, Jason P. Campbell, Amin Pourvali Kakhki, Richard Al Hadi, Rod Kim*

IEEE Journal of Microwaves (JMW), IEEE

Affiliations: University of Massachusetts Amherst; National Institute of Standards and Technology (NIST); Indian Institute of Technology Jodhpur; Tel Aviv University; École de technologie supérieure, Montreal

**Status:** Published — October 2025

#### Summary:

- Presents temperature-compensated cryogenic CMOS modulators operating from **10 K to 300 K** for cryogenic communications.
- Addresses limitations of conventional metal-based coax cables (thermal load vs. frequency-dependent attenuation trade-off).
- Motivated by demand for scalable cryogenic interconnects in **high-performance computing** and **quantum computing**.
- Implemented a **current-steering 2-bit modulator** in 65 nm bulk CMOS:
  - Achieved **13 Gb/s** at 10 K with **15.4 mW** power under 1.2 V supply.
  - Energy efficiency: **1.18 pJ/b**.
- Demonstrated **150 GHz transmitter** in 28 nm CMOS with same modulator scheme.
- Established **contactless connections** between 10 K and 300 K systems, achieving **8 Gb/s**.

**Keywords:** Contactless Connection, Cryogenic Interface, CMOS, Millimeter-Wave, Modulator, Multi-Level Signaling, Temperature Compensation

**Funding Acknowledgments:** Supported by the Defense Advanced Research Projects Agency (DARPA) Grant D22AP00139.

**Ceramic Fiber Interconnects Beyond 1000° C Enabled by Automatic Gain Compensated Millimeter-Wave CMOS Transceivers** *Abhishek Sharma, Christopher Kniss, Ratanak Phon, Rod Kim*  
2025 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1–5

Publisher: IEEE

**Status:** Published — May 25, 2025

**Summary:**

- Investigates hollow-core ceramic (alumina) fiber for millimeter-wave communications at temperatures up to 1100°C.
- Measured EM wave propagation through alumina fiber across 50–75 GHz range at high temperatures.
- Found transmission magnitude decreases non-linearly with temperature but remains stable (<0.5 dB variation) after one hour at 1100°C.
- Paired fiber with a 57 GHz CMOS transceiver to demonstrate a high-speed communication link at high temperatures.
- Implemented automatic gain control loop in the receiver chain to compensate for temperature-related transmission variations.
- Achieved a **data rate of 5 Gb/s** at extreme operating conditions.

**Applications:** Aerospace, avionics, geothermal systems, and other extreme environment electronics.

## CONFERENCES & PRESENTATIONS

---

**Inaugural Riccio College of Engineering Innovation Day — November 17, 2025** *Type:* Poster Presentation

University of Massachusetts Amherst

- Presented recent research paper during the student poster and networking session.

**Status:** Completed — November 2025

**NIST SURF Colloquium Presentation — July 2025** *Type:* Oral Presentation

Gaithersburg, MD

- Presented research conducted during the NIST SURF Program internship.
- Focused on cryogenic PCB design and lab instrumentation.
- Practiced technical communication with a broad scientific audience.
- [View Presentation](#)

**Status:** Completed — July 2025

**Poster Presentation — Folding Amplifier Project — Spring 2025** *Type:* Poster Presentation

Stevens Institute of Technology, Hoboken, NJ

- Presented the design and development of an analog folding amplifier operational up to 100 MHz.
- Shared project outcomes with peers and faculty, strengthening presentation skills and technical discussion.
- [View Poster](#)

**Status:** Completed — Spring 2025

**iCNS Launch Event Demo — High-Temperature Alumina Fiber Waveguide — Fall 2023** *Type:* Demonstration / Poster Presentation

Stevens Institute of Technology, Hoboken, NJ

- Performed lab demonstration of alumina waveguide experiments at extreme temperatures (up to 1100°C).

- Presented data collection and VNA characterization results to a multidisciplinary audience.

**Status:** Completed — Sep–Dec 2023

## COURSEWORK

---

### Graduate Core (UMass Amherst):

- **E&C-ENG 606 Electromagnetic Field Theory:** Electromagnetic fields in dielectric and lossy media, transmission lines, antennas and resonators treated with the concepts of duality, image theory, reciprocity, integral equations and other techniques. Boundary and initial value problems solved for several frequently encountered symmetries.

### Undergraduate Core (Stevens):

- **Senior Design Project:** Speaker Spine, a brand-agnostic smart home audio system (team of 6).
- **Electronics Design:** Intro. VLSI Design, Electronic Circuits, Design of Dynamical Systems, Digital System Design.
- **Device Physics:** Electromagnetism, Gen. Chem. II, Thermodynamics, Design with Materials, Quantum Mechanics w.E.A.
- **Embedded Systems:** Digital & Comp. Sys. Architecture, Real-Time & Embedded Sys., Microprocessor Systems, Computational Data Structures and Algorithms, Information Sys. Engineering I.

## SKILLS

---

- **Software:** Cadence, Git, Altium Designer, Renesas E2 Studio, MATLAB, Vivado, Arduino, SolidWorks, MS Office.
- **Programming:** C and C++ (Experienced), Linux CLI, VHDL, x86 and ARMv8 Assembly, Java (Proficient).