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Lab assignment#02

Subject: Digital & Logic design

Presented to: Sir Sarmad Hassan

Question no:01

A. Design a Half Adder and Full Adder using 74153 IC.

Let truth table variables are

A= Selection input

B= Input S=Sum

C= Carry

Truth table of Half Adder:

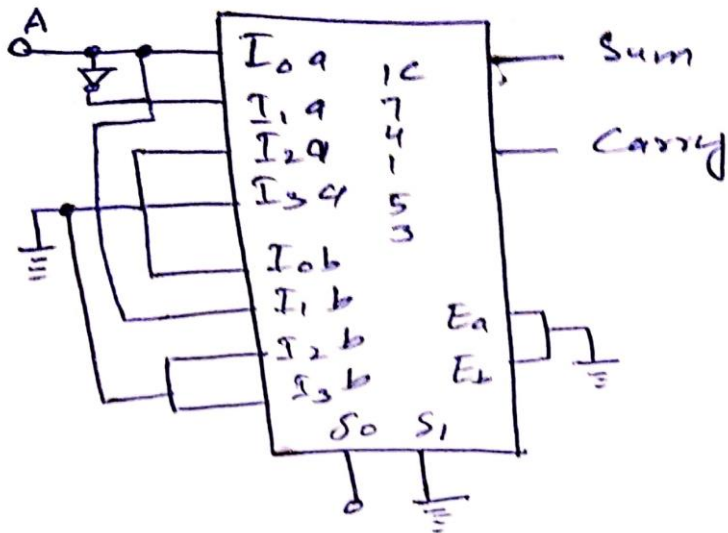
| A | B | S | C | N1 | N2 |
|---|---|---|---|----|----|
| 0 | 0 | 0 | 0 | B | 0 |
| 0 | 1 | 1 | 0 | | |
| 1 | 0 | 1 | 0 | B' | B |
| 1 | 1 | 0 | 1 | | |

Truth table of Full Adder:

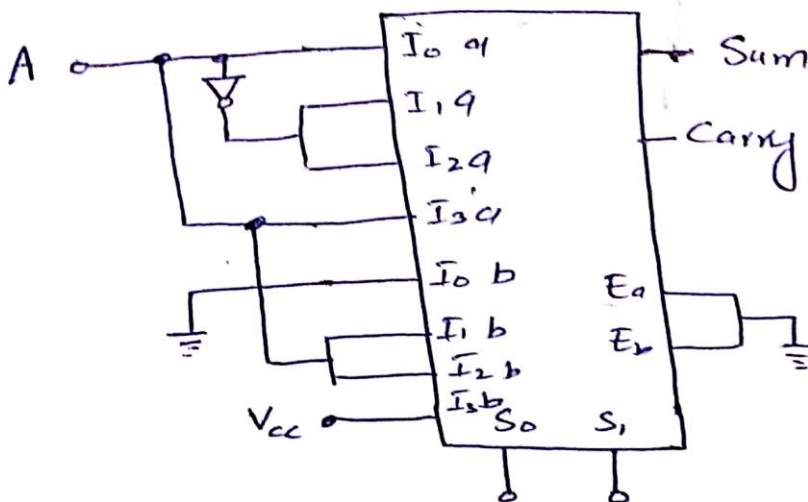
| A | B | C | S | Carry | N1 | N2 |
|---|---|---|---|-------|----|----|
| 0 | 0 | 0 | 0 | 0 | C | 0 |
| 0 | 0 | 1 | 1 | 0 | | |
| 0 | 1 | 0 | 1 | 0 | C' | C |
| 0 | 1 | 1 | 0 | 1 | | |
| 1 | 0 | 0 | 1 | 0 | C' | C |
| 1 | 0 | 1 | 0 | 1 | | |
| 1 | 1 | 0 | 0 | 1 | C | 1 |
| 1 | 1 | 1 | 1 | 1 | | |

Designing logic circuit of Half & Full Adder using IC:

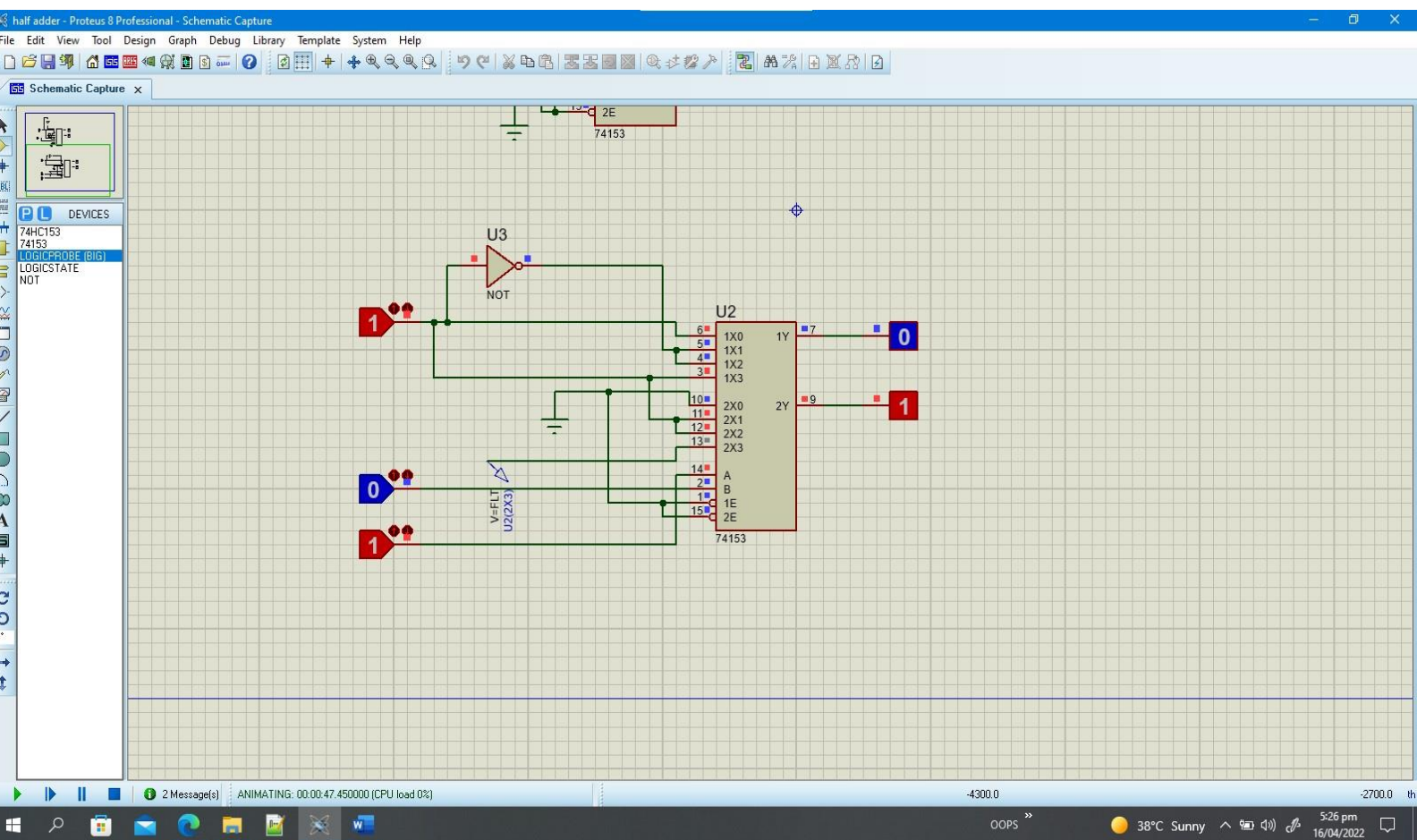
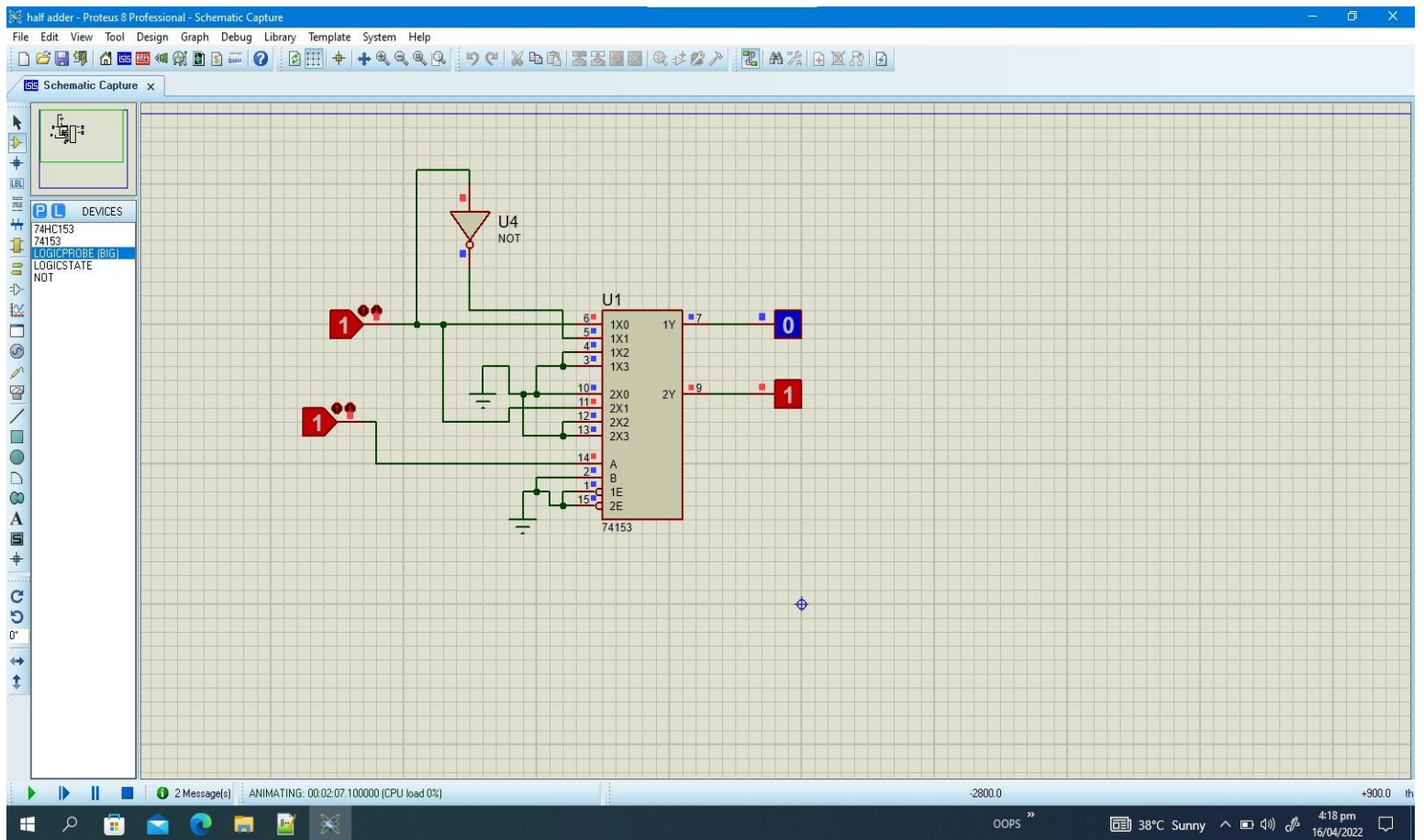
Half Adder:



Full Adder



Implemented circuit of Half Adder & Full Adder on Proteus:



B. Design a Half and Full Subtractor using 74153 IC.

Truth table of Half Subtractor:

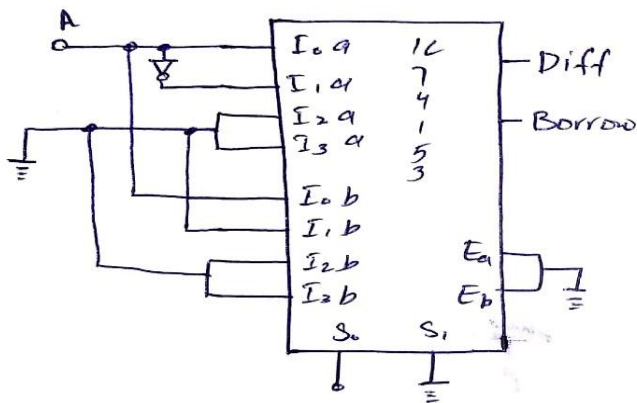
| A | B | difference | Carry | N1 | N2 |
|---|---|------------|-------|----|----|
| 0 | 0 | 0 | 0 | B | B |
| 0 | 1 | 1 | 1 | | |
| 1 | 0 | 1 | 0 | B' | 0 |
| 1 | 1 | 0 | 0 | | |

Truth table of Full Subtractor:

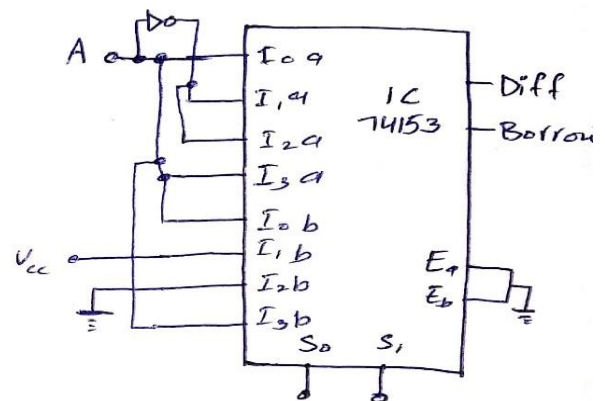
| A | B | C | Difference | Carry | N1 | N2 |
|---|---|---|------------|-------|----|----|
| 0 | 0 | 0 | 0 | 0 | C | C |
| 0 | 0 | 1 | 1 | 1 | | |
| 0 | 1 | 0 | 1 | 1 | C' | 1 |
| 0 | 1 | 1 | 0 | 1 | | |
| 1 | 0 | 0 | 1 | 0 | C' | 0 |
| 1 | 0 | 1 | 0 | 0 | | |
| 1 | 1 | 0 | 0 | 0 | C | C |
| 1 | 1 | 1 | 1 | 1 | | |

Logic Diagram of Half & Full Subtractor:

Half Subtractor :



Full Subtractor



Output of Half & Full Subtractor on Proteus:

