Console Interface (relational instructions) –

```
Register file contents after 1 clock cycles:

zero: 00000000 at: 00000000 v0: 00000000 v1: 00000000 a0: 00000000
a1: 00000000 a2: 00000000 a3: 00000000 t0: 00000000 t1: 00000000
t2: 00000000 t3: 00000000 t4: 00000000 t5: 00000000 t6: 00000000
t7: 00000000 s0: 00000000 s1: 00000000 s2: 00000000 s3: 00000000
s4: 00000000 s5: 00000000 s6: 00000000 s7: 00000000 t8: 00000000
t9: 00000000 k0: 00000000 k1: 00000000 gp: 00000000 sp: 00000000
fp: 00000000 ra: 00000000


Register file contents after 2 clock cycles:

zero: 00000000 at: 00000000 v0: 00000000 v1: 00000000 a0: 00000000
a1: 00000000 a2: 00000000 a3: 00000000 t0: 00000000 t1: 00000000
t2: 00000001 t3: 00000000 t4: 00000000 t5: 00000000 t6: 00000000
t7: 00000000 s0: 00000000 s1: 00000000 s2: 00000000 s3: 00000000
s4: 00000000 s5: 00000000 s6: 00000000 s7: 00000000 t8: 00000000
t9: 00000000 k0: 00000000 k1: 00000000 gp: 00000000 sp: 00000000
fp: 00000000 ra: 00000000


Register file contents after 3 clock cycles:

zero: 00000000 at: 00000000 v0: 00000000 v1: 00000000 a0: 00000000
a1: 00000000 a2: 00000000 a3: 00000000 t0: 00000000 t1: 00000000
t2: 00000001 t3: 00000000 t4: 00000000 t5: 00000000 t6: 00000000
t7: 00000000 s0: 00000000 s1: 00000000 s2: 00000000 s3: 00000000
s4: 00000000 s5: 00000000 s6: 00000000 s7: 00000000 t8: 00000000
t9: 00000000 k0: 00000000 k1: 00000000 gp: 00000000 sp: 00000000
fp: 00000000 ra: 00000000


Register file contents after 4 clock cycles:

zero: 00000000 at: 00000000 v0: 00000000 v1: 00000000 a0: 00000000
a1: 00000000 a2: 00000000 a3: 00000000 t0: 00000000 t1: 00000001
t2: 00000001 t3: 00000000 t4: 00000000 t5: 00000000 t6: 00000000
t7: 00000000 s0: 00000000 s1: 00000000 s2: 00000000 s3: 00000000
s4: 00000000 s5: 00000000 s6: 00000000 s7: 00000000 t8: 00000000
t9: 00000000 k0: 00000000 k1: 00000000 gp: 00000000 sp: 00000000
fp: 00000000 ra: 00000000
```

```
Register file contents after 3 clock cycles:

zero: 00000000 at: 00000000 v0: 00000000 v1: 00000000 a0: 00000000
a1: 00000000 a2: 00000000 a3: 00000000 t0: 00000000 t1: 00000000
t2: 00000001 t3: 00000000 t4: 00000000 t5: 00000000 t6: 00000000
t7: 00000000 s0: 00000000 s1: 00000000 s2: 00000000 s3: 00000000
s4: 00000000 s5: 00000000 s6: 00000000 s7: 00000000 t8: 00000000
t9: 00000000 k0: 00000000 k1: 00000000 gp: 00000000 sp: 00000000
fp: 00000000 ra: 00000000


Register file contents after 4 clock cycles:

zero: 00000000 at: 00000000 v0: 00000000 v1: 00000000 a0: 00000000
a1: 00000000 a2: 00000000 a3: 00000000 t0: 00000000 t1: 00000001
t2: 00000001 t3: 00000000 t4: 00000000 t5: 00000000 t6: 00000000
t7: 00000000 s0: 00000000 s1: 00000000 s2: 00000000 s3: 00000000
s4: 00000000 s5: 00000000 s6: 00000000 s7: 00000000 t8: 00000000
t9: 00000000 k0: 00000000 k1: 00000000 gp: 00000000 sp: 00000000
fp: 00000000 ra: 00000000


Register file contents after 5 clock cycles:

zero: 00000000 at: 00000000 v0: 00000000 v1: 00000000 a0: 00000000
a1: 00000000 a2: 00000000 a3: 00000000 t0: 00000000 t1: 00000001
t2: 00000001 t3: 00000000 t4: 00000000 t5: 00000000 t6: 00000000
t7: 00000000 s0: 00000000 s1: 00000000 s2: 00000000 s3: 00000000
s4: 00000000 s5: 00000000 s6: 00000000 s7: 00000000 t8: 00000000
t9: 00000000 k0: 00000000 k1: 00000000 gp: 00000000 sp: 00000000
fp: 00000000 ra: 00000000


Total clock cycles: 5

Number of instructions executed for each type are given below:-
add: 0, addi: 1, beq: 1, bne: 0, j: 2
lw: 0, mul: 0, slt: 1, sub: 0, sw: 0
Program executed successfully!
```