**Pipeline**

1. Let A(P)=B(Q) A(P)≠A(Q) C(P)=D(Q) ES19PL

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| A | B | C | D | E | Notation: A(P)=B(Q) means that execution of program A on architecture P and execution of program B on architecture Q has same effect.  Write final values of b, c and d when program E is executed on architecture P. Let initially a=57. |
| a=g+k  b=g+d  g=a\*b  d=b-a  k=d\*g | k=d\*g  a=g+k  g=a\*b  b=g+d  d=b-a | a=12+g  b=a+9  g=a+b  d=a\*b  u=b+d | g=a+b  a=12+g  b=a+9  d=a\*b  u=b+d | a=a+129  b=a+523  c=a+924  d=a+428  print(b,c,d) |

1. Pipeline of an architecture appears as following: In unit time an instruction is fetched then nothing is done for 63 unit time. Then in unit time operands are fetched. How many instructions are bypassed?

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| IF | nop-63 | FO | nop-87 | CP | nop-49 | ST | Give reason as given in following example. |

Example: when nop are 12, 17, 17 then 36 bypass.

Reason: The first instruction is done during 0<t<50. The 38th instruction starts at t=37. It fetches its operands at t=50. The effect of first instruction is visible. But not visible to 37th instruction. MS19PL

1. Let a=12 b=3 c=19 d=41 x=a\*b y=p1+c z=q1p2 w=p2q3 u=dr2. What are final values of x, y, z, w and u? Notation: pi means the value of register ‘p’ ‘i’ steps back. MS18PL

Example: f=d+c g=q1b h=p1\*c k=r2q2 m=p1+r4 makes f=60 g=16 h=361 k=5.33 m=76

1. An operation of the type a=b\*c is done in 4 stages: Instruction fetch (IF), fetch operands (FO), compute (CP) and store result (SR). In IF the machine code of a=b\*c is put in the instruction register. In FO p=b and q=c is done. In CP r=p\*q is done. In SR a=r is done. What is the output of the following program: g=147;d=174;e=816;d=e+g;g=g+d;f=dr;nop;nop;nop;print(g,f) ES16PL

Example: j=10;k=87;u=421;v=34;u=u+v;v=k+v;h=r\*j;m=u+v;nop;nop;print(h,m); o/p 4550 489

1. Write a program whose sequential execution is same as pipeline execution of program R.

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| 1. P is a portion of program. It is executed in pipeline manner. Q is equivalent portion of program executed in sequential manner. R is executed in pipelined manner. Write similar for it. ES16PL | P | Q | R |
| u=v+w  b=c\*b  a=b+d  c=bc  b=b\*c  d=ba | u=v+w  a=b+d  d=c\*b  b=d\*c  c=d-c  d=da | u=k+z  b=c\*b  a=b+d  c=zc  d=b\*c  e=d+b  u=u+c |

1. An operation of the type a=b\*c is done in 4 stages: Instruction fetch (IF), fetch operands (FO), compute (CP) and store result (SR). In IF the machine code of a=b\*c is put in the instruction register. In FO p=b and q=c is done. In CP r=p\*q is done. In SR a=r is done. The time needed in IF, FO and SR be 100 units each. Let time needed by p+q, p-q, p\*q, pq be 420, 125, 365, 75 respectively. Assume that there are many ALU’s. Example: The following program outputs 100, 120, 59, 124. Hint: r becomes 16 at t=620. At t=600 p=r does p=74. At t=600 q=46 is done.

Example: a=12+4; b=82-27; c=45\*2; d=1482; x=r+45; y=r+46; z=r+43; w=r+34; print(x,y,z,w);

Question: What is the output of following program? ES15PL

e=41+2; f=14\*5; g=86-22; h=1642; i=r+9100; j=r+6200; k=r+8300; m=r+3400; print(i,j,k,m)

1. Write code for a=c/d; a=d-a under an architecture which can be understood in following example. ES15PL

b=a; d=c+a; ay,yz,zb,cx,xp,yq,+m,mw,wd

c=b\*d; a=b-d; bx,xp,dy,yq,\*m,-n,mz,nw,zc,wa

d=(a/c)+b ax,xp,cy,yq,/n,nw wx,xp,by,yq,+m,mz,zd

a=b-c;d=b/a bx,cy,xp,yq,-n,nw,wa wx,xq,/m,mz,zd

a=a+b;c=d-b ax,xp,by,yq,+m,mz za,dx,xp,-m,mw,wc

c=a+b;d=a-b;a=c;c=b+f ax,xp,by,yq,+m,-n,mz,nw,wd za,fx,xq,yp,+m,mw,wc

1. What are missing (mis-1 and mis-2) in the following? MS15PL

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| d=a+b; g=e\*f; | | | u=vw; w=k/u; | | | a=b+a; k=a\*c; | | | mis-1 | | | f=b\*c | |
| a1 b2 + | e1 f2 d | g\* | v1 w2  | 2 k1 u | w/ | b1 a2 + | 1 a c2 | \*k | q1 h2\* | 1 m2 | r | b1 c2 | mis2 |