Instruction:

Complete all questions in 1 hour.

1. Which one is the characteristic of Harvard Architecture?
   A. Program and Data stored in Separate Memory
   B. Program and Data stored in same Memory
   C. Program and data stored in Cache Memory
   D. All of Above
2. Which of the following is the working cycle of CPU
   A. Decode, Execute, Fetch
   B. Fetch, Decode, Execute
   C. Fetch, Execute , Decode
   D. All of Above
3. Any condition that causes a processor to stall is called as _____
   A. Hazard
   B. Page fault
   C. System error
   D. None of the mentioned
4. What does the control unit generate to control other units?
   A. Transfer signals
   B. Command Signal
   C. Control signals
   D. Timing signals
5. What do the processors of all computers must have?
   A. Control unit
   B. ALU
   C. Primary Storage
   D. All of these
6. Which is the fastest memory in the computer?
   A. Cache
   B. Ram
   C. Register
   D. Hard disk
7. With the help of _____ we reduce the memory access time:
   A. SDRAM

B. Cache
C. Heaps
D. Higher capacity RAMs

8. For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution?
   A. ISA
   B. ANSA
   C. Super-scalar
   D. All of the mentioned
9. A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____
   A. Super-scaling
   B. Pipe-lining
   C. Parallel Computation
   D. None of the mentioned
10. A 24 bit address generates an address space of _____ locations.
   A. 1024
   B. 4096
   C. 2^{48}
   D. 16,777,216

11. The USA contains about 3100 counties. Suppose you have a table that stores, for each county, its name (up to 40 characters in 8-bit ASCII), its state (a two-letter code), its population, and its median income (both as 32-bit numbers). How much space would the whole database take in memory?

- USA contains 3100 counties. Each county can take upto 40 characters in 8-bit ASCII. So each county can take upto 40 bytes of memory. Each state code is a two letter code. So, each state code will take upto two bytes of memory. The median and population are 32 bit numbers. So both of these fields will each take upto 4 bytes of memory.
- Byte count of county = 40 byte
- Byte count of state = 2 bytes

- Byte count of population = 4 bytes
- Byte count of median = 4 bytes

  Now,
- Total bytes of one county = 50 bytes
- Total bit of 3100 counties = 50*3100 = 155000 bytes

  The answer is 155000 bytes which is then converted into kb. The final result is approximately 155 kb. Therefore, the whole database will take upto 155 kilobytes.

12. The computer has a maximum addressable memory of 16 Gigabytes. Its address bus width is 32.
    a) Calculate the width of the data bus.

       Solution:
       - Data bus width = maximum addressable memory/ (2^address bus width)

         Now,

       Data bus width = 16 GB/(2^32)
       = 16 GB/ (4,294,967,296)
       = 0.0037252902984619140625 GB
       = 3.7252902984619140625 MB

       Therefore, the width of the data bus is **3.7**MB

    b) State the effect that adding one new line to the address bus would have on the maximum addressable memory.

       The maximum addressable memory of a computer is determined by the number of bits in the address bus.

       Maximum addressable memory = 2^ address bus width

       If one new line is added to the address bus, then the width of the address bus would increase by 1 bit. Therefore, the new width of the address bus would be 33 bits.

       Now,

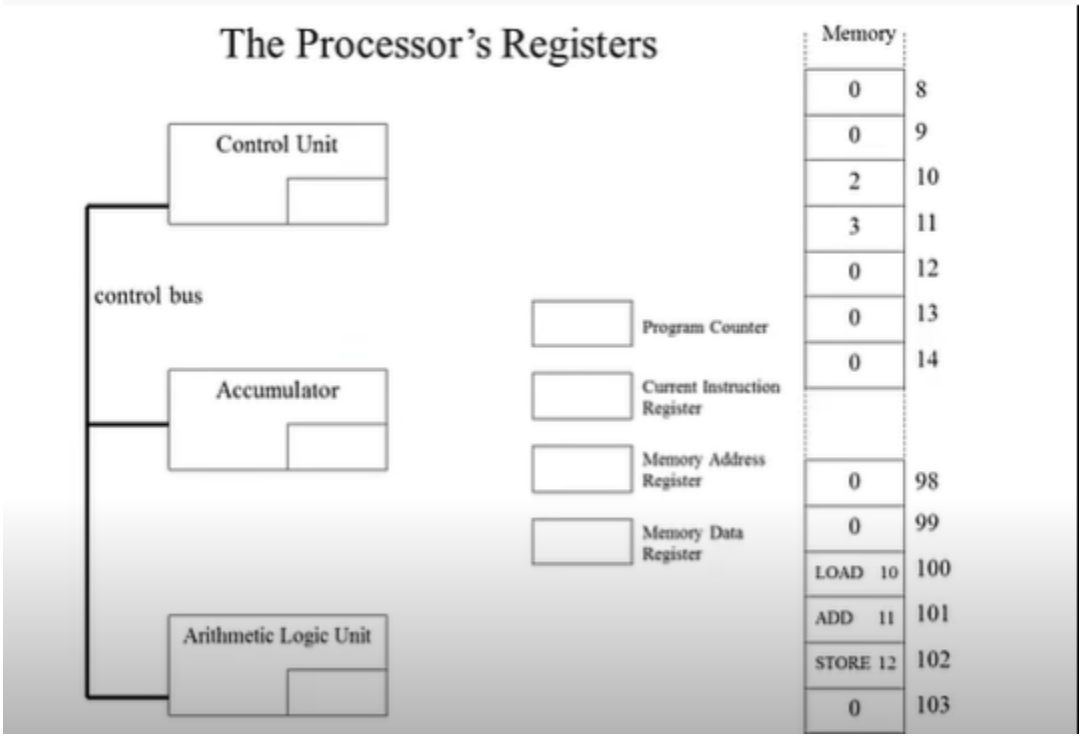
       Maximum addressable memory = 2*33

       Maximum addressable memory = 8,589,934,592 bytes

       Maximum addressable memory = 8.59 GB

Therefore, adding one line to the address bus would increase the maximum addressable memory from 16 GB to 8.59 GB.

13. Explain the *Instruction cycle* of the processor by taking an example of the program
    Load: [10]
    Add : [11]
    Store: [12]



In the above example, the instruction cycle has the following registers:Control Unit, Arithmetic Logic Unit, Accumulator, Program Counter, Current instruction Register, Memory address register and Memory Data Register. In the beginning, value 10 is loaded in the memory which is 100. This value moves from the program counter to the Memory register. Then, we need to look at the memory lines from the top. The value 2 is in the 10th line. This value is loaded in the control unit and then in the accumulator.
Now, value 11 is added in the memory line 101. Then, we need to look at the 11th line from top and its value is 3. The value 3 loads through the Current Instruction Register and Memory Data Register. Then, the memory value 3 goes to the Control unit. Now the previously stored value in accumulator which is 2 and the value

stored in control unit, which is 3 is taken by Arithmetic Logic Unit. ALU adds these values and it becomes 5.
Now, we need to store the value 12 in the 102th memory line. Looking from the top, the 12th line has value 0. The memory value is loaded through the Current Instruction Register and Memory Data Register. It is at last stored in the Control unit. This was the overall instruction cycle of the processor.

14. Write short notes on the following topic:

a) Von Neumann and Harvard Architecture

- Von Newman architecture was first published by von Newman in 1945 AD and the design is still used in many computers today. It describes the basic design of a digital computer. It is based on the stored-based computer concept where instruction and program are stored in the same memory and this memory is called the Von Newman bottleneck. Its main components are the Central Processing Unit(CPU), Input/Output Unit(I/O unit) and a control unit.
- Harvard Architecture was named after Harvard University where it was first implemented in the 1930s. It is a computer architecture that separates the memory for data and instructions. In this type of architecture, the CPU accesses separate memories for instructions and data. This simply means that the CPU can fetch and process data and instructions at the same time. The processing time becomes faster in this architecture. Its major components are CPU, data memory, a program memory and input/output unit.

b) RISC vs CISC architecture

- RISC stands for Reduced Instruction Set Number and CISC stands for Complex Instruction Set Number. It simply means RISC has less number of instructions and CISC has larger number of instructions. RISC uses fixed instruction format which is 32 bit whereas CISC does not have fixed instruction format, it can use 16 bits, 32 bits or 64 bits. RISC is cheaper but less powerful as compared to CISC. In CISC, we can get a maximum number of instructions to perform any operation and it can take instructions in multiple cycles but RISC offers a limited number of instructions and takes single cycle instructions. In CISC, the manipulation of instructions takes

place in memory whereas in RISC, the manipulation of instructions takes place in the registers.