Intel® Firmware Support Package (Intel® FSP) for Intel Atom® x6000E Series, and Intel® Pentium® and Celeron® N and J Series Processors (*formerly known as Elkhart Lake*)

Release Notes – MR1

August 2021

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Revision History

These are the main releases of Intel® Firmware Support Package (Intel® FSP) for Intel® processor codenamed Elkhart Lake.

Date	Revision	Description
April 2020	Alpha (3)	Initial release (Elkhart Lake label v2115_00_423)
September 2020	Beta (2)	Beta release (Elkhart Lake label v2341_05_33)
October 2020	Beta (3)	Beta 3 release (ElkhartLake_Daily2411_00_215)
December 2020	Beta (4)	Beta 4 release (ElkhartLake_Label2463_00_122)
March 2021	PV	PV Release (ElkhartLake_Label3092_03_101)
March 2021	Fusa PV	PV Release (ElkhartLake_Label3125_02_104)
April 2021	PR1	PR1 Release (ElkhartLake_Label3162_01_105)
August 2021	MR1	MR1 Release (ElkhartLake_Label3273_04_122)

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1.0 Introduction

This package contains required binary image(s) and collateral for the Intel® Firmware Support Package (Intel® FSP) for Intel® processor codenamed Elkhart Lake.

Compliant with Intel® FSP 2.1 External Architecture Specification.

This document provides system requirements, installation instructions, issues and limitations, and legal information.

To learn more about this product, see:

- New and previously new features listed in Section 2.0, New in This Release.
- Reference documentation listed in Section 1.2, Related Documentation, Tools, and Packages.

The following table lists the relevant platform software components used during development and validation of this release.

Table 1. Platform Software Component Information

Please use the correct microcode when integrating Intel® FSP. Any processor that does not have the correct microcode update loaded is considered to be operating out of specification. See the relevant bootloader's release notes for more details regarding microcode loading.

Supported Silicon Stepping	Microcode Version
B0	m_01_90661_00000011

1.1 Terminology

The following terms are used in this document.

Table 2. Terminology

Term	Description
API	Application Programming Interface
BSF	Binary Settings File
BCT	Intel® Binary Configuration Tool
CRB	Customer Reference Board

Term	Description
Intel® EDC	Intel® Embedded Design Center
Intel® FSP	Intel® Firmware Support Package
SoC	System on Chip

1.2 Related Documentation, Tools, and Packages

Table 3. Related Documentation, Tools, and Packages

Document	Location
ElkhartLake_FSP_Integration_Guide.pdf	Available in this release package
Intel® Binary Configuration Tool for Intel® Firmware Support Package	www.intel.com/fsp
Intel® Firmware Support Package (Intel® FSP) External Architecture Specification (EAS) v2.1	https://cdrdv2.intel.com/v1/dl/getContent/611786

1.3 Intended Audience

The intended audience is platform and system developers who intend to use an Intel® FSP-based bootloader for the firmware solution for their overall design based on the Intel® processor codenamed Elkhart Lake. This group includes, but is not limited to, system BIOS developers, bootloader developers, and system integrators.

1.4 Customer Support

Intel offers support for this software at the API level only, defined in the Intel® FSP Integration Guide and reference manuals listed in Section 1.2, Related Documentation, Tools, and Packages.

For technical support, raise an IPS (Intel® Premier Support) ticket at https://intel.my.salesforce.com/

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2.0 New in This Release

2.1 MR1 Features

- Adopting Elkhart Lake IAFW external release Elkhart Lake Label 3273_04_122

3.0 Fixed Issues

The following list contains the fixed issues in this release:

- None.

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4.0 Limitations

4.1 Current Release

- Default max C-state supported: C9

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5.0 Known Issues

5.1 Current Release

- The max 4K option of "DDR Frequency Limit" in current Intel® FSP UPD was not shown.

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6.0 Split Intel® FSP Image into Individual FSP-T/M/S Components

The Intel® FSP 2.1 image can be split to three individual components using the *SplitFspBin.py* script in the release package. For further details on splitting and integrating the Intel® FSP, refer to the relevant bootloader release notes.

Rebase address:

The bootloader will rebase and relocate the Intel® FSP binary dynamically, so the base address is not hard coded with the default base address and location. Once the user configures the Intel® FSP binary as XIP, the bootloader can decide where the binary will be placed in the coreboot's CBFS or Intel® Slim Bootloader's Fv, and will take care of rebasing it during build.

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7.0 Where to Find the Release

This package can be found from the ***Elkhart Lake*** **Firmware Best Known Configuration (BKC)** searchable at Intel® Resource & Design Center (RDC) Software Kits:
https://www.intel.com/content/www/us/en/secure/design/confidential/software-kits/view-all.html?s=Newest

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8.0 Release Content

This release contains:

- Intel® FSP Integration Guide
- Intel® FSP Binary
- Binary Settings File (BSF)
- Release Notes

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9.0 Hardware and Software Compatibility

9.1 Supported Hardware

This Intel® Firmware Support Package (Intel® FSP) release is specifically targeted for Intel Atom® x6000E series, and Intel® Pentium® and Celeron® N and J Series processors (*Formerly known as Elkhart Lake*).

9.2 Supported Bootloaders

This release can be installed on either a Windows* or a Linux* system. However, the Intel® FSP binary itself can be used with any software development environment to generate a complete bootloader solution.

The software in this release has been validated on customer reference boards (CRBs) with the bootloader and operating systems listed in the following table.

Table 4. Operating System/Bootloader Support

Product Family	Bootloader	Operating System
Intel® Processor codenamed Elkhart Lake	Elkhart Lake Intel® Slim Bootloader with the UEFI/OsLoader payload	Yocto Project*-based OS Windows* 10
Intel® Processor codenamed Elkhart Lake	coreboot* with the UEFI payload	Yocto Project*-based OS Windows* 10

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10.0 Source Code Level Intel® FSP UPD Values Configuration

Intel® FSP UPD settings can be configured from respective bootloaders at the source code level. Details provided here for modifying default values are provided by Intel® FSP UPDs in supported bootloaders as mentioned in Section 9.2.

Here are two potions of Intel® FSP that can be changed from bootloaders:

FSP Potion	FSP Headers file (UPD reference codes)
FSP-M	Include/**FspmUpd.h**
FSP-S	Include/**FspsUpd.h**

The respective UPDs can be found inside the respective Intel® FSP headers file.

10.1 coreboot*

To modify the default FSP UPD values in coreboot, navigate to these respective files:

FSP Potion to change	Source code
FSP-M	src\soc\intel\elkhartlake_dev\romstage**fsp_params.c**
FSP-S	src\soc\intel\elkhartlake_dev**fsp_params.c**

Here are the **examples** to change the UPD values: -

1. For UPDs that have been exposed in the source code, change the value (highlighted in yellow) to the desired value:

```
/* Vt-D config */

m_cfg->VtdDisable = 0;
```

2. For UPDs that have not been exposed in coreboot* source code, insert code as shown below.

FSP-M (insert code below in this function: void platform_fsp_memory_init_params_cb(FSPM_UPD *mupd, uint32_t version))	**FSP-S** (insert code below in this function: void platform_fsp_silicon_init_params_cb(FSPS_UPD *supd))
m_cfg-> {UPD} = {desired value}	params-> {UPD} = {desired value}

10.2 Intel® Slim Bootloader

To modify the default Intel® FSP UPD values in the Intel® Slim Bootloader, navigate to these respective files:

FSP Potion to Change	Source code
FSP-M	SblInternal\Platform\ElkhartlakeBoardPkg\Library\Stage1BBoardInitLib\ **Stage1BBoardInitLib.c**
FSP-S	SblInternal\Platform\ElkhartlakeBoardPkg\Library\Stage2BoardInitLib\ **Stage2BoardInitLib.c**

Here are the **examples** to change the UPD values:

3. For UPDs that have been exposed in the source code, change the value (highlighted in yellow) to the desired value:

```
/* Vt-D config */

Fspmcfg->VtdDisable = 0;
```

4. For UPDs that have not been exposed in the Intel® Slim Bootloader source code, insert code as shown here.

FSP-M (insert code below in this function: *VOID UpdateFspConfig (VOID *FspmUpdPtr)*)	**FSP-S** (insert code below in this function: *VOID UpdateFspConfig (VOID *FspsUpdPtr)*)
Fspmcfg-> {UPD} = {desired value}	Fspscfg-> {UPD} = {desired value}

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