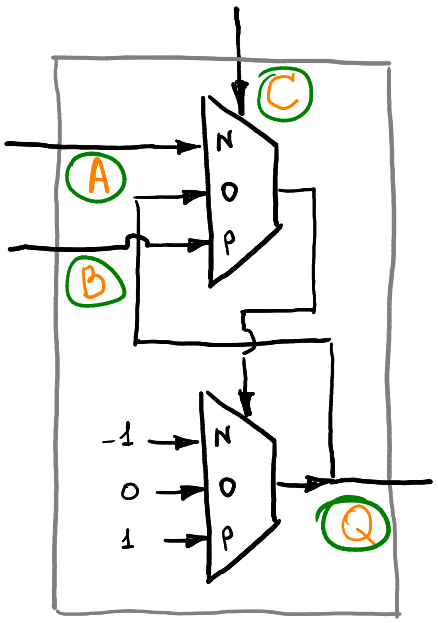
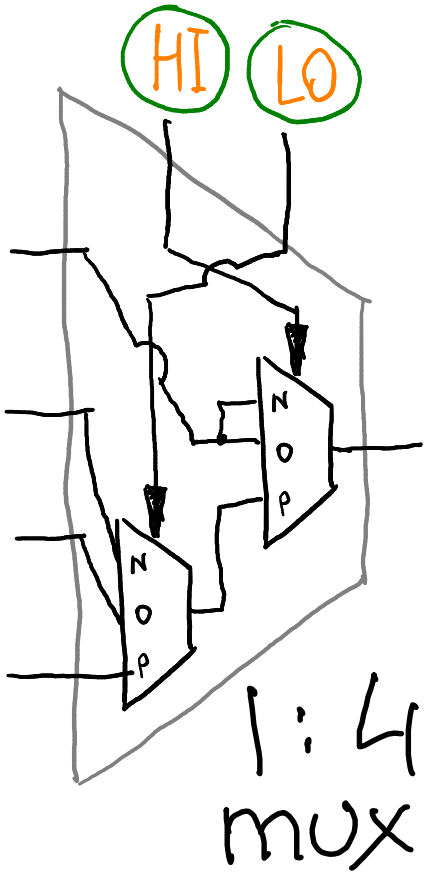
ternary memory latch



C	A	B	Q
-1	-1	×	-1
-1	0	×	0
-1	1	×	1
0	×	×	Q_{prev}
1	×	-1	-1
1	×	0	0
1	×	1	1



1:4 mux