AN 15.13

USB3290 PHY Layout Guidelines

1 Introduction

This application note provides general PCB layout guidelines for SMSC's USB3290 PHY. The Universal Serial Bus (USB) is capable of operating at 480 Mbps. Excellent signal integrity is required to operate reliably at high-speed data rates. The PCB layout is a critical component in maintaining signal integrity.

1.1 Audience

This document is written for a reader that is familiar with hardware design, USB protocols and the USB 2.0 specification. The goal of the application note is to provide information on sensitive areas of the PCB layout.

1.2 Overview

The following recommendations for PCB layout with SMSC parts is not the only way to layout the USB3290. PWB design engineers will have his/her own preference, and the implementation will be dependent on complexity and density of layout, PCB real estate, number and types of devices in circuit and the environment that the final product will reside in.

1.3 References

The following documents should be referenced when using this application note:

- SMSC USB3290 Datasheet
- SMSC EVB-USB3290 User Manual
- Universal Serial Bus Specification Revision 2.0

2 Review of Sensitive Circuits

This chapter provides guidelines for the sensitive circuits associated with the system application of the USB3290.

2.1 Controlled Impedance for USB Traces

The USB 2.0 specification requires the USB DP/DM traces maintain a nominal 90 Ohms differential impedance +/- 15 % (see USB specification Rev 2.0, paragraph 7.1.1.3 for more details). In this design the traces are 6 mil wide with minimum line spacing of 7 mils. These numbers are derived for 5 mil distance from ground reference plane. For different dielectric thickness, copper weight or board stack-up, trace width and spacing will need to be recalculated. A continuous ground plane is required directly beneath the DP/DM traces and extending at least 5 times the spacing width to either side of DP/DM lines.

Maintain symmetry between DP/DM lines in regards to shape and length.

Single ended impedance is not as critical as the differential impedance, a range of 42 to 78ohms is acceptable (equivalently, common mode impedance must be between 21 Ohms and 39 Ohms).

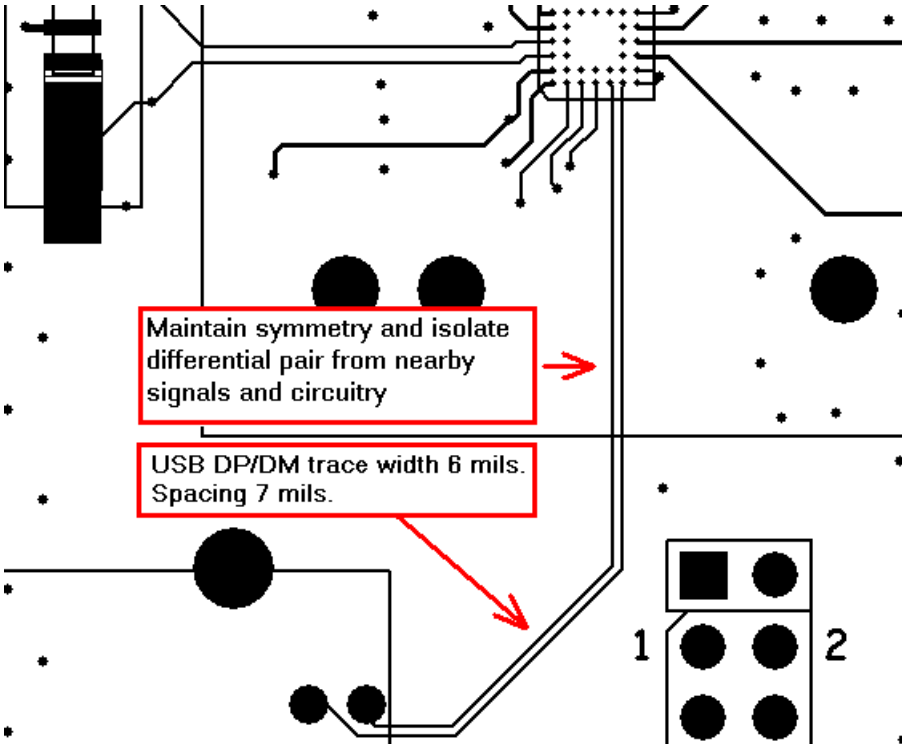

Figure 2.1 Example of Routing DP/DM to Type B Connector

Figure 2.1 shows DP/DM traces with approximately equal trace length and symmetry. It is important to maintain a conductor width and spacing that provides differential and common mode impedances compliant with the USB specification. Use 45 degree turns to minimize impedance discontinuities.

2.2 Isolation of DP/DM Traces

The DP/DM traces must be isolated from nearby circuitry and signals. Maintain a distance of parts to lines that is greater than or equal to 5 times the distance of the 7 mil spacing between the traces. Do not route differential pairs under parts. Do not cross DP/DM lines with other PCB traces unless the traces are on the opposite side of the ground plane from DP/DM. Route DP/DM traces over solid plane, not over power planes.

2.3 Isolated Shielding on the USB Connector

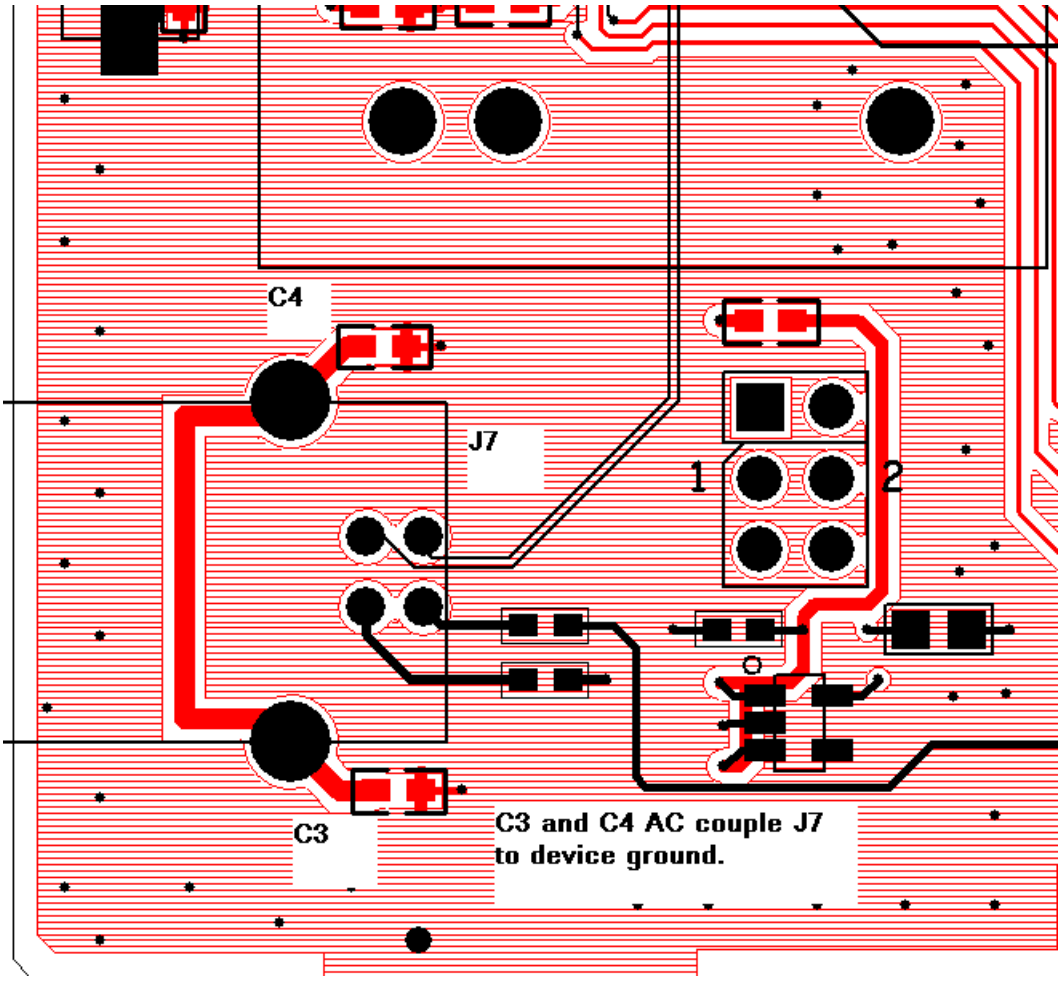

Figure 2.2 Connections to Shield of Type B USB Connector

The USB3290 is a USB peripheral device PHY. Figure 2.2 shows J7 the B-connector housing DC isolated but AC coupled to the device ground. Industry convention is to ground only the host side of the cable shield. This is done to provide cable shielding while preventing possible ground currents from flowing in the USB cable if there happens to be a potential difference between the host and device grounds.

2.4 Crystal Oscillator

The crystal oscillator is sensitive to stray capacitances and noise from other signals, and should be placed away from high frequency devices and traces. It can also disturb other signals and cause EMI noise. The load capacitors, crystal and parallel resistors should be placed close to each other. The ground connection for the load capacitors should be short and out of the way from return currents from USB, VBUS and power lines. The load capacitors return paths should be to the digital logic power supply.

Figure 2.3 shows a schematic of the crystal oscillator circuit.

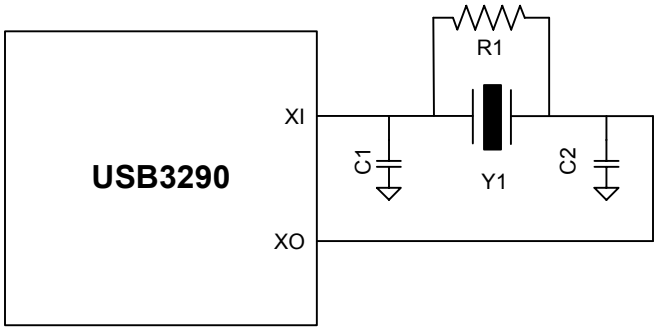

Figure 2.3 Crystal Oscillator Schematic

Figure 2.4 illustrates a suggested PCB layout of the crystal circuit. All components are far removed from USB lines.

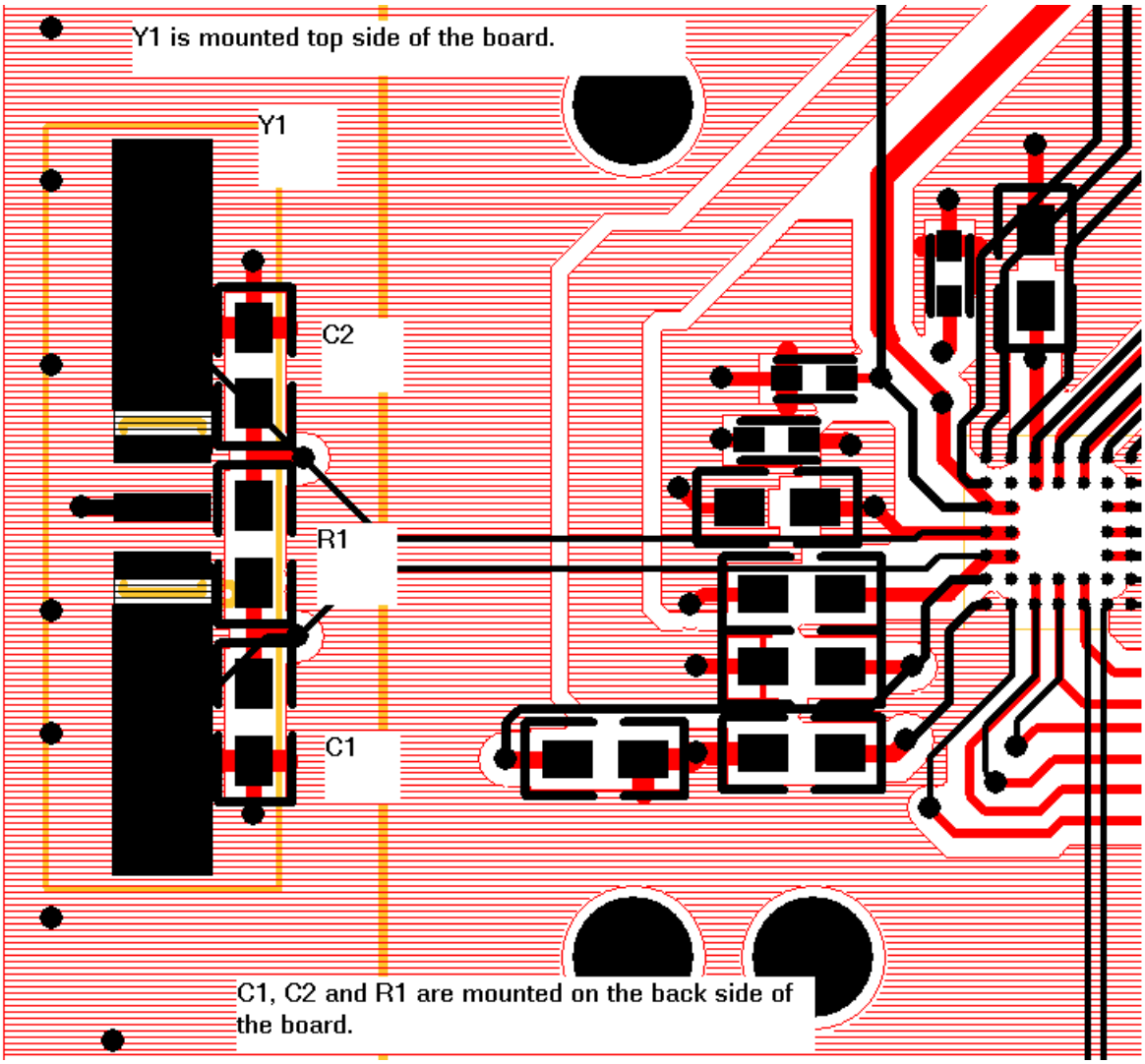

Figure 2.4 Crystal Oscillator Component Layout

2.5 RBIAS

The RBIAS resistor sets an internal current source reference. Thus, the RBIAS pin is a high impedance node and so any noise induced on the RBIAS traces will directly impact internal current references and negatively degrade eye-diagram quality. The RBIAS resistor should be placed close to the RBIAS pin and the ground return should be short and direct to VSS with RBIAS placed the same way as bypass capacitors as described in paragraph 2.6. Traces for resistor should be very short and isolated from nearby traces if possible.

2.6 Power Supply Bypass Capacitors

This example has bypass capacitors for the BGA placed on the opposite side of board as shown in figure 2.5. Bypassing should be as near as possible to it's respective power pin. In this example, the physical dimensions of the 0603 bypass caps and the USB3290 dictates the distance between the USB3290 and the bypass caps. Make power traces as short and as wide as board space will allow. The USB3290 evaluation board has bypassing under the device, with return current paths tied to the internal ground plane.

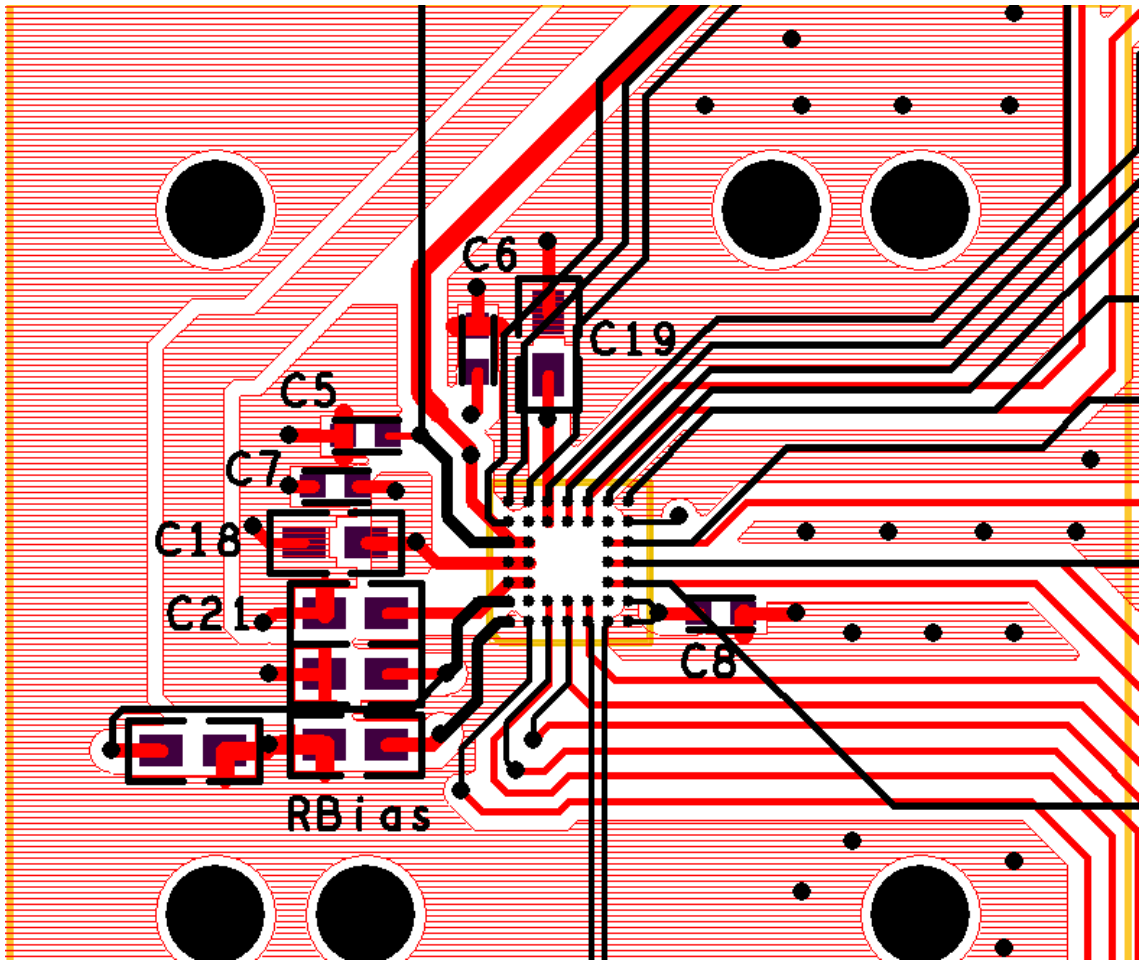

Figure 2.5 Placement of Bypass Capacitors

3 Summary

Layout guidelines have been presented for the USB3290. SMSC has found these guidelines to be effective in creating a systems application circuit for the USB PHY.

80 Arkay Drive
Hauppauge, NY 11788
(631) 435-6000
FAX (631) 273-3123