Introduction of Pentium

- The concepts of 80386 microprocessor and 80387 coprocessor together evolved the 80486 microprocessor.
  - **Only new idea here is the introduction of 8K cache**
  - The cache is used for storing both *data* and *instructions*

- Pentium was introduced in 1993
- Pentium processor is an improvement to the architecture found in 80486.

Pentium Improvements

- Improved cache structure
  - Reorganized to form **two level (L2) caches** that are each 8K bytes in size
    - One for caching *data*
    - Another for caching *instructions*
- Wider data bus width
  - Increased from 32 bit to 64 bits
- Faster numeric processor
  - Operates about 5 times faster than the 80486 numeric processor

Pipelining in Pentium

- Pentium has two pipelines
- **U pipeline**
  - U-pipeline can execute ***any Pentium instruction***
- **V pipeline**
  - V-pipeline only executes only ***simple instructions***
- Each pipeline has 5 stages
  - i. Pre-fetch
  - ii. Instruction Decode
  - iii. Address Generation
  - iv. Execute, Cache, and ALU Access
  - v. Write back

Pipelining Stages in Pentium

- **Pre-fetch:**
  - Instructions are fetched from the Instruction cache and aligned in prefetch buffers for decoding
- **Instruction Decode:**
  - Instructions are decoded into the Pentium's internal instruction format.
- **Address Generation:**
  - Address computations take place at this stage
- **Execute, Cache, and ALU Access:**
  - The integer hardware executes the instruction
- **Write-back:**
  - The results of the computation are written back to the register file

Super Scalar Machine

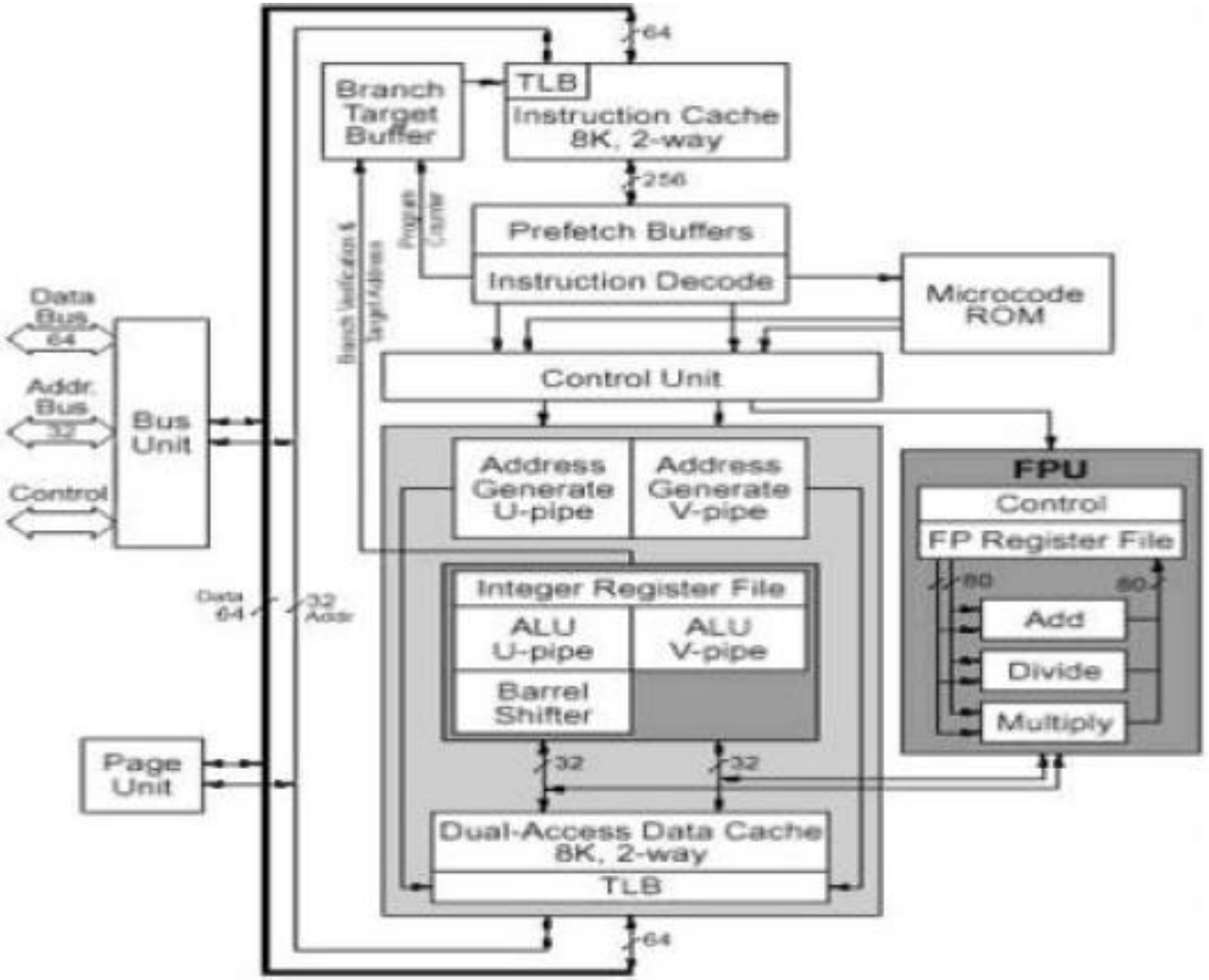
- Any Processor capable of parallel instruction execution of multiple instructions is known as **superscalar machine.**

- As, in Pentium, there are two execution lines --- U-line and V-line, so Pentium is a ***Super Scalar Processor***

- What are the differences? to understand the concepts in terms of processor execution stages:
  - Parallelelism
  - Simultaneity – Simultaneously Parallel
  - Pipelining – Parallel and Simultaneous

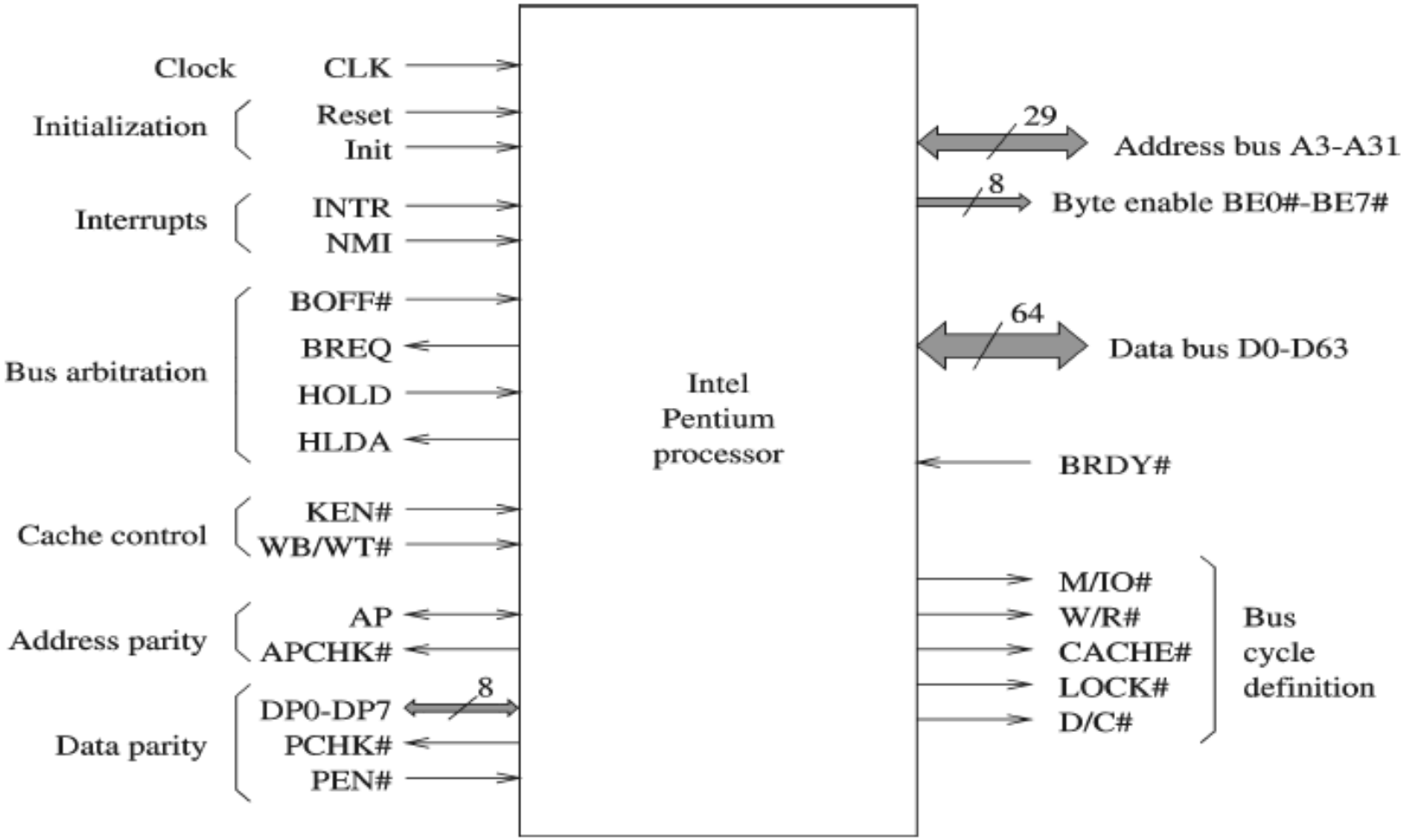
Pentium Architecture

- It has all the units similar to 80386.
  - *Instruction unit*
  - *Segmentation unit*
  - *Paging unit*
  - *Bus unit*
  - *Execution unit*
- The newer one introduced as-
  - *Floating Point unit (FPU)*



Pentium Architecture

- Pin Diagram



Pentium Architecture: **Floating Point Unit (FPU)**

- FPU has 8 80-bit general purpose floating point registers, ST(0) through ST(7)
- **It has 8-stage pipeline**
  - First 5 stages are identical to U and V pipelines
  - 2 additional execution stages
    - First execution stage (X1 stage)
    - Second execution stage (X2 stage)
    - In these two stages FPU reads the data from data cache and executes the floating point computation
  - One additional error reporting stage

Pentium Architecture: **Pins**

- Packaged in 273 pins
  - Data Bus 64 pins
  - Address Bus 29 pins plus 3 pins
  - Control Bus 75 pins
  - Vcc + Ground 99 pins
  - No Connection (NC) 6 pins

Pentium Data Bus

- 64-bit data bus
- D0 through D63 (Data Bus)
- Bi-Directional
- These signals make up the Pentium's 64-bit bidirectional data bus.

Pentium Address Bus

- 32-bit address bus.
- A3 through A31 (Address Lines)
  - Output/Input --- bi-directional
- These 29 address lines, together with the byte enable outputs *BE0-BE7, form the* Pentium's 32-bit address bus.
- A memory space of 4 GB is possible, along with 65536 I/O ports.
- The address lines are used as input during an inquire cycle to read an address *into the Pentium, for* examination by the internal cache.

Pentium Address Bus

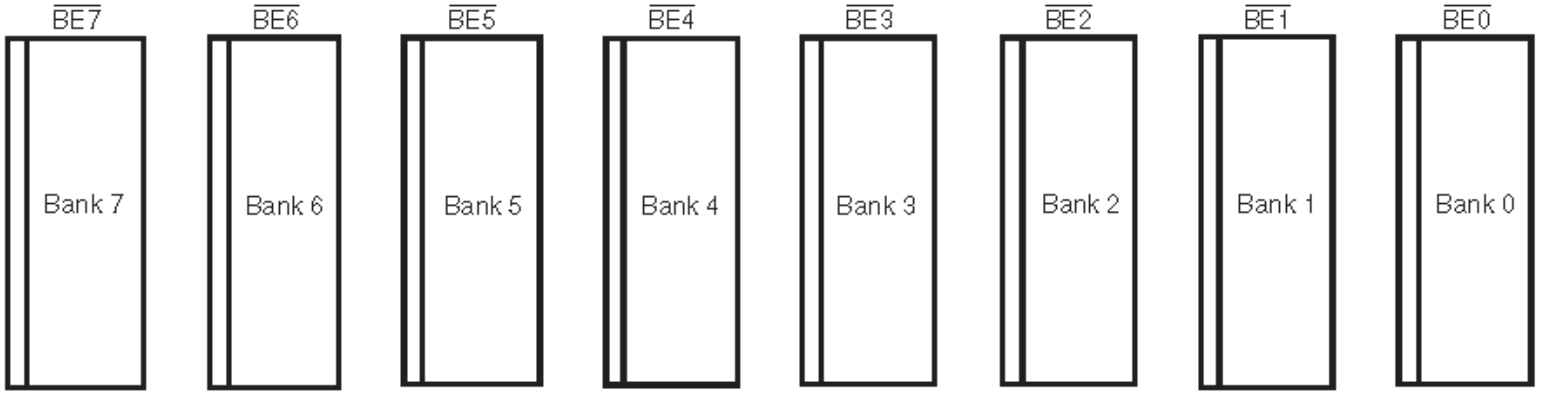
- No A0, A1 and A2 address lines are available in Pentium
  - They are internally decoded to produce BE0 to BE7 signals

- **BE0 through BE7**
  - Byte (Bank???) Enable lines
  - Memory are arranged in total 8 banks

- **Output**
  - These, together with A3 through A31, make up the 32-bit address output by the Pentium.
  - Each byte enable is used to control a different 8-bit portion of the processor's 64-bit data bus.
  - BE0 enables Bank 0

Pentium Memory System

- Pentium's memory arranged in 8 banks
- Each bank stores 1 byte of data ***with parity bit***
  - **It helps for error detection and correction in data**
- BE0 to BE7 selects the banks
- New feature added to Pentium is its capability to generate and check parity for address bus



Pentium Pro: Salient Features

- The notable difference in the Pentium Pro than the earlier Pentium is that
  - **There are provisions for a 36-bit address bus, which allows access to 64G bytes of memory.**
- ***This is meant for future use*** because no system today contains anywhere near that amount of memory.
- Pentium Pro is available in two versions.
  - One version contains a 256K level 2 cache;
  - The other contains a 512K level 2 cache
- Pentium Pro microprocessor is packaged in an immense 387-pin PGA (pin grid array).

Pentium II: Salient Features

- Extension to Pro architecture with some differences
  - Internal cache in PII has been moved out of the chip
  - PII is not available as a single chip
  - Rather is available on a small plug-in circuit board, known as ***Cartridge, along with level 2*** (L2) cache chip

- Various versions are available
  - **Celeron** is a version without L2 cache
  - **Xeon** is enhanced by having up to 2M L2 cache

Pentium III: Salient Features

- Based on Pro architecture, not on Pentium II
- Like PII, PIII is packaged in a cartridge instead of IC chip
- Additionally a **Coppermine** is packaged in an IC with 370 pins
- **Coppermine** is an internal cache with 256K advanced transfer mechanism within the IC running at processor speed
- ***Why not used 512K Cache?***
  - ***It has been observed that, increasing cache size from 256K to 512K improves the performance by only a few percent***

Pentium III: Salient Features

- Various versions of Pentium III are also available like Pentium II
  - **Standard** Pentium III
  - **Celeron** Pentium III uses 66MHz bus speed
  - **Xeon** Pentium III allows larger cache for server applications
    - Still Xeon is popular for server processors

Pentium IV: Salient Features

- Based on Pro architecture, not on P II or P III
- P IV is packaged in 421 pins IC
- It uses physically smaller transistors
  - Makes it much smaller and faster than P III
- Released initially in November 2000 with 1.3GHz speed
  - Now available with speed more than 3GHz