Programmable Peripheral Interface (PPI) 8155 and 8255

Course Teacher:

Md. Obaidur Rahman, Ph.D.
Professor
Department of Computer Science and Engineering (CSE)
Dhaka University of Engineering & Technology (DUET), Gazipur.

Course ID: CSE - 4619
Course Title: Peripherals, Interfacing and Embedded Systems
Department of Computer Science and Engineering (CSE),
Islamic University of Technology (IUT), Gazipur.

Lecture References:

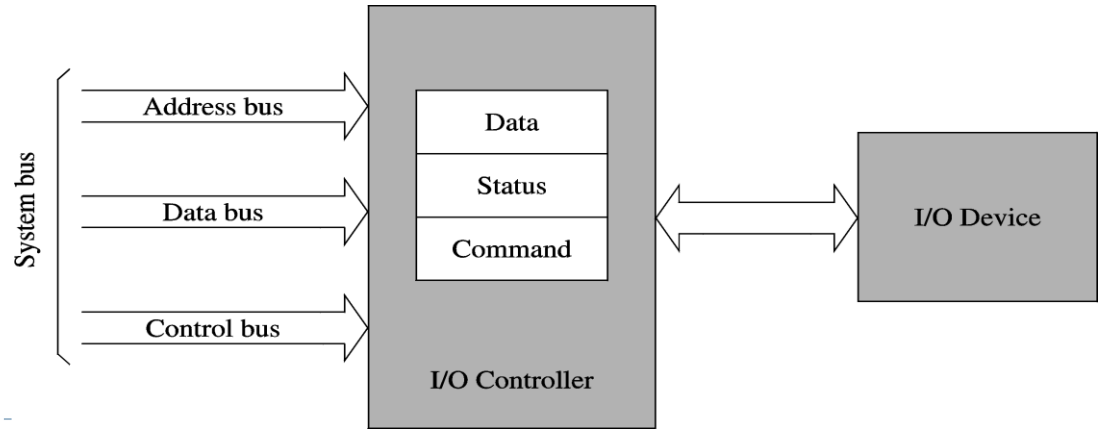
- Book:
  - *Microprocessor Architecture, Programming and Applications with 8085 (Chapter-15)*, **Author:** Ramesh Gaonkor
- Lecture Materials:
  - *I/O System Design*, Dr. Esam Al_Qaralleh, CE Department, Princess Sumaya University for Technology.

Peripherals (I/Os) and Interfacing

- The primary functions of the microprocessor/microcontroller are:
  - to accept data from input devices such as – keyboards and A/D converters
  - read instructions from the memory
  - process data according to the instructions and
  - send the results to output devices such as – LEDs, printers and monitors.
- The input and output devices are called either **peripherals or I/O**.
- Designing logic circuits (hardware) and writing instructions (software) to enable microprocessor to communicate with I/Os is called **interfacing** and logic circuits are called **I/O ports** or **interfacing devices**.

Basic Concepts in I/O Devices Interfacing

- I/O devices serve two main purposes
  - To communicate with outside world
  - To store data
- I/O controller acts as an interface between the systems bus and I/O device
  - Relieves the processor of low-level details
  - Takes care of electrical interface
- I/O controllers have three types of registers
  - Data
  - Command
  - Status



Types of I/O Interfacing

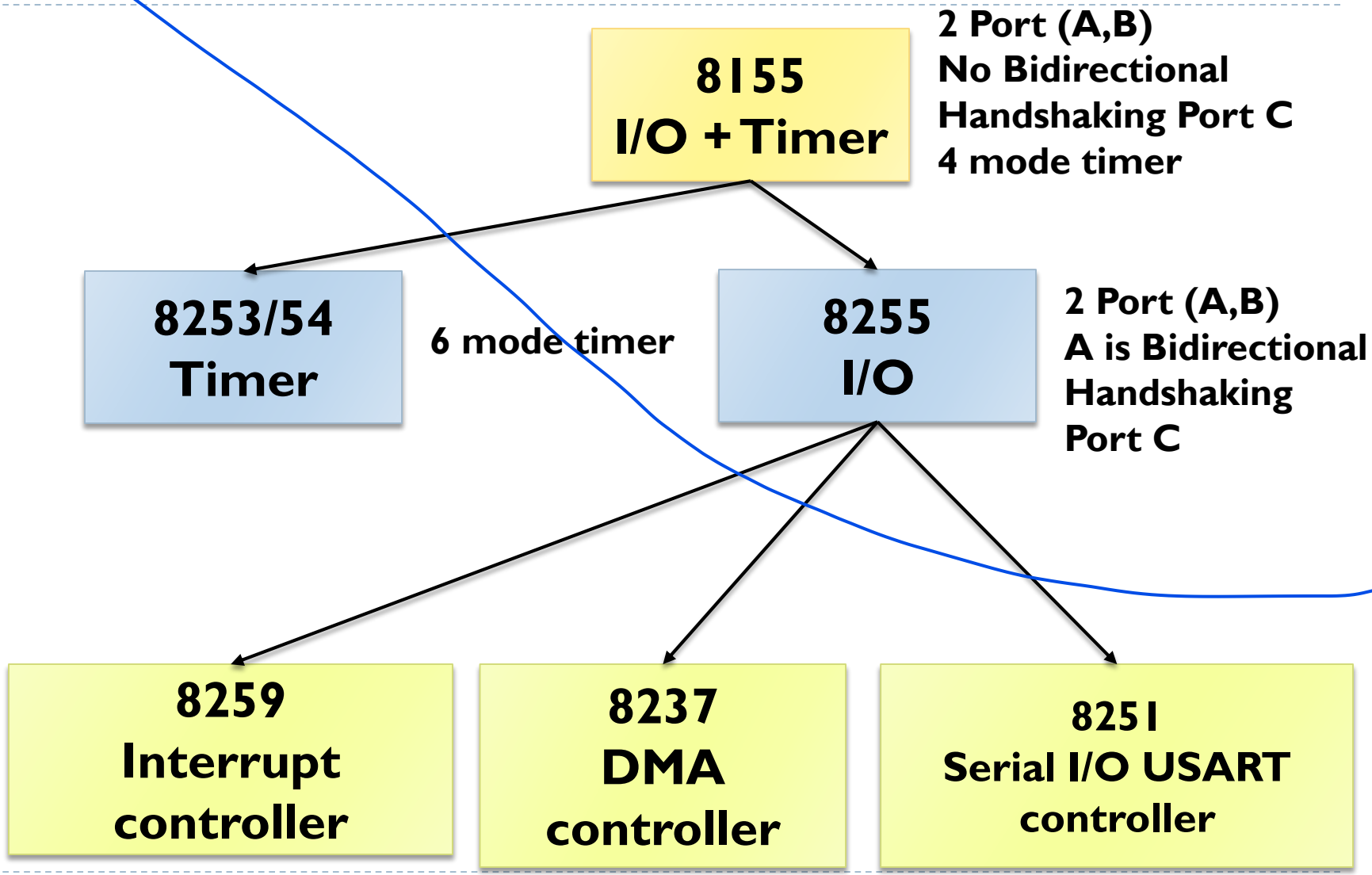
- **Internal I/O Interface**
  - In PCs internal chips (e.g., 8155A, 8255A PPI) are built into the system board and can be seen by inspection.
  - In modern Computers the functionality of these chips has been built into the system board chipset.

- **External I/O Interface**
  - Peripherals are connected to an external interface.
  - **Examples**: RS-232 serial interface, 8251 USART etc.

Internal I/O Interfacing

- Intel has developed several peripheral controller chips designed to support its processors.
- The goal is to give a complete **Internal** I/O interface in one chip.
- **Examples:**
  - 8155 Programmable Peripheral Interface (PPI)
  - 8255 Programmable Peripheral Interface (PPI).
  - 8253/8254 Programmable Interval Timer (PIT)
  - 8259 Programmable Interrupt Controller (PIC)
  - 8237 Programmable DMA controller.

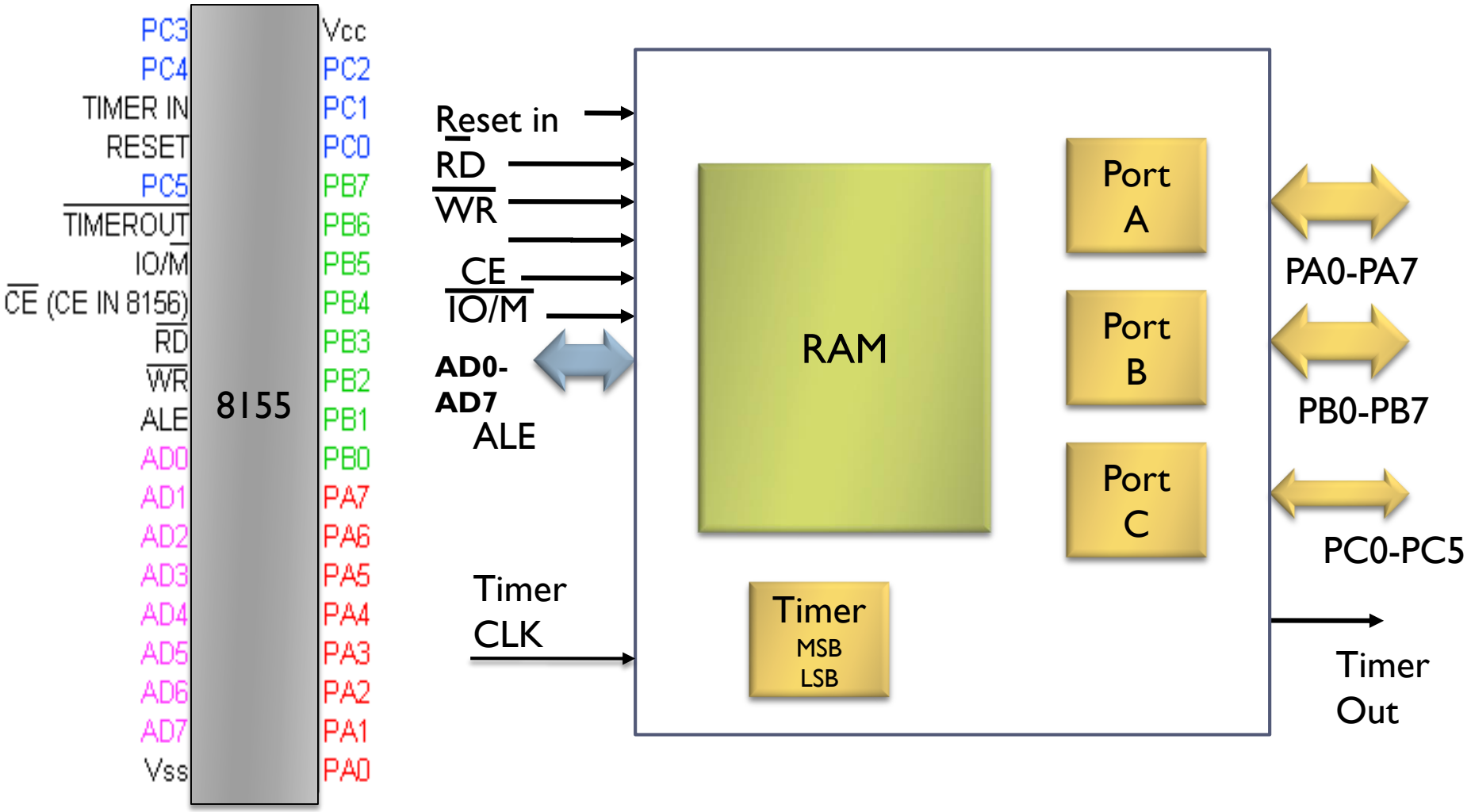
Hierarchy of I/O Control Devices



8155 PPI

- Compatible to work with 8085 Microprocessor
- 2-kbits static RAM 256x8 BYTES
- 2 programmable 8 bit I/O ports … **PORT A and B**
- 1 programmable 6 bit I/O port …. **PORT C**
- 1 programmable 14 bit binary counter/timer
- Internal address latch to Demux AD0-AD7, using ALE (Address Latch Enable) line using a 3-to-8 Decoder.
  - It provide 8-bit addresses of the ports and timers.

8155 Block Diagram



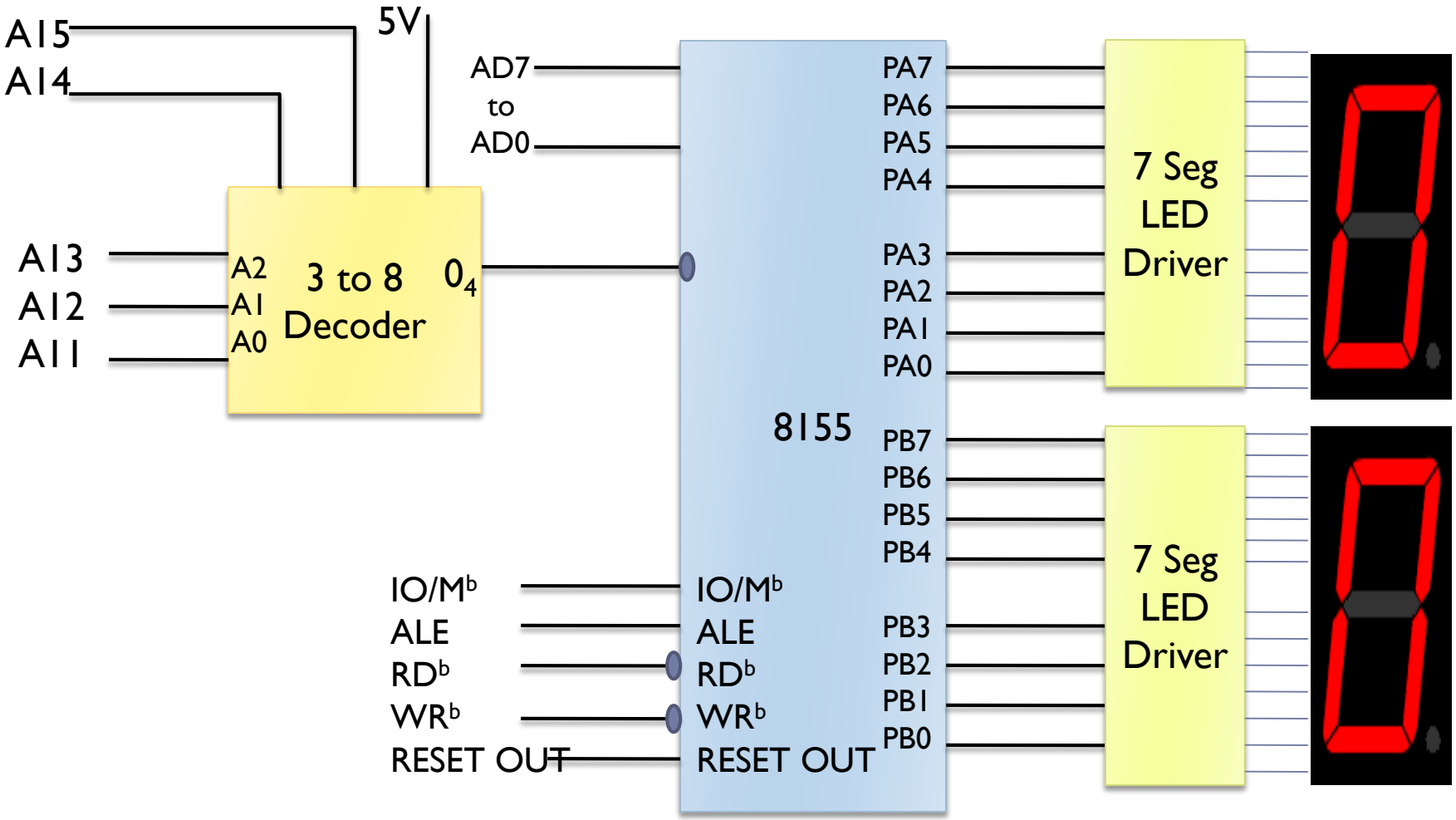
Control Word (Command Register Format)

D7	D6	D5	D4	D3	D2	D1	D0
Timer Command		IEB	IEA	PC		PB	PA

- D0, D1: mode for PA and PB, 0=IN, 1=OUT
- D2, D3: mode for PC
- D4, D5: interrupt EN for PA and PB, 0=disable 1=enable
- Port C bits (D2, D3) four alternatives.
- D6, D7: Timer command:
  - **00:** No effect
  - **01:** Stop **if** running **else** no effect
  - **10:** Stop after Terminal Count (TC) **if** running, else no effect
  - **11:** Start if not running, reload at TC **if** running.

ALT	D3	D2	PC5	PC4	PC3	PC2	PC1	PC0
1	0	0	IN	IN	IN	IN	IN	IN
2	0	1	OUT	OUT	OUT	OUT	OUT	OUT
3	1	0	OUT	OUT	OUT	STB_A / ACK_A	IBF_A / OBF_A	$INTR_A$
4	1	1	STB_B / ACK_B	IBF_B / OBF_B	$INTR_B$	STB_A / ACK_A	IBF_A / OBF_A	$INTR_A$

Interfacing 7 Segment LEDs to output port using 8155



Interfacing 7 Segment LEDs to output port using 8155

- Port Addresses
  - Control Register=20H, Port A= 21H, Port B= 22H
- Control word:

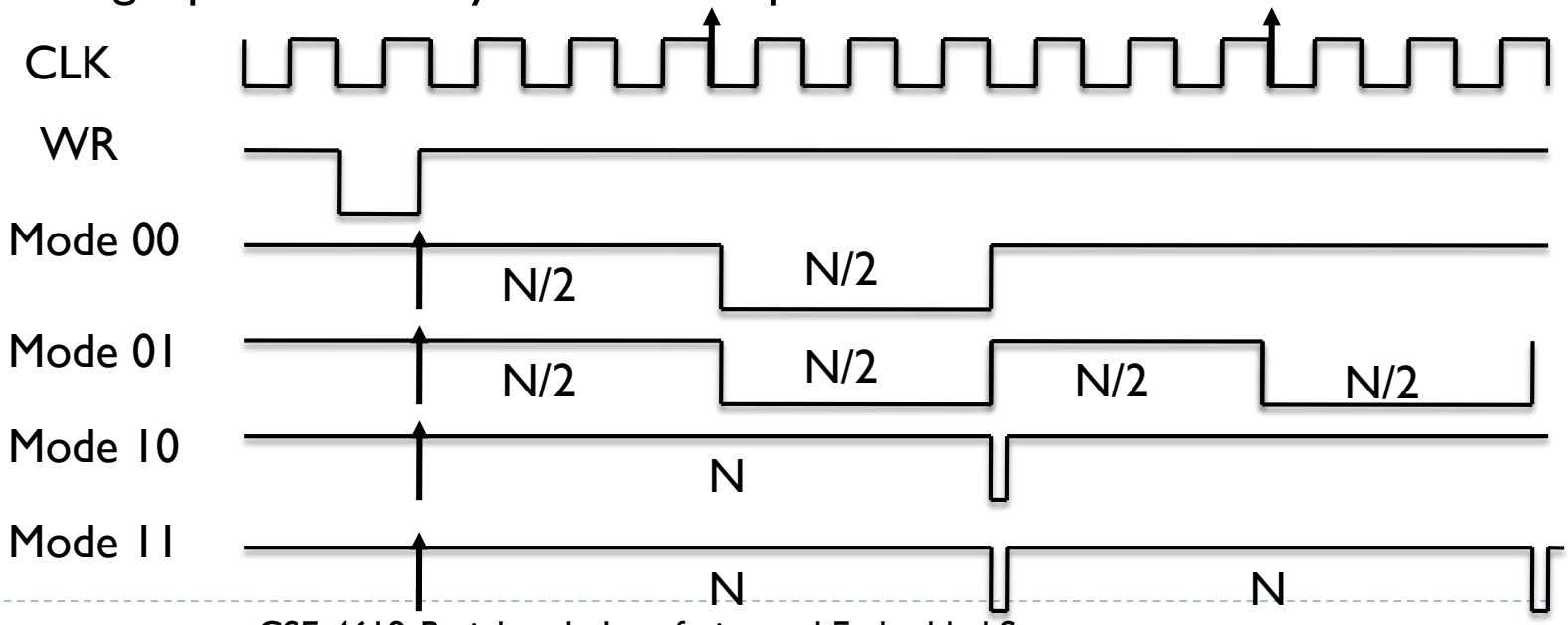
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	1
Timer		Not Applicable		Used for Port C		Port B Output	Port A Output

- Program

```
MVI   A, 03      ; initialize Port A & B for OUTPUT
OUT   20H
MVI   A, BYTE1 ; Display BYTE1 at Port A
OUT   21H
MVI   A, BYTE2 ; Display BYTE2 at port B
OUT   22H
```

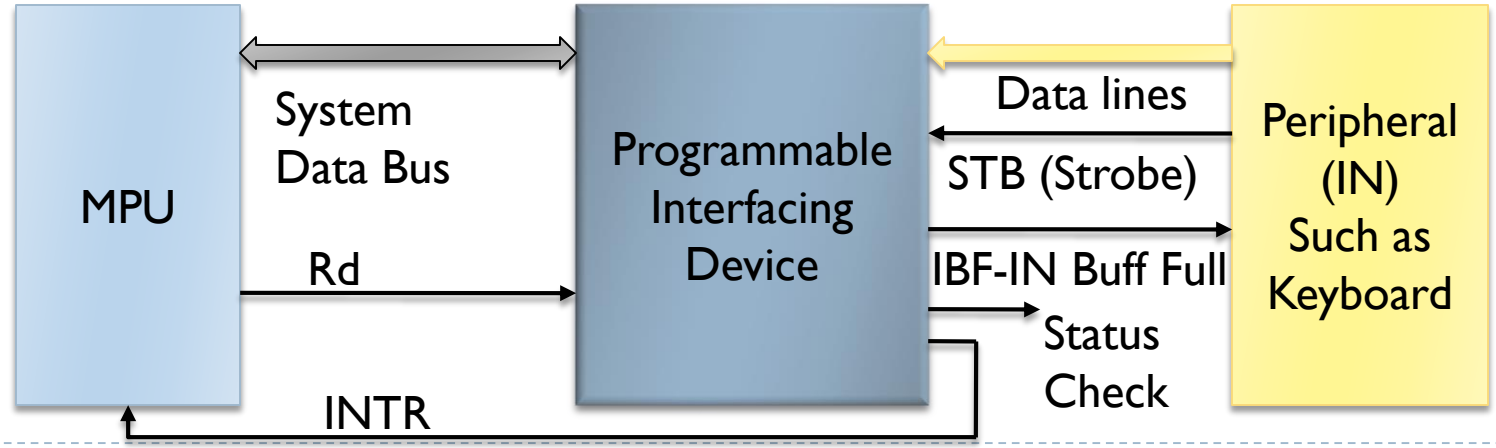
8155 Timer/Counter

- M2, M1: mode bits:
  - **00:** Single square wave of wavelength TC/2 (TC/2, TC/2 if TC is **even**; [TC+1/2], [TC-1/2] if TC is **odd**); It is not continuous.
  - **01:** Square waves of wavelength TC (TC/2, TC/2 if TC is **even**; [TC+1/2],[TC-1/2] if TC is **odd**); It is continuous.
  - **10:** Single pulse *on* the TC'th clock pulse and it is not continuous.
  - **11:** Single pulse *on* every TC'th clock pulse and it is continuous.



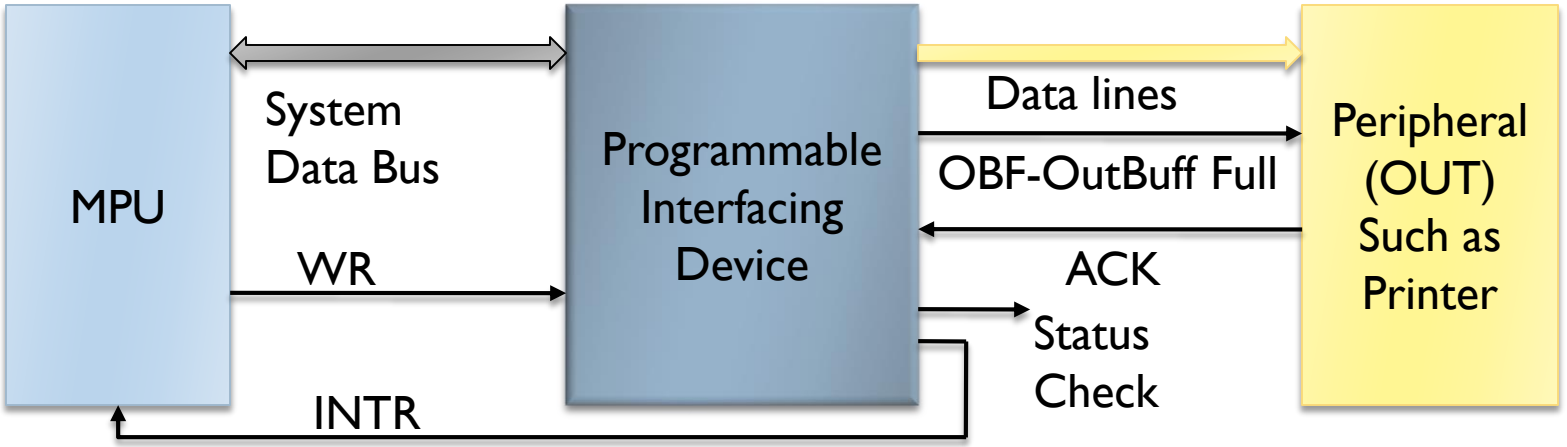
8155 Signals: Input Handshake Signals

- Two Handshake signal (STB, IBF)
- Steps in data input from IN device using 8155
  - Peripheral put data in data line & send handshake signal STB
  - Device inform Peripheral that IN port is full, don't send next byte until read by IBF signal
  - Either MPU check status or Device interrupt to MPU for Reading data from Device



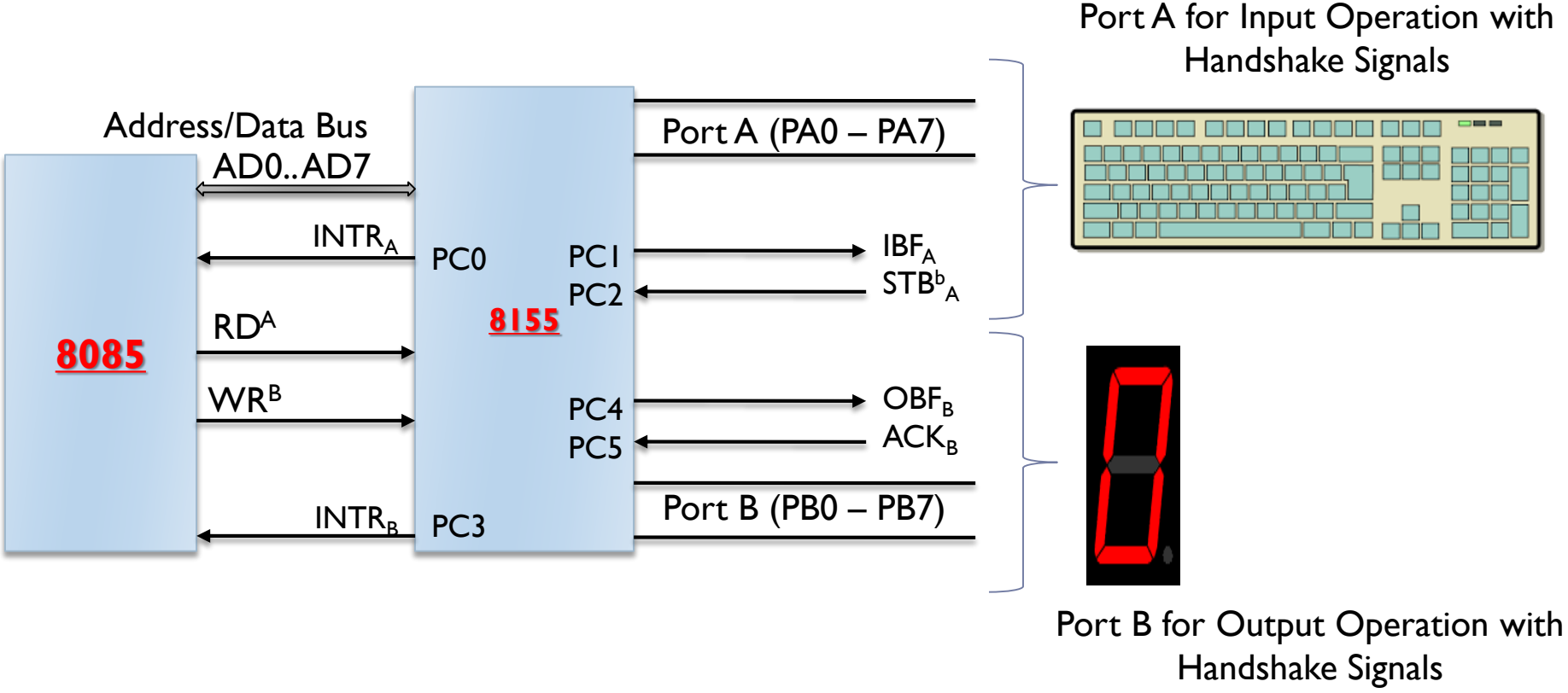
8155 Signals: Output Handshake Signals

- MPU writes byte to the out port of Device by sending WR signal
- Device inform the peripheral by sending handshake OBF, that a byte on the way
- Peripheral ACK the byte by signal to device
- Device Interrupt the MPU to ask to next byte or MPU check the status of Device



8155 Handshake Mode

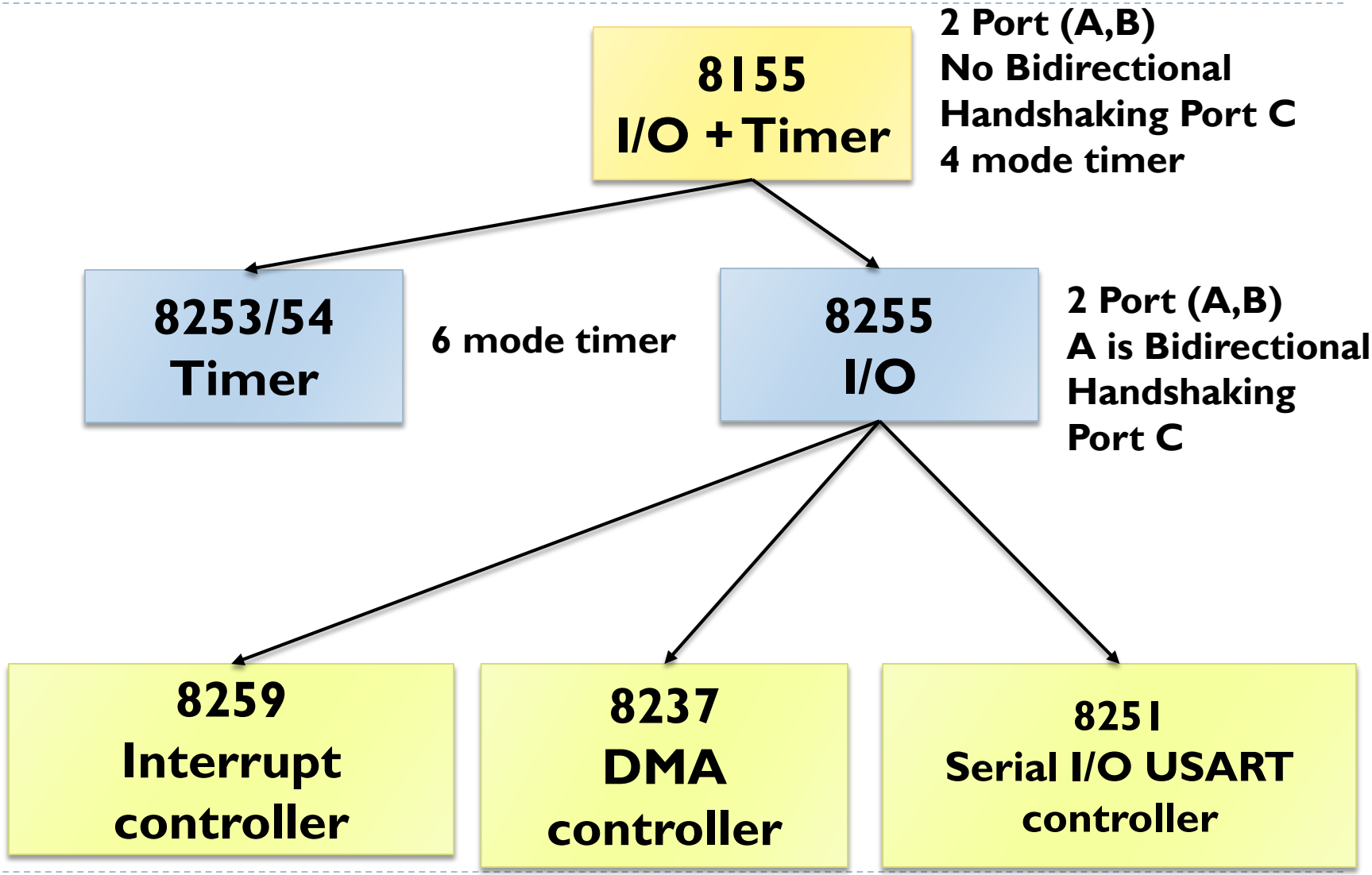
- Port A and B: configured in Handshake mode
- Port A uses PC0, PC1, PC2 of Port C
- Port B uses PC3, PC4, PC5 of Port C



8155 Handshake Mode

- Control Signals
  - STB (Strobe input):
  - BF (Buffer Full): IBF for Input and OBF for Output
  - INTR (INTerrupt Request): Rising edge of STB if INTE =1
  - INTE (INTerrupt Enable): D4 and D5 for Port A & B
- Input, Output Operation: As discussed earlier
- Status Register:
  - MPU check the status Register of port or timer
  - Control register & Status register have same port
  - Differentiated by RD and WR signals

Hierarchy of I/O Control Devices

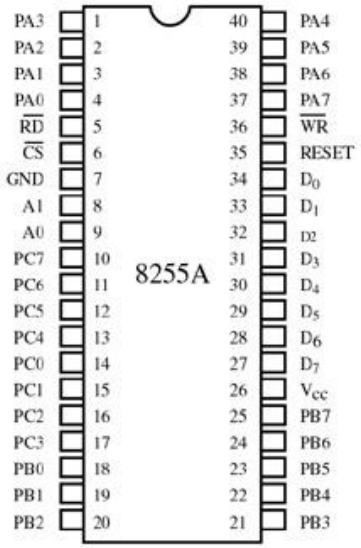


8255 PPI

- Is one of the peripheral controller chips designed to support its processors.
- 8255 is Programmable Peripheral Interface (PPI).
- It is a general purpose parallel I/O Interfacing device.
- It provides 24 I/O lines organized in three 8-bit I/O ports in one 40-pin package.
- The ports are usually labeled A,B, and C.

8255A PPI

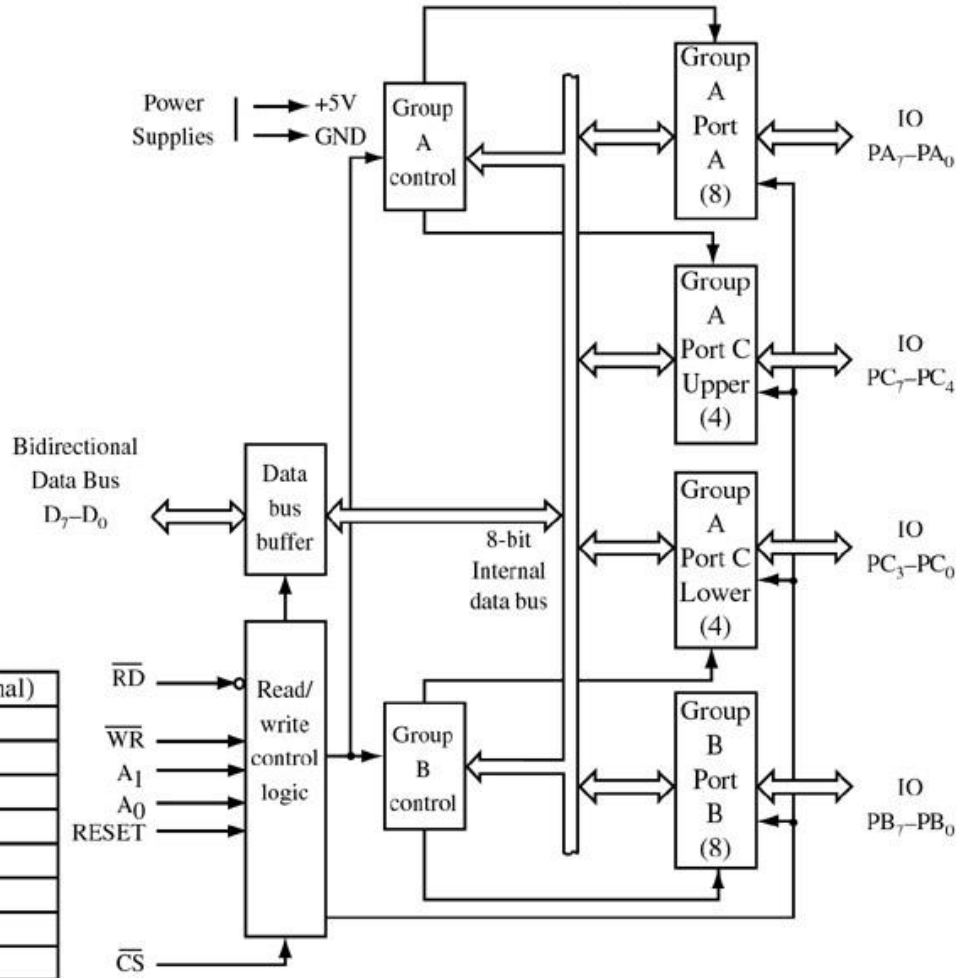
Pin Configuration



Pin Names

D_7–D_0	Data Bus (Bidirectional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0, A1	Port Address
PA7–PA0	Port A (bit)
PB7–PB0	Port B (bit)
PC7–PC0	Port C (bit)
V_{cc}	+5V
GND	0V

8255 Block Diagram



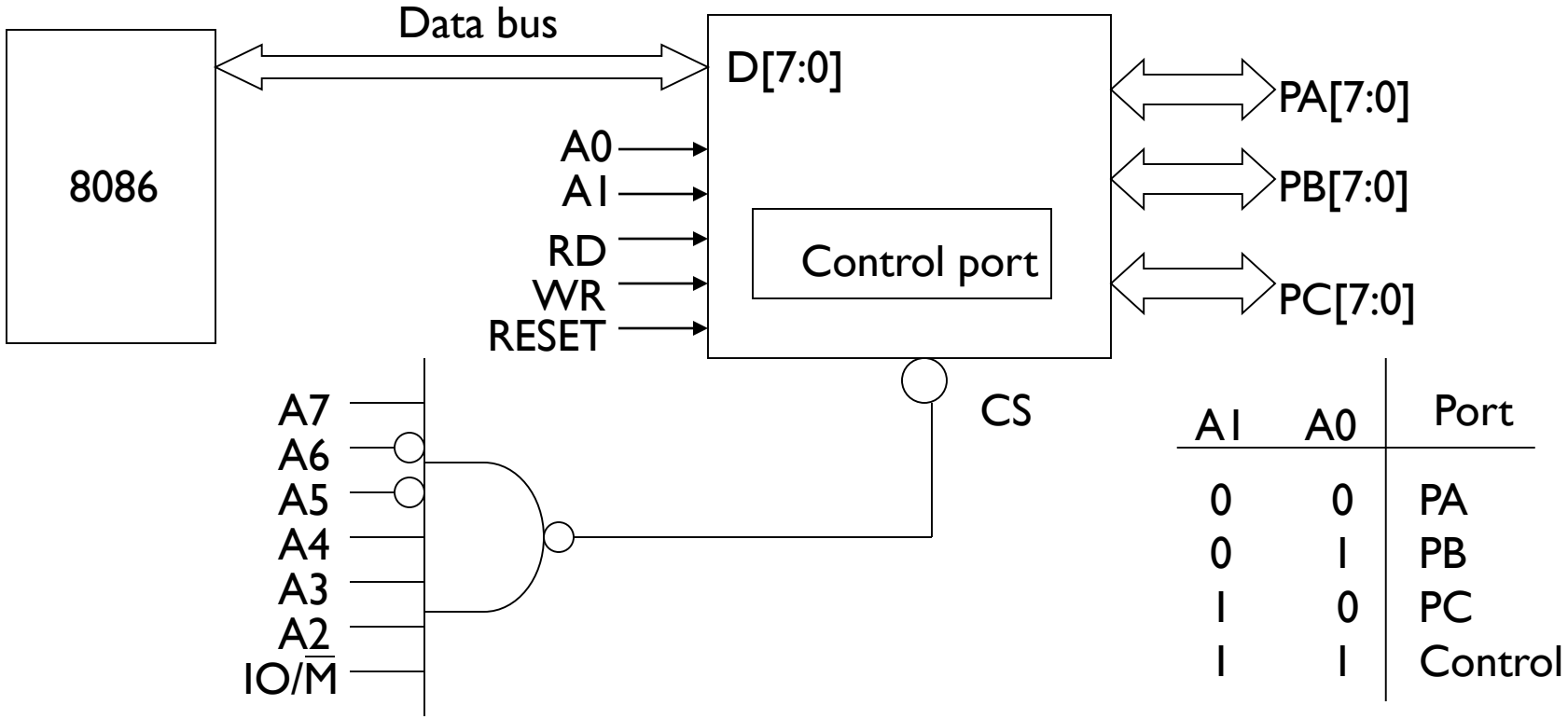
Pins and Ports of 8255A

- 8255A PPI has 24 pins for I/O that are programmable in groups of 12 pins and has three distinct modes of operation.
- In the PC, an 8255 or its equivalent is decoded at I/O ports 60H-63H.

8255 register	Port address
PA (input/output port)	60H
PB (input/output port)	61H
PC (input/output port)	62H
Command register	63H

- Ports A and B can be programmed as an 8-bit input or output port.
- In port C each nibble (four bits) can be programmed separately to be a 4-bit input or output port.
- Only the above size of ports (byte or nibble) can be programmed. **For Example,** individual bit in a port cannot be programmed.
- However, what make 8255 a versatile devise is its programming modes

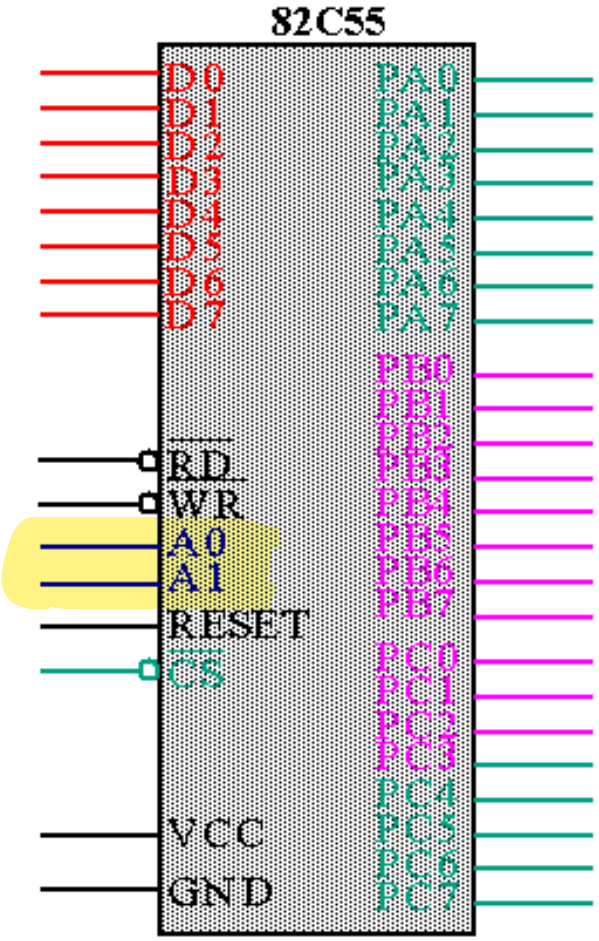
8255A Interfacing with 8086



A1	A0	Port
0	0	PA
0	1	PB
1	0	PC
1	1	Control

- A2 to A7 are decoded to provide Chip Select. Hence 2^6 8255A chips can be used is a system. (for Isolated I/O use IO/$\overline{M}$=1, else IO/$\overline{M}$=0).
- A0 and A1 are used to select port and control register

8255A Interfacing with 8086



Group A

Port A (PA7-PA0) and upper half of port C (PC7 - PC4)

Group B

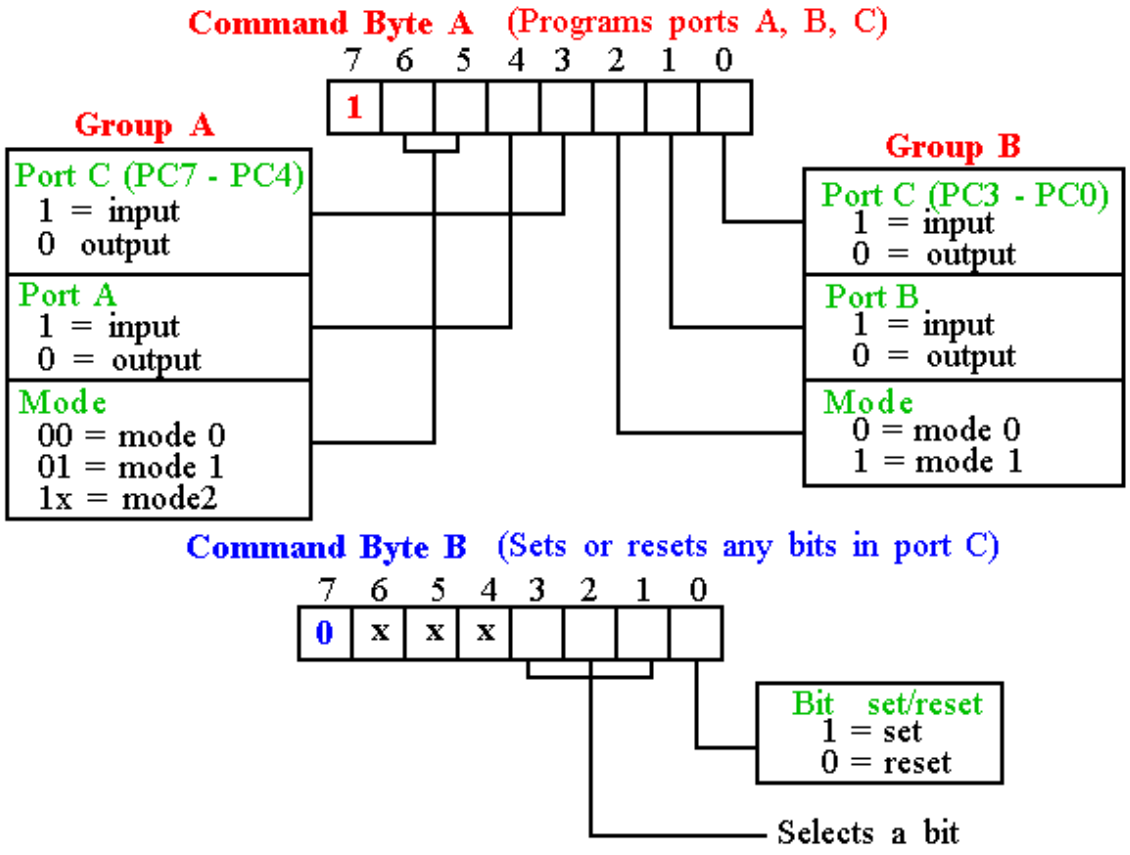
Port B (PB7-PB0) and lower half of port C (PC3 - PC0)

I/O Port Assignments

A_1	A_0	Function
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Command Register

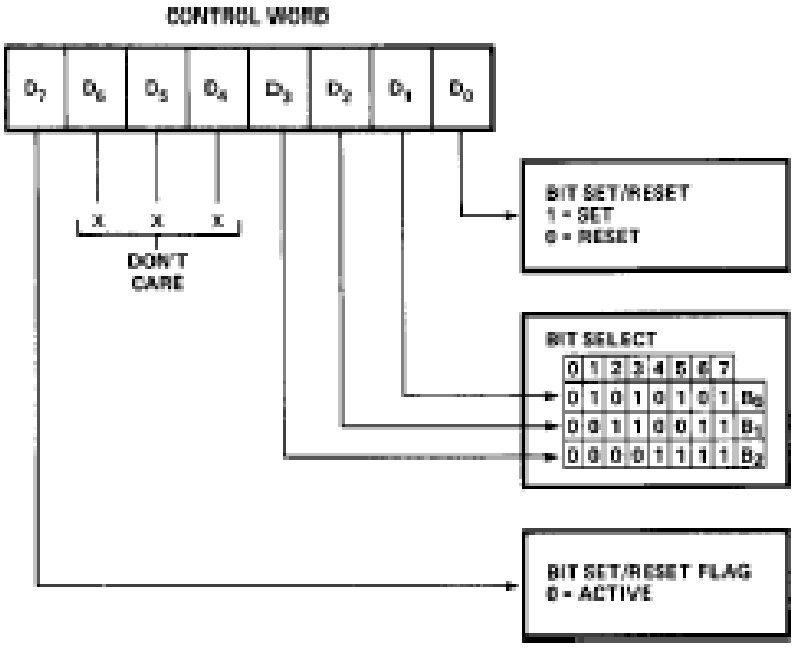
Programming Modes of 8255A

- 8255 has three operation modes: *mode 0, mode 1, and mode 2*
- **Mode 0:** For basic Input-Output
- **Mode 1:** For Strobe (with handshaking) Input-Output
- **Mode 2:** Strobe (with handshaking) bi-directional Input-Output



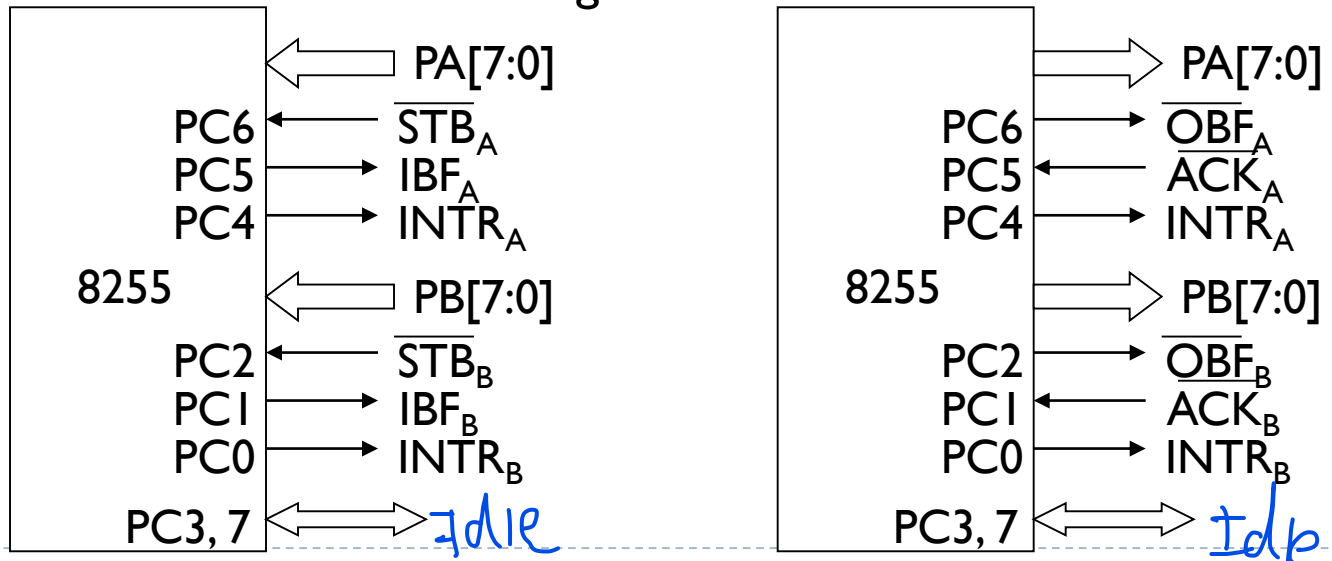
8255 Control Word

- There is a control word to program the actions of the chip.
- **The chip mode is set when bit D7 of the control word has the value 1**
- Data direction is controlled by several bits where 1 indicates **input** and 0 indicates **output**:
  - D0 - Port C lower nibble
  - D1 - Port B
  - D3 - Port C upper nibble
  - D4 - Port A
- D2 sets the mode for port B.
- D6, D5 set the mode for port A.



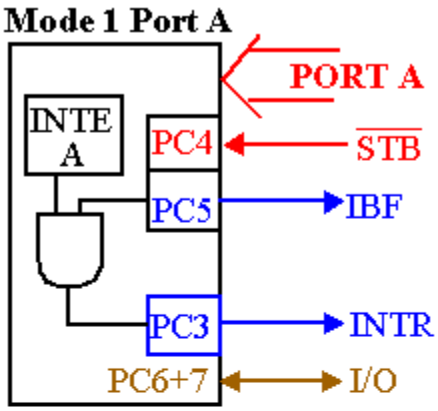
Programming Modes of 8255A

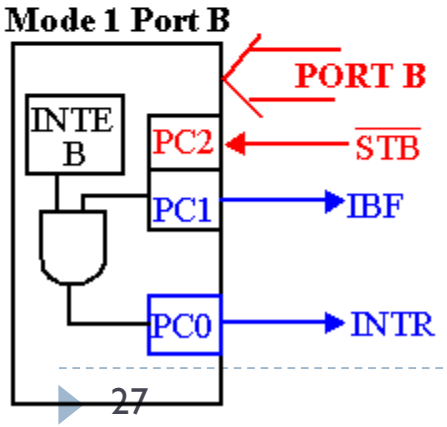
- **Mode 0:**
  - Ports A, B, and C can be individually programmed as input or output ports
  - Port C is divided into two 4-bit ports (for Input or output) which are independent from each other
- **Mode 1:**
  - Ports A and B as a whole are programmed as input or output ports
  - Port C is used for handshaking

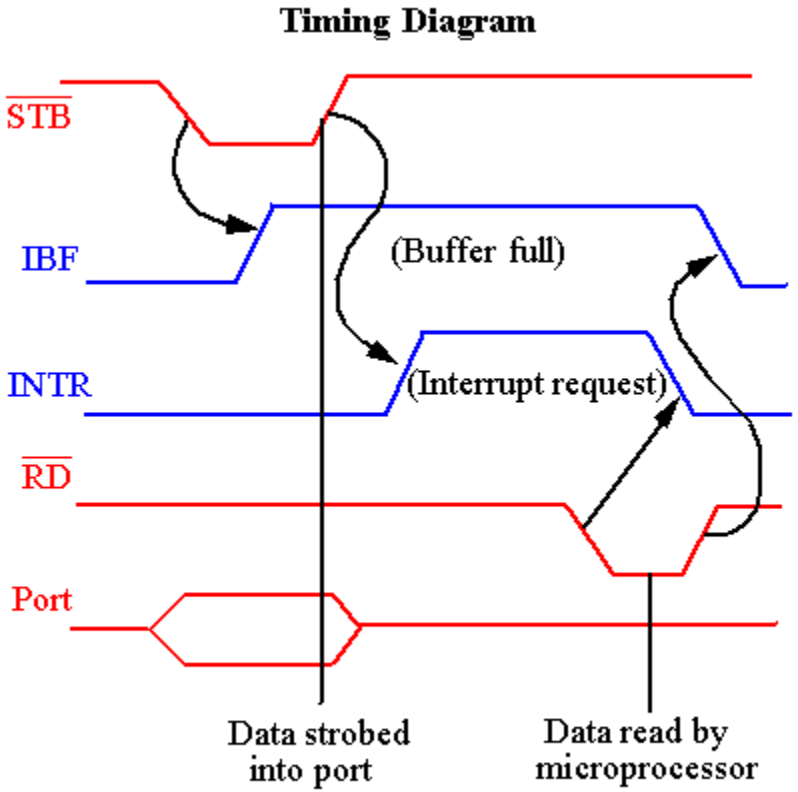


Mode 1

$\overline{\text{STB}}$	The strobe input loads data into the port latch on a 0-to-1 transition
IFB	**Input buffer full** is an output indicating that the input latch contain information
INTR	**Interrupt request** is an output that requests an interrupt
INTE	The **interrupt enable signal** is neither an input nor an output; it is an internal bit programmed via the PC4(port A) or PC2(port B) bits.
PC7,PC6	The port C pins 7 and 6 are general-purpose I/O pins that are available for any purpose.







Mode 1

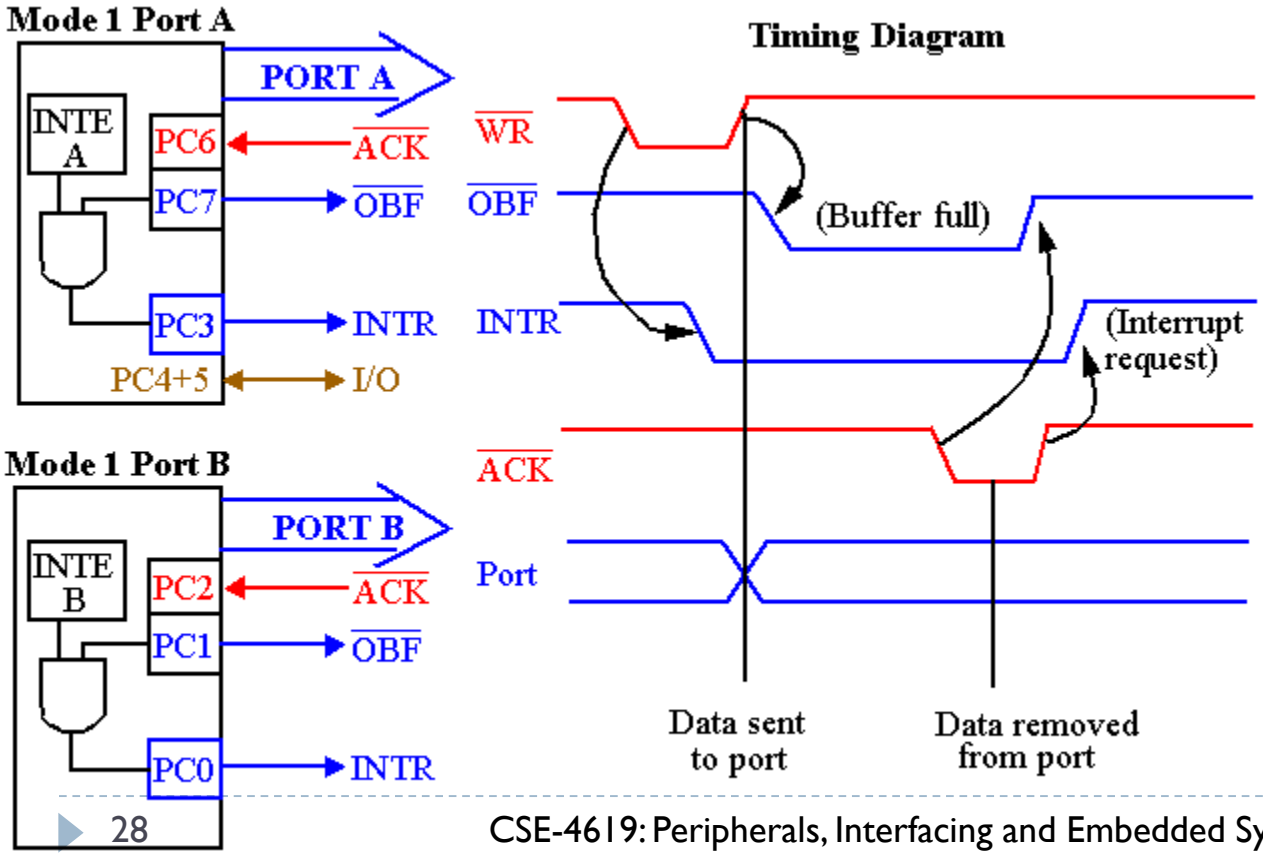
$\overline{\text{OBF}}$ **Output buffer full** is an output that goes low when data is latched in either port A or port B. Goes low on $\overline{\text{ACK}}$.

$\overline{\text{ACK}}$ The **acknowledge** signal causes the $\overline{\text{OBF}}$ pin to return to 0. This is a response from an external device.

INTR **Interrupt request** is an output that requests an interrupt

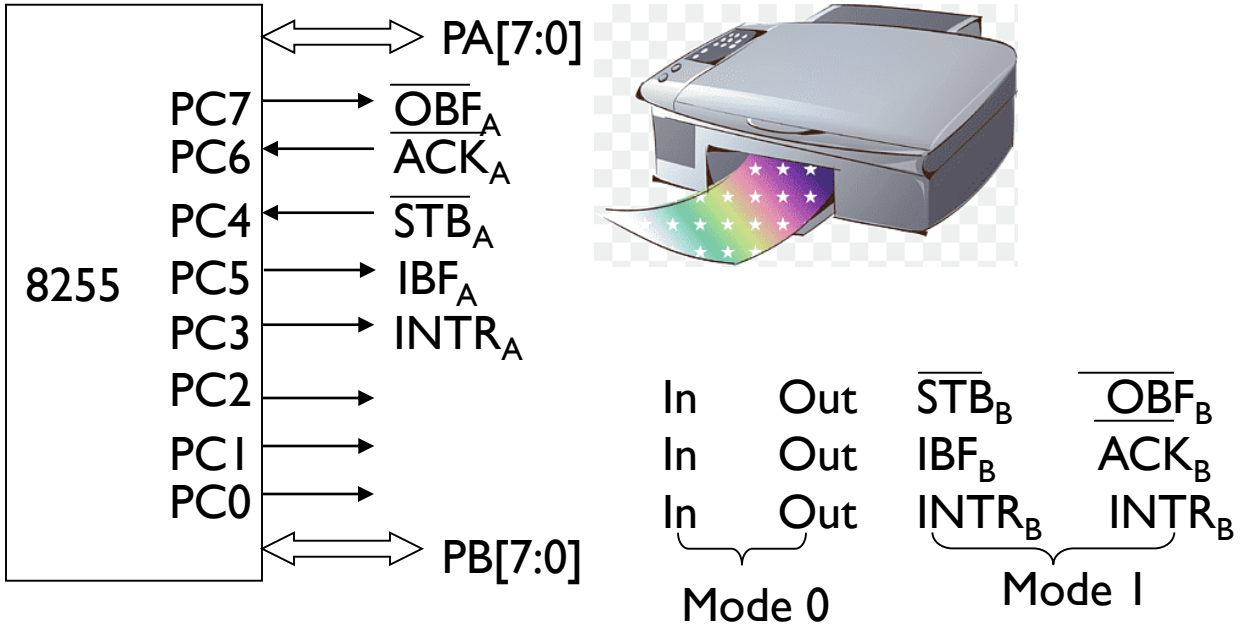
INTE The **interrupt enable signal** is neither an input nor an output; it is an internal bit programmed via the PC6(port A) or PC2(port B) bits.

PC5,PC4 The port C pins 5 and 4 are general-purpose I/O pins that are available for any purpose.



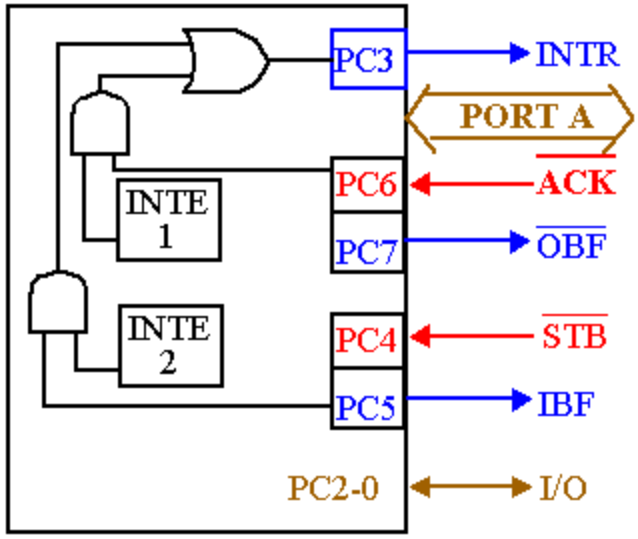
Programming Modes of 8255A

- **Mode 2:**
  - Port A is programmed to be bi-directional input-output port
  - Port C is for handshaking
  - Port B can be either input or output in mode 0 or mode 1



Mode 2

INTR	**Interrupt request** is an output that requests an interrupt
$\overline{\text{OBF}}$	**Output buffer full** is an output indicating that the output buffer contains data for the bi-directional bus
$\overline{\text{ACK}}$	**Acknowledge** is an input that enables tri-state buffers which are otherwise in their high-impedance state
$\overline{\text{STB}}$	The strobe input loads data into the port A latch
IFB	**Input buffer full** is an output indicating that the input latch contains information for the external bi-directional bus
INTE	**Interrupt enable** are internal bits that enable the INTR pin. Bit PC6(INTE1) and PC4(INTE2)
PC2,PC1 and PC0	Theses port C pins are general-purpose I/O pins that are available for any purpose.



This timing diagram is a combination of the Mode 1 Strobed Input and Mode 1 Strobed Output Timing diagrams.

Thank You !!