Islamic University of Technology

Lab 5

EEE-4484

Digital Electronics and Pulse Techniques

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Task – 1: Full Adder Circuit

VHDL:

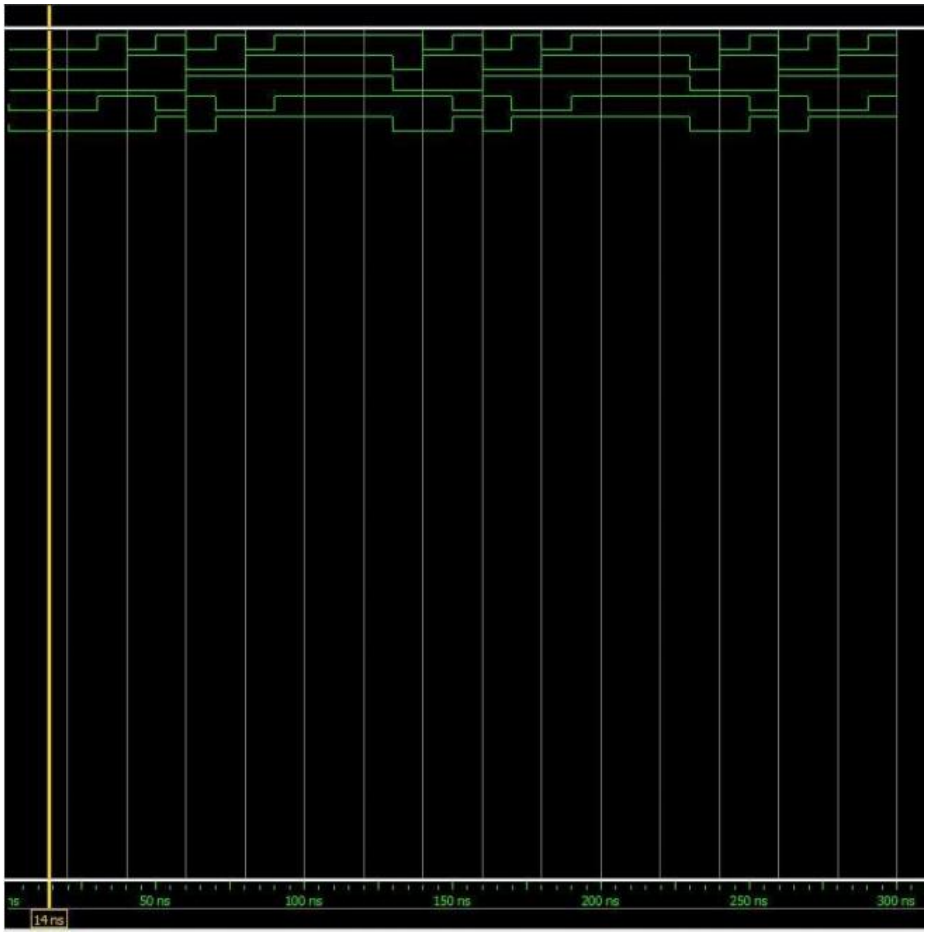
```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity full_adder is
port(
    A, B, Cin : in STD_LOGIC;
    S, Cout : out STD_LOGIC
);
end full_adder;

architecture gate_level of full_adder is

begin
    S <= A XOR B XOR Cin ;
    Cout <= (A AND B) OR (Cin AND A) OR (Cin AND B) ;
end gate_level;
```

Testbench:

```vhdl
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY tb_full_adder IS
END tb_full_adder;

ARCHITECTURE behavioral OF tb_full_adder IS

COMPONENT full_adder
PORT(
    A, B, Cin : IN std_logic;
    S, Cout : OUT std_logic
);
END COMPONENT;

-- Inputs
signal A : std_logic := '0';
signal B : std_logic := '0';
signal Cin : std_logic := '0';

-- Outputs
signal S : std_logic;
signal Cout : std_logic;

BEGIN

uut: full_adder PORT MAP(
    A => A,
    B => B,
    Cin => Cin,
    S => S,
    Cout => Cout
);

```

```
stim_proc: process
begin
    wait for 30 ns;

    A <= '1';
    B <= '0';
    Cin <= '0';
    wait for 10 ns;

    A <= '0';
    B <= '1';
    Cin <= '0';
    wait for 10 ns;

    A <= '1';
    B <= '1';
    Cin <= '0';
    wait for 10 ns;

    A <= '0';
    B <= '0';
    Cin <= '1';
    wait for 10 ns;

    A <= '1';
    B <= '0';
    Cin <= '1';
    wait for 10 ns;

    A <= '0';
    B <= '1';
    Cin <= '1';
    wait for 10 ns;

    A <= '1';
    B <= '1';
    Cin <= '1';
    wait for 10 ns;

end process;

END architecture behavioral;
```

Output:



Task – 2: 1 to 8 Multiplexer

VHDL:

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity demux_1x8 is
5  port(
6      i:in std_logic;
7      s:in std_logic_vector(2 downto 0);
8      o:out std_logic_vector(7 downto 0)
9  );
10 end demux_1x8;
11
12 architecture behavioral of demux_1x8 is
13 begin
14     o(0)<=i when s="000" else'0';
15     o(1)<=i when s="001" else'0';
16     o(2)<=i when s="010" else'0';
17     o(3)<=i when s="011" else'0';
18     o(4)<=i when s="100" else'0';
19     o(5)<=i when s="101" else'0';
20     o(6)<=i when s="110" else'0';
21     o(7)<=i when s="111" else'0';
22 end behavioral;
23
```

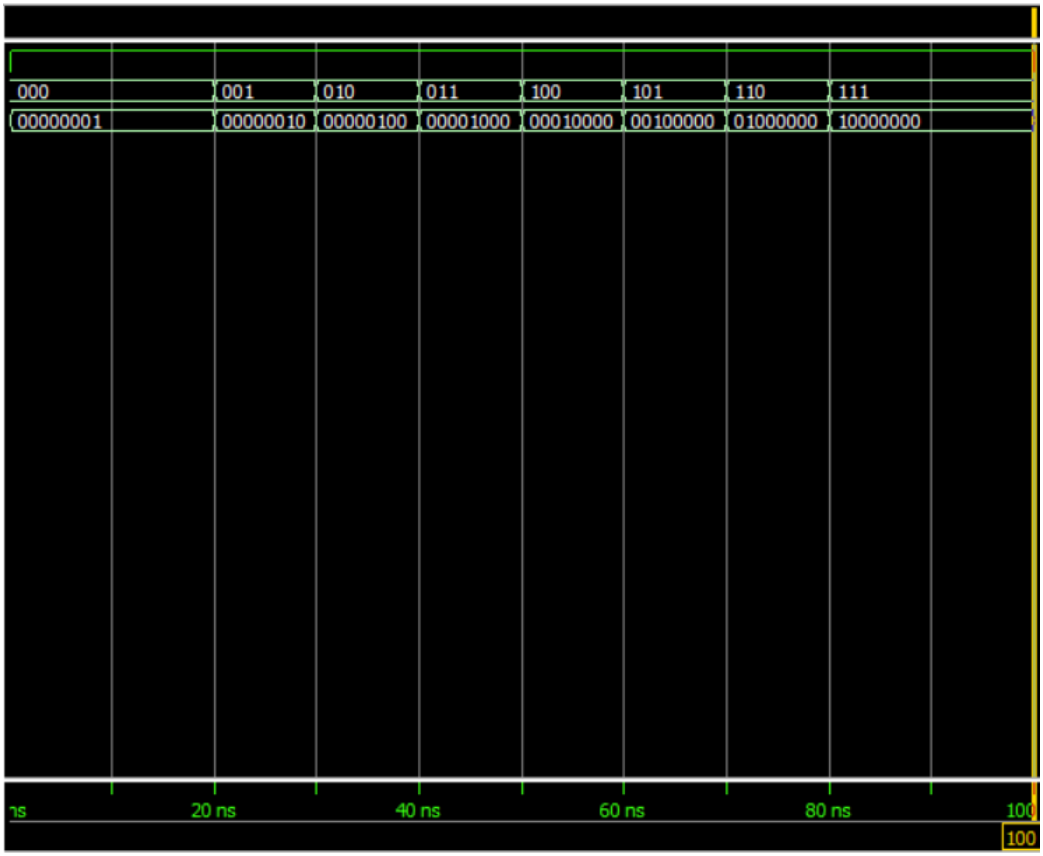
Testbench:

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity tb_demux_1x8 is
5  end tb_demux_1x8;
6
7  architecture behavioral of tb_demux_1x8 is
8
9  component demux_1x8
10 port(
11     i:in std_logic;
12     s:in std_logic_vector(2 downto 0);
13     o:out std_logic_vector(7 downto 0)
14 );
15 end component;
16
17 -- Inputs
18 signal tb_i : std_logic := '0';
19 signal tb_s : std_logic_vector (2 downto 0) := (others => '0');
20
21 -- Outputs
22 signal tb_o : std_logic_vector (7 downto 0) := (others => '0');
23
24 begin
25
26 uut: demux_1x8 port map (
27     i => tb_i,
28     s => tb_s,
29     o => tb_o
30 );
31
```

```
33 -- stimulus process
34 stim_process: process
35 begin
36     tb_i<='1';
37     wait for 10 ns;
38     tb_s <= "000";
39     wait for 10 ns;
40     tb_s <= "001";
41     wait for 10 ns;
42     tb_s <= "010";
43     wait for 10 ns;
44     tb_s <= "011";
45     wait for 10 ns;
46     tb_s <= "100";
47     wait for 10 ns;
48     tb_s <= "101";
49     wait for 10 ns;
50     tb_s <= "110";
51     wait for 10 ns;
52     tb_s <= "111";
53     wait for 20 ns;
```

```
    tb_i<='0';
    wait for 10 ns;
    tb_s <= "000";
    wait for 10 ns;
    tb_s <= "001";
    wait for 10 ns;
    tb_s <= "010";
    wait for 10 ns;
    tb_s <= "011";
    wait for 10 ns;
    tb_s <= "100";
    wait for 10 ns;
    tb_s <= "101";
    wait for 10 ns;
    tb_s <= "110";
    wait for 10 ns;
    tb_s <= "111";
    wait for 20 ns;
end process;

end architecture behavioral;
```

Output:



Task – 3: 4-bit Arithmetic Logic Unit (ALU)

VHDL:

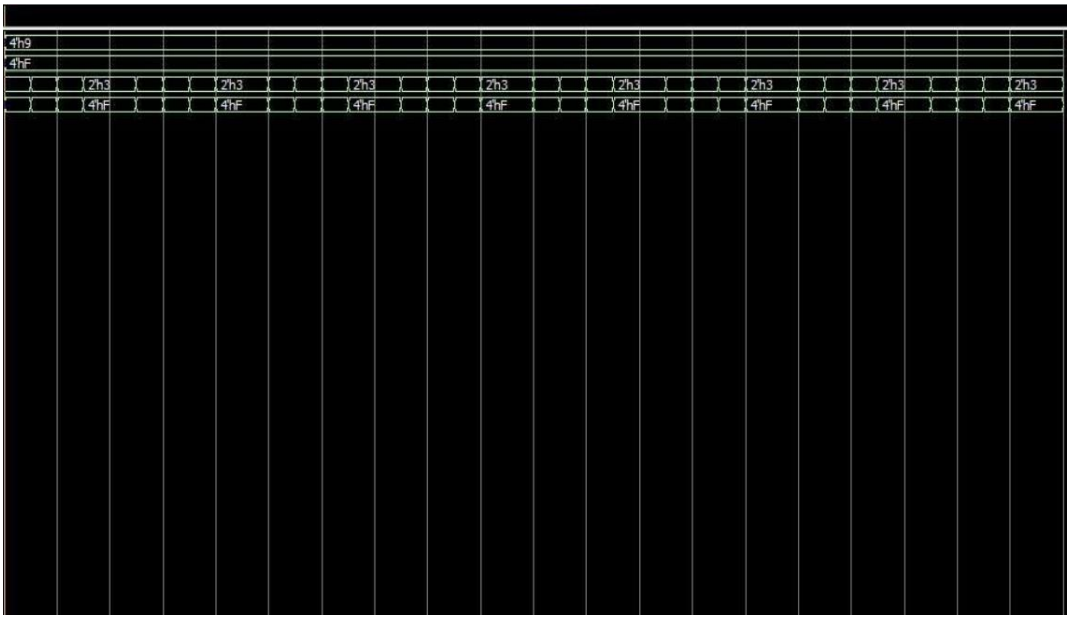
```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.NUMERIC_STD.ALL;
4
5  entity ALU_4bit is
6  port (
7      a : in signed(3 downto 0);
8      b : in signed(3 downto 0);
9      s : in STD_LOGIC_VECTOR (1 downto 0);
10     o : out signed(3 downto 0));
11 end ALU_4bit;
12
13 architecture behavioral of ALU_4bit is
14 begin
15 process(a, b, s)
16     begin
17     case s is
18         when "00" => o <= a + b;
19         when "01" => o <= a - b;
20         when "10" => o <= a AND b;
21         when "11" => o <= a OR b;
22         when others => NULL;
23     end case;
24 end process;
25
26 end behavioral;
```

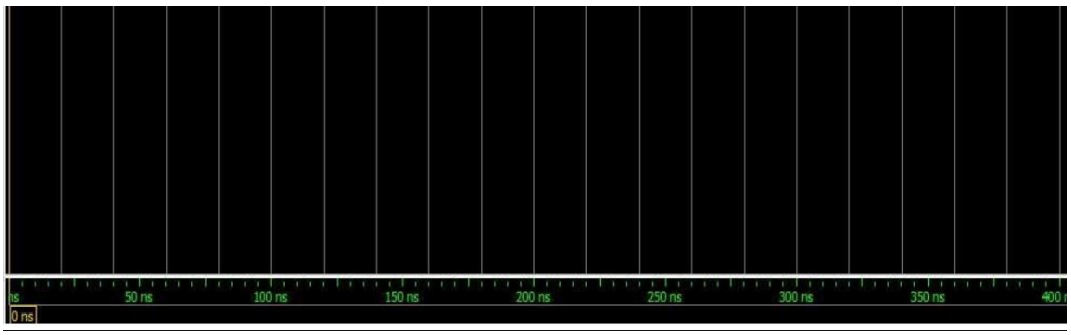
Testbench:

```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.ALL;
3  USE ieee.numeric_std.ALL;
4
5  ENTITY tb_ALU_4BIT IS
6  END tb_ALU_4BIT;
7
8  ARCHITECTURE behavioral OF tb_ALU_4BIT IS
9
10 -- Component Declaration for the Unit Under Test (UUT)
11
12 COMPONENT ALU_4BIT
13 PORT(
14     a : IN signed(3 downto 0);
15     b : IN signed(3 downto 0);
16     s : IN std_logic_vector(1 downto 0);
17     o : OUT signed(3 downto 0)
18 );
19 END COMPONENT;
20
21
22 -- Inputs
23 signal tb_a : signed(3 downto 0) := (others => '0');
24 signal tb_b : signed(3 downto 0) := (others => '0');
25 signal tb_s : std_logic_vector(1 downto 0) := (others => '0');
26
27 -- Outputs
28 signal tb_o : signed(3 downto 0);
29
30 BEGIN
31
32 -- Instantiate the Unit Under Test (UUT)
33 uut: ALU_4BIT PORT MAP(
34     a => tb_a,
35     b => tb_b,
36     s => tb_s,
37     o => tb_o
38 );
39
```

```
40    -- Stimulus process
41    stim_proc: process
42    begin
43
44        tb_a <= "1001";
45        tb_b <= "1111";
46
47        tb_s <= "00";
48        wait for 10 ns;
49        tb_s <= "01";
50        wait for 10 ns;
51        tb_s <= "10";
52        wait for 10 ns;
53        tb_s <= "11";
54        wait for 20 ns;
55
56    end process;
57
58    END behavioral;
```

Output:





Task – 4: Synchronous 5-bit Shift Register

VHDL:

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity shift_reg_5bit is
port(
     clk : in std_logic;
     D: in std_logic_vector(3 downto 0);
     Q: out std_logic_vector(3 downto 0)
);
end shift_reg_5bit;

architecture behavioral of shift_reg_5bit is

begin
process (clk,D)
     begin
     if (clk'event and clk='1') then Q <= D;
     end if;
end process;

end behavioral;
```

Testbench:

```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity tb_shift_reg_5bit is
end tb_shift_reg_5bit;

architecture behavioral of tb_shift_reg_5bit is

component shift_reg_5bit
port(
     clk : in std_logic;
     D : in std_logic_vector(3 downto 0);
     Q : out std_logic_vector(3 downto 0)
);
end component;

signal tb_clk : std_logic;
signal tb_D : std_logic_vector(3 downto 0);
signal tb_Q : std_logic_vector(3 downto 0);
constant clk_period : time := 100 ns;

begin
uut: shift_reg_5bit port map(
     clk => tb_clk,
     D => tb_D,
     Q => tb_Q
);

-- clock process
clk_process: process
begin
     tb_clk <= '0';
     wait for clk_period/2;
     tb_clk <= '1';
     wait for clk_period/2;
end process;

```

```
38  -- stimulus process
39  stim_process: process
40  begin
41      tb_D<="0000";
42      wait for 100 ns;
43      tb_D <= "0100";
44      wait for 100 ns;
45      tb_D <= "1010";
46      wait for 100 ns;
47      tb_D <= "0110";
48      wait for 100 ns;
49  end process;
50
51  end architecture behavioral;
52
53
```

Output: