ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
Department of Computer Science and Engineering (CSE)

SEMESTER FINAL EXAMINATION **WINTER SEMESTER, 2019-2020**

DURATION: 1 Hour **FULL MARKS: 50**

CSE 4305: Computer Organization and Architecture

General Instructions

- Write your **Name**, **Student-ID** and **Course Code** on the top of the first page. Maintain a **serial number** on the Top-right corner of each page.
- Answer all the questions. Figures in the right margin indicate marks.
- Sit in proper position and maintain the environment as per the Guidelines.
- No examinee is allowed to scan the file unless 1 hour is finished.
- For any circumstances, follow the instructions of the invigilator.

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1 What is the difference between *micro-operation* and *micro-instruction*? Write the sequence of events (micro-operations) of ***"interrupt cycle"*** symbolically employing common processor registers with appropriate data flow diagram. 3+4 +3

2 Many processor designs include a register or set of registers, often known as the program status word (PSW) or flags, that contain status information. These flags typically contain condition codes plus other status information resulted from the immediately last operation. If the last operation was a subtraction operation between two operands, A and B containing 11110000 and 00010100 (***i.e.*** A-B), what would be the value of <u>any three</u> of the following flags? 3

i. Carry
ii. Zero
iii. Overflow
iv. Sign
v. Even Parity
vi. Equal

3 Briefly describe different kinds of data hazards in any instruction pipeline system. (**Note:** Appropriate examples from each type are highly appreciable). 5

4 The Intel 8088 consists of a bus interface unit (BIU) and an execution unit (EU), which form a 2-stage pipeline. The BIU fetches instructions into a 4-byte instruction queue. The BIU also participates in address calculations, fetches operands, and writes results in memory as requested by the EU. If the bus is free and there is no outstanding requests and branch instructions, then answer the following questions: 2+3 +3

i. If the tasks done by the both units take equal time, by what factor does pipeline improve the performance of the 8088?
ii. Draw the timing diagram of instruction pipeline operation for 5 instructions.
iii. If there are 100 instructions in a program to be executed by the 8088, calculate the total time required to complete this program availing the instruction pipeline advancement.

5 In a 16-bit processor, at a certain time of the execution of instructions from main memory, following instructions are appeared (figure a): 6

Memory address	Content
200	XXMM
201	YYYY
202	WXYZ

Figure a: Contents of memory

Where XX denotes the opcode that instructs to load content to the register AC (accumulator), MM signifies the mode field, YYYY contains the decimal value 500 and WXYZ indicates the next instruction. For a specific mode, register R1 might be used containing the value 400. Assume that location 399 contains 999, location 400 contains 1000 and onwards accordingly. Determine the **effective address** and the **operand** to be loaded for <u>any two</u> of the following address modes represented by MM:

i. Direct
ii. Indirect
iii. PC Relative
iv. Register
v. Register Indirect

6 Convert the following high-level language statement to corresponding machine language program using one-address instruction format: 4

$$Y = (A\ X\ B) + (C\ X\ D) + E$$

7 Briefly describe the operation of the TLB and Cache to fetch any appropriate page in virtual memory system following the depiction given in figure b: 4

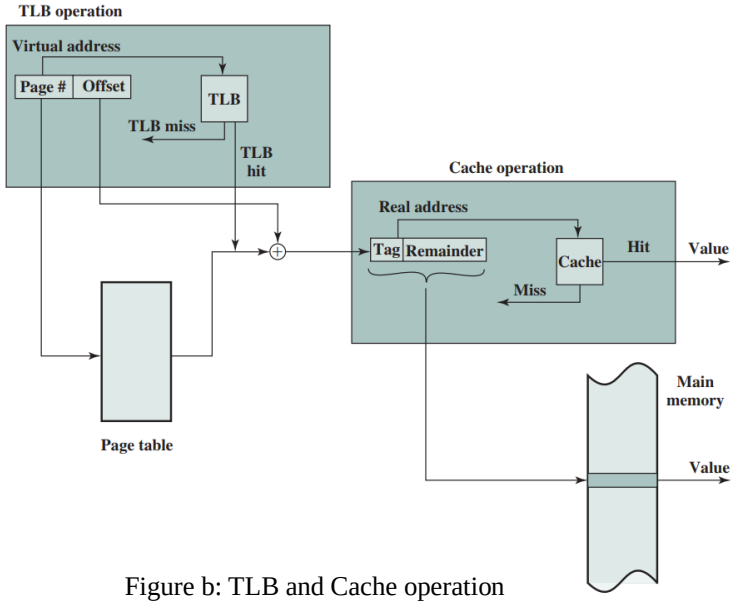

Figure b: TLB and Cache operation

8 What are the design issues to implement an interrupt driven I/O if there are multiple I/O devices? Mention the name of the appropriate approaches to overcome those issues. 5

9 Consider a magnetic disk drive with 10 surfaces, 600 tracks per surface, and 72 sectors per track. Sector size is 512 B. The average seek time is 10 ms, the track-to-track access time is 1.5 ms, and the drive rotates at 3600 rpm. Successive tracks in a cylinder can be read without head movement. 5

i. What is the disk capacity?
ii. What is the average access time? Assume this file is stored in successive sectors and tracks of successive cylinders start at sector 0, track 0 of cylinder ***i***.
iii. Estimate the time required to transfer a 5-MB file.