CSE 4305
Computer Organization and Architecture

Internal Memory

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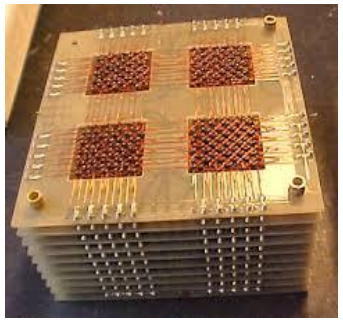
Internal Memory

Semiconductor Main Memory

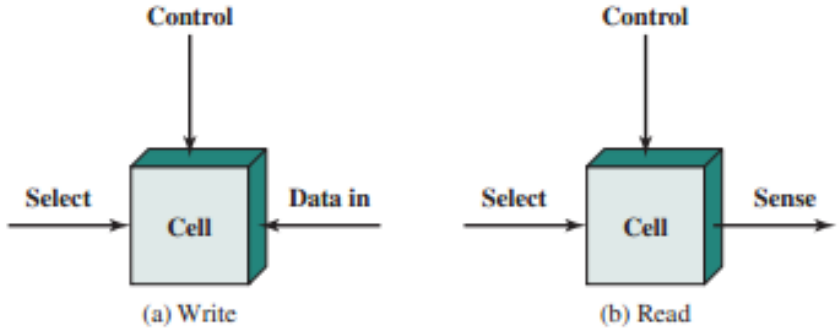
- **Previously** doughnut shaped ferromagnetic loops (cores) were used in **main memory** – but now, **semiconductor chips** are used in the place of magnetic core memory. Types:



Memory Type	Category	Erasure	Write Mechanism	Volatility
Random-access memory (RAM)	Read-write memory	Electrically, byte-level	Electrically	Volatile
Read-only memory (ROM)	Read-only memory	Not possible	Masks	Nonvolatile
Programmable ROM (PROM)			Electrically	
Erasable PROM (EPROM)	Read-mostly memory	UV light, chip-level		
Electrically Erasable PROM (EEPROM)		Electrically, byte-level		
Flash memory		Electrically, block-level		

Organization

- **Basic element** of semiconductor memory – **memory cell**
- **Property** of memory cell:
  - Has **two stable states** – 1 and 0
  - Capable of being **written** to set state
  - Capable of being **read** to sense state
- Has **3 functional terminals**



RAM

- **R**andom **A**ccess **M**emory
- **Most common type** of semiconductor memory
- **Misuse of this term** of only confining this device as accessing random even though others like ROM, Flash memory are also capable of accessing random
- **Application** - Temporary storage
- **Volatile**
- Possible both **read and write**
- **Newer RAM are non volatile**
- **Two forms** – DRAM and SRAM

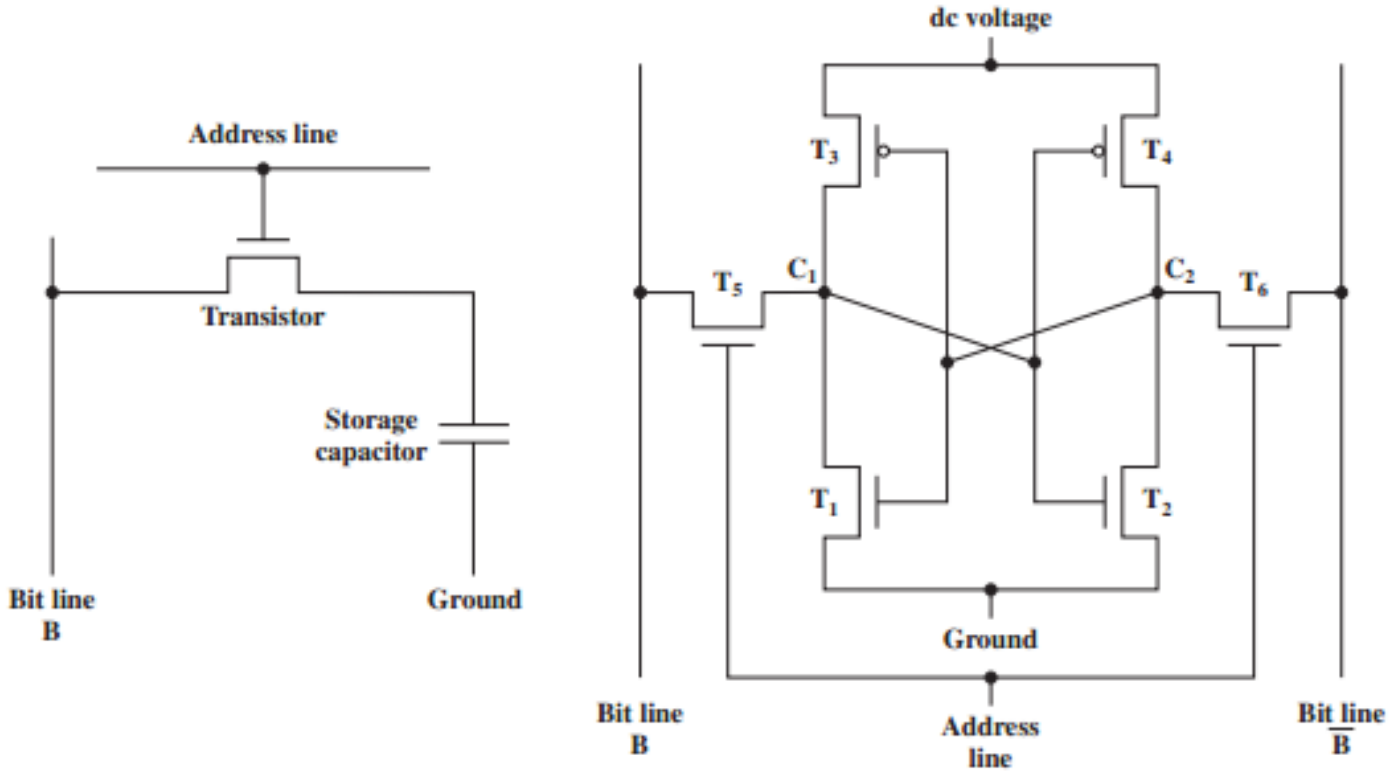
DRAM

- **D**ynamic RAM
- **Store data** as **charge** or **capacitance**
- As charge or capacitance has the **tendency of decaying naturally**, a **refreshing circuitry** is required though power is supplied – **Dynamic**
- **Write operation** – voltage applied
- **Read operation** – sense the charge through an amplifier

SRAM

- **S**tatic RAM
- Store value using **flip flops**
- Hold data as long as power is supplied
- **4 transistors** are used to store data
- Data is available both in its **original and complement form**
- **No refresh circuit** is required

SRAM and DRAM: 1 bit cell structure



(a) Dynamic RAM (DRAM) cell

(b) Static RAM (SRAM) cell

SRAM vs DRAM

- Which one is better?
  - Cost
  - Capacity
  - Power consumption
  - So on

ROM

- **R**ead **O**nly **M**emory
- **Permanent** pattern of data
- **Non volatile** - No power source is required
- **Easy to read** but **impossible to write**
- **Application**:
  - Microprogramming
    - Process of writing microcode for a microprocessor. Microcode is low-level code that defines how a microprocessor should function when it executes machine-language instructions.
  - Library subroutines
  - System programs
  - Function tables

ROM…

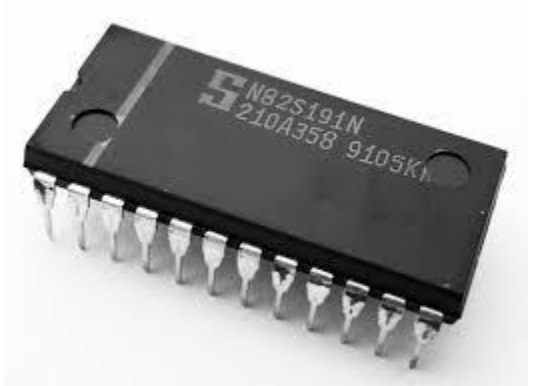
- **Created as any other IC** – data is actually **wired/ fabricated**
- **Problems:**
  - **Data insertion cost** is huge
  - **No room for error** – if one bit is wrong, whole batch of ROMs (produced in bulk) will be invalid

Types of ROM

- PROM
- EPROM
- EEPROM
- Flash Memory

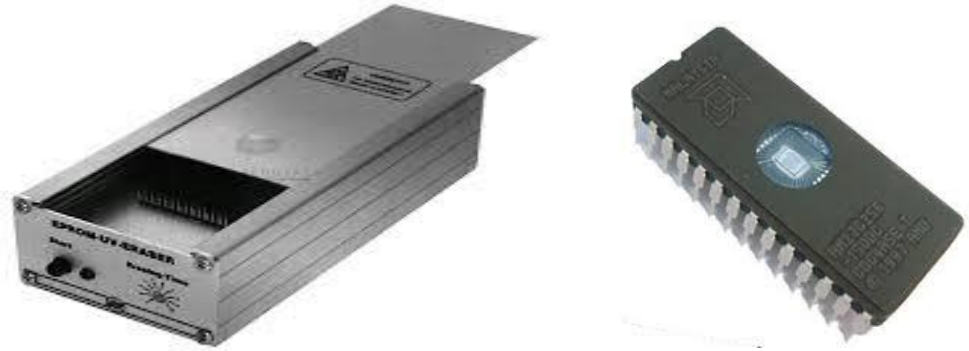
PROM

- **P**rogrammable ROM
- **Less expensive**
- **Non volatile**
- **Written only once - electrically**



EPROM

- Read **mostly** memory – **writing is possible**
- **E**rasable **P**rogrammable ROM
- **Written electrically**
- **Erasure** – performed by shining an intense **UV light** through a window into the chip – takes 20 mins to erase
- **Alterable multiple times**
- **Expensive**

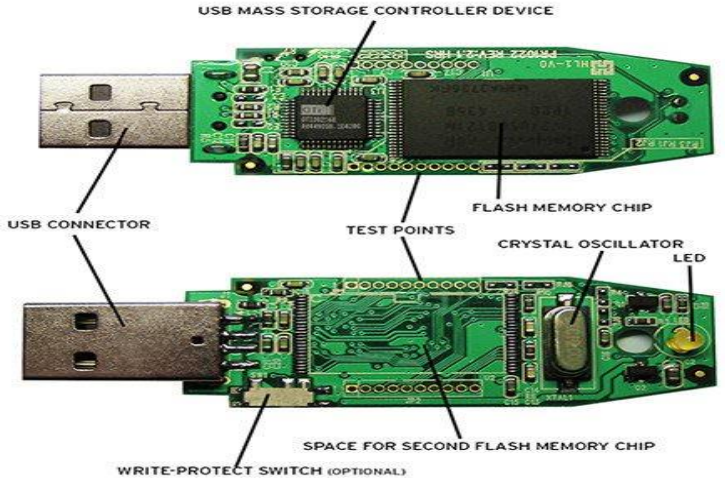


EEPROM

- Read **mostly** memory
- **E**lectrically **E**rasable Programmable ROM
- **Written at anytime** – without erasing prior content **– just the desired byte(s)**
- Write operation is longer than read operation
- **More expensive**

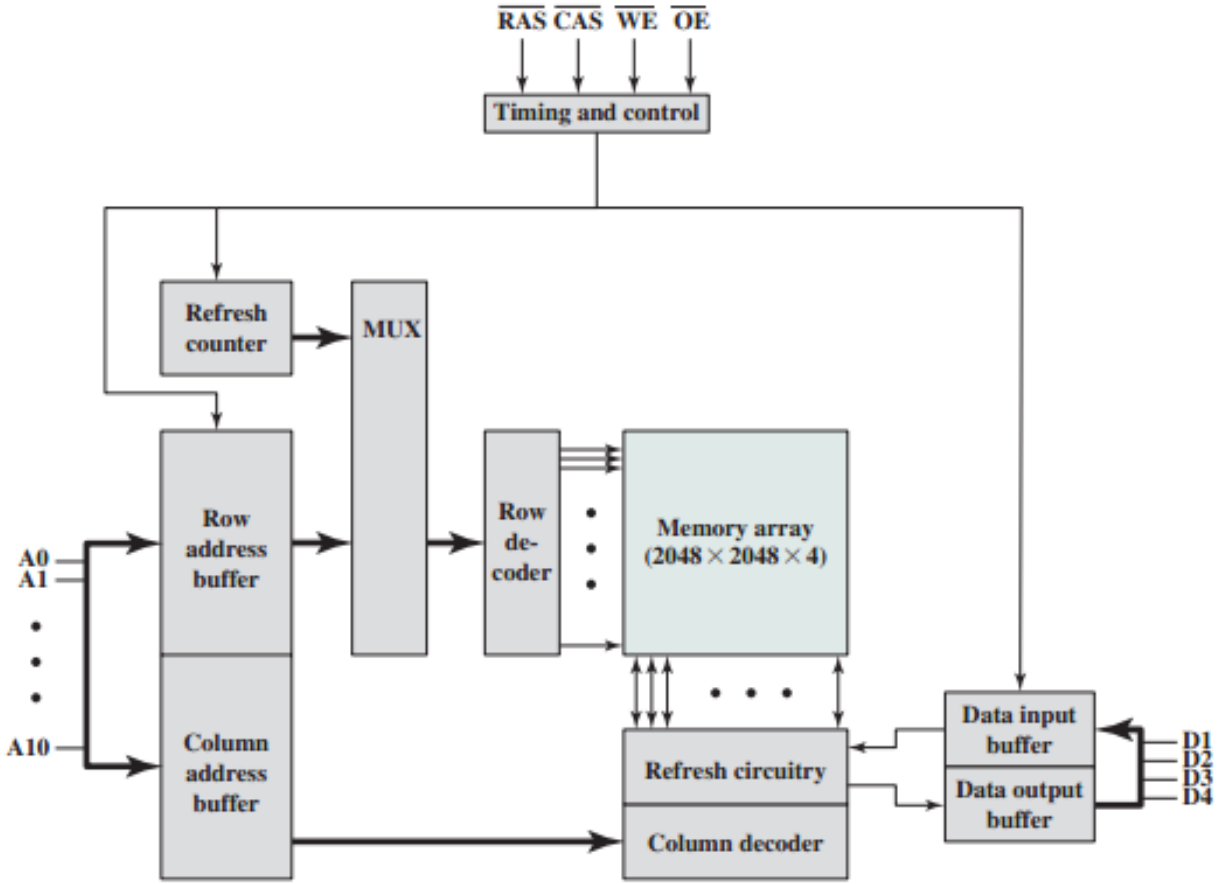
Flash Memory

- Read **mostly** memory
- **Named as** speed of reprogramming
- **Electrical erasure**
- Erased in <u>minutes or seconds</u>
- <u>Erase just block</u> rather than whole content



Chip Logic

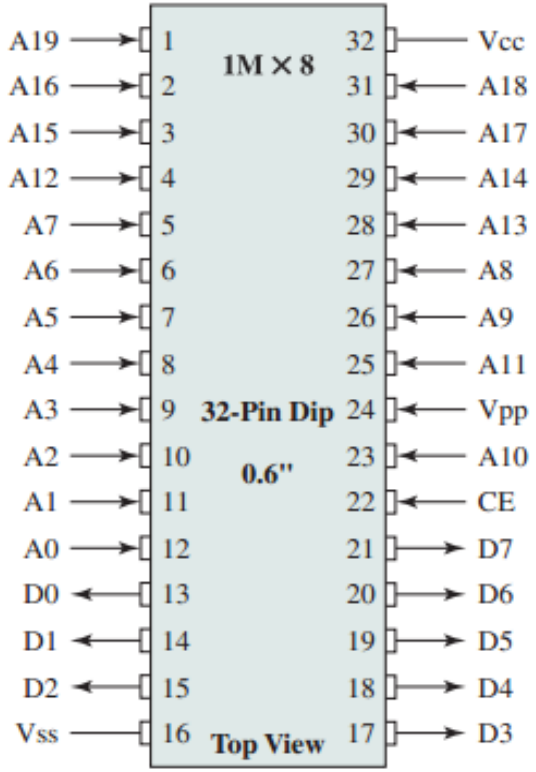
- Cells are **arranged in array** as logical arrangement
- **Read or write is possible** in bit or word (of several bytes) level



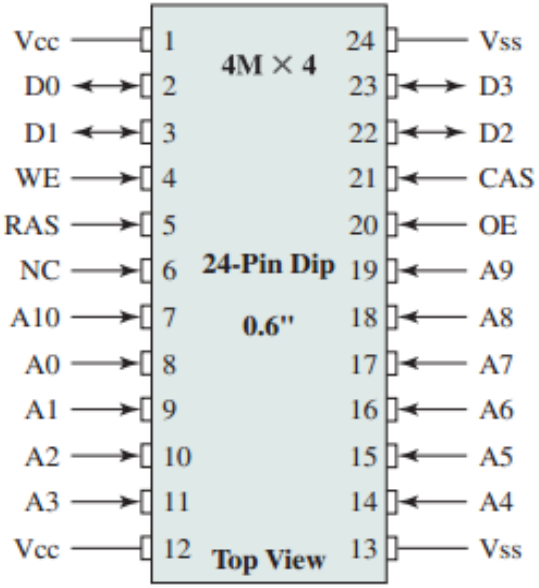
16M bit RAM

Chip Packaging

- An IC is mounted on a **package** that contains **pin** for connection
- **Pins support** –
  - Address of the word
  - Data
  - Power supply
  - Ground
  - Chip enable
  - Program voltage
    - during programming - write



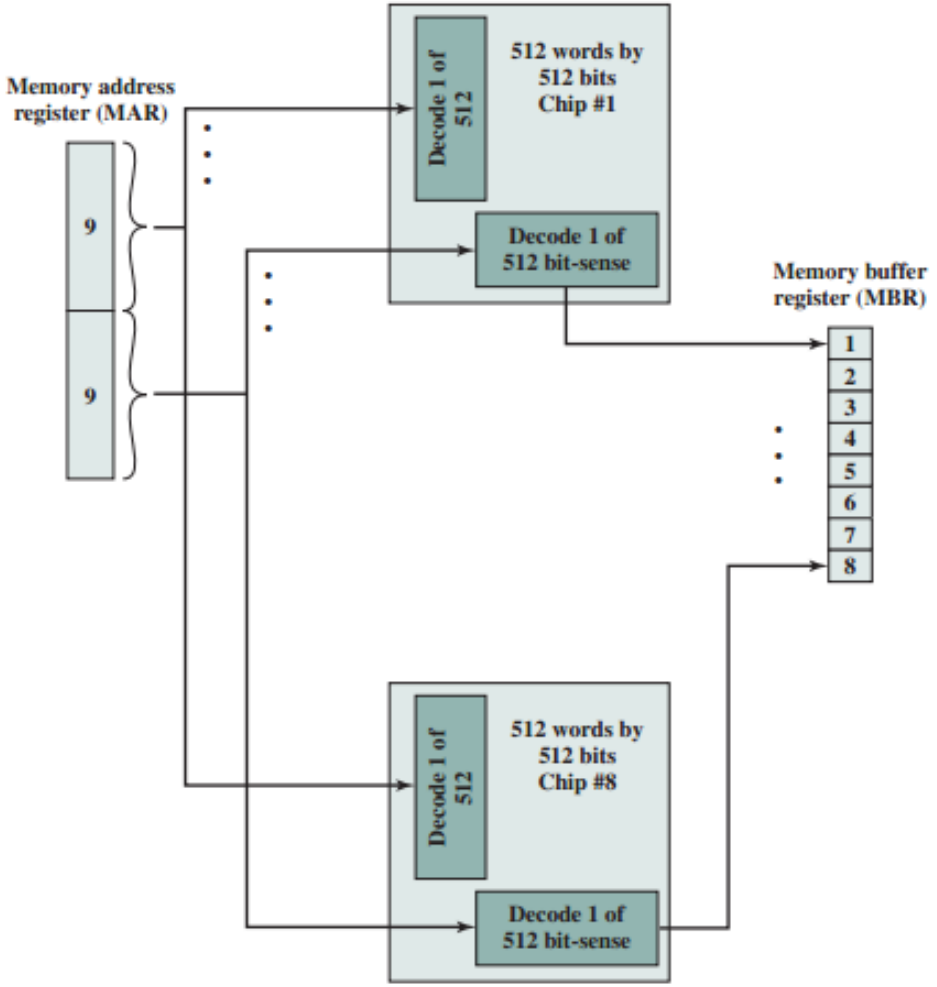
(a) 8-Mbit EPROM



(b) 16-Mbit DRAM

Module Organization

- How many memory modules are required and how they are arranged:



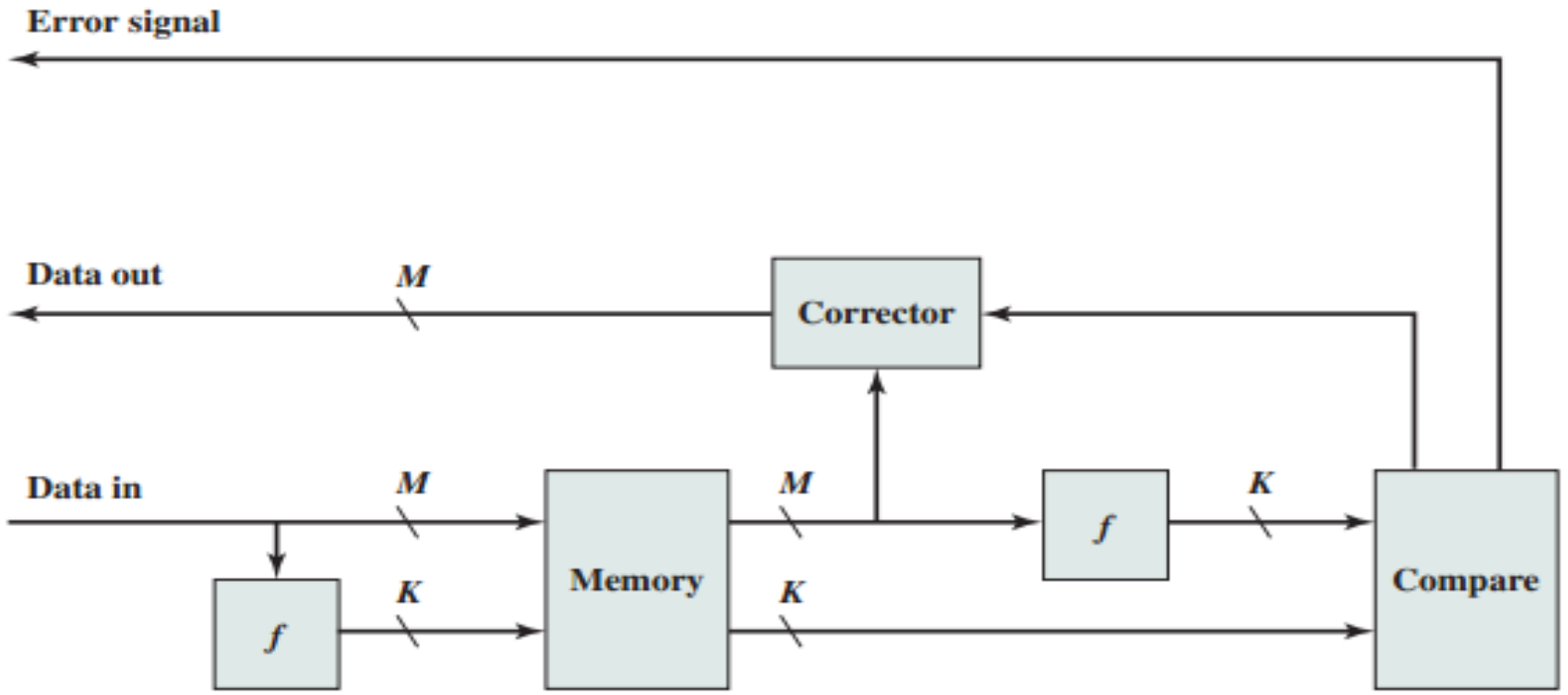
Interleaved Memory

- Main memory is composed of collection of DRAM chips – **grouped together** to form **memory bank** – **independently** able to service a memory read and write
- Example:
  - Odd bank
  - Even bank

Error Correction

- A semiconductor memory is subject to errors:
  - **Hard failure**: Permanent physical defect so that the memory cell are affected to store data - Always 0/1/switching – harsh environmental abuse, manufacturing defects, destroy
  - **Soft error**: random, non-destructive – altering one or more bits without damaging memory – caused power supply problems or alpha/ radioactive particles
- A code is generated from the data which is stored in memory and also stored in memory associated with that data - when that data is fetched from memory **another code generated** from data in same way to compare it with previous one. Results may be:
  - No errors are detected.
  - An error is detected and it is possible to correct – error correction bits are generated to produce corrected data
  - An error is detected and it is impossible to correct

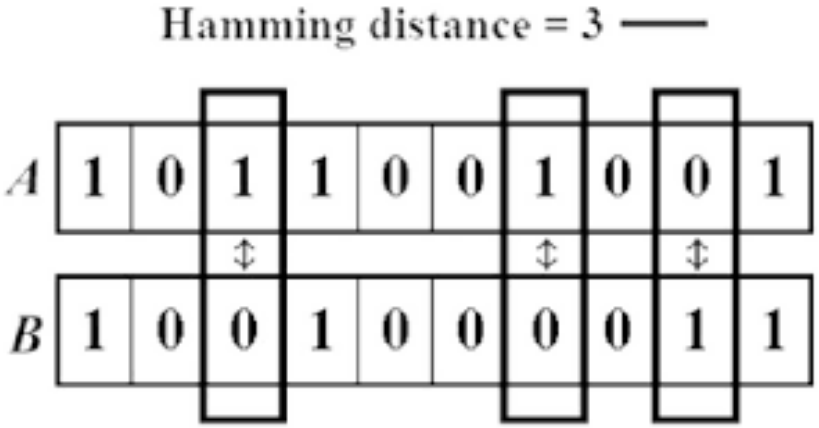
Error Correction…



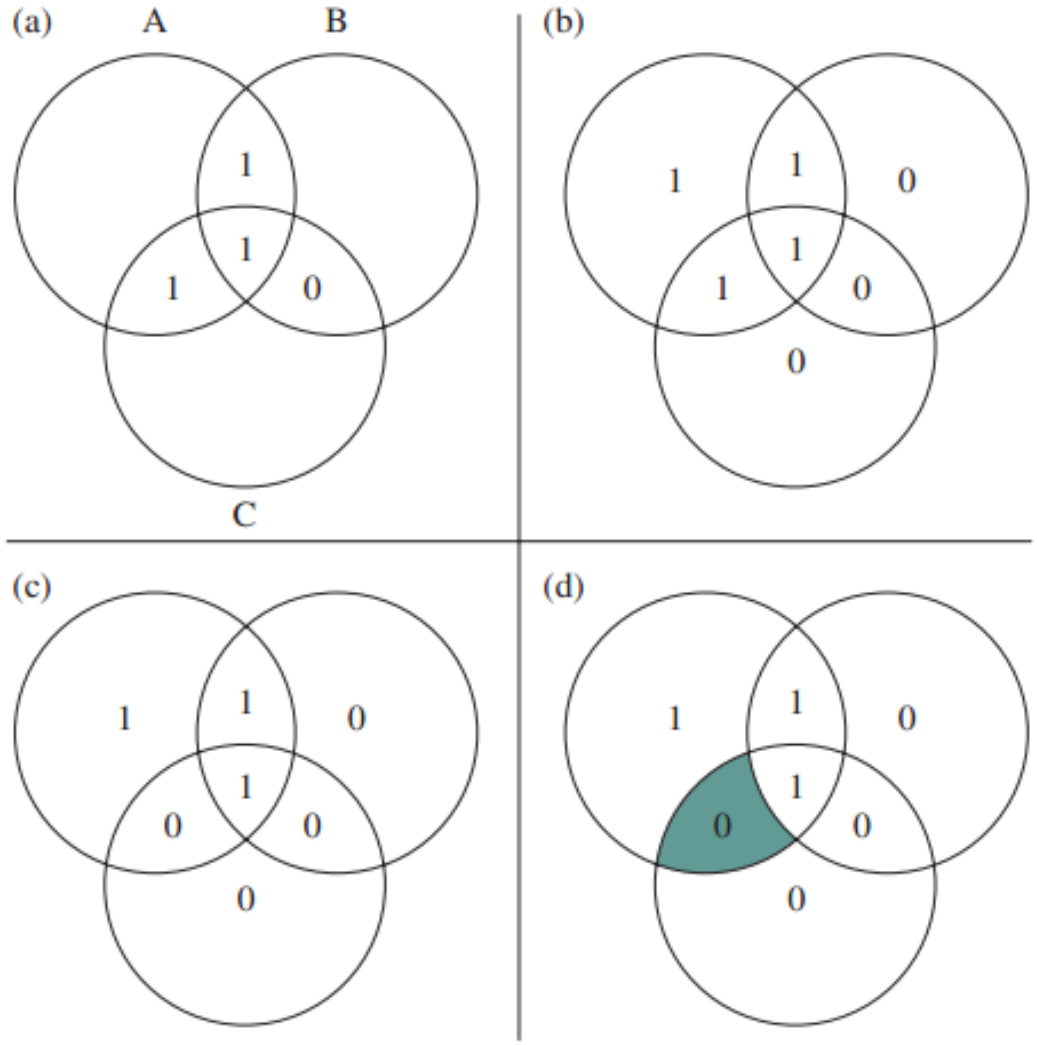
f = calculation function that produces code from data
M = data word
K = code word

Error Correction…

- **Error Correcting Code:** Code that will help to correct the erroneous data
- Hamming Code is the **simplest way** of error correcting
- Hamming code is **different from Hamming distance** where the **Hamming distance** between two strings of equal length is the number of positions at which the corresponding symbols are different.



Hamming Code



Hamming Code…

- At first, we have to determine **the length of the code: *(M+K)***
- Two K-length codes (for old and newly fetched) will be compared bit by bit by performing XOR between them – the **result is called syndrome word** (k bits long)
- Each bit of the syndrome is 0 or 1 according to if there is a match or not
- **If $k=0_{10}$; there is no error.**
- **The length (M+K) must satisfy**: $2^K - 1 \geq M + K$

  - $K = 3: 2^3 - 1 < 8 + 3$
  - $K = 4: 2^4 - 1 > 8 + 4$

Where M = 8

Single Error Correction Code

For 8 bit data

Bit position	12	11	10	9	8	7	6	5	4	3	2	1
Position number	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001
Data bit	D8	D7	D6	D5		D4	D3	D2		D1		
Check bit					C8				C4		C2	C1

Single Error Correction Code

- If the syndrome contains all 0s, no error has been detected.
- If the syndrome contains one and only one bit set to 1, then an error has occurred in one of the 4 check bits. No correction is needed.
- If the syndrome contains more than one bit set to 1, then the numerical value of the syndrome indicates the position of the data bit in error. This data bit is inverted for correction.

Single Error Correction Code

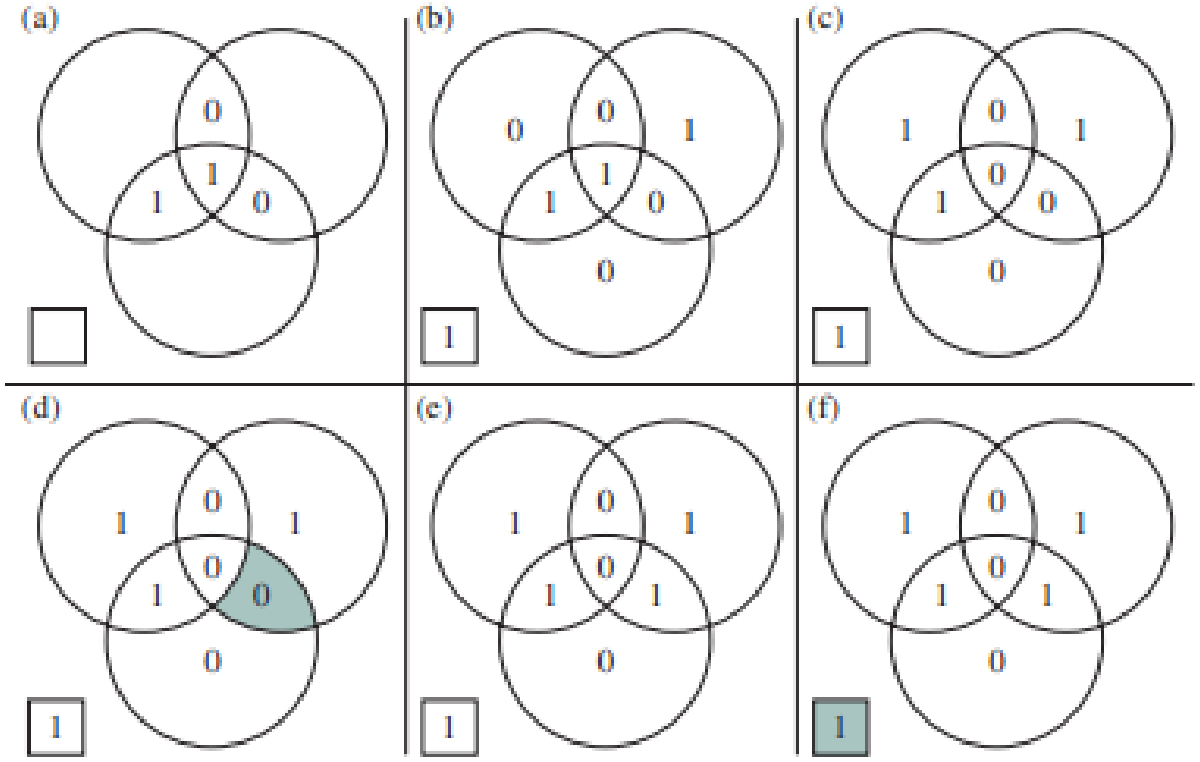
- Data Stored: 00111001 (D1 is rightmost position)
- Data Fetched: 00111101

$$C1 = 1 \oplus 0 \oplus 1 \oplus 1 \oplus 0 = 1$$
$$C2 = 1 \oplus 0 \oplus 1 \oplus 1 \oplus 0 = 1$$
$$C4 = 0 \oplus 0 \oplus 1 \oplus 0 = 1$$
$$C8 = 1 \oplus 1 \oplus 0 \oplus 0 = 0$$

$$C1 = 1 \oplus 0 \oplus 1 \oplus 1 \oplus 0 = 1$$
$$C2 = 1 \oplus 1 \oplus 1 \oplus 1 \oplus 0 = 0$$
$$C4 = 0 \oplus 1 \oplus 1 \oplus 0 = 0$$
$$C8 = 1 \oplus 1 \oplus 0 \oplus 0 = 0$$

	C8	C4	C2	C1
	0	1	1	1
$\oplus$	0	0	0	1
	0	1	1	0

SEC and Double Error Detecting Code



Module Organization

- Error

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- Error