



Islamic University of Technology

EEE 4483

Digital Electronics & Pulse Techniques

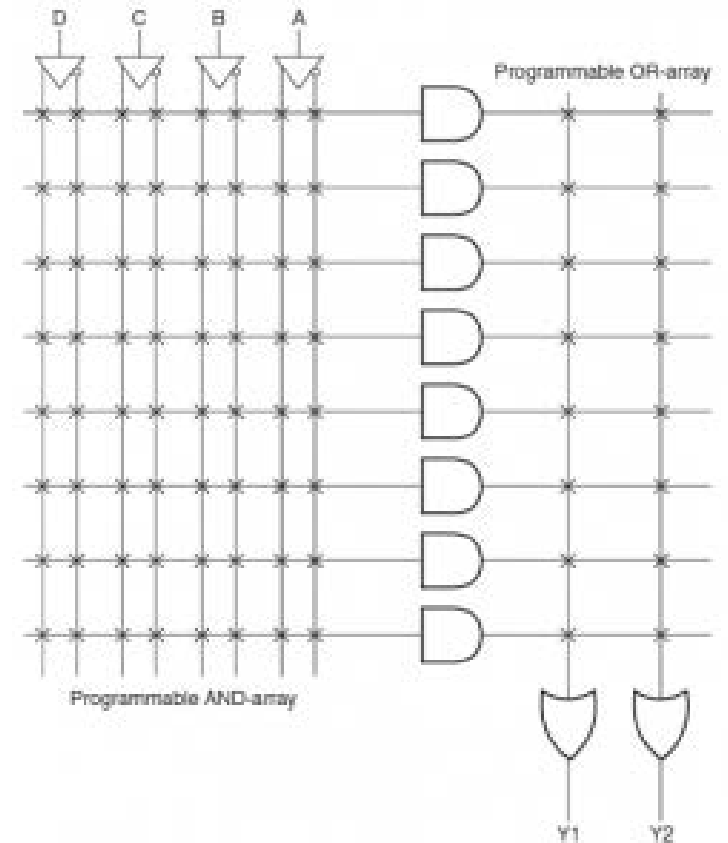
Lecture- 11

Programmable Logic Devices

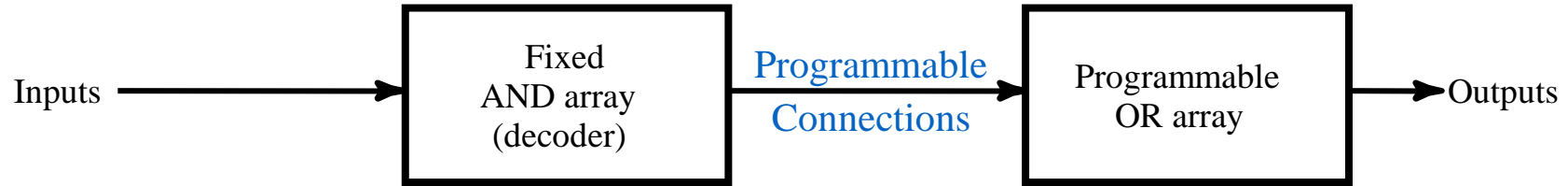
Programmable Logic Devices (PLDs) are the integrated circuits. They contain an array of AND gates & another array of OR gates. There are three kinds of PLDs based on the type of array(s), which has programmable feature.

- ☐ Programmable Read Only Memory
- ☐ Programmable Array Logic
- ☐ Programmable Logic Array

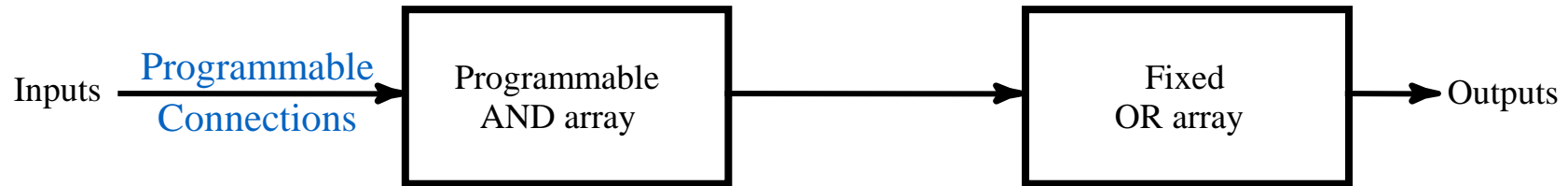
The process of entering the information into these devices is known as programming. Basically, users can program these devices or ICs electrically in order to implement the Boolean functions based on the requirement. Here, the term programming refers to **hardware programming but not software programming**.



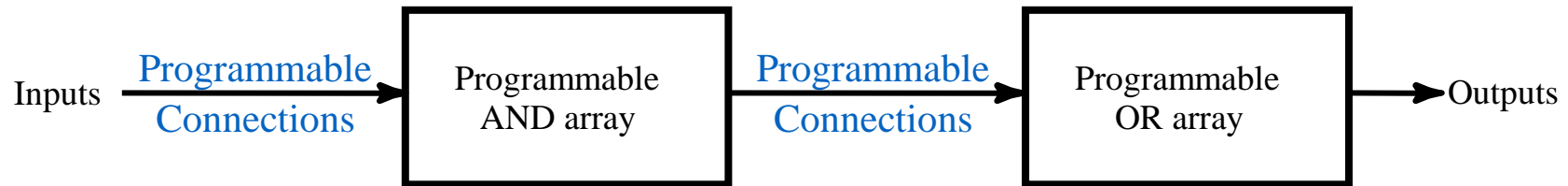
POM, PAL and PLA Configurations



(a) Programmable read-only memory (PROM)



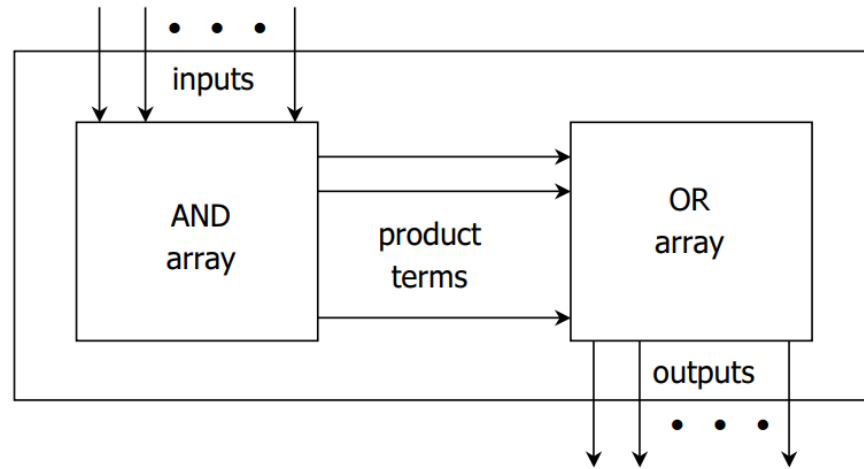
(b) Programmable array logic (PAL) device



(c) Programmable logic array (PLA) device

Programmable Logic Array

PLA is a programmable logic device that has both Programmable AND array & Programmable OR array. Hence, it is the most flexible PLD. The block diagram of PLA is shown in the following figure.



Here, the inputs of AND gates are programmable. That means each AND gate has both normal and complemented inputs of variables. So, based on the requirement, we can program any of those inputs. So, we can generate only the required product terms by using these AND gates.

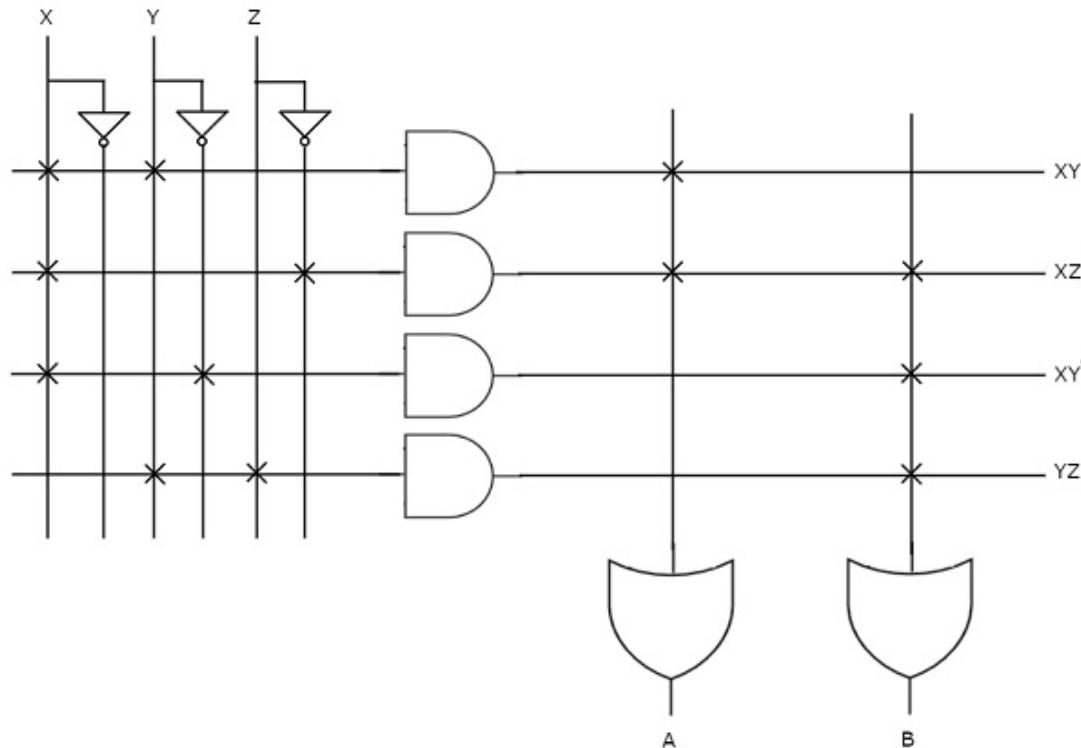
Here, the inputs of OR gates are also programmable. So, we can program any number of required product terms, since all the outputs of AND gates are applied as inputs to each OR gate. Therefore, the outputs of PAL will be in the form of sum of products form.

Example: Programmable Logic Array

$$A = XY + XZ'$$
$$B = XY' + YZ + XZ'$$

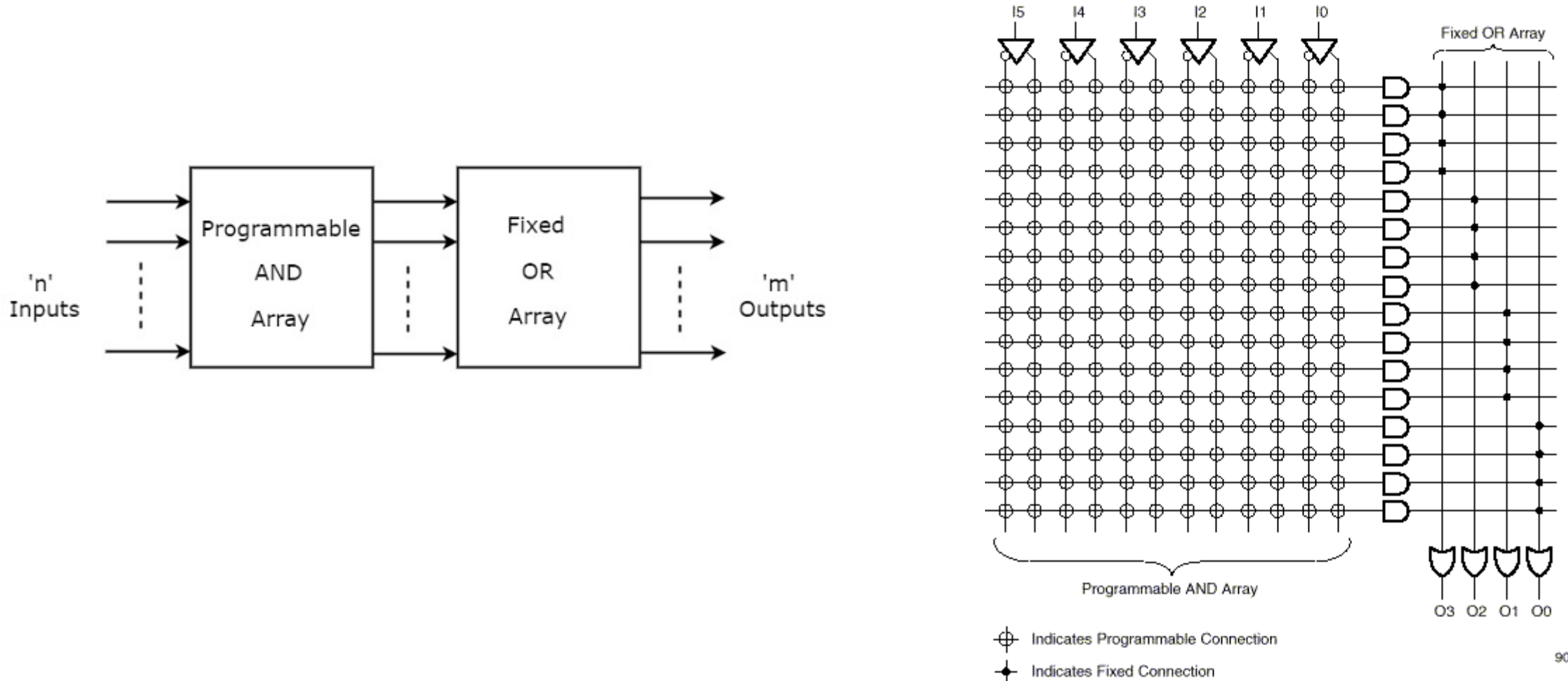
The given two functions are in sum of products form. The number of product terms present in the given Boolean functions A & B are two and three respectively. One product term, XZ' is common in each function.

So, we require four programmable AND gates & two programmable OR gates for producing those two functions. The corresponding PLA is shown in the following figure.



Programmable Array Logic (PAL)

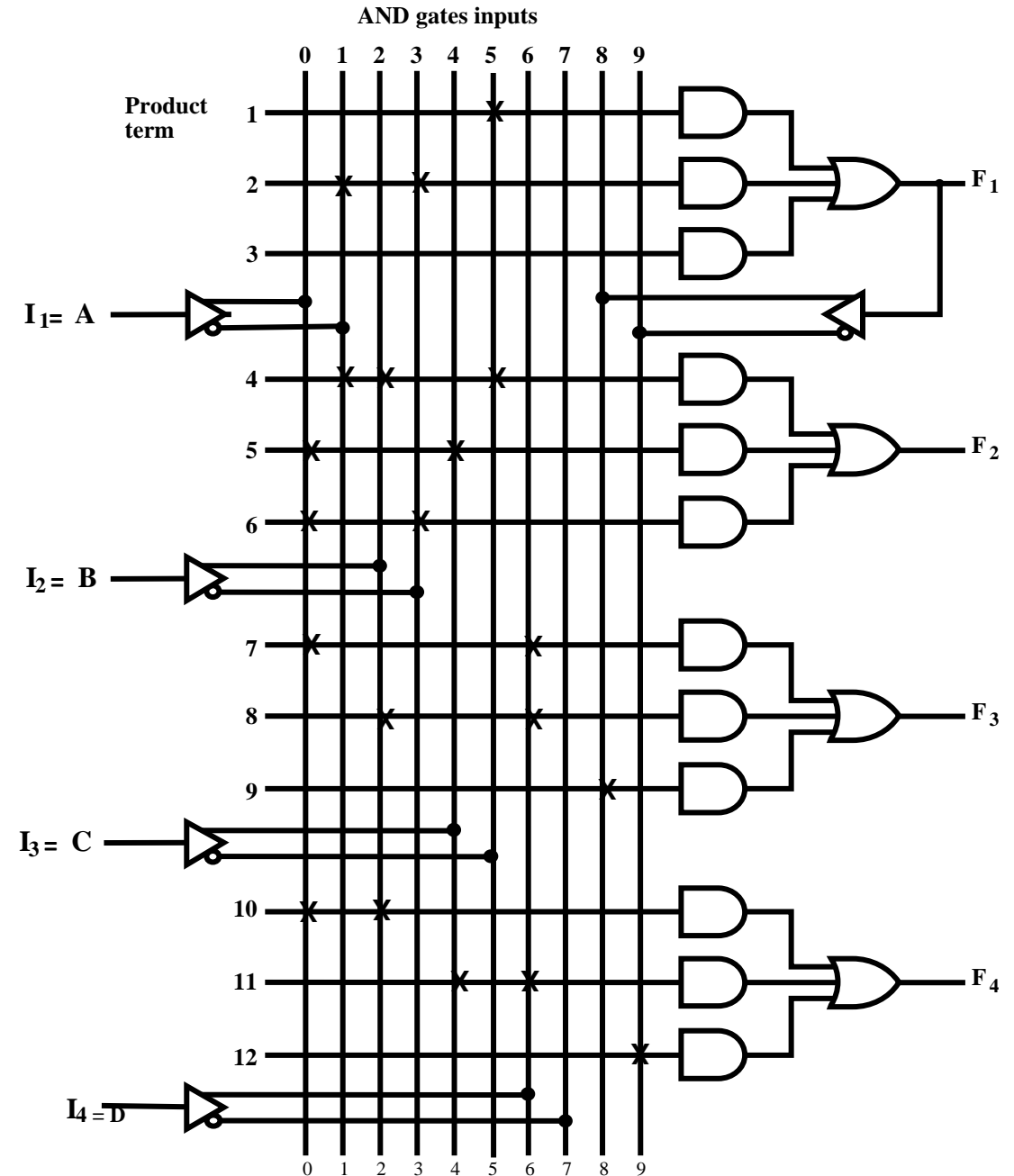
The general structure of this device is similar to PLA, but in a PAL device only AND gates are programmable. The OR array in this device is fixed by the manufacturer. This makes PAL devices easier to program and less expensive than PLA. On the other hand, since the OR array is fixed, it is less flexible than a PLA device.



Programmable Array Logic (PAL) : Example

- 4-input, 3-output PAL with fixed, 3-input OR terms
- What are the equations for F1 through F4?

$$\begin{aligned}F1 &= C' + A'B' \\F2 &= A'BC' + AC + AB' \\F3 &= AD + BD + F1 \\F4 &= AB + CD + F1'\end{aligned}$$



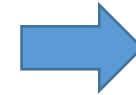
Minterms and Canonical Forms

In general, the unique algebraic expression for any Boolean function can be obtained from its truth table by using an OR operator to combined all **Minterms** for which the function is equal to 1.

x	y	z	Minterms	Notation
0	0	0	$x' y' z'$	m_0
0	0	1	$x' y' z$	m_1
0	1	0	$x' y z'$	m_2
0	1	1	$x' y z$	m_3
1	0	0	$x y' z'$	m_4
1	0	1	$x y' z$	m_5
1	1	0	$x y z'$	m_6
1	1	1	$x y z$	m_7

$$\begin{aligned} F &= x'yz + xy'z + xyz' + xyz \\ &= m_3 + m_5 + m_6 + m_7 \end{aligned}$$

$$F(x, y, z) = \sum (3, 5, 6, 7)$$



Express the Boolean function **F = x + y z** as a sum of **Minterms**

$$\begin{aligned} F &= x + y z \\ &= x (y + y') (z + z') + (x + x') y z \\ &= x y z + x y z' + x y' z + x y' z' + x y z + x' y z \\ &= x' y z + x y' z' + x y' z + x y z' + x y z \\ &= m_3 + m_4 + m_5 + m_6 + m_7 \\ &= \Sigma(3, 4, 5, 6, 7) \end{aligned}$$