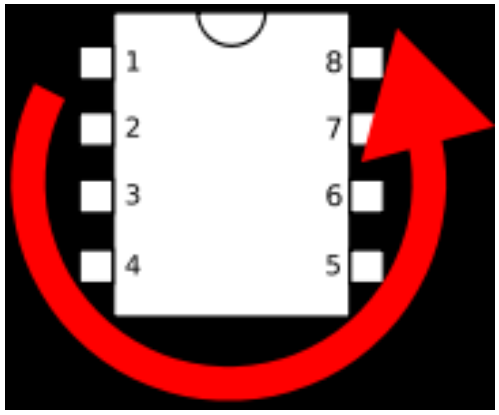
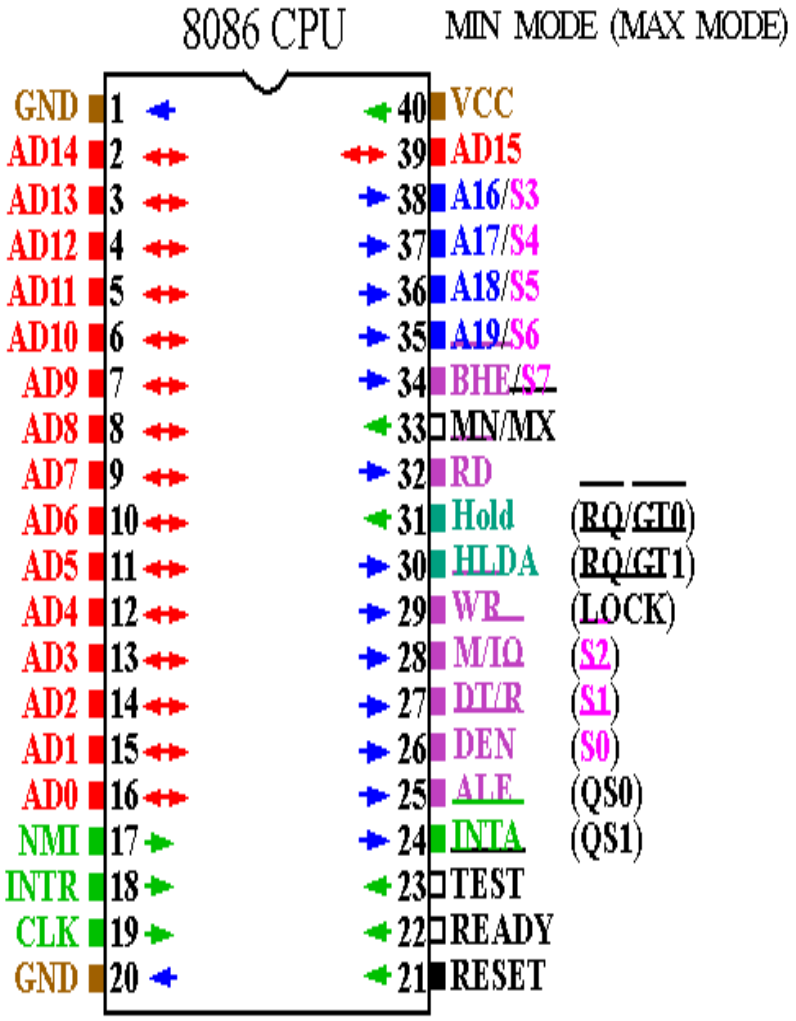
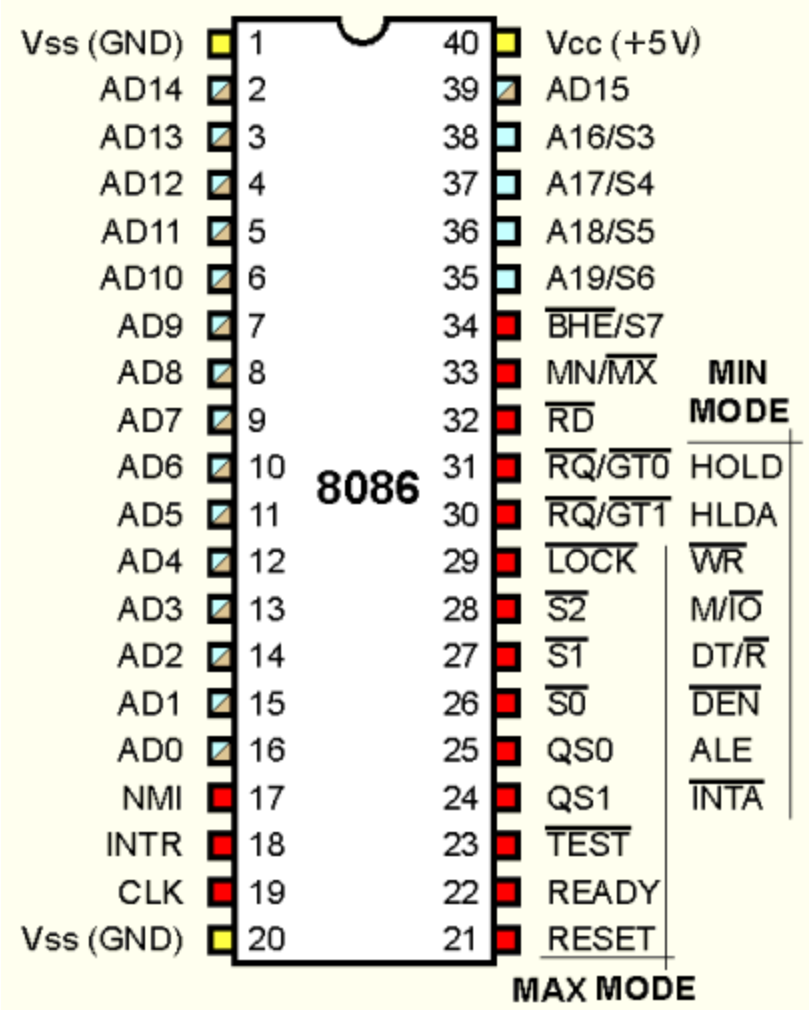
8086 Pin Specification

- 8086 is packaged as 40-pin DIPs.
- In micro-electronics **DIP** stands for **Dual in-line package.**
- DIP packaging refers to a rectangular housing with two parallel rows of electrical connection pins.
- DIP chips have a notch on one end to show its correct orientation.
- The pins are then numbered as shown in the figure below.



8086 Pin Specification





Minimum and Maximum Mode

- The mode is selected by PIN 33
  - 1 = Minimum, 0 = Maximum
  - Use of Pin 24 to 31 changes with the mode.

- The **minimum mode** is intended for single-processor systems on one printed circuit board (PCB).

- The **maximum mode** is intended for more complex system with separate I/O and memory boards.

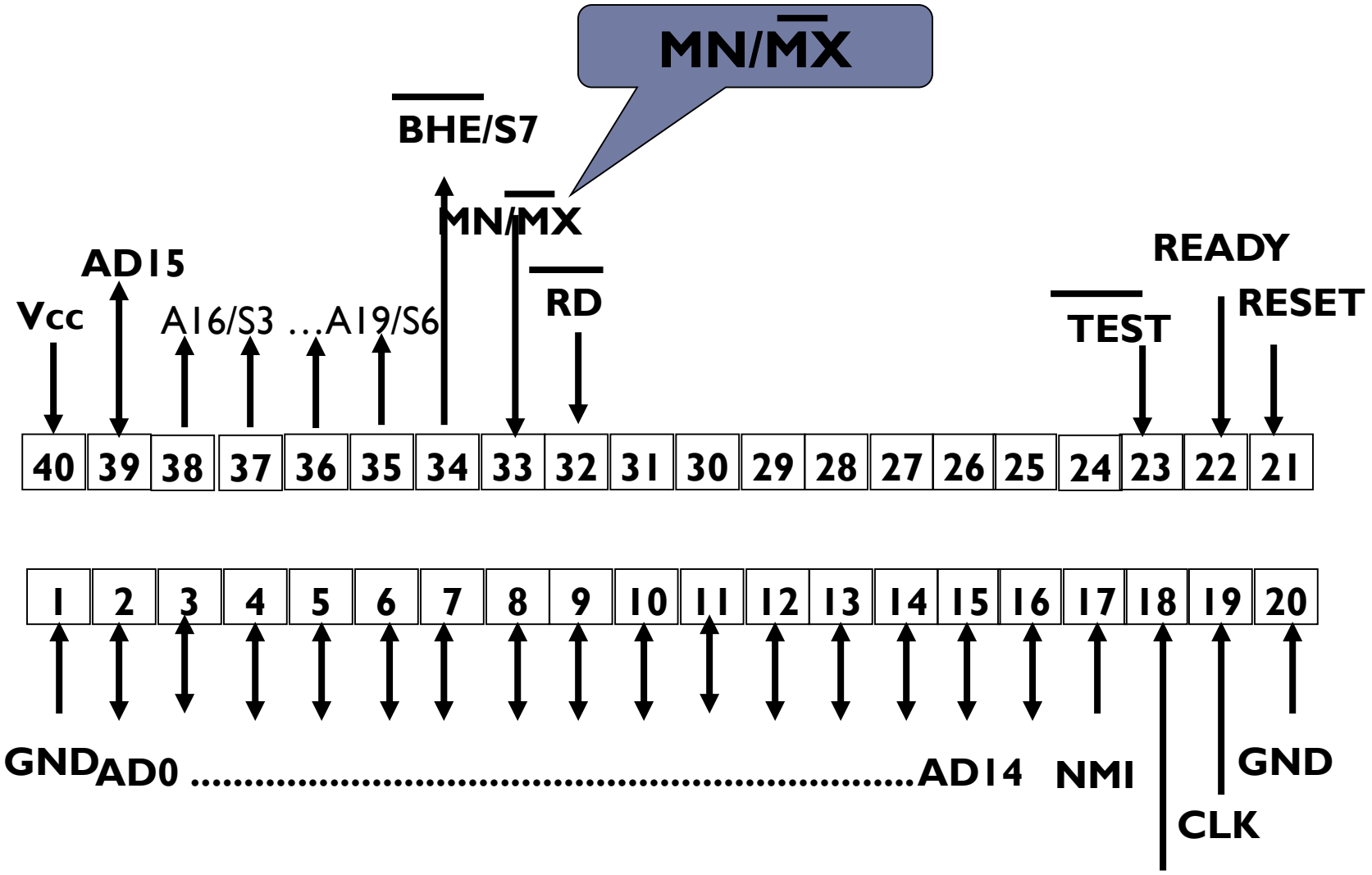
Minimum and Maximum Mode

Minimum mode	Maximum mode
In minimum mode there can be only one processor i.e. 8086.	In maximum mode there can be multiple processors with 8086, like 8087 and 8089.
MN/$\overline{MX}$ is 1 to indicate minimum mode.	MN/$\overline{MX}$ is 0 to indicate maximum mode.
ALE for the latch is given by 8086 as it is the only processor in the circuit.	ALE for the latch is given by 8288 bus controller as there can be multiple processors in the circuit.
$\overline{DEN}$ and DT/$\overline{R}$ for the trans-receivers are given by 8086 itself.	And DT/$\overline{R}$ for the trans-receivers are given by 8288 bus controller.
Direct control signals M/$\overline{IO}$, $\overline{RD}$ and $\overline{WR}$ are given by 8086.	Instead of control signals, each processor generates status signals called $\overline{S2}$, $\overline{S1}$ and $\overline{S0}$.

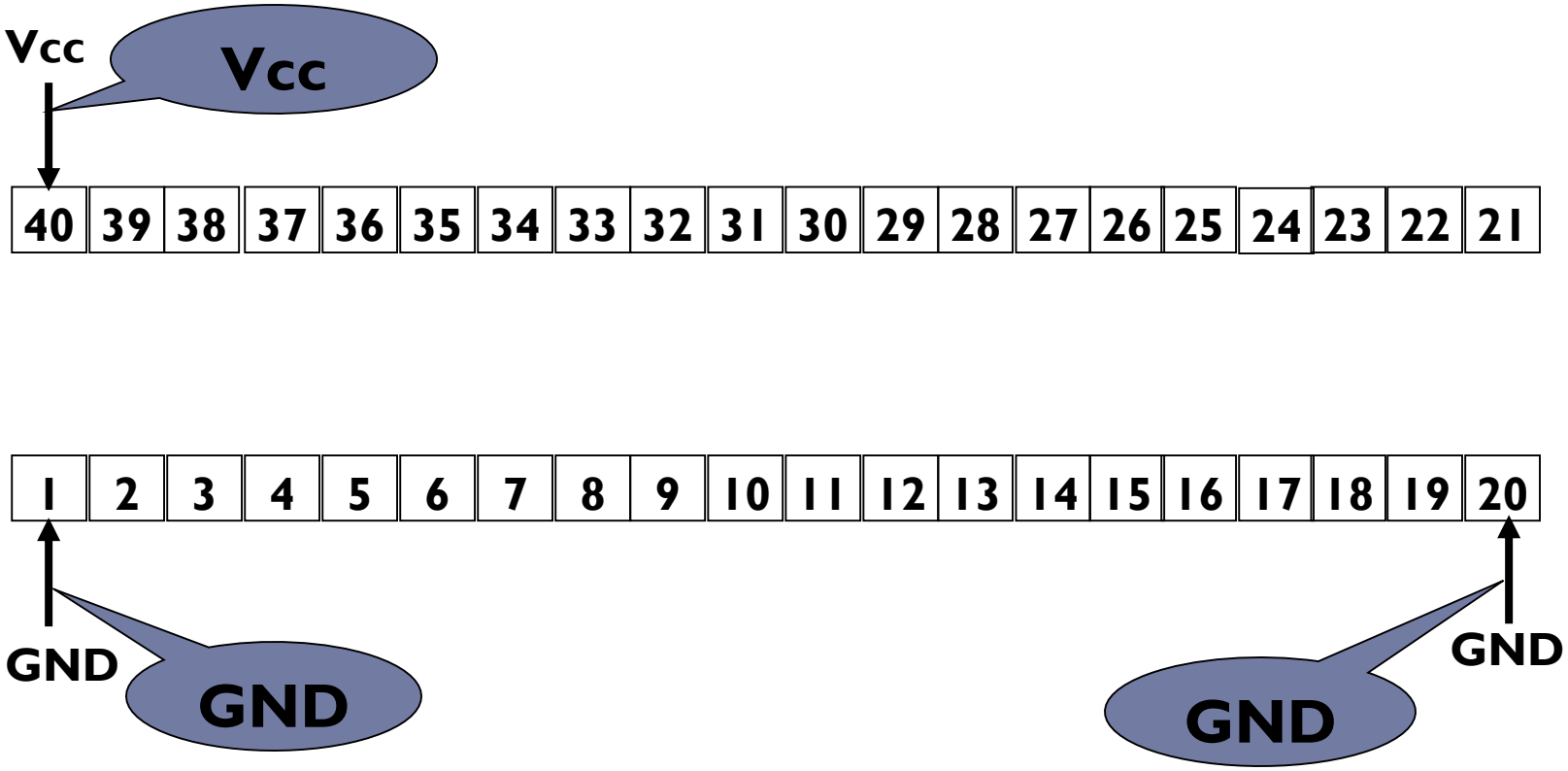
Minimum and Maximum Mode

Minimum mode	Maximum mode
Control signals $M/\overline{IO}$, $\overline{RD}$ and $\overline{WR}$ are decoded by a 3:8 decoder like 74138.	Status signals $\overline{S2}$, $\overline{S1}$ and $\overline{S0}$ are decoded by a bus controller like 8288 to produce control signals.
$\overline{INTA}$ is given by 8086 in response to an interrupt on INTR line.	$\overline{INTA}$ is given by 8288 bus controller in response to an interrupt on INTR line.
HOLD and HLDA signals are used for bus request with a DMA controller like 8237.	$\overline{RQ}/\overline{GT}$, lines are used for bus requests by other processors like 8087 or 8089.
The circuit is simpler.	The circuit is more complex.
Multiprocessing cannot be performed hence performance is lower.	As multiprocessing can be performed, it can give very high performance.

Control Signal – Minimum and Maximum Mode



Power Supply



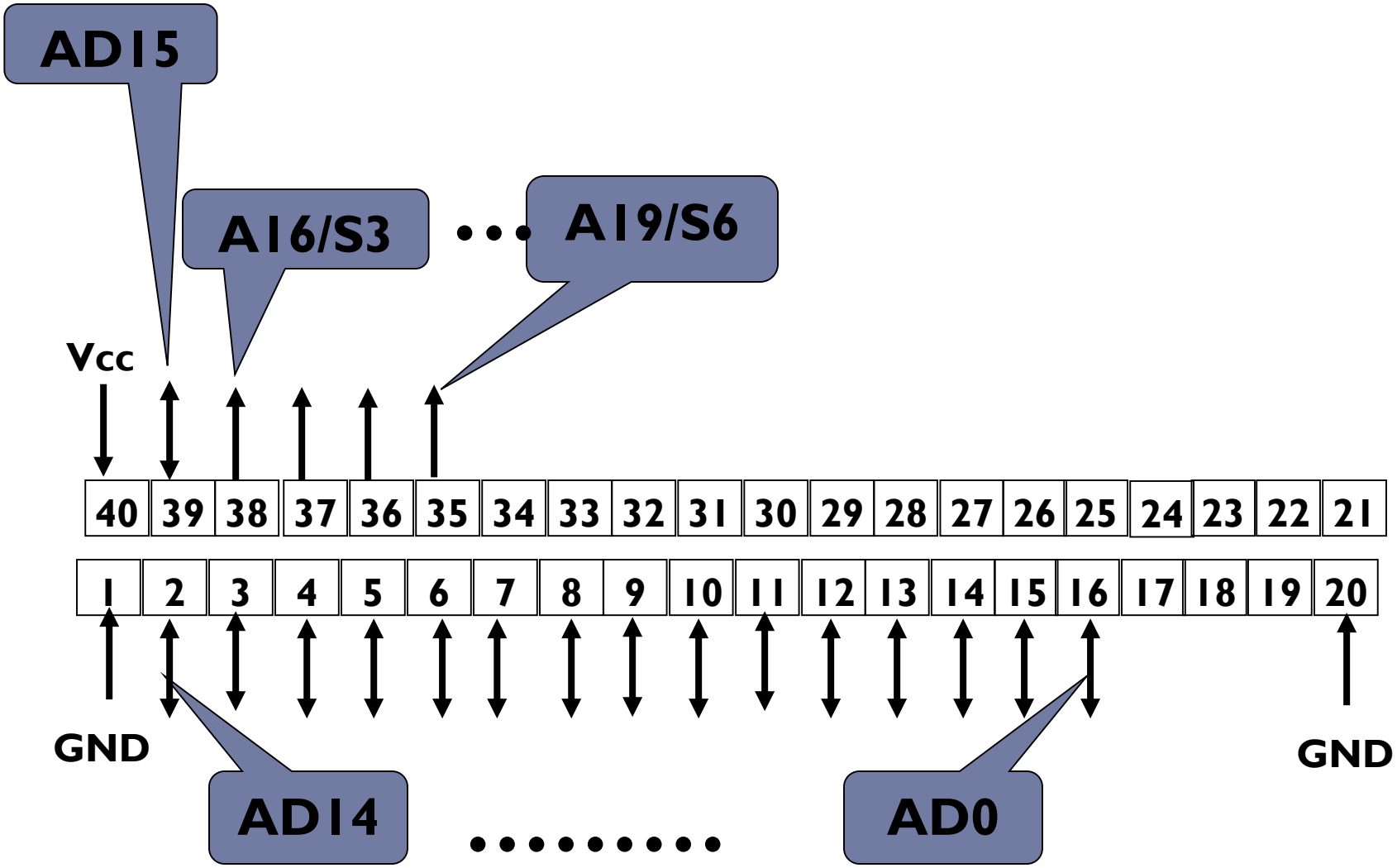
Pins for Data and Address Bus

- **Data Bus (AD0 – AD15)**
  - These 16 pins form the CPU's bidirectional data bus

- **Address Bus (AD0 – AD15 and A16/S3 – A19/S6)**
  - These 20 pins correspond to the CPU's 20-bit address bus and allow the processor to access 2^{20} or 10, 48, 576 unique memory locations.

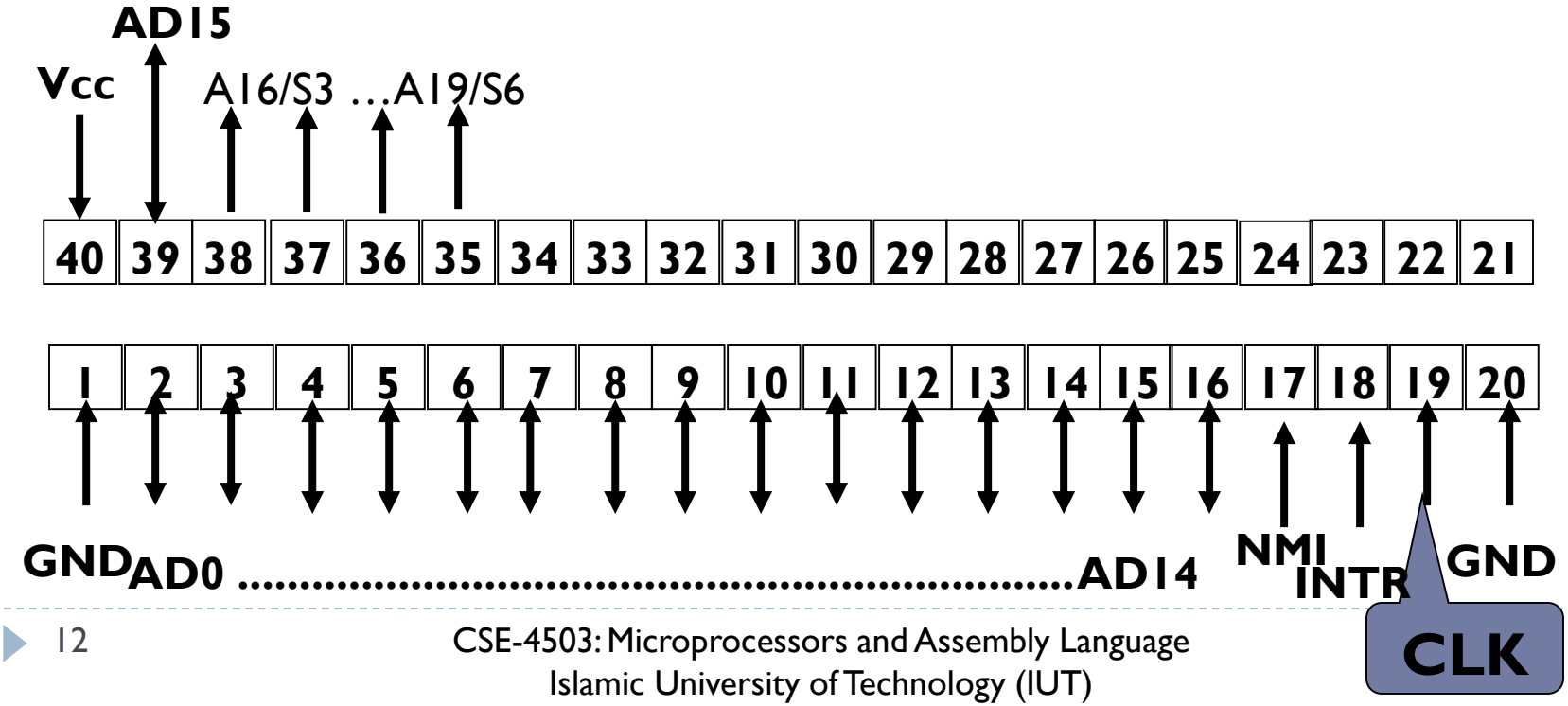
- **Address Latch Enable (ALE)** (Pin 25)
  - Line carries address when ALE =1
  - Line carries data when ALE =0

Pins for Data and Address Bus



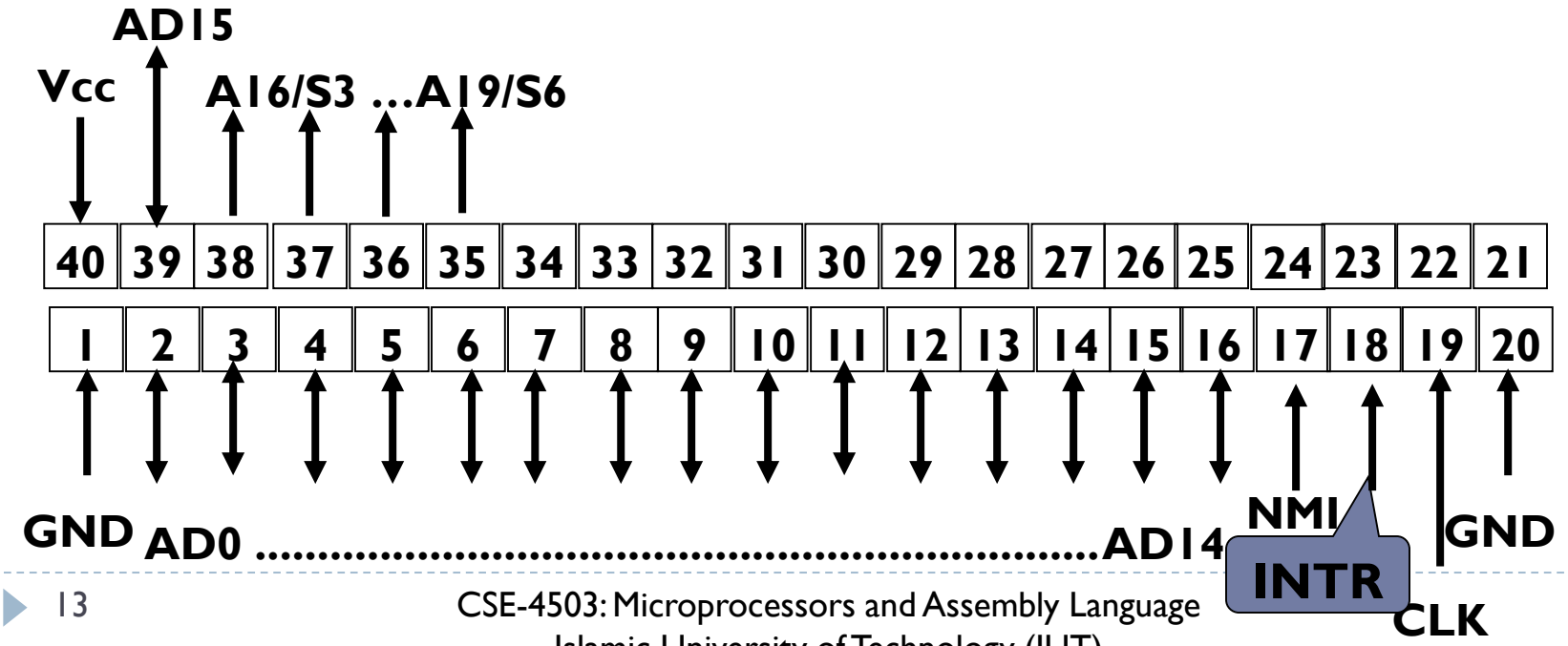
Control Signal – Clock

- Clock provides the basic timing for the processor and bus controller.
- It is asymmetric with a 33% duty cycle to provide optimized internal timing.
- 8086 is found to operate in 5 and 10 Mhz.



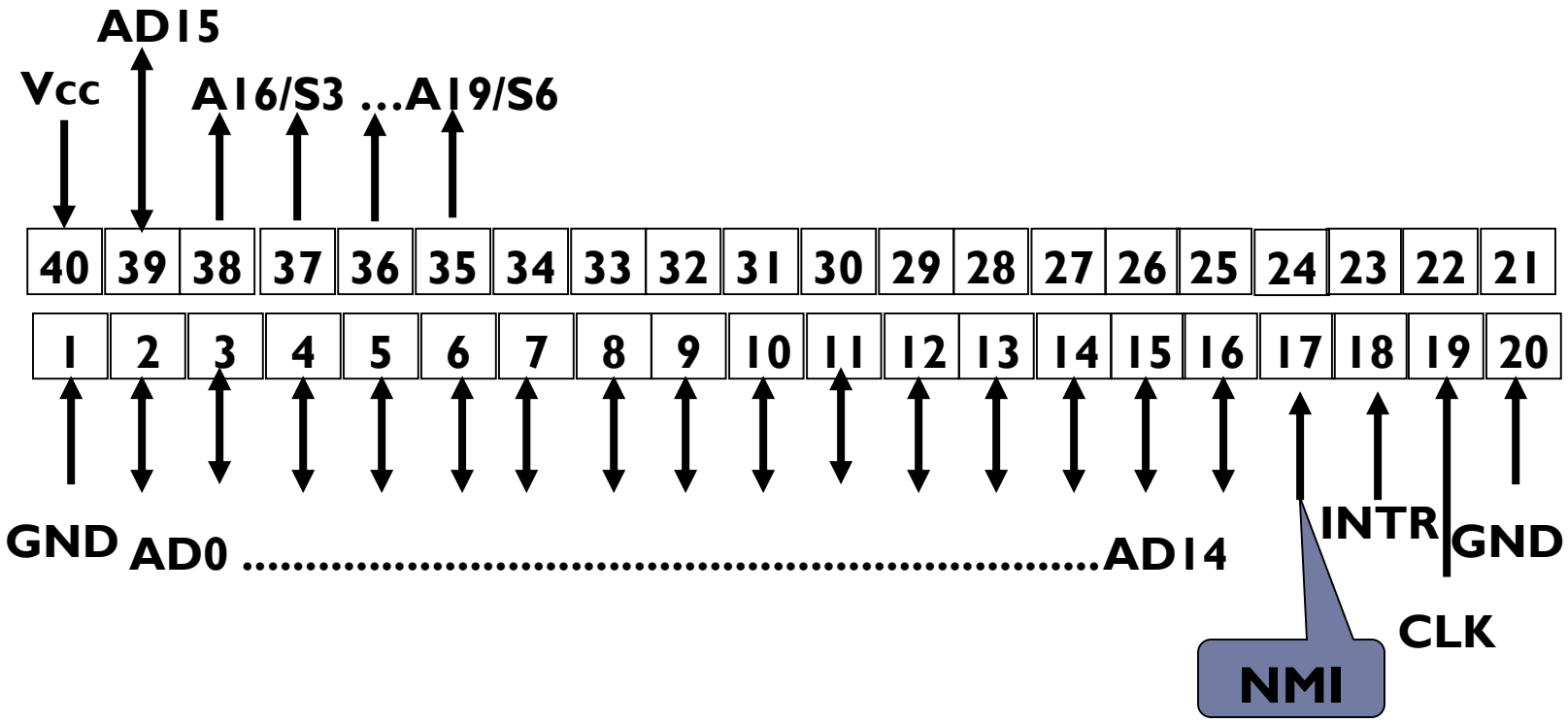
Control Signal – Interrupts

- **INTR: Interrupt request** pin is used to request a hardware interrupt.
- If INTR is held at high when **Interrupt Flag (IF=1)**, the processor goes into the interrupt acknowledgement cycle. INTA becomes active when interrupt is being serviced.



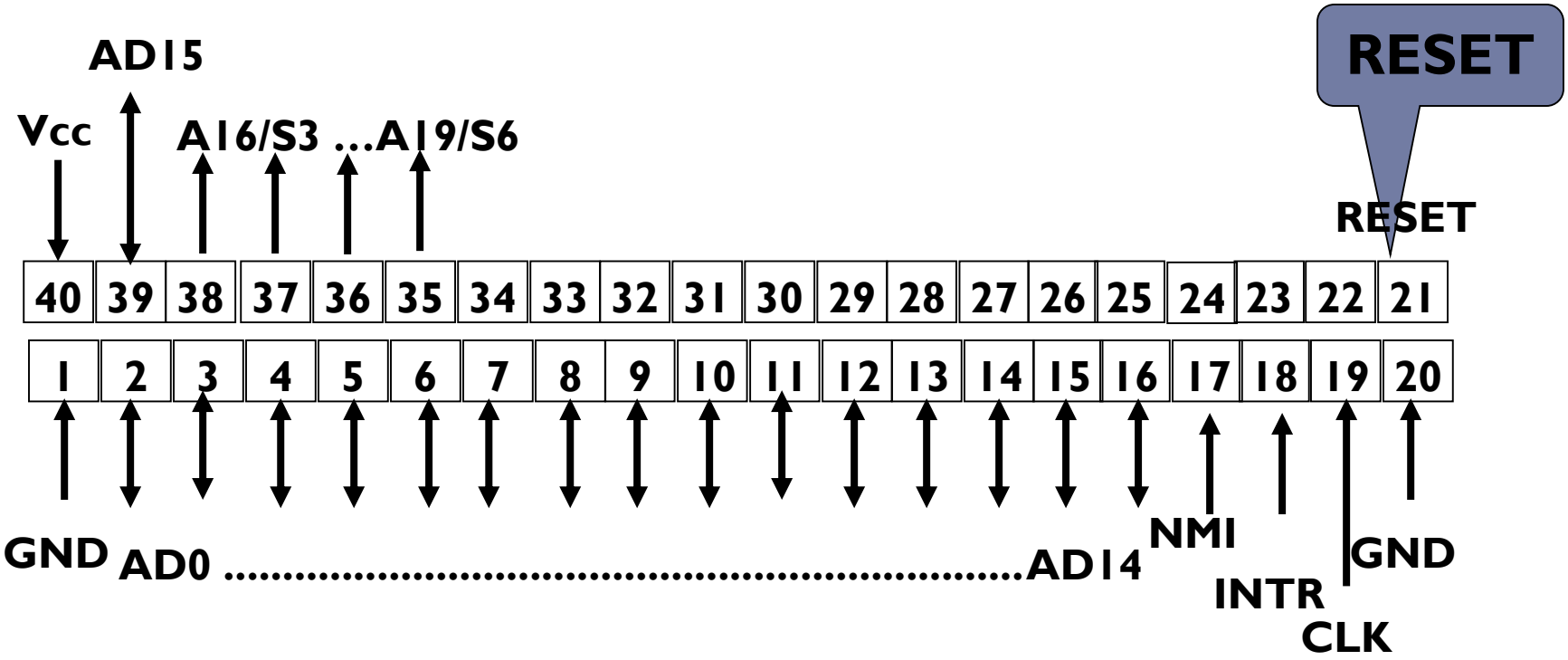
Control Signal – Interrupts

- **NMI: Non-maskable interrupt** input is similar to INTR expect that the NMI interrupt does not check **Interrupt Flag (IF)** or priority.



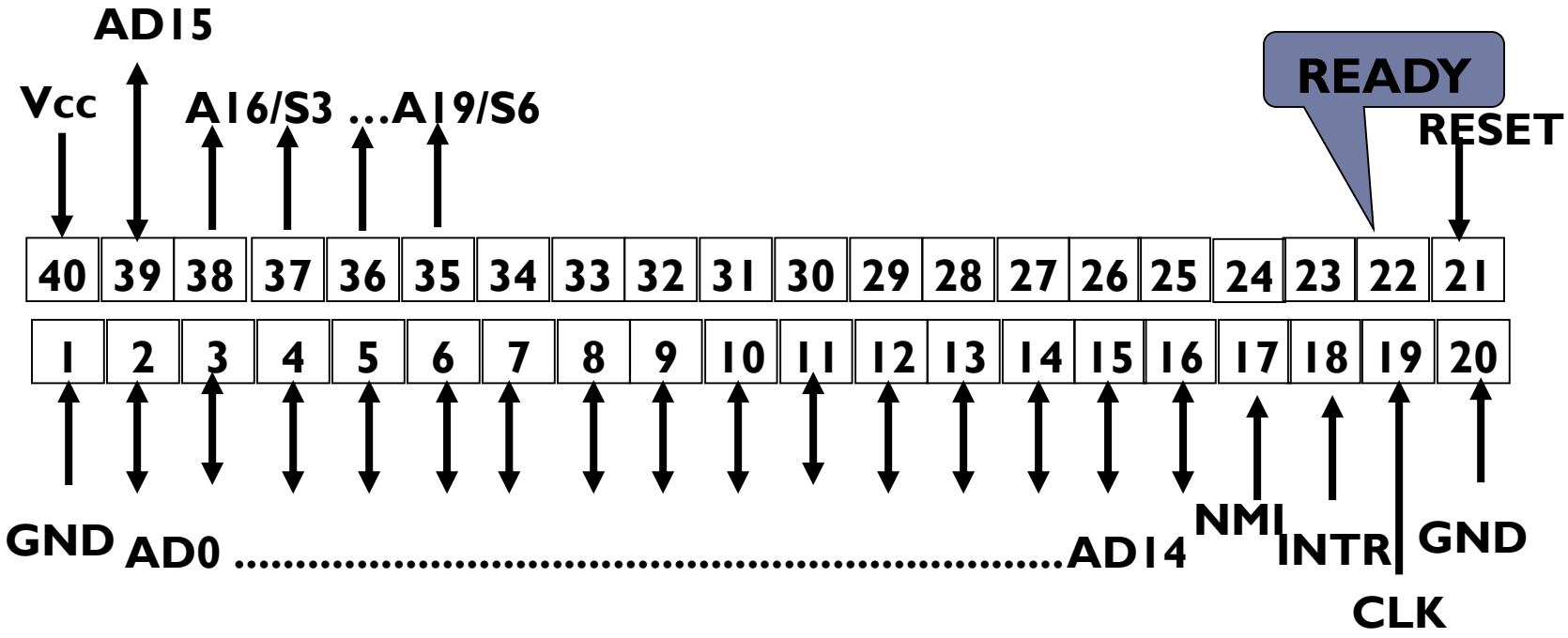
Control Signal – RESET

- **RESET** pin is held HIGH for at least 4 clock cycles to reset the microprocessor. It causes the processor to immediately terminates its present activity.



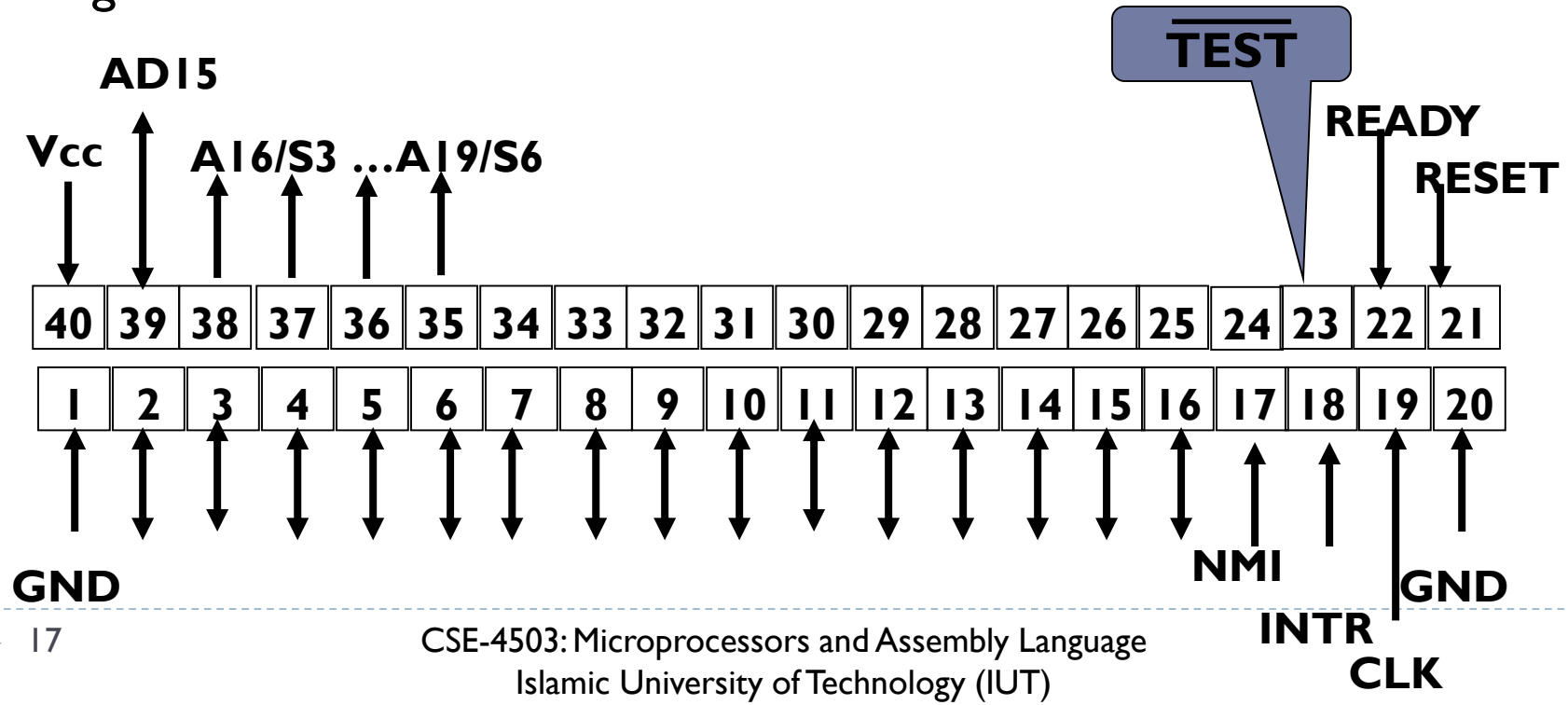
Control Signal – READY

- The READY pin is used to enforce a waiting state.
  - READY pin at 0 – the microprocessor goes into idle state.
    READY pin at 1 – the microprocessor does normal operation.



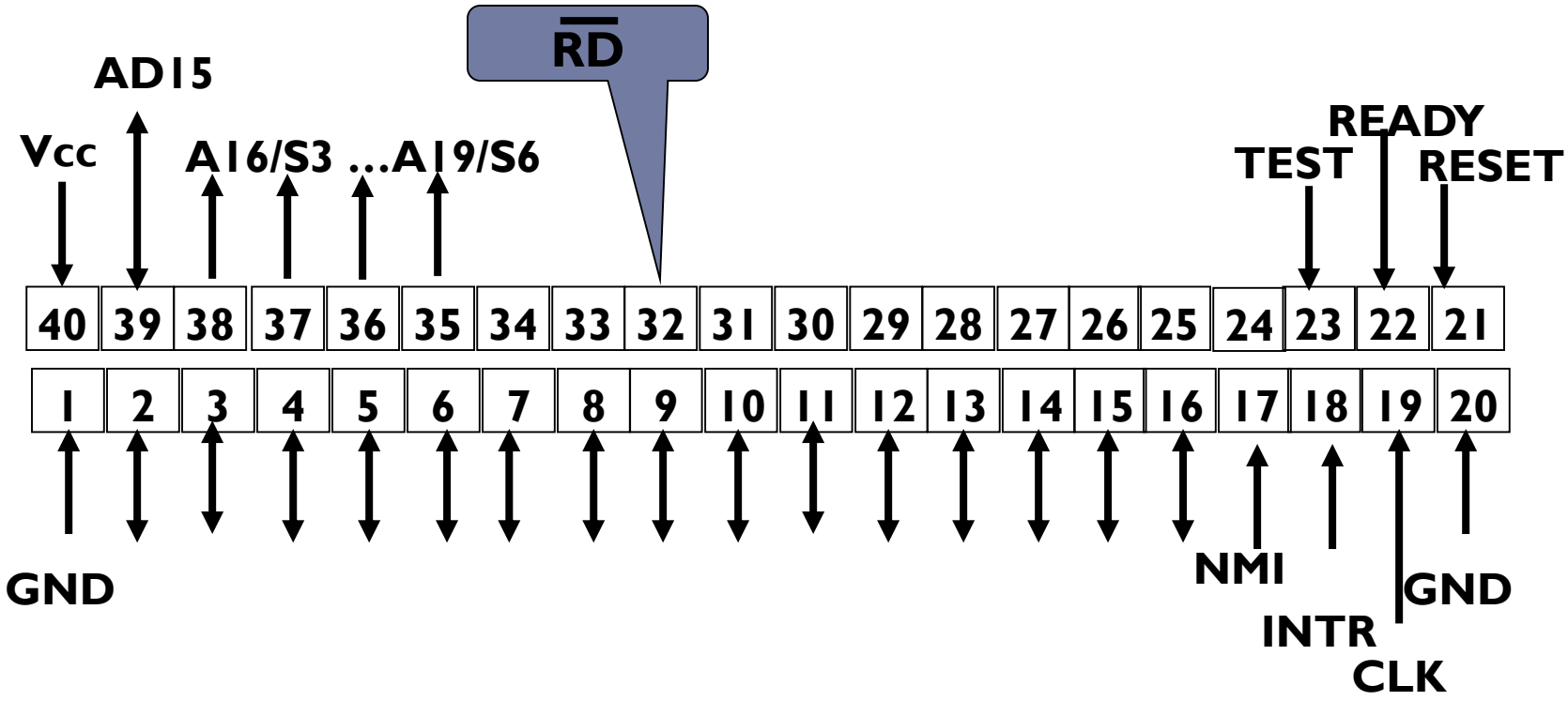
Control Signal – TEST

- **$\overline{\text{TEST}}$:** Test pin is an input that is tested by the **WAIT** instruction.
- If the test pin is at logic 0 the WAIT instruction functions as NOP.
- If test is a logic 1, the WAIT instruction wait for TEST to become logic 0.



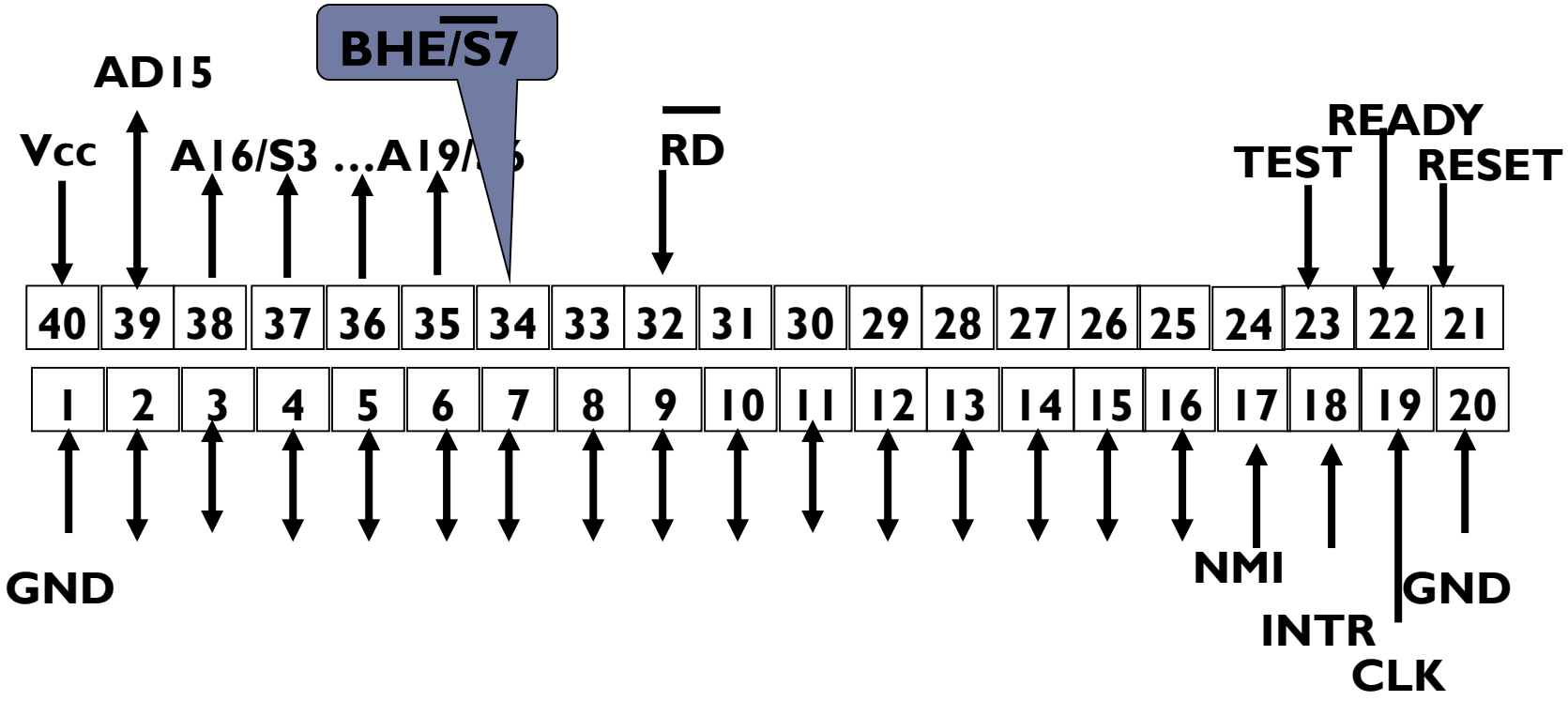
Control Signal – READ

- **$\overline{RD}$:** When this **read signal** pin is at logic 0, the data bus is receptive to data from memory or I/O devices.



Control Signal – BHE

- The **Bus High Enable (BHE)** pin is used in the 8086 to enable the Most significant data bus bits (**AD8 to AD15**) during a read or write operation.



Control Signal –Segment Register Status

- This information indicates which segment register is presently being used for data accessing.

S4	S3	Function
0	0	ES
0	1	SS
1	0	CS
1	1	DS

S5 indicates the status of I-flag

S6 low indicates that μP is using the bus

S7 spare status bit

Control Signals – Minimum Mode

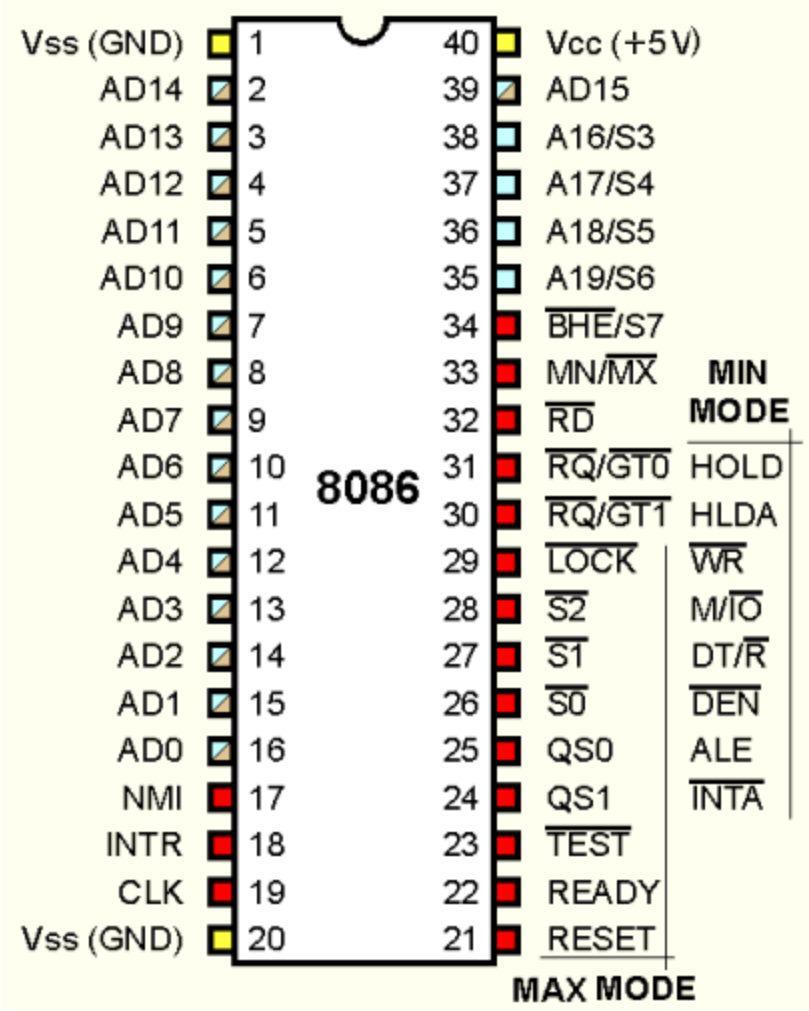
- **$\overline{\text{INTA}}$ (Pin 24): Interrupt acknowledgement** signals is a response to INTR input pin. This is used when the interrupt vector is placed on the address bus by the microprocessor.
- **ALE (Pin 25): Address Latch enable** shows whether the multiplexed AD lines carry address or data.
- **DEN (Pin 26): Data Enable bus** activates external data bus buffers.
- **DT/$\overline{\text{R}}$ (Pin 27): Data transmit/receive** shows that the microprocessor data bus is transmitting(1) or receiving(0) data. This is used to control buffers.

Control Signals – Minimum Mode

- **M/$\overline{IO}$ (Pin 28):** This pin indicates whether the address bus contains a memory address or an I/O port address.
- **$\overline{WR}$ (Pin 29):** The **write line** is a used when the microprocessor is writing data to memory and the memory bus contains a valid address.
- **HOLD (Pin 30): HOLD** pin is used to input request DMA (Direct Memory Access). Hold set to 1 microprocessor gives up control of buses to DMA controller.
- **HLDA (Pin 31): HLDA** pin is used to acknowledge DMA request.

Control Signals – Maximum Mode

S2	S1	S0	
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Inactive



Instruction Queue Status

QS1	QS0	
0	0	No operation
0	1	First byte of opcode fetched from queue
1	0	Empty queue
1	1	Subsequent byte from queue