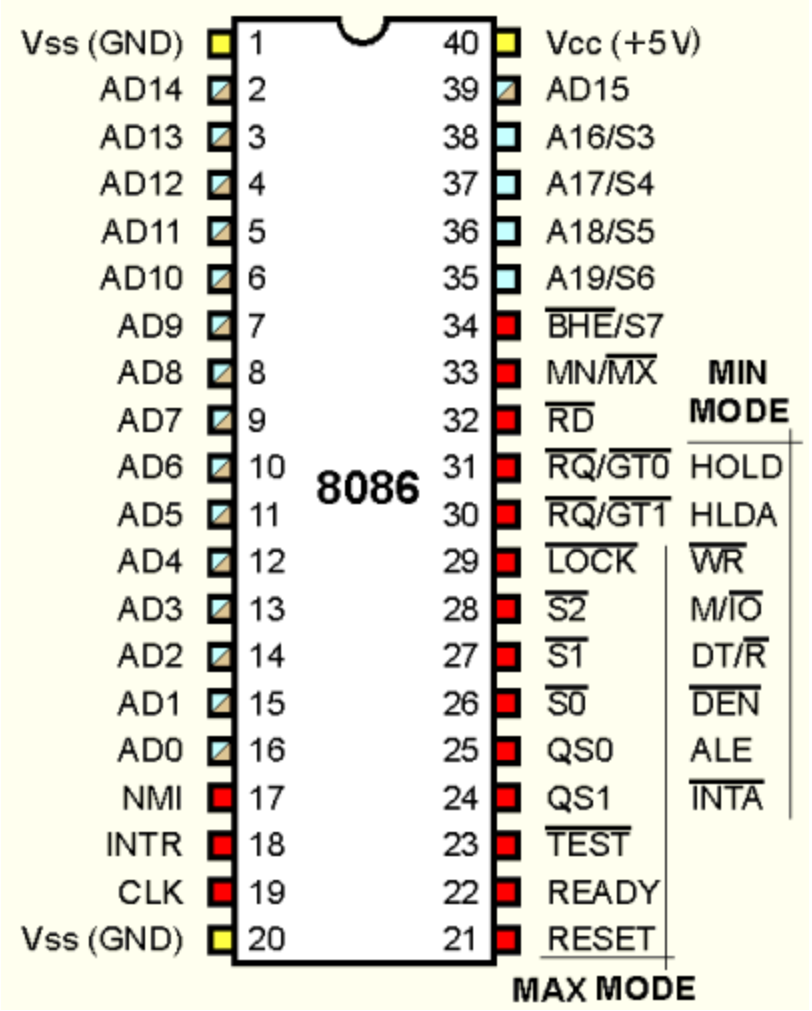
Remember !! 8086 Pin Specifications

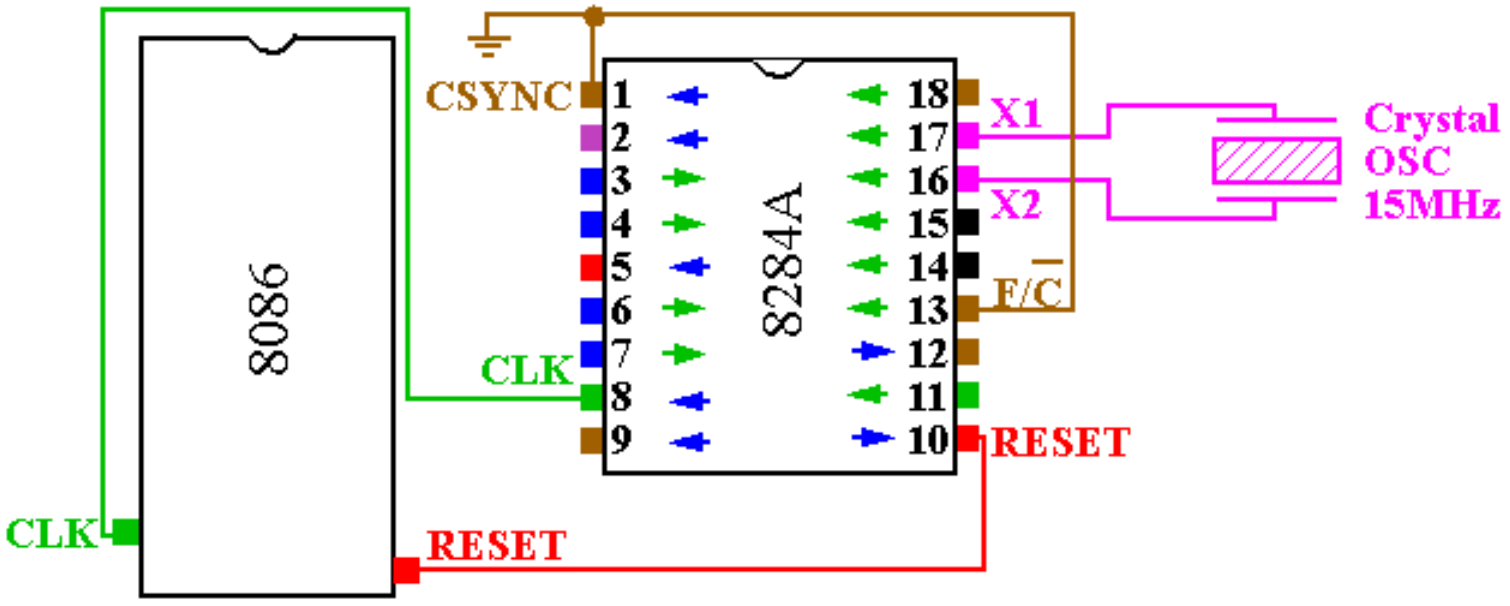


Microprocessor Operation

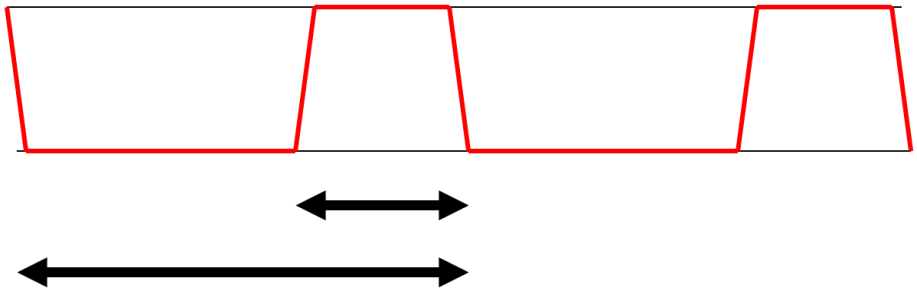
- The time a µP requires to complete **fetch-decode-execute** operation of a single instruction is known as ***Instruction Cycle***
- An ***Instruction Cycle*** consists of one or more ***Machine Cycles***
- A basic µP operation such as reading or writing a byte/word from or to memory or I/O port is called a ***Machine Cycle or Bus cycle***
- A ***Machine (bus) cycle*** consists of at least **four** clock cycles, called **T** states.
- One cycle of a clock is called a **State**

Clock Generation

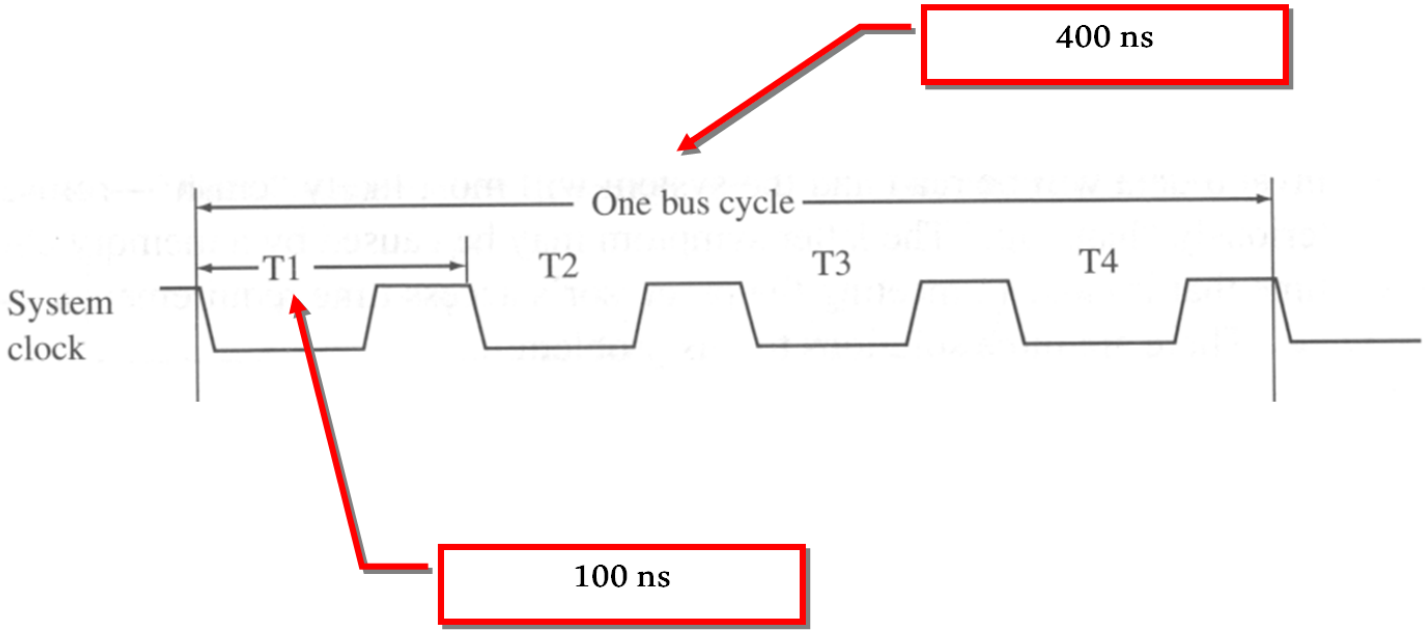
- Clock generator circuit is 8254A and connected to **pin 19** (**CLK**) of 8086.



System Clock Concept



33% Duty Cycle



System Clock Concept

- 8086 is found to operate in between 5 to 10 Mhz.
- Each **bus cycle** consists of at least 4 **clock cycles**.
- An 8086 running at 5MHz, it's clock pulses will be of 200ns and it would take 800ns for a complete bus cycle.
- Again, an 8086 running at 10MHz, it's clock pulses will be of 100ns and it would take 400ns for a complete bus cycle.
- Each **read** or **write** operation take 1 bus cycles.

Clock States

- **Why are there T states?**
  - In the 8086, the address and data lines are multiplexed.
  - The microprocessor needs time to change the signals during each bus cycle.
  - Memory devices need time to interpret the address value and then **read/write** the data (*access time*)

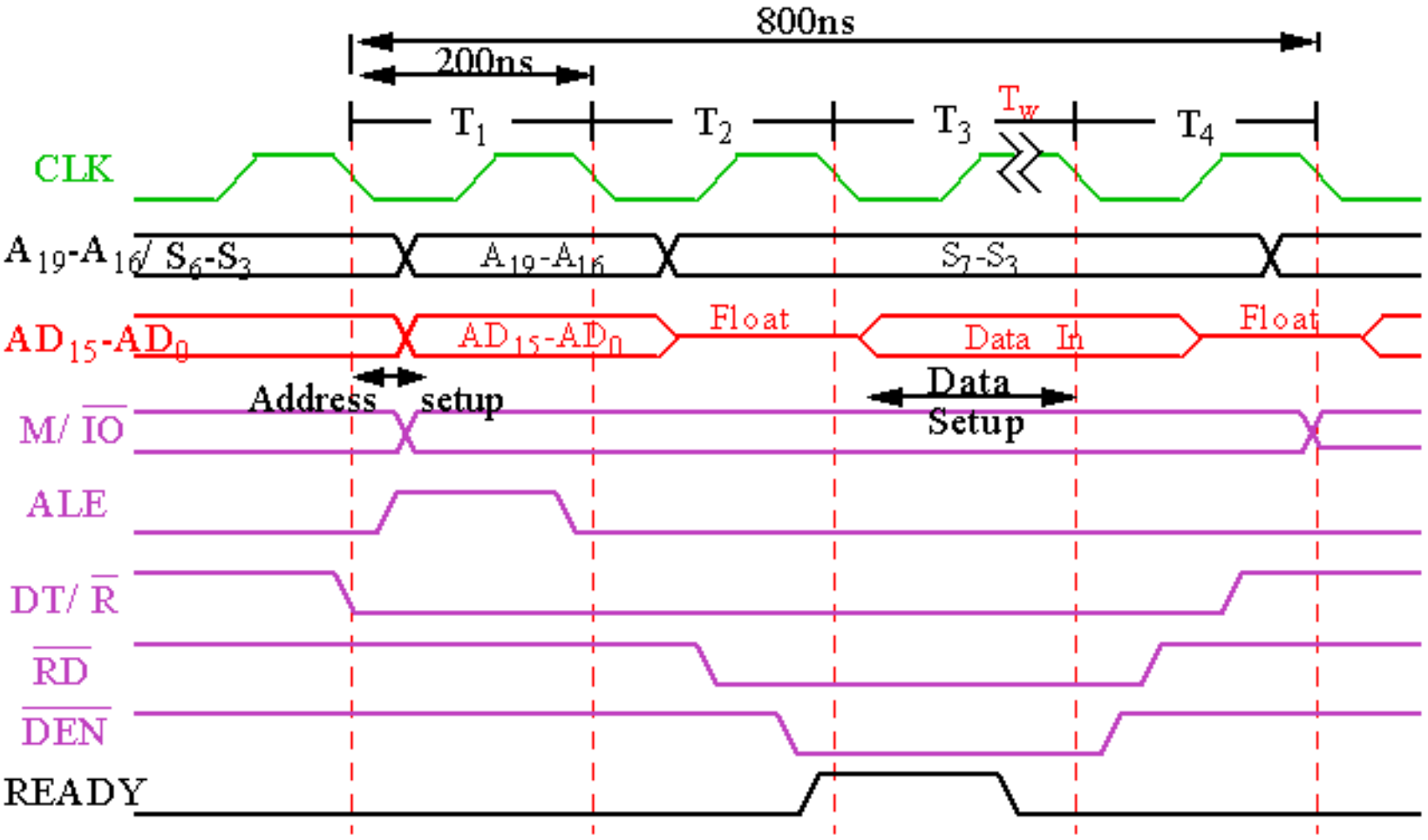
Clock States

- A specific, defined action occurs during each T states (labeled $T_1 - T_4$)
- **T_1: *Address is output***
  - Address of memory or I/O is sent out by 8086 via address bus
  - Used Control signals: ALE, DT/R', M/IO' shows some output
- **T_2: *Bus cycle type (MEMORY/IO, READ/WRITE)***
  - 8086 issues either RD' or WR' and DEN'
  - In case of **WRITE (WR)** operation, data to be written appear on data bus

Clock States

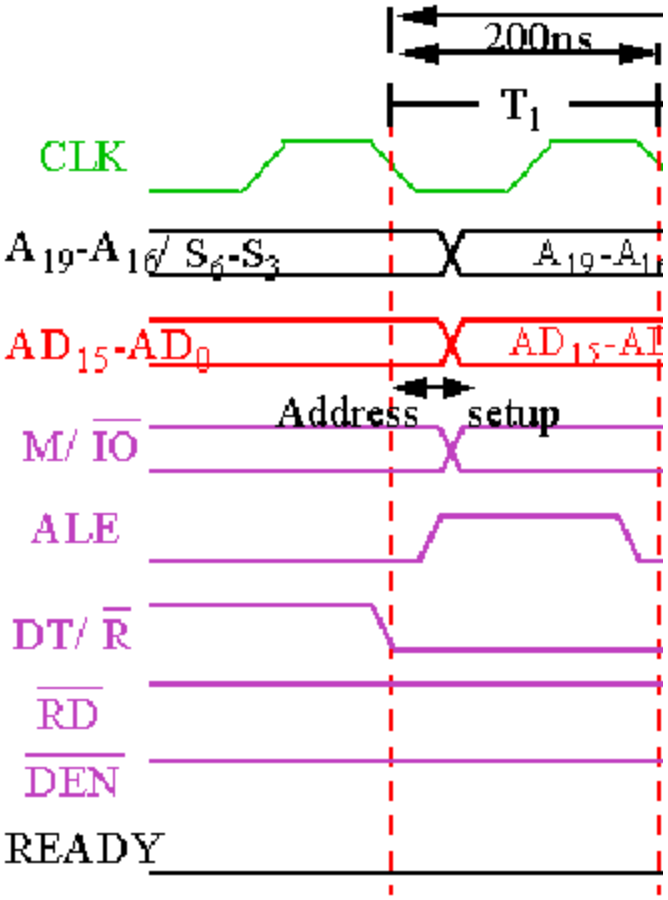
- **T_3: *Data is supplied***
  - READY is sampled at the end of T2
    - If READY is low, T3 becomes a wait state (TW), means no operation (NOP).
    - In **READ** bus cycle data bus is sampled at end of T_3
- **T4: *Data latched by μP, and control signals removed***
  - All bus signals deactivated in preparation for next bus cycle
  - μP sampled data bus for data that read from M or I/O
  - At trailing edge of WR', transfer data to M or I/O

READ BUS Timing (Complete BUS Cycle)



Bus Timing for a Read Operation

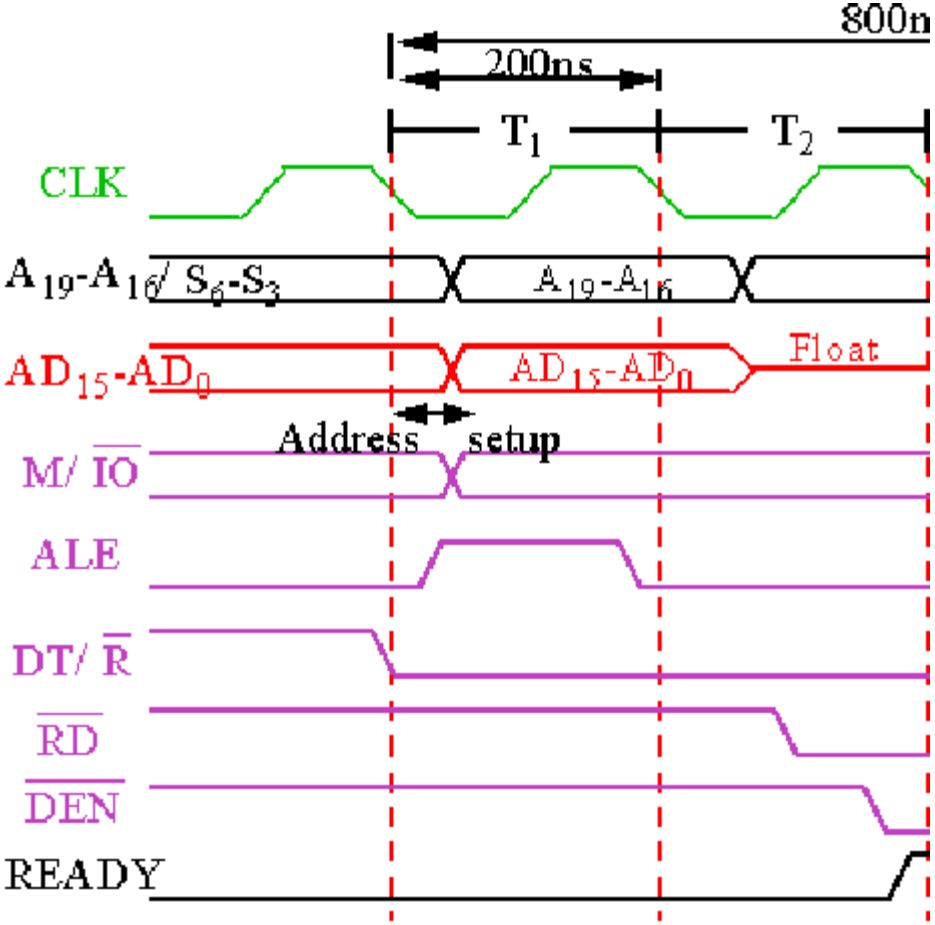
READ BUS Timing (During T_1 State)



During T_1 :

- *The address is placed on the Address/Data bus.*
- *Control signals*
  - ***M/ IO'*** *specify memory or I/O,*
  - ***ALE*** *latch the address onto the address bus and*
  - ***DT/R'*** *set the direction of data transfer on data bus.*

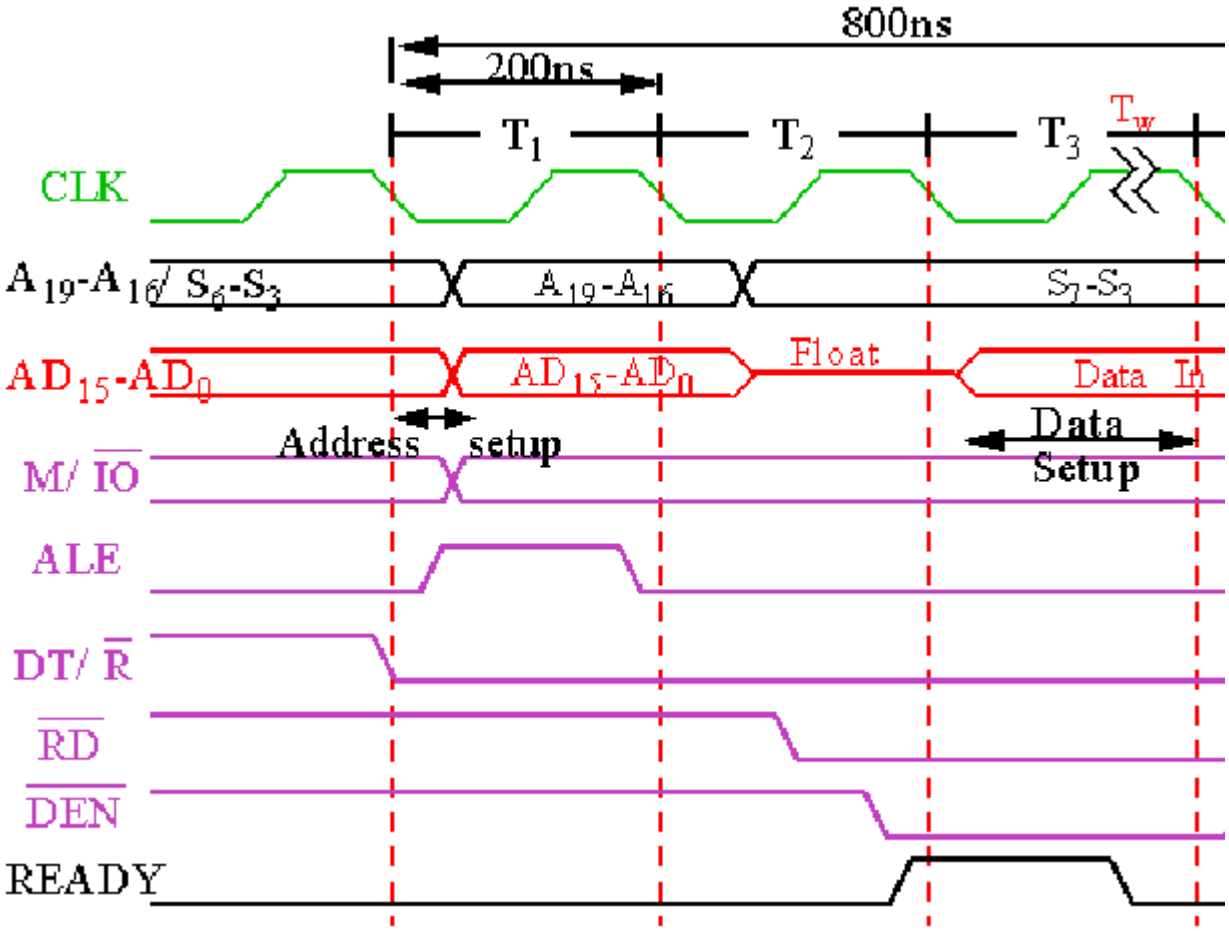
READ BUS Timing (During T_2 State)



During T_2 :

- *8086 issues the* **RD'** *(or* **WR'** in case of write operation) *signal.*
- **DEN'** *enables the 8086 to receive the data for* ***READ*** *operation (or the memory or I/O device to receive the data for* ***WRITE*** *operation).*

READ BUS Timing (During T_3 State)

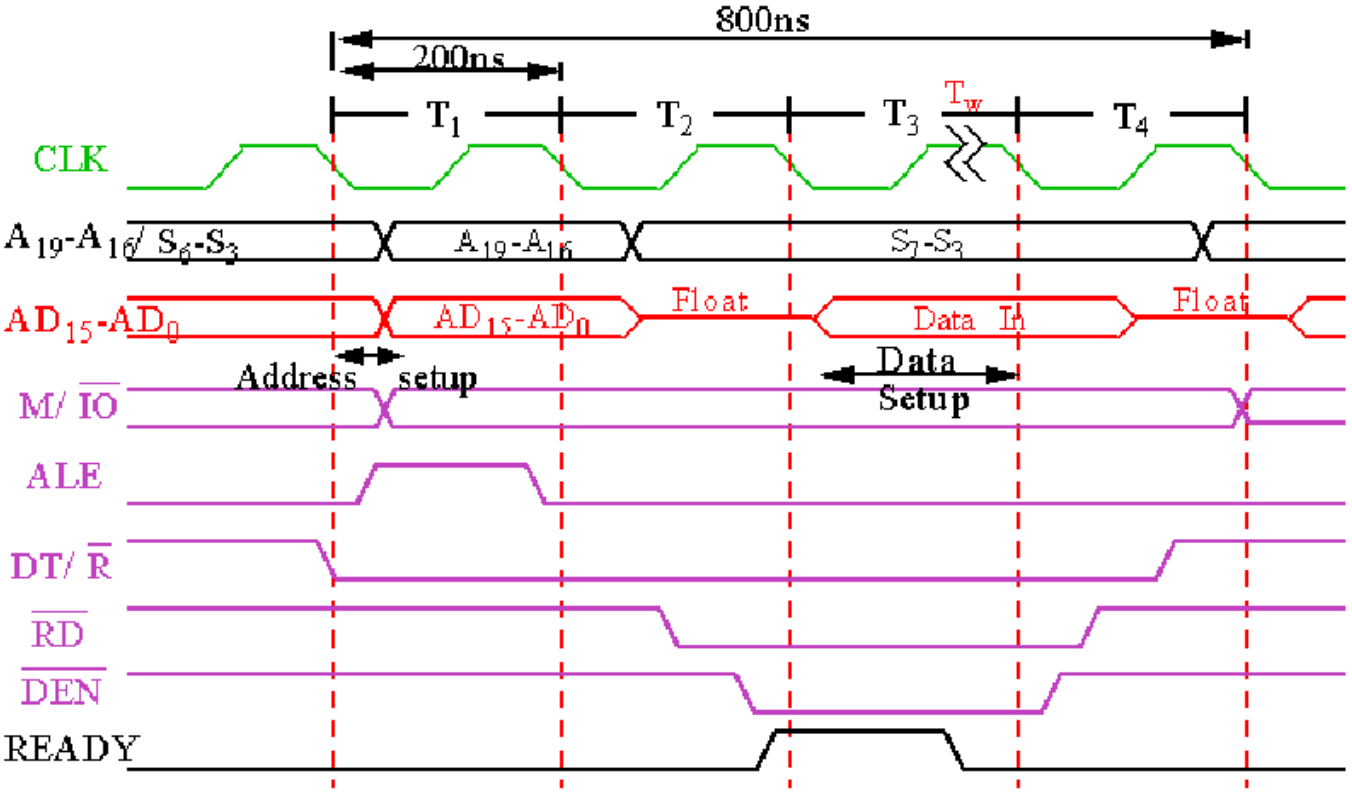


During T_3 :

- *This cycle is provided to allow memory to access data.*

- ***READY** is sampled at the end of T_2 .*
  - *If low, T_3 becomes a **wait** state.*
  - *Otherwise, the data bus is sampled at the end of T_3 .*

READ BUS Timing (During T_4 State)

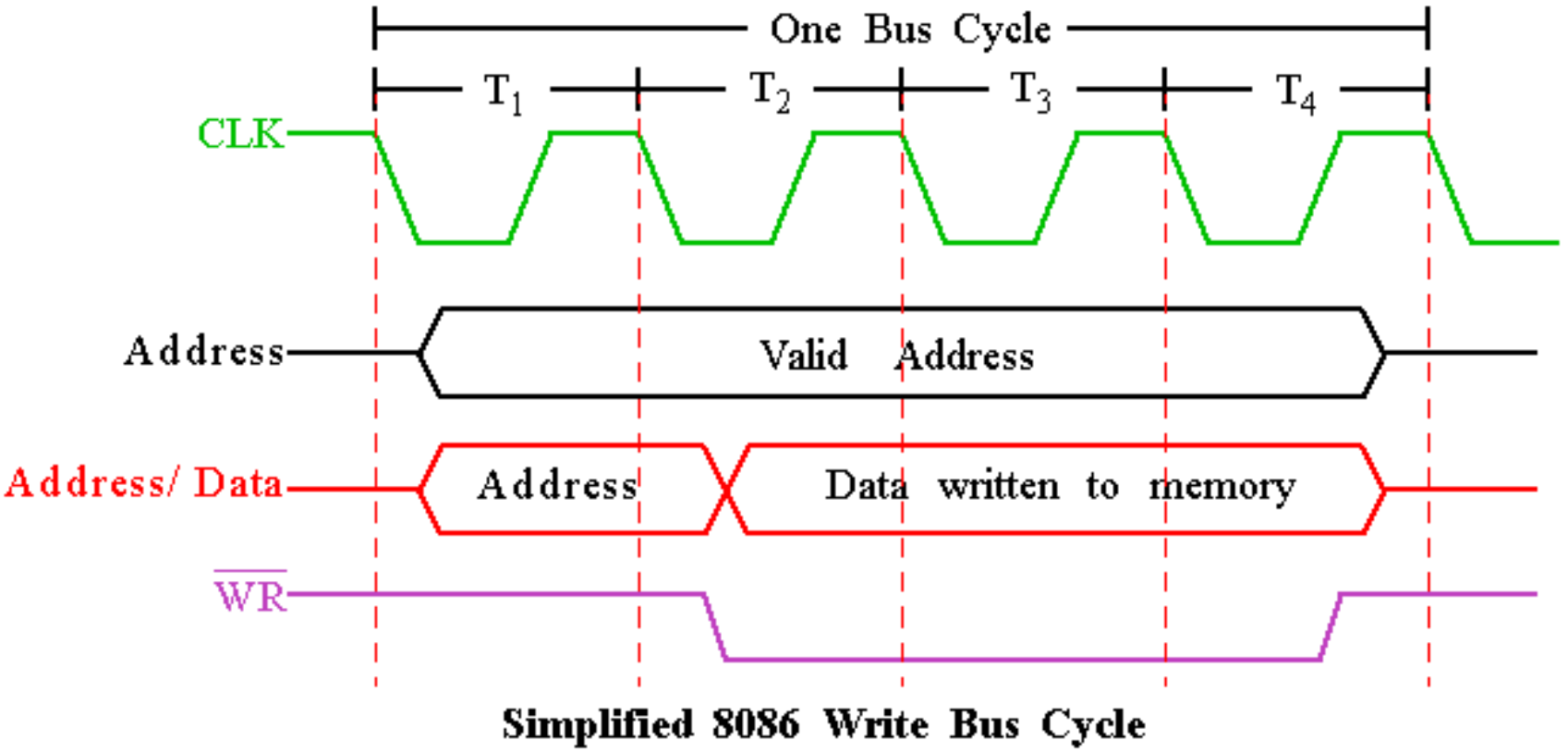


Bus Timing for a Read Operation

During T_4 :

- *All bus signals are deactivated, in preparation for next bus cycle.*
- *Data is sampled for **READ** (or **WRITE** occurs for write) data.*

WRITE BUS Timing

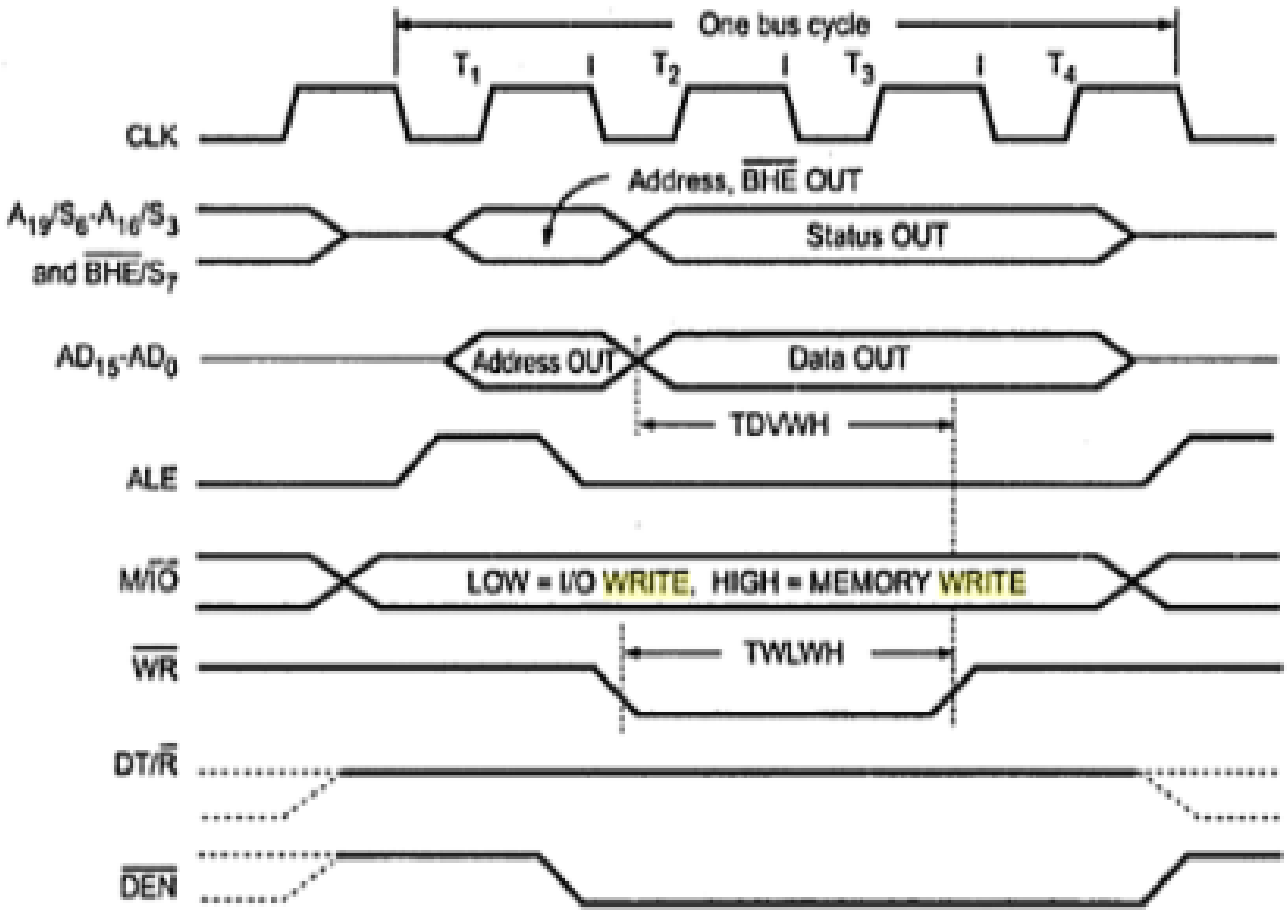


Simplified 8086 Write Bus Cycle

- What are the functions of each pin in different **T states** during **WRITE** operation ??

Write Bus Timing Full Diagram

(Ready Pin will be same as Read bus timing)



Write operation