Assignment - 01

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Questions

1. What is Schmitt Trigger (ST)?

Ans: The comparator circuit with hysteresis implemented by applying positive feedback to the non-inverting input of a comparator of differential amplifier is called Schmitt Trigger (ST). It's called 'trigger' because the output will keep its value until input changes sufficiently.

2. Why is it used?

Ans: Comparators are not limited by output slew rate and transmission times are in order of nanoseconds. Because comparators are, by nature, very fast. They have sensible inputs because of very high gains and so, tiny changes in input can cause big changes in output.

The problem gets worse when it is required to maintain a stable output. The input also has a lot of noise which can change the output signal.

The remedy is to use hysteresis. In this case, with addition of a signal register before the inverting terminals. That is why Schmitt triggers are used.

3. Draw Inverting Schmitt Trigger circuit.

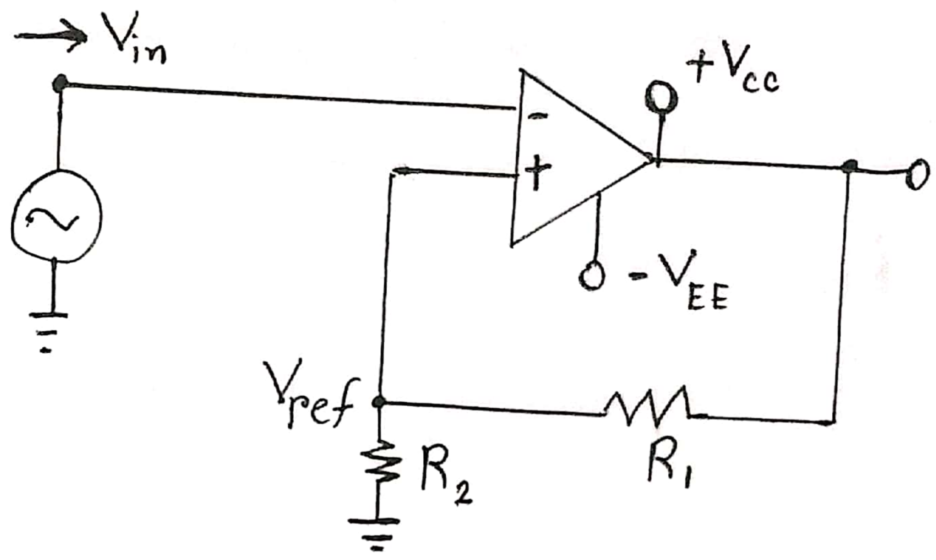


Fig: Inverting Schmitt Trigger Circuit

4. Draw a non-inverting Schmitt Trigger Circuit.

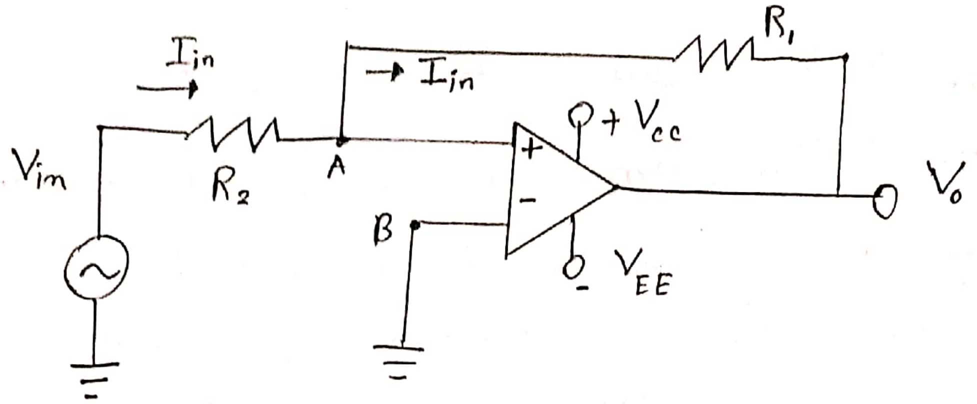


Fig: Non-inverting Schmitt Trigger Circuit

5. How comparator circuit is utilized in ST circuit?

Ans: A Schmitt trigger is nothing but comparator with positive feedback. In Schmitt trigger when V_{in} is positive, the output will be low and if V_{in} is negative, the output will be high. If the input contains noise with a peak of 1 mV or higher, the comparator will identify zero crossing produced by this noise. If the input is noisy then comparator can be utilized for zero-crossing.

6. What do you mean by UTP and LTP. Briefly explain.

Ans:

→ UTP: UTP stands for Upper Trigger Point. For input voltage, the value that triggers the ST circuit and causes output voltage to jump from 'Low' to 'High' state is called Upper Trigger point or UTP. The input needs to be sufficiently changed for the ST circuit to trigger. This upper limit is UTP.

→ LTP: LTP stands for Lower Trigger Point. For input voltage, the value which triggers the ST circuit from 'High' to 'Low' state is Lower Trigger Point or LTP. Just like UTP, LTP is the sufficient input voltage required to change states but in opposite direction.

7. How ST exhibits hystensis? Elaborate with details. Draw diagrams and waveshapes to elucidate explanations.

Ans: In the non-inverting configuration, when the input is higher than the threshold, the output is high and this threshold is UTP. On the other hand, when the input is below another threshold or LTP, the output will also be low. The output retain its value when the input is between these two threshold values. In this way, the property of hystensis is exhibited by ST circuit.

Inverting Schmitt Trigger:

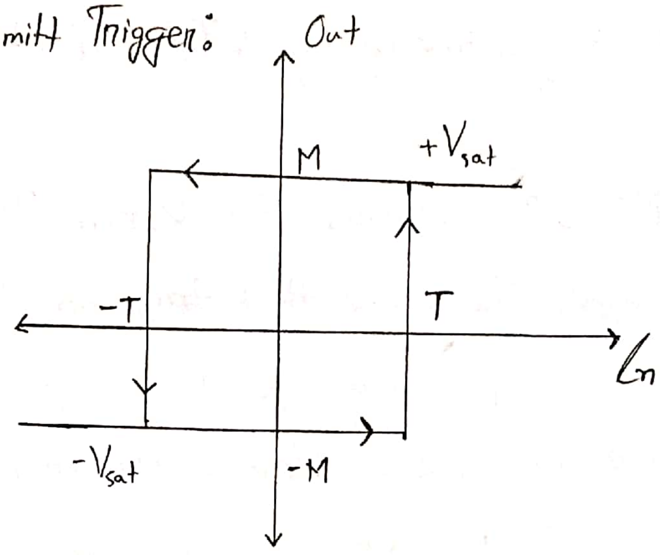
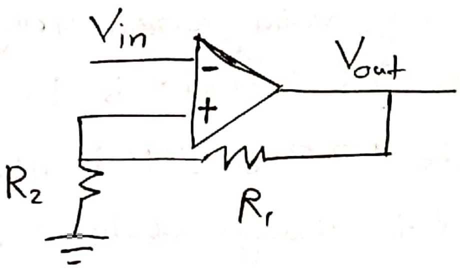


Fig: The hysteresis loop for Schmitt trigger where T and -T are switching thresholds and M and -M are output voltages.



Here, $UTP = \frac{R_2}{R_1+R_2} \times V_{sat}$

$LTP = \frac{R_2}{R_1+R_2} \times (-V_{sat})$

$$V_{hys} = UTP - LTP$$

$$= 2 \times \frac{R_2}{R_1+R_2} \times V_{sat}$$

$$= 2\beta \times V_{sat}$$

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When $V_{out} = +V_{sat}$, the reference valtage or UTP is given by

$$UTP = \frac{(V_{sat} - V_R) \times R_2}{R_1 + R_2} + V_R$$

$$= \beta V_{sat} + \frac{R_1 V_R}{R_1 + R_2}$$

Similarly, when $V_{out} = -V_{sat}$, the reference valtage LTP is

$$LTP = \frac{(-V_{sat} - V_R) R_2}{R_1 + R_2} + V_R$$

$$= -\beta V_{sat} + \frac{R_1 V_R}{R_1 + R_2}$$

For positive value of V_R, the loop is shifted to the right and for negative value, it is shifted to the left. The hystensis voltage V_{hys} remains the same in both cases.

Non-inventing Schmitt Trigger:

For this implementation, the feedback is at non-inventing terminal, the inventing terminal is grounded and the input valtage is conned to non-inventing input.

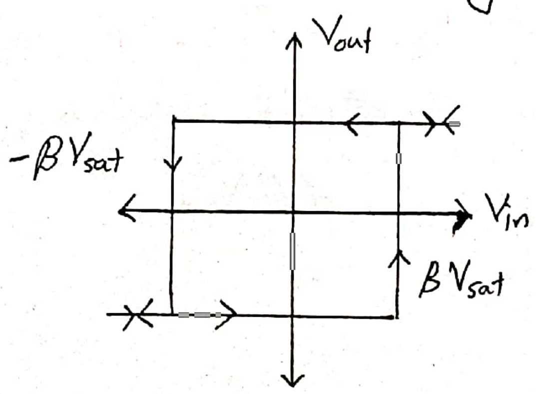
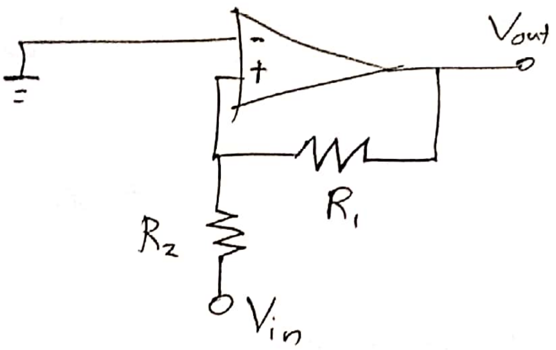


Fig: Hystensis loop for non-inventing Schmitt Trigger



Assuming negatively saturated output, we get negative feedback voltage. The feedback voltage will hold the output in negative saturation until input becomes positive enough to make positive voltage.

$$V_t = \frac{(-V_{sat} - V_{in})}{R_1 + R_2} R_2 + V_{in}$$

$$= \frac{R_1}{R_1 + R_2} \times \left(-\frac{R_2 V_{sat}}{R_1} + V_{in}\right)$$

When V_{in} is in negative with magnitude greater than $\left(\frac{R_2}{R_1}\right) \times V_{sat}$ then the output switches to $-V_{sat}$. Therefore

$$LTP = -\frac{R_2}{R_1} V_{sat} = -\beta V_{sat}$$

$$\text{Here, } V_{hys} = UTP - LTP$$

$$= \beta V_{sat} - (-\beta V_{sat})$$

$$= 2\beta V_{sat}.$$

8. Mention 5 applications of Schmitt Trigger circuit.

Ans:

(i) Schmitt triggers can be used to make simple oscillator. Having two thresholds give Schmitt triggers the ability like 555 timer IC to act like predictable oscillators.

(ii) Changing sine waves to square waves.

(iii) Schmitt triggers are used as switch debouncers.

(iv) In signal controlling, it is used to remove noise from signals.

(v) Used in function generators and switching power supplies.

9. Design a voltage level detector with noise immunity according to given condition.

Ans:

In our voltage level detector, an inverting configuration is required for the triggered action. Let the hysteresis voltage be 20% larger than the maximum PP noise voltage.

$$\therefore V_{hys} = 0.2 + (20\% \times 0.2) = 0.24\ V$$

So, upper trigger level $= -2.5 + 0.12 = -2.38\ V$

lower trigger level $= -2.5 - 0.12 = -2.62\ V$

The output levels are V_H and V_L instead of $+V_{sat}$ and $-V_{sat}$. So, hystersis voltage is

$$V_{hys} = \frac{R_2}{R_1+R_2}(V_H - V_L)$$

$$\Rightarrow \frac{R_1}{R_2}\ \frac{V_H - V_L}{V_{hys}} = 1 + \frac{R_1}{R_2}$$

$$\Rightarrow \frac{R_1}{R_2} = \frac{V_H - V_L}{V_{hys}} - 1$$

$$\Rightarrow \frac{R_1}{R_2} = \frac{10-0}{0.24} = 40.7$$

The reference voltage V_R can be optained from the expression of LTP,

$$LTP = \beta V_L + \frac{R_1 V_R}{R_1+R_2}$$

$$\Rightarrow V_R = \left(1+\frac{R_1}{R_2}\right) LTP$$

$$\Rightarrow V_R = (1+40.7^{-1})(-2.62)$$

$$= -2.68\text{ V}$$

Here,
$LTP = -2.62\text{ V}$
$V_L = 0$

Here any value of R_1 and R_2 can be selected that satisfies the ratio 40.7. It is better to use more than 100 kΩ for sum of R_1 and R_2, and 1.3 kΩ for pull-up resistor on output.

The final design can be

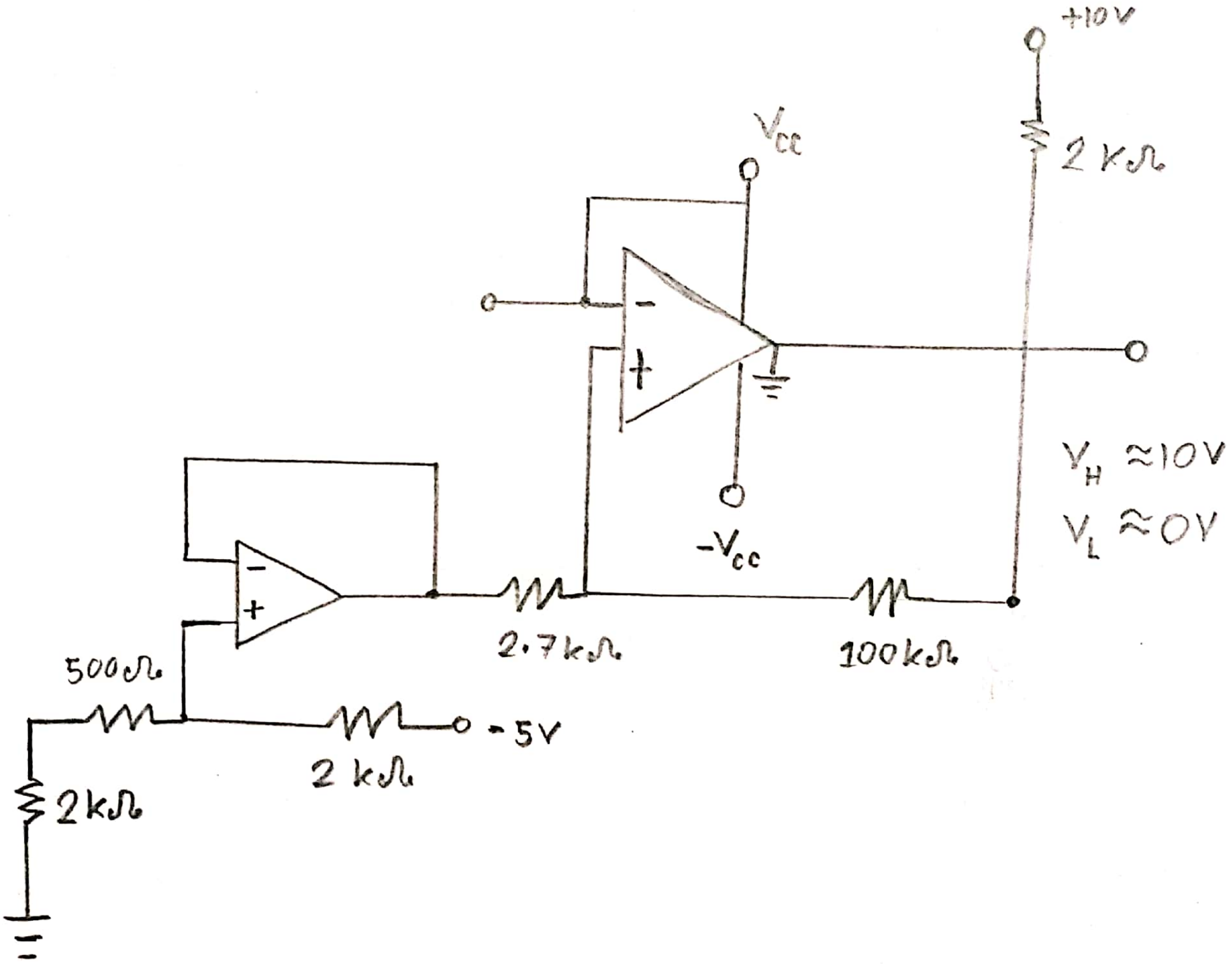


Fig: Final Design of Voltage Level Detector