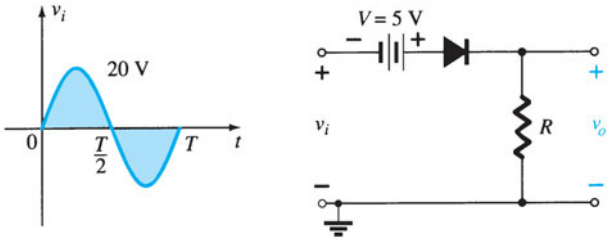


FIG. 2.74
Series clipper for Example 2.18.

Step 3: The transition model is substituted in Fig. 2.75, and we find that the transition from one state to the other will occur when

$$v_i + 5\text{ V} = 0\text{ V}$$

or

$$v_i = -5\text{ V}$$

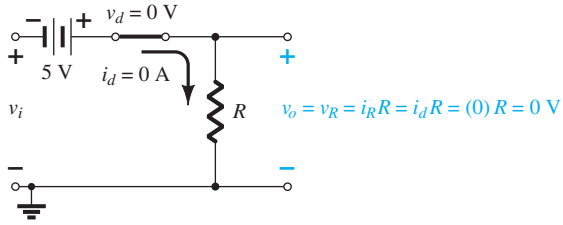


FIG. 2.75
Determining the transition level for the clipper of Fig. 2.74.

Step 4: In Fig. 2.76 a horizontal line is drawn through the applied voltage at the transition level. For voltages less than −5 V the diode is in the open-circuit state and the output is 0 V, as shown in the sketch of v_o. Using Fig. 2.76, we find that for conditions when the diode is on and the diode current is established the output voltage will be the following, as determined using Kirchhoff's voltage law:

$$v_o = v_i + 5\text{ V}$$

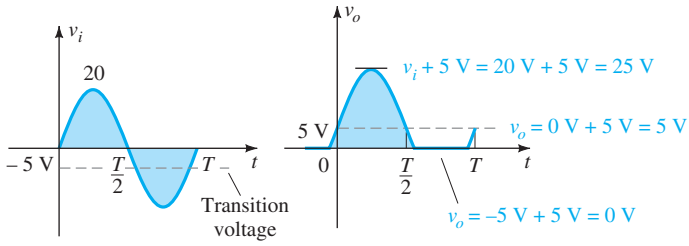


FIG. 2.76
Sketching v_o for Example 2.18.

The analysis of clipper networks with square-wave inputs is actually easier than with sinusoidal inputs because only two levels have to be considered. In other words, the network can be analyzed as if it had two dc level inputs with the resulting v_o plotted in the proper time frame. The next example demonstrates the procedure.

EXAMPLE 2.19 Find the output voltage for the network examined in Example 2.18 if the applied signal is the square wave of Fig. 2.77.

Solution: For $v_i = 20\text{ V}\ (0 \rightarrow T/2)$ the network of Fig. 2.78 results. The diode is in the short-circuit state, and $v_o = 20\text{ V} + 5\text{ V} = 25\text{ V}$. For $v_i = -10\text{ V}$ the network of Fig. 2.79

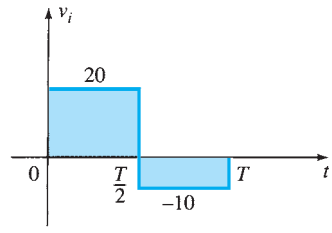


FIG. 2.77
Applied signal for Example 2.19.

results, placing the diode in the "off" state, and $v_o = i_R R = (0)R = 0$ V. The resulting output voltage appears in Fig. 2.80.

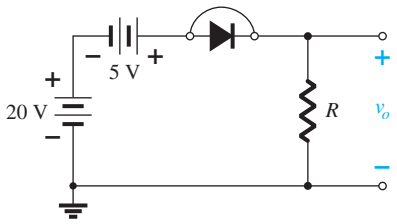


FIG. 2.78
v_o at $v_i = +20$ V.

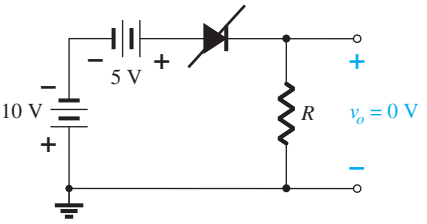


FIG. 2.79
v_o at $v_i = -10$ V.

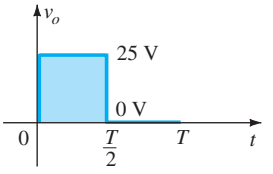


FIG. 2.80
Sketching v_o for Example 2.19.

Note in Example 2.19 that the clipper not only clipped off 5 V from the total swing, but also raised the dc level of the signal by 5 V.

Parallel

The network of Fig. 2.81 is the simplest of parallel diode configurations with the output for the same inputs of Fig. 2.68. The analysis of parallel configurations is very similar to that applied to series configurations, as demonstrated in the next example.

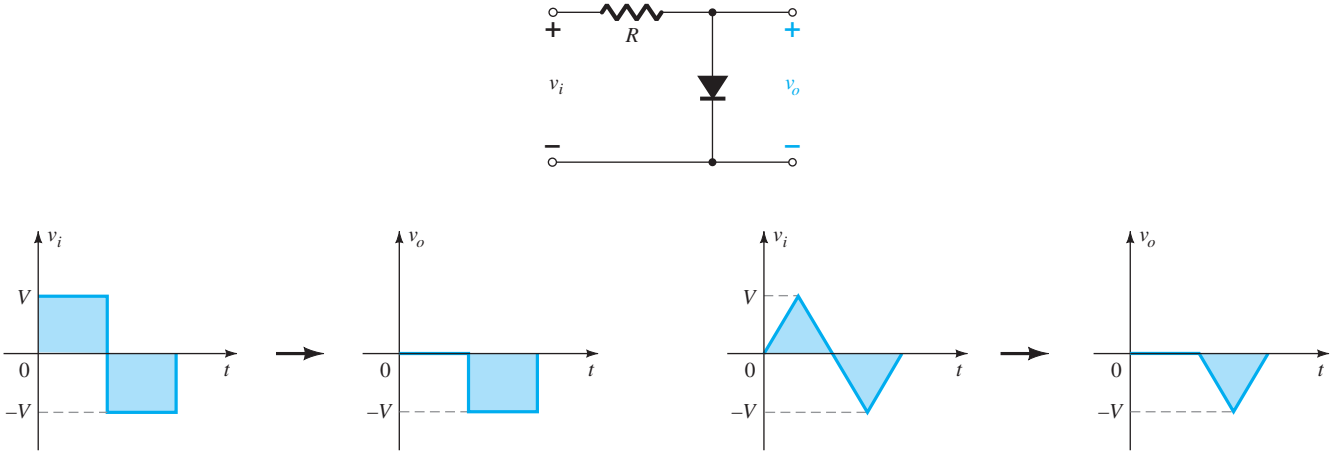


FIG. 2.81
Response to a parallel clipper.

EXAMPLE 2.20 Determine v_o for the network of Fig. 2.82.

Solution:

Step 1: In this example the output is defined across the series combination of the 4-V supply and the diode, not across the resistor *R*.

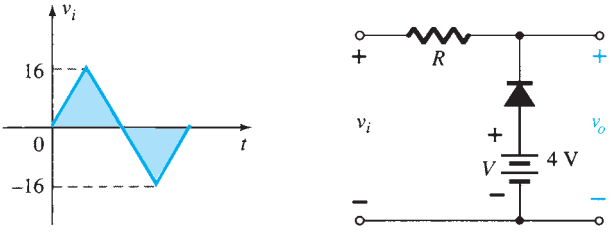


FIG. 2.82
Example 2.20.

Step 2: The polarity of the dc supply and the direction of the diode strongly suggest that the diode will be in the "on" state for a good portion of the negative region of the input signal. In fact, it is interesting to note that since the output is directly across the series combination, when the diode is in its short-circuit state the output voltage will be directly across the 4-V dc supply, requiring that the output be fixed at 4 V. In other words, when the diode is on the output will be 4 V. Other than that, when the diode is an open circuit, the current through the series network will be 0 mA and the voltage drop across the resistor will be 0 V. That will result in $v_o = v_i$ whenever the diode is off.

Step 3: The transition level of the input voltage can be found from Fig. 2.83 by substituting the short-circuit equivalent and remembering the diode current is 0 mA at the instant of transition. The result is a change in state when

$$v_i = 4 \text{ V}$$

Step 4: In Fig. 2.84 the transition level is drawn along with $v_o = 4$ V when the diode is on. For $v_i \geq 4$ V, $v_o = 4$ V, and the waveform is simply repeated on the output plot.

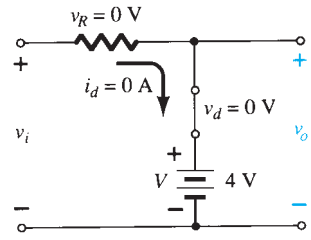


FIG. 2.83
Determining the transition level for Example 2.20.

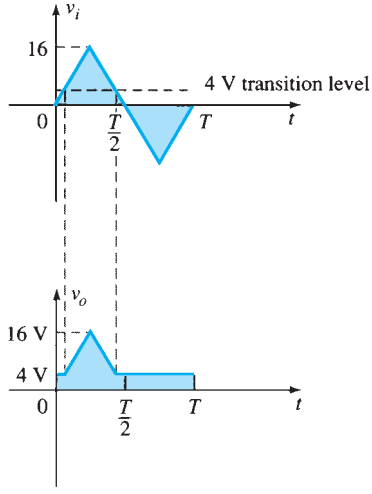


FIG. 2.84
Sketching v_o for Example 2.20.

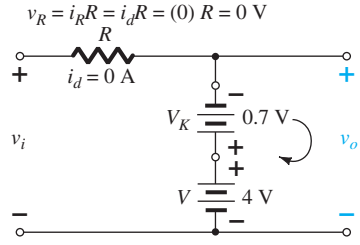


FIG. 2.85
Determining the transition level for the network of Fig. 2.82.

To examine the effects of the knee voltage V_K of a silicon diode on the output response, the next example will specify a silicon diode rather than the ideal diode equivalent.

EXAMPLE 2.21 Repeat Example 2.20 using a silicon diode with $V_K = 0.7$ V.

Solution: The transition voltage can first be determined by applying the condition $i_d = 0$ A at $v_d = V_D = 0.7$ V and obtaining the network of Fig. 2.85. Applying Kirchhoff's voltage law around the output loop in the clockwise direction, we find that

$$v_i + V_K - V = 0$$

and

$$v_i = V - V_K = 4 \text{ V} - 0.7 \text{ V} = \mathbf{3.3\ V}$$

For input voltages greater than 3.3 V, the diode will be an open circuit and $v_o = v_i$. For input voltages less than 3.3 V, the diode will be in the "on" state and the network of Fig. 2.86 results, where

$$v_o = 4 \text{ V} - 0.7 \text{ V} = \mathbf{3.3\ V}$$

The resulting output waveform appears in Fig. 2.87. Note that the only effect of V_K was to drop the transition level to 3.3 from 4 V.

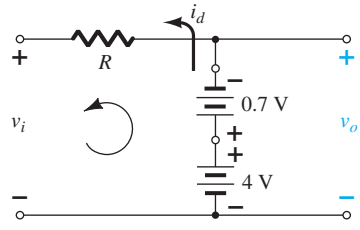


FIG. 2.86
Determining v_o for the diode of Fig. 2.82 in the "on" state.

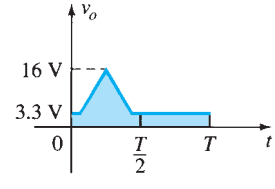
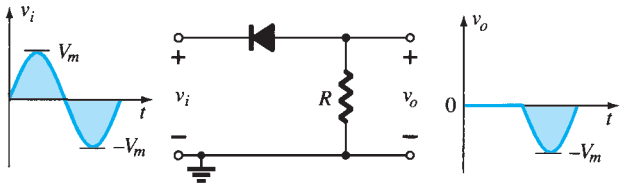


FIG. 2.87
Sketching v_o for Example 2.21.

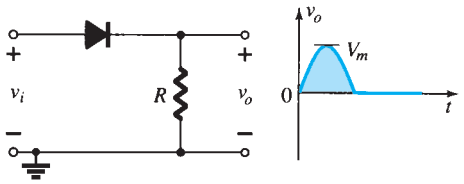
There is no question that including the effects of V_K will complicate the analysis somewhat, but once the analysis is understood with the ideal diode, the procedure, including the effects of V_K, will not be that difficult.

Simple Series Clippers (Ideal Diodes)

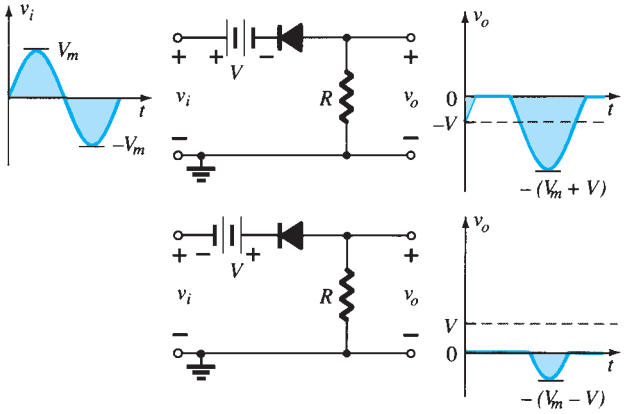
POSITIVE

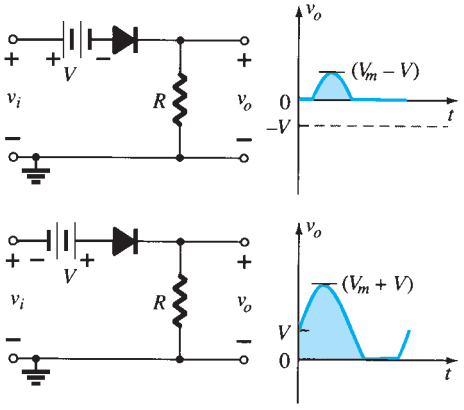


NEGATIVE

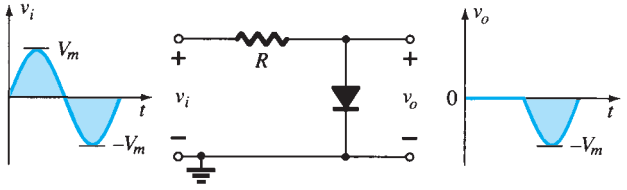


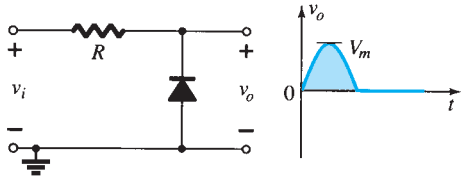
Biased Series Clippers (Ideal Diodes)



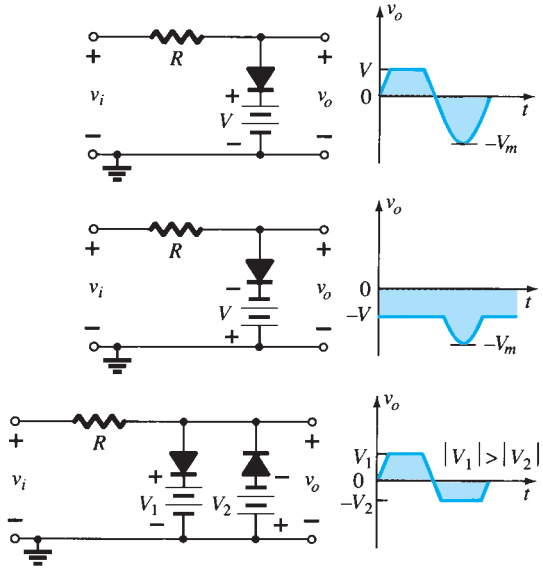


Simple Parallel Clippers (Ideal Diodes)





Biased Parallel Clippers (Ideal Diodes)



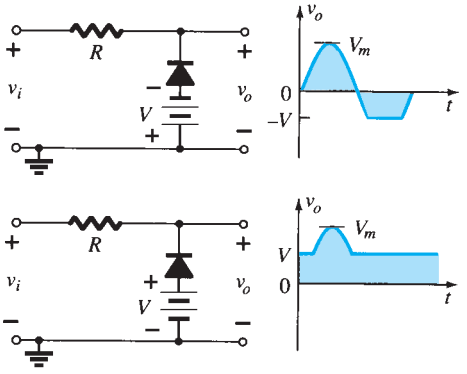


FIG. 2.88
Clipping circuits.

Summary

A variety of series and parallel clippers with the resulting output for the sinusoidal input are provided in Fig. 2.88. In particular, note the response of the last configuration, with its ability to clip off a positive and a negative section as determined by the magnitude of the dc supplies.

2.9 CLAMPERS

The previous section investigated a number of diode configurations that clipped off a portion of the applied signal without changing the remaining part of the waveform. This section will examine a variety of diode configurations that shift the applied signal to a different level.

A clamper is a network constructed of a diode, a resistor, and a capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signal.

Additional shifts can also be obtained by introducing a dc supply to the basic structure. The chosen resistor and capacitor of the network must be chosen such that the time constant determined by $\tau = RC$ is sufficiently large to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is nonconducting. Throughout the analysis we assume that for all practical purposes the capacitor fully charges or discharges in five time constants.

The simplest of clamper networks is provided in Fig. 2.89. It is important to note that the capacitor is connected directly between input and output signals and the resistor and the diode are connected in parallel with the output signal.

Clamping networks have a capacitor connected directly from input to output with a resistive element in parallel with the output signal. The diode is also in parallel with the output signal but may or may not have a series dc supply as an added element.

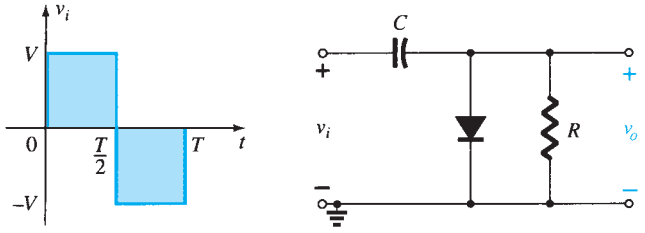


FIG. 2.89
Clamper.

There is a sequence of steps that can be applied to help make the analysis straightforward. It is not the only approach to examining clampers, but it does offer an option if difficulties surface.

Step 1: Start the analysis by examining the response of the portion of the input signal that will forward bias the diode.

Step 2: During the period that the diode is in the "on" state, assume that the capacitor will charge up instantaneously to a voltage level determined by the surrounding network.

For the network of Fig. 2.89 the diode will be forward biased for the positive portion of the applied signal. For the interval 0 to $T/2$ the network will appear as shown in Fig. 2.90. The short-circuit equivalent for the diode will result in $v_o = 0$ V for this time interval, as shown in the sketch of v_o in Fig. 2.92. During this same interval of time, the time constant determined by $\tau = RC$ is very small because the resistor R has been effectively "shorted out" by the conducting diode and the only resistance present is the inherent (contact, wire) resistance of the network. The result is that the capacitor will quickly charge to the peak value of V volts as shown in Fig. 2.90 with the polarity indicated.

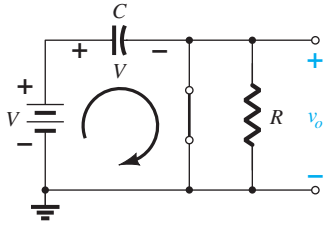


FIG. 2.90
Diode "on" and the capacitor charging to V volts.

Step 3: Assume that during the period when the diode is in the "off" state the capacitor holds on to its established voltage level.

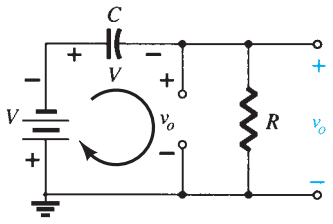


FIG. 2.91
Determining v_o with the diode "off."

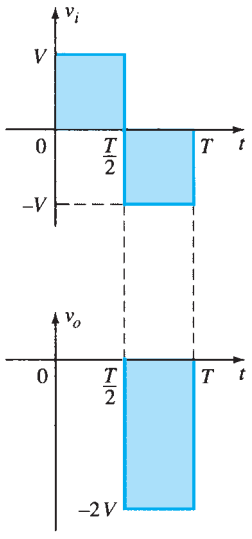


FIG. 2.92
Sketching v_o for the network of Fig. 2.91.

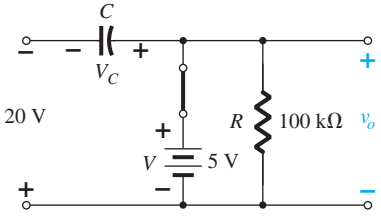


FIG. 2.94
Determining v_o and V_C with the diode in the "on" state.

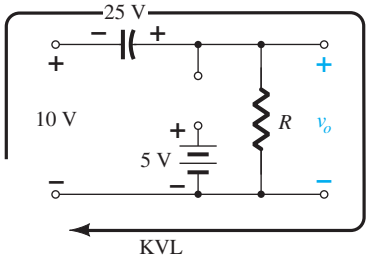


FIG. 2.95
Determining v_o with the diode in the "off" state.

Step 4: Throughout the analysis, maintain a continual awareness of the location and defined polarity for v_o to ensure that the proper levels are obtained.

When the input switches to the $-V$ state, the network will appear as shown in Fig. 2.91, with the open-circuit equivalent for the diode determined by the applied signal and stored voltage across the capacitor—both "pressuring" current through the diode from cathode to anode. Now that R is back in the network the time constant determined by the RC product is sufficiently large to establish a discharge period 5τ, much greater than the period $T/2 \rightarrow T$, and it can be assumed on an approximate basis that the capacitor holds onto all its charge and, therefore, voltage (since $V = Q/C$) during this period.

Since v_o is in parallel with the diode and resistor, it can also be drawn in the alternative position shown in Fig. 2.91. Applying Kirchhoff's voltage law around the input loop results in

$$-V - V - v_o = 0$$

and

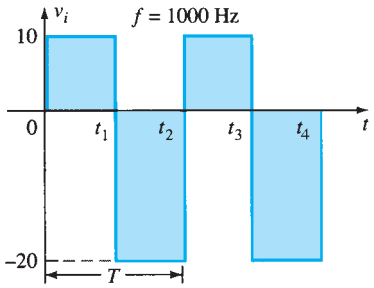
$$v_o = -2V$$

The negative sign results from the fact that the polarity of $2V$ is opposite to the polarity defined for v_o. The resulting output waveform appears in Fig. 2.92 with the input signal. The output signal is clamped to 0 V for the interval 0 to $T/2$ but maintains the same total swing ($2V$) as the input.

Step 5: Check that the total swing of the output matches that of the input.

This is a property that applies for all clamping networks, giving an excellent check on the results obtained.

EXAMPLE 2.22 Determine v_o for the network of Fig. 2.93 for the input indicated.



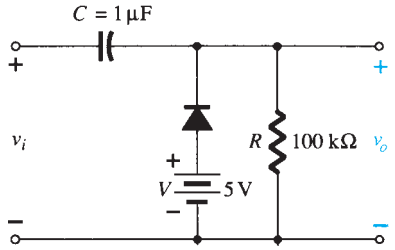


FIG. 2.93
Applied signal and network for Example 2.22.

Solution: Note that the frequency is 1000 Hz, resulting in a period of 1 ms and an interval of 0.5 ms between levels. The analysis will begin with the period $t_1 \rightarrow t_2$ of the input signal since the diode is in its short-circuit state. For this interval the network will appear as shown in Fig. 2.94. The output is across R, but it is also directly across the 5-V battery if one follows the direct connection between the defined terminals for v_o and the battery terminals. The result is $v_o = 5$ V for this interval. Applying Kirchhoff's voltage law around the input loop results in

$$-20\text{ V} + V_C - 5\text{ V} = 0$$

and

$$V_C = 25\text{ V}$$

The capacitor will therefore charge up to 25 V. In this case the resistor R is not shorted out by the diode, but a Thévenin equivalent circuit of that portion of the network that includes the battery and the resistor will result in $R_{Th} = 0\ \Omega$ with $E_{Th} = V = 5$ V. For the period $t_2 \rightarrow t_3$ the network will appear as shown in Fig. 2.95.

The open-circuit equivalent for the diode removes the 5-V battery from having any effect on v_o, and applying Kirchhoff's voltage law around the outside loop of the network results in

$$+10\text{ V} + 25\text{ V} - v_o = 0$$

and

$$v_o = 35\text{ V}$$

The time constant of the discharging network of Fig. 2.95 is determined by the product RC and has the magnitude

$$\tau = RC = (100\,\text{k}\Omega)(0.1\,\mu\text{F}) = 0.01\text{ s} = 10\text{ ms}$$

The total discharge time is therefore $5\tau = 5(10\text{ ms}) = 50\text{ ms}$.

Since the interval $t_2 \rightarrow t_3$ will only last for 0.5 ms, it is certainly a good approximation that the capacitor will hold its voltage during the discharge period between pulses of the input signal. The resulting output appears in Fig. 2.96 with the input signal. Note that the output swing of 30 V matches the input swing as noted in step 5.

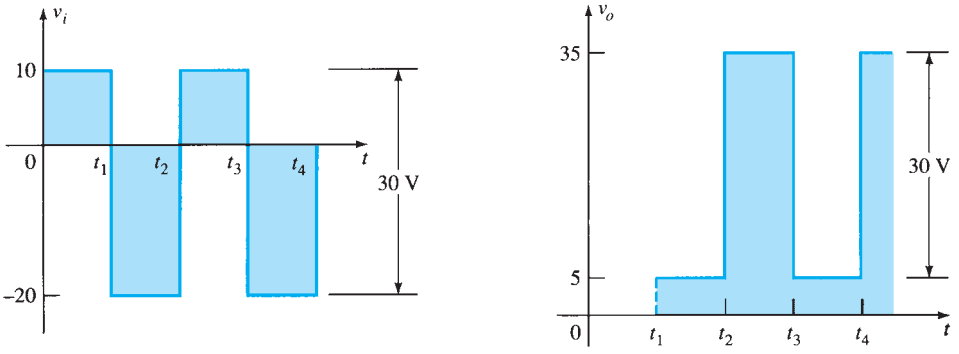


FIG. 2.96
v_i and v_o for the clamper of Fig. 2.93.

EXAMPLE 2.23 Repeat Example 2.22 using a silicon diode with $V_K = 0.7$ V.

Solution: For the short-circuit state the network now takes on the appearance of Fig. 2.97, and v_o can be determined by Kirchhoff's voltage law in the output section:

$$+5\text{ V} - 0.7\text{ V} - v_o = 0$$

and

$$v_o = 5\text{ V} - 0.7\text{ V} = 4.3\text{ V}$$

For the input section Kirchhoff's voltage law results in

$$-20\text{ V} + V_C + 0.7\text{ V} - 5\text{ V} = 0$$

and

$$V_C = 25\text{ V} - 0.7\text{ V} = 24.3\text{ V}$$

For the period $t_2 \rightarrow t_3$ the network will now appear as in Fig. 2.98, with the only change being the voltage across the capacitor. Applying Kirchhoff's voltage law yields

$$+10\text{ V} + 24.3\text{ V} - v_o = 0$$

and

$$v_o = 34.3\text{ V}$$

The resulting output appears in Fig. 2.99, verifying the statement that the input and output swings are the same.

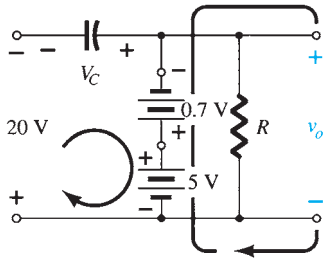


FIG. 2.97
Determining v_o and V_C with the diode in the "on" state.

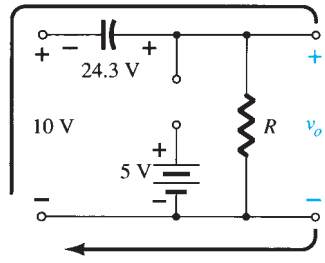


FIG. 2.98
Determining v_o with the diode in the open state.

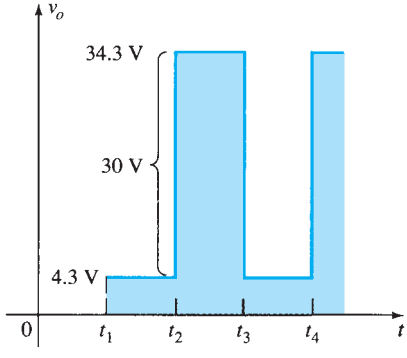


FIG. 2.99
Sketching v_o for the clamper of Fig. 2.93 with a silicon diode.

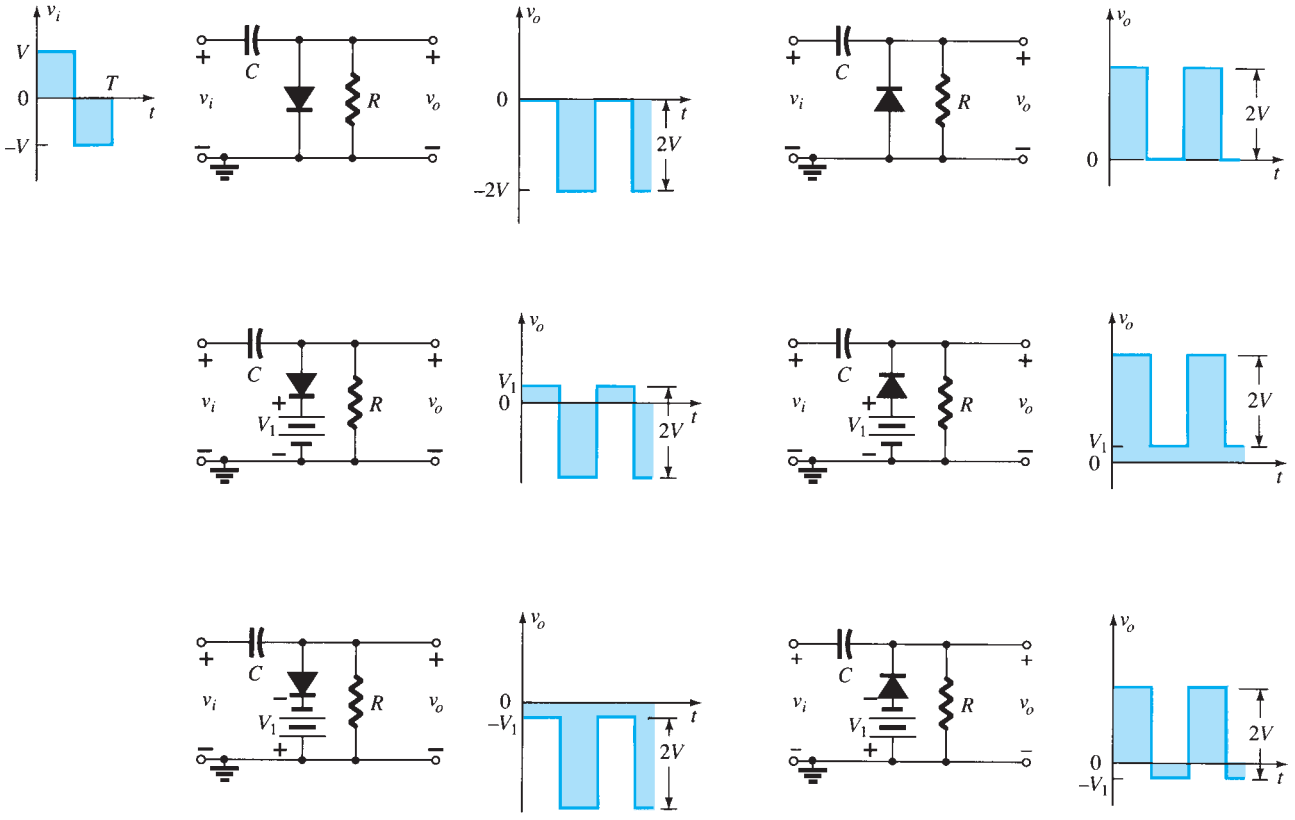


FIG. 2.100
Clamping circuits with ideal diodes ($5\tau = 5RC \gg T/2$).

A number of clamping circuits and their effect on the input signal are shown in Fig. 2.100. Although all the waveforms appearing in Fig. 2.100 are square waves, clamping networks work equally well for sinusoidal signals. In fact, one approach to the analysis of clamping networks with sinusoidal inputs is to replace the sinusoidal signal by a square wave of the same peak values. The resulting output will then form an envelope for the sinusoidal response as shown in Fig. 2.101 for a network appearing in the bottom right of Fig. 2.100.

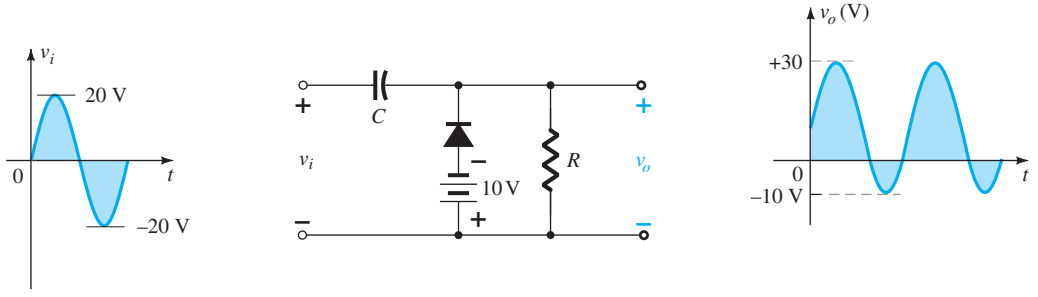


FIG. 2.101
Clamping network with a sinusoidal input.

2.10 NETWORKS WITH A DC AND AC SOURCE

The analysis thus far has been limited to circuits with a single dc, ac, or square wave input. This section will expand that analysis to include both an ac and a dc source in the same configuration. In Fig. 2.102 the simplest of two-source networks has been constructed.