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Section : CSE-1
Course Code : CSE 4503
Course Name : Microprocessor and Assembly Language
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Ans.to Q.no.1(a)

Real Mode: Real-address mode is one of two modes of operation where maximum 1 Mb RAM (20 bit addressing) is possible. All the earlier generations of microprocessor starting from Intel 8085 use this real mode.

The key characteristics are:

i) Allows microprocessor to address first 1Mb RAM only (80286)
ii) Segment and offset is used in this mode.
iii) Any area of the memory can be accessed.
iv) Can perform single-tasking only.
v) Supported by DOS but can not run windows as it needs more RAM.
vi) Memory management and protection are disabled.

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Protected Mode: The addressing mode introduced with 80286, where all address lines (24 bits) are used to access the maximum 16 Mb memory and 1GB virtual memory is protected mode. Key characteristics are:

i) For 80286, 16 Mb memory and 1 GB virtual memory can be accessed.
ii) Allows memory management and protection capabilities.
iii) Can run Windows by providing higher memory.
iv) Designed for multi-tasking.

80286 first implements protected mode.

It has a seperate Memory Management Unit where a 16 bit selector is used with 16 bit Offset. Selector is used to access a descriptor for the desired segment in a table of descriptors in main memory.

A descriptor can describe 64Kb and 80286 has 16K descriptors which results in a (64×16) Mb = 1Gb virtual memory described by the system. The descriptor contains the 24-bit physical address.

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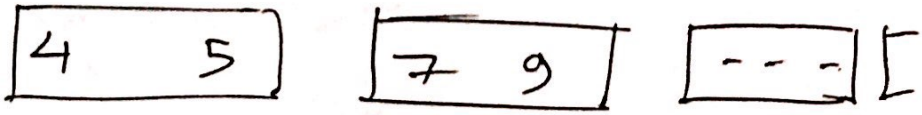
Ans. to Q. no. 1 (b)

A thread is a unit of execution of sequence of instructions that can be managed by scheduler independantly. A process can have multiple threads and each ~~thread~~ thread can be assigned by a different core.

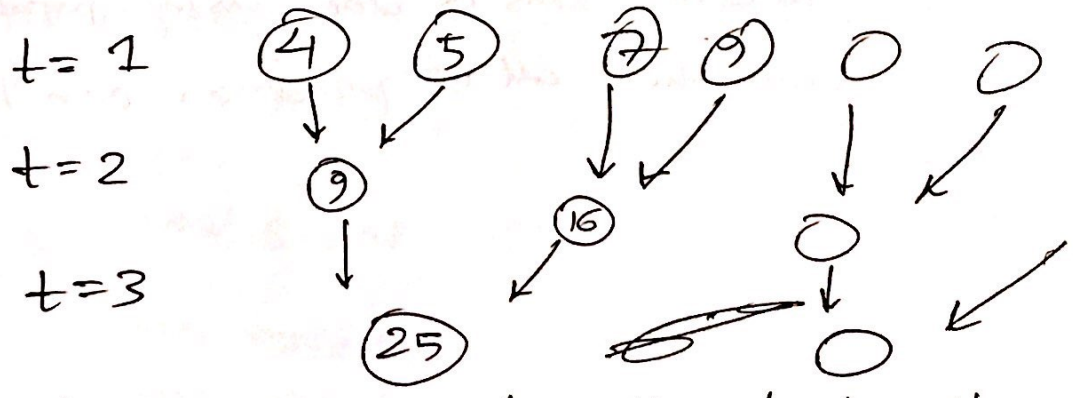
Ex – We sum these numbers



Thread-1 (Done by core-0)

~~Thread~~ Thread-2 (Done by core-1)

Now, ~~the~~ each thread can work on a pair of summation and the time of summation is reduced by half



If we had 100 numbers and 50 threads then it would ~~take~~ be distributed between ~~120~~ those 50 threads and thus parallel processing will reduce time than serial processing.

∴ Thread ensure fasten processing.

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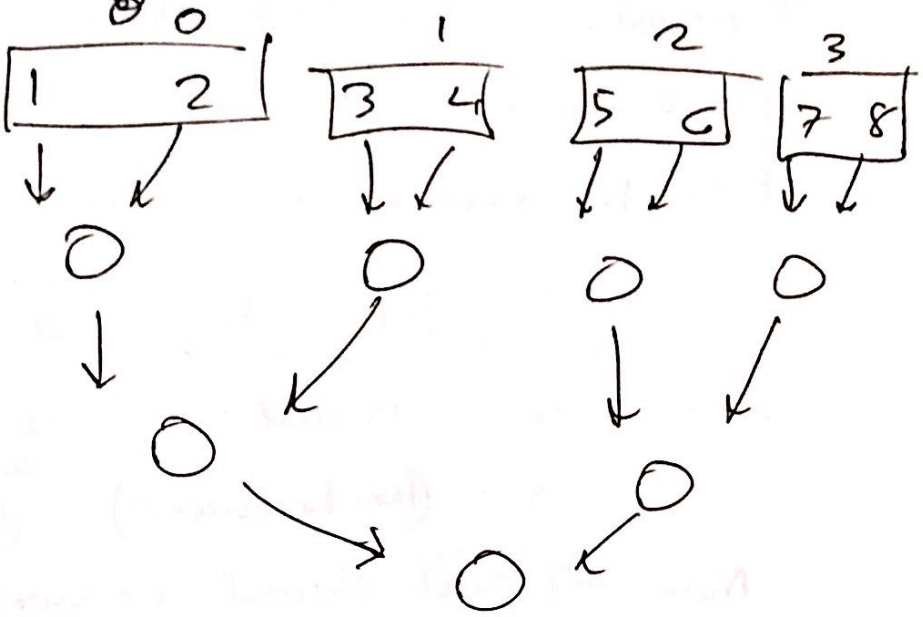
Ans to Q no. 1(c)

By parallel programming, we can multithreading and message passing to compute quickly.

Core: 0 1 2 3



In the example, we see multiple processors can work on the sum if we divide the work among the processes. This is done using parallel programming and thus all the processors can be used parallely.

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Ans. to Q.no. 2(a)

There are 27 reserved locations for 8086 vector table.

They are INT 5 to INT 31

INT 5 = (5X4) h = 14 (starts)

INT 31 = (31 X 4) h = 7C (starts)

Ans: Memory location 00014H to 0007FH are reserved.

(i) INT 10 B = INT 2H

~~= (10×4) B~~ = (2×4) H

= 8H

Memory location 00008 H

IP: 00008H
00009H

CS: 0000AH
0000BH.

(ii) INT 3 = INT 3H

= (3×4) H

= CH

Memory location 0000CH

IP: 0000CH
~~0000DH~~ 0000DH

CS: 0000EH
0000FH

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Ans. to Q. no. 2(b)

The necessary instructions are:

```
MOV ds, @data
MOV SI, Offset A
MOV DI, offset B
MOV BX, offset C
MOV BP, offset D
```

The DS register value is 7000H

SI	"	"	0000H
DI	"	"	0005H
BX	"	"	0008H
BP	"	"	000AH

Ans. to Q. no. 2(c)

```
.CODE
    MAIN PROC
        MOV AH,1
        INT 21H
        MOV BL, AL

        MOV CL,1
        SUB BL,CL

        MOV AH,2
        MOV DL,BL
        INT 21H
    MAIN END
    END MAIN
    RET
```

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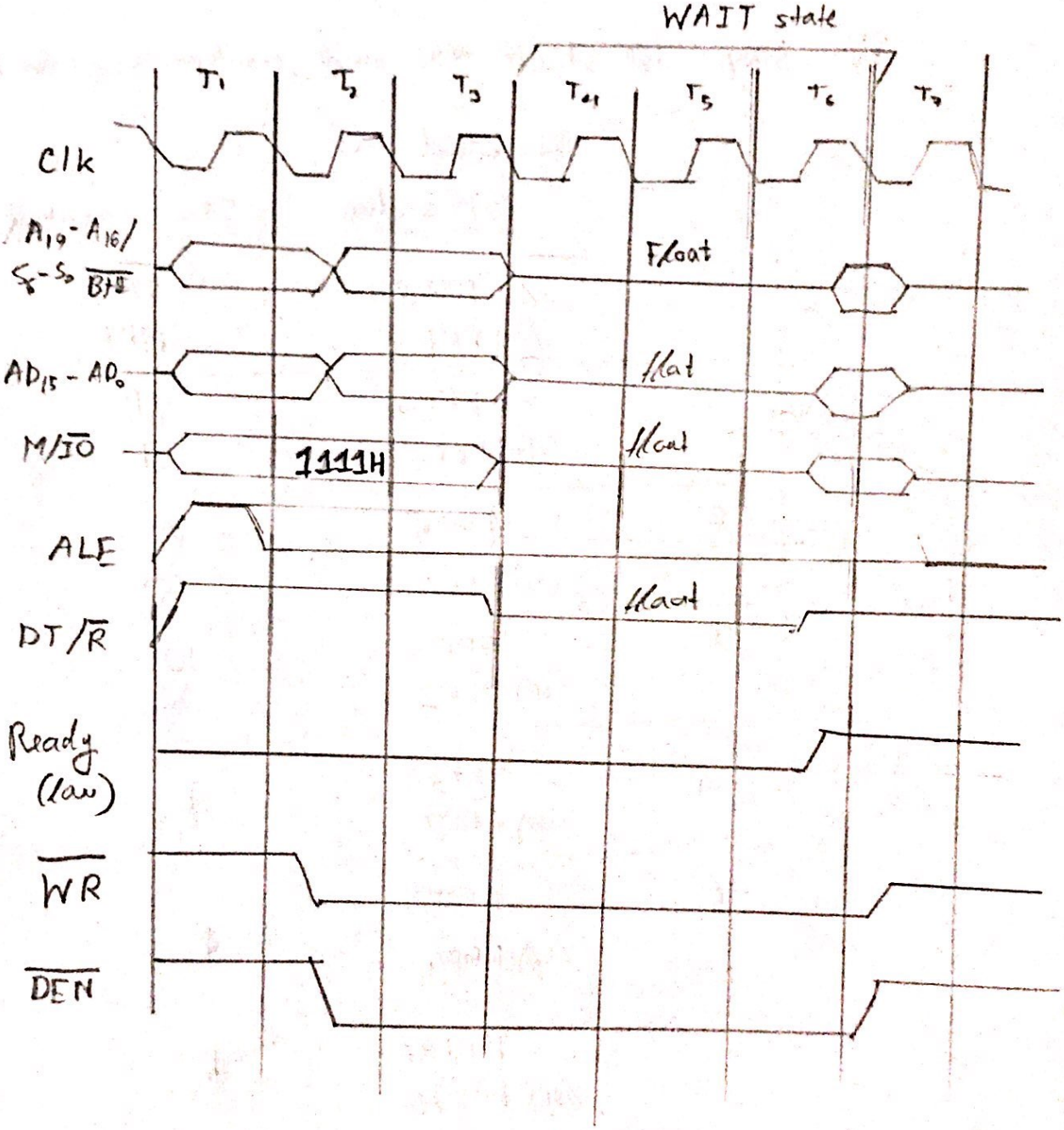
Ans. to Q. no. 3(a)



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Ans. to Qns. 3(b)

The steps of stack value and content is given below:

~~Stack Val~~

		SP value	Stack content
increase	0	FFF89 (SP) FFF 8	~~01~~ $ ~~02~~ $
	1	FFF7 (SP) FFF6	10 01
	2	FFF5 (SP) FFF4	70 00
	3	FFF3 (SP) FFF2	10 00
decrease	4	FFF3 (SP) FFF2	$
	5	~~FFF5~~ (SP) FFF4	$
	6	FFF87 (SP) FFF26	$
	7	FFF89 (SP) FFF8	$

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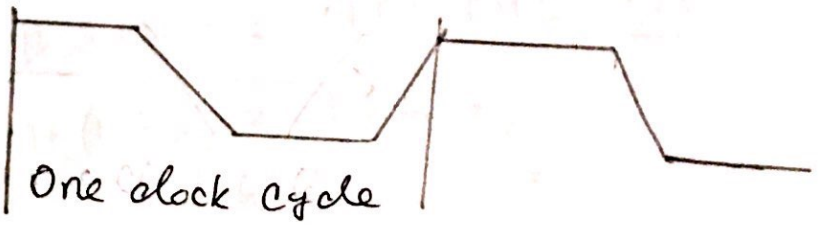
Ans. to Q no. 3(c)

i) **Clock Cycle:-** Time between high and low state of CPU clock is a clock cycle. A single pulse of the oscillator for clock cycle generation is one clock cycle.

Ex- A 5 MHz clock oscillates at 5×10^6 time a second.

So, clock cycle is 200 ns.

In 200 ns it goes from ON state to the next cycle's ON state.



ii) **Bus cycle:-** Most basic microprocessor operation for reading/writing from/to memory. Composed of at least 4 clock cycles.

Ex - Read operation from memory.

iii) **Instruction cycle:-** Consists of multiple bus cycles and is the total time by up to complete an instruction.

Ex - A MOV operation has 1 instruction cycle.

iv) **Machine cycle:** Same as bus cycle.

v) T duration for 12 MHz is

$$T = \frac{1}{12 \times 10^6} = 83.33 \text{ ns.} \quad \text{(Ans.)}$$