CSE 4305
Computer Organization and Architecture

Basic Concepts

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Organization and Architecture

- **Distinction** between "**Computer Architecture**" and "**Computer Organization**"

Computer Architecture

- Refers those attributes of a system visible to a programmer (programmer is aware of its presence)
- Has direct impact on the **logical execution of a program**
- Often used as **Instruction Set Architecture (ISA)** – instruction format, instruction opcodes, registers, instruction and data memory; effect of execution instruction on the registers and memory; algorithm for controlling instruction execution.
- **Logical Components** – Instruction set, addressing modes, data types, cache optimization

Computer Organization

- Refers to **operational units and their interconnections** – according to the architectural specifications (**implement of architecture**)
- **Includes physical components** – control signals, interface, memory technology, circuit design, adders, peripherals
- **Hardware details** which is transparent to the programmer - (programmer is not aware of its presence)

Example

To multiply two integer numbers

Architectural Issue – whether a computer use a multiply instruction

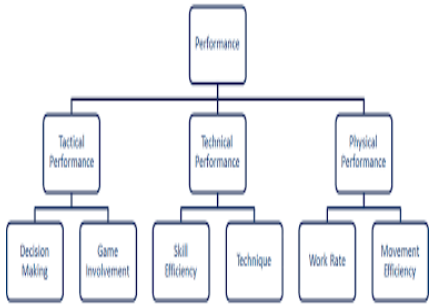
Organizational Issue – whether that instruction will be implemented by a multiply unit or repeated use of the add unit

And More…

- There is a family of computer models having **same architecture** but **different organizations**. Because it will protect the customer's software investment. *(Old soft wares [e.g. from Windows XP] are still runnable in Windows 10!!!)*
- **Changes in technology** not only influence organization but also result in the introduction of more powerful and more complex architecture
- But they have less requirement for **generation to generation compatibility** for smaller machines

To understand a complex system

- Bottom – up approach
- Top – down approach (Hierarchical approach)
- A hierarchical system is a set of **interrelated subsystems**, each of the **latter, in turn, hierarchical in structure** until we reach some lowest level of elementary subsystem. At each level, the designer is concerned with **structure** and **function**.
  - **Structure:** The way in which the **components are interrelated**.
  - **Function:** The **operation** of each individual component as part of the structure.



Root: A computer

Functions:

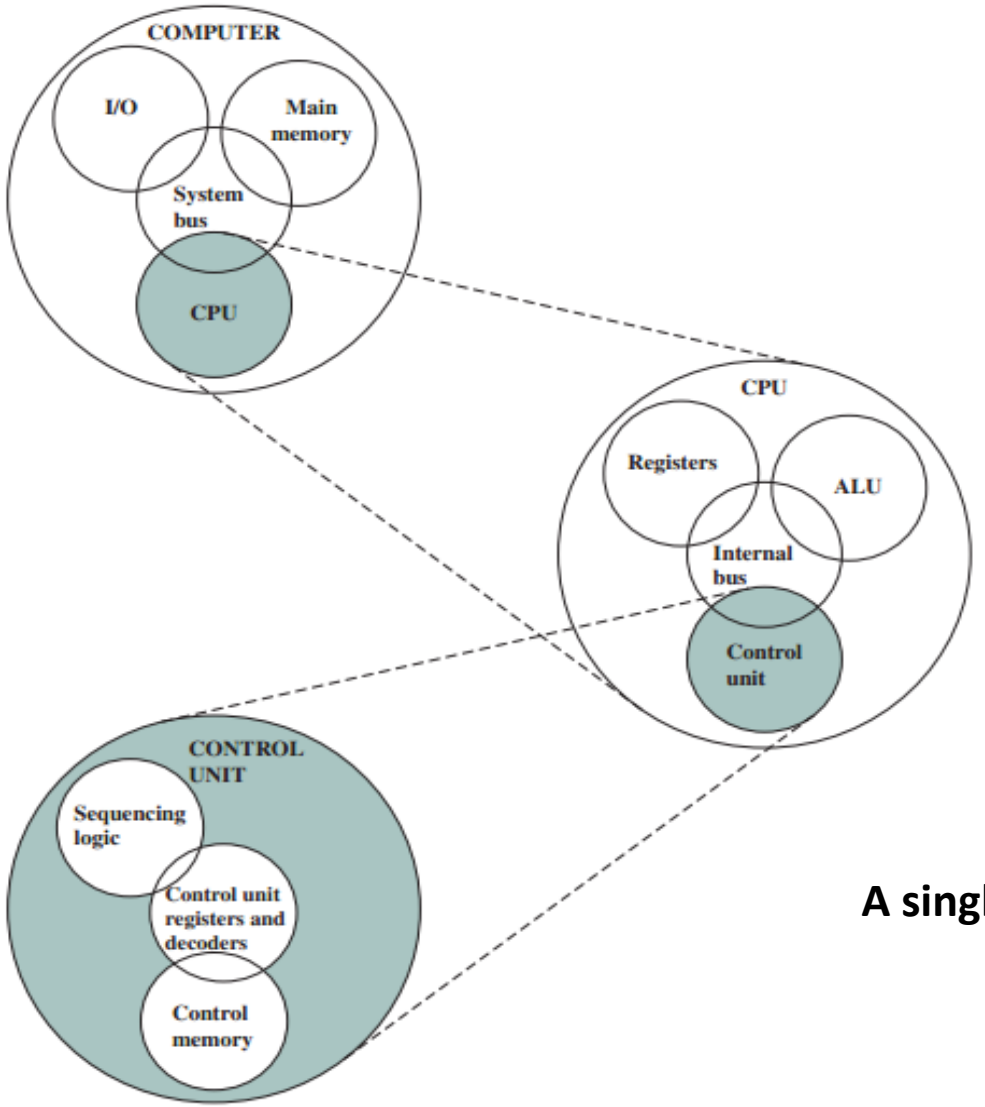
- **Data processing**: **Take** a wide variety of data in forms and **process** as requirements
- **Data Storage**: At least store temporary data (being worked on) at **short term data storage**. It equally requires **long term data storage**
- **Data movement:** In a computing environments, there are various devices as **source or destination of data**. (**input output process** will be there with peripherals or memory) – data communication
- **Control: Manage** computer resources and **arrange** the performance of the functional parts.

Root: A computer…

Structure: (Simple Single Processor Computer)

- **Central Processing Unit**: Controls the operation and performs its data processing- known as CPU or Processor
- **Main Memory**: Stores data
- **I/O**: Moves data between the computer and ***external world***
- **System Interconnection**: Provides communication among CPU, memory, I/O through **system bus.** *Keep components attached.*

Root: A computer…



A single processor computer

Root: A computer…

Major components of CPU:

- **Control Unit:** Controls the operation of the CPU
- **Arithmetic And Logic Unit (ALU):** Perform data process
- **Registers:** Internal storage
- **CPU Interconnection:** Provides communication among the components

Some Terminologies having same essence

Multicore Computer Structure:

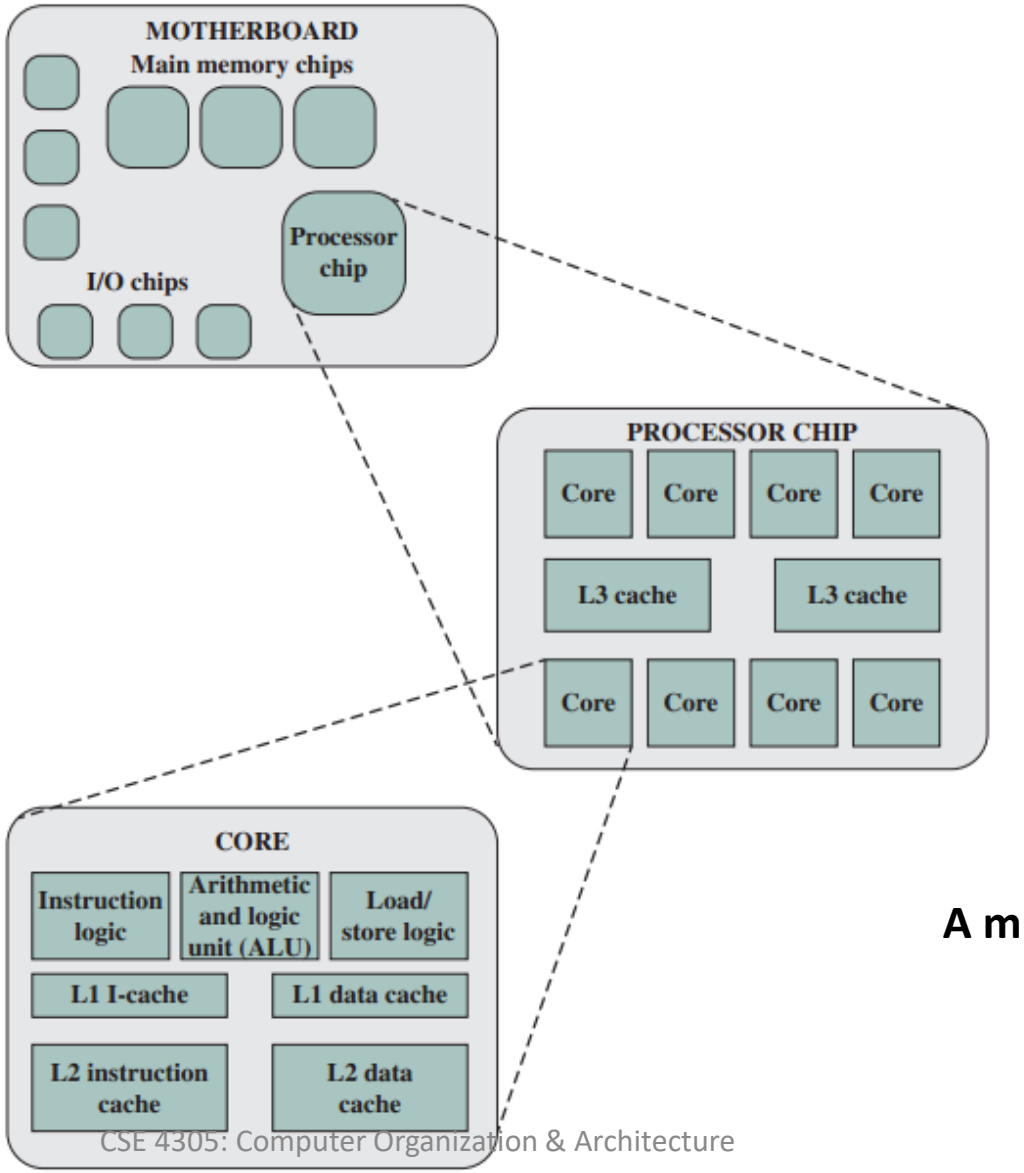
- **Central Processing Unit: Fetch and execute** instructions **containing ALU, control unit, registers** – known as processor in single processor computer
- **Core**: **An single processing unit** on processor chip. Functionally equivalent to a CPU on a single CPU System. *Special processing units* also referred as core – vector processor
- **Processor**: **A physical piece of silicon** having one or more cores which interprets and execute instructions.

Root: A computer…

Structure: (Multicore Computer)

- **Multicore Computer**: *All processors* resides on *a single chip*; each *processing unit (named as **core**)* contains control unit, ALU, registers and cache(optional)
- **Cache Memory**: **Memory layer** between processor and main memory – smaller and faster than main memory. **Place data** from main memory to cache to speed up the processing. It has **multiple levels**. **Near to the core, smaller and faster than others. (L1, L2, L3…)**
- **Motherboard**: The **main PCB** (printed circuit board) where the computer system is housed.
- **Chips**: A **piece of semiconductor material** upon which electronic circuit and logic gates are fabricated – also known integrated circuit.

Root: A computer…



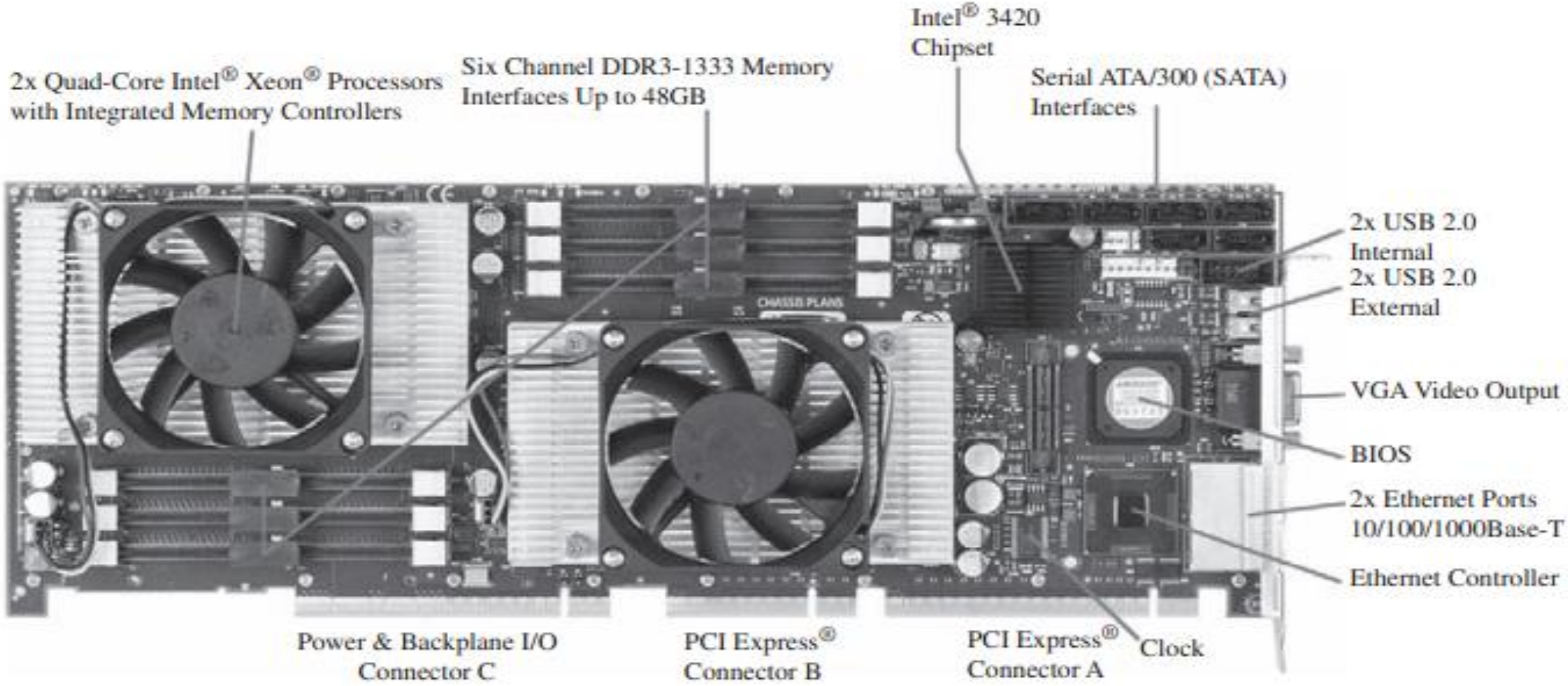
A multicore computer

Elements of a CORE

- **Instruction Logic**: **Fetch** instructions, **decode** them to *determine the operation and memory location* of the operands
- **Arithmetic Logic Unit (ALU)**: **Performs operation** specified by an *instruction*
- **Load/Store Logic**: **Transfer data** *to and from main memory via cache*
- **L1 Cache**: instruction cache and data cache to transfer instructions, operands and results.
- **L2 Cache**: instruction cache and data cache to transfer instructions, operands and results.

Real Life Computer - 1

Intel Quad Core Xenon Processor:



Real Life Computer – 1…

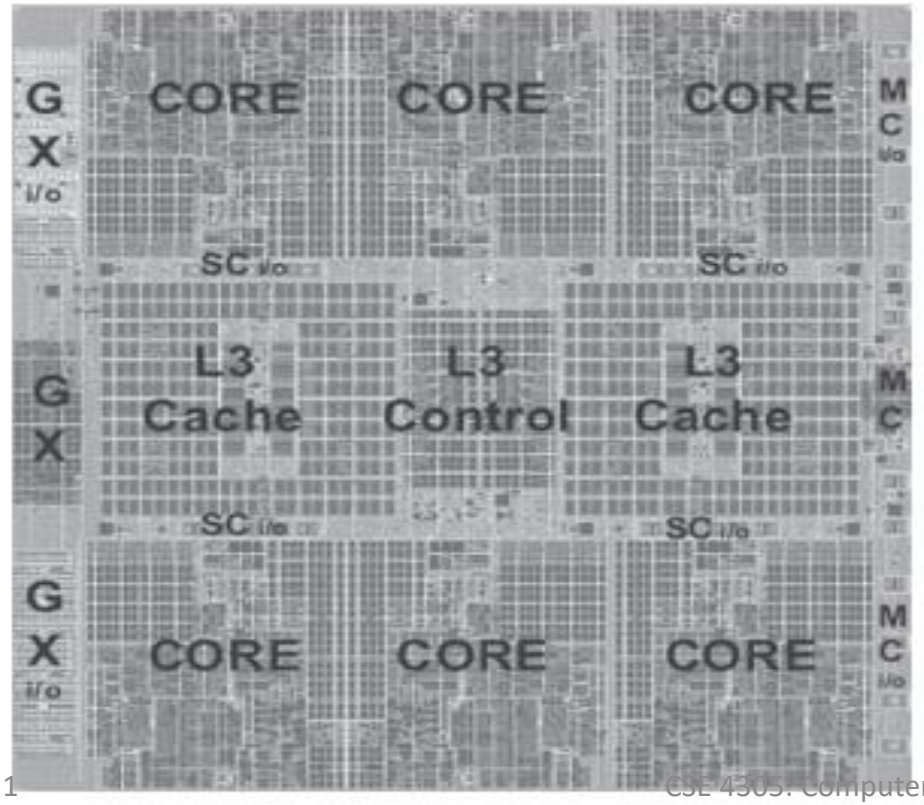
It contains:

- **PCI Express slots** – for additional displays and peripherals
- **Ethernet Controller and Ethernet Port** – for network connections
- **USB sockets** – for peripheral devices
- **Serial ATA sockets** – to connect disk memory/ secondary storage
- **Interface of DDR** – for main memory chips
- **Intel 3420 chipset** – I/O controller for *Direct Memory Access*
- **BIOS** – basic I/O system, non volatile firmware employed to initialize hardware during booting process.
- **Clock** – for required clock cycle to execute each instruction

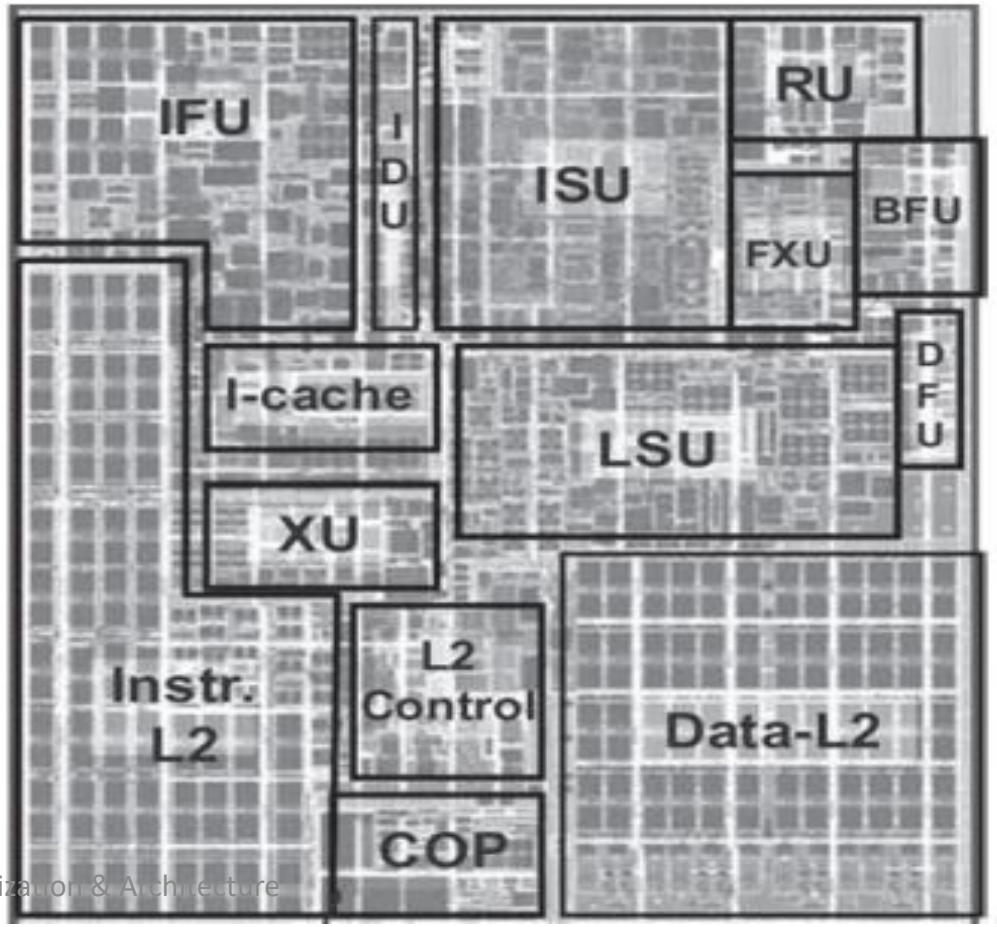
Real Life Computer - 2

IBM zEnterprise EC12 mainframe Computer

Processor Unit



Core Layout



Real Life Computer – 2…

It contains:

- **L3 Cache control**: to control traffic
- **Storage Control (SC):** to control storage in cache
- **Memory Controller (MC)**: to control access memory external to the chip
- **GX I/O**: to control the interface to access I/O

Real Life Computer – 2…

A core contains:

- **Instruction Sequence Unit (ISU)**
- **Instruction Fetch Unit (IFU)**
- **Instruction Decode Unit (IDU)**
- **Load Store Unit (LSU) – contains L1 cache**
- **Translation Unit (XU) – translate logical address to physical Address**
- **Fixed Point Unit (FXU)**
- **Binary Floating-point Unit (BFU)**
- **Decimal Floating-point Unit (DFU)**
- **Recovery Unit (RU) – keeps a copy of the complete state of the system**
- **Dedicated Co-processor (COP)**
- **I-cache**
- **L2 control**
- **Data L2**
- **Instr L2**

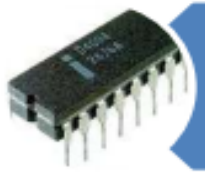
Fixed Point arithmetic - integers
Floating Point arithmetic - rationale

A Brief History Of Computers : Overview

First Generation (The period of first generation: 1946-1959. Vacuum tube based.)

Second Generation (The period of second generation: 1959-1964. Transistor based.)

Third Generation (The period of third generation: 1964-1971. Integrated Circuit based.)



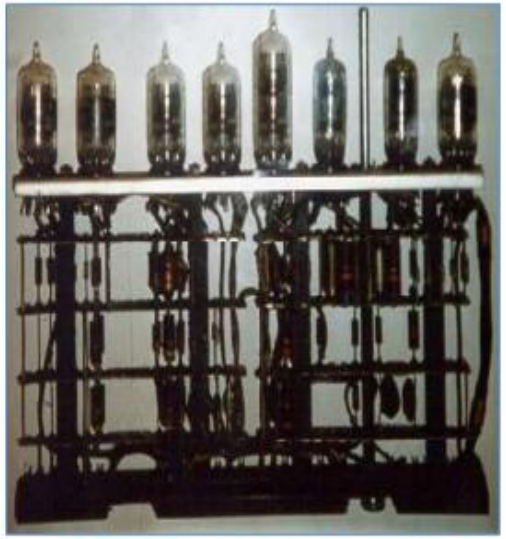
Fourth Generation (The period of fourth generation: 1971-1980. VLSI microprocessor based.)

Fifth Generation (The period of fifth generation: 1980-onwards. ULSI microprocessor based.)

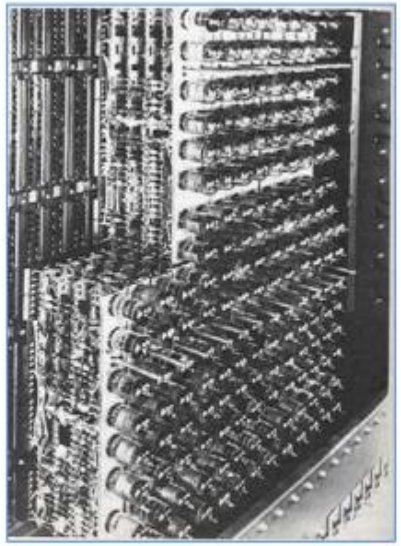
1st Generation: Vacuum Tubes

Vacuum tube for circuitry

Vacuum tube (electronic tube)



This circuit board block is one of hundreds of blocks that held the 4000 vacuum tubes for IBM's Model 701



A part of computer using vacuum tube

Magnetic drum for data store

Magnetic drum

1st Generation…

Some computers of this generation :

- ENIAC
- EDVAC
- UNIVAC
- IBM-701
- IBM-650

ENIAC

1st Generation: Main Features

- **Vacuum tubes** both for logic and memory elements
- Known as IAS Computer following *stored program concept* by John von Newmann at Princeton Institute for Advanced Studies
- Consisting of:
  - **Main memory**
  - **ALU**
  - **Control Unit**
  - **I/O**

1st Generation: IAS Structure

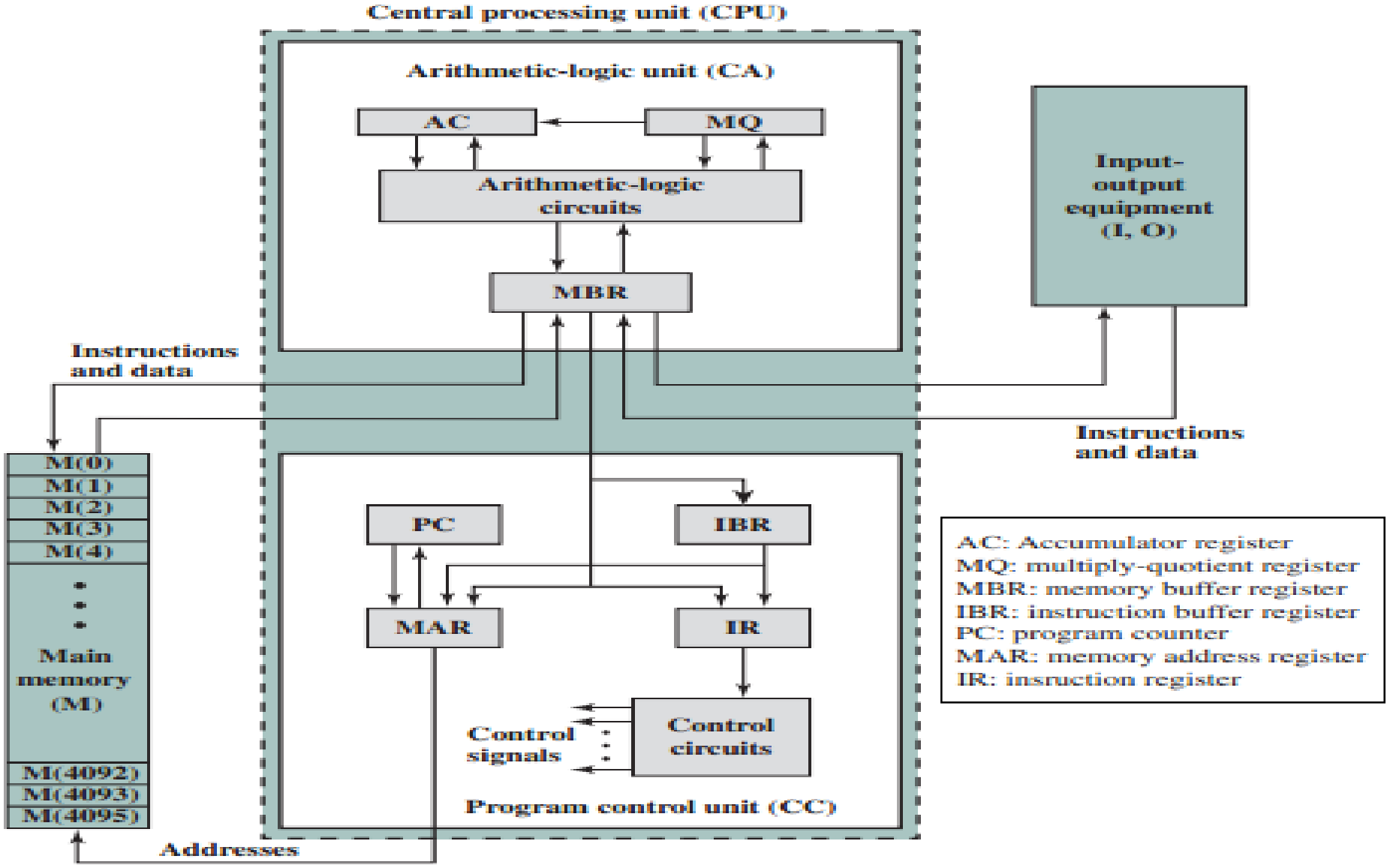
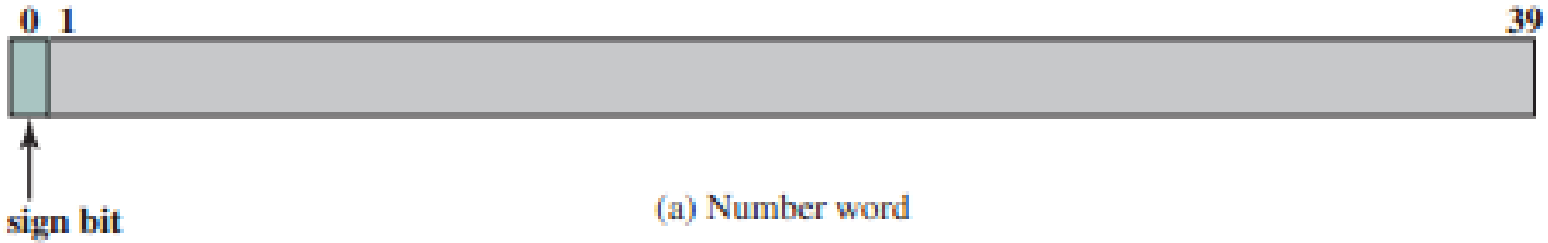


Figure 1.6 IAS Structure

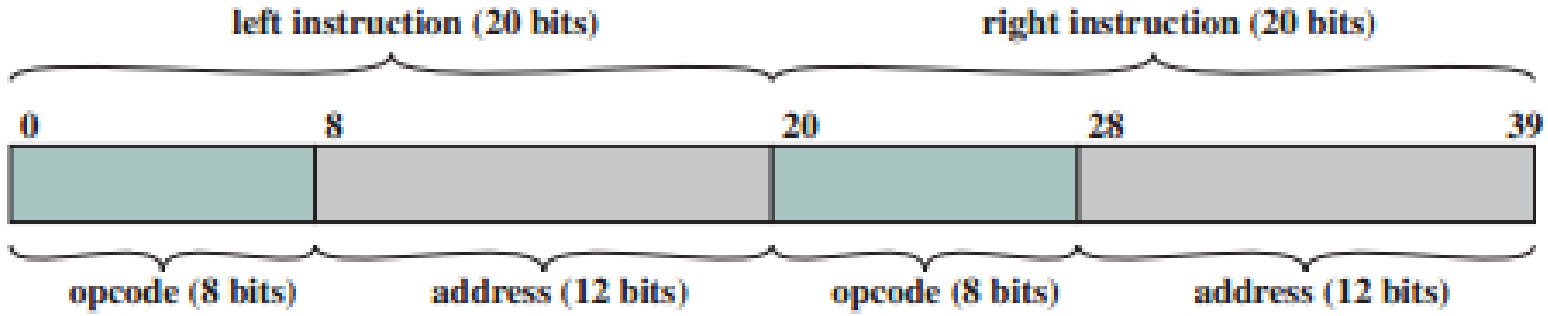
1st Generation: IAS Structure…

- In its memory, it has **4096 storage locations-** called **words** containing **40 bits** each – both for data and instructions
- Data in binary form – a sign bit and 39-bit value
- Instructions in binary coded form – also contain two 20-bit instructions having 8-bit opcode (operation) and 12-bit address (for words in memory)
- **Central Control (CC)** and **Central Arithmetic (CA)** both have different storages – **registers** as MBR, MAR, IR, IBR, PC, AC, MQ
- IAS is operated based on **instruction cycle** – **2 sub cycles**: **fetch** and **execution**
- **Address** specifies which of the *4096 memory locations* is used to execute instruction

1st Generation: IAS Memory Format

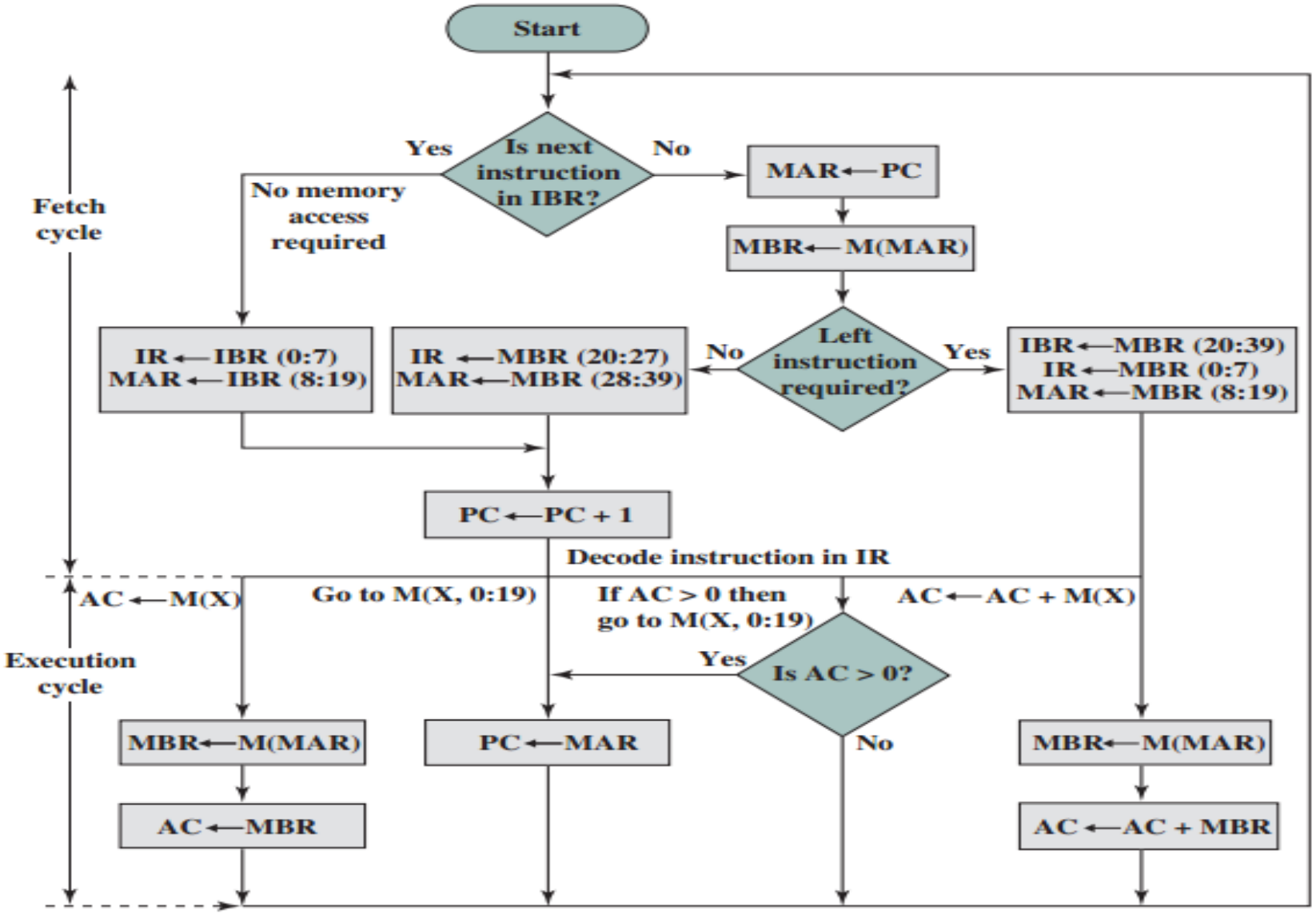


(a) Number word



(b) Instruction word

1st Generation: IAS Instruction Cycle



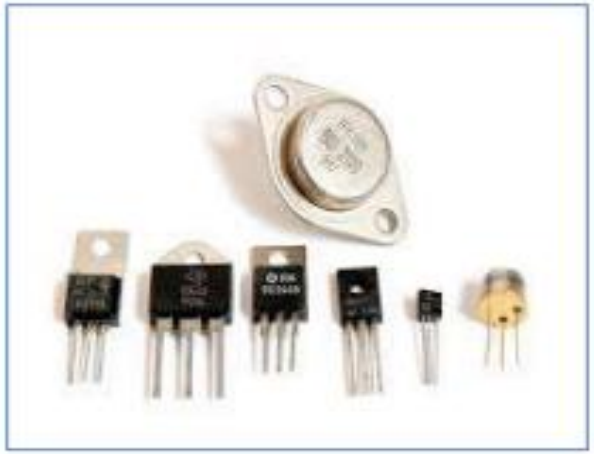
1st Generation: Instruction Sets

Instruction Type	Opcode	Symbolic Representation	Description
Data transfer	00001010	LOAD MQ	Transfer contents of register MQ to the accumulator AC
	00001001	LOAD MQ,M(X)	Transfer contents of memory location X to MQ
	00100001	STOR M(X)	Transfer contents of accumulator to memory location X
	00000001	LOAD M(X)	Transfer M(X) to the accumulator
	00000010	LOAD –M(X)	Transfer –M(X) to the accumulator
	00000011	LOAD |M(X)|	Transfer absolute value of M(X) to the accumulator
	00000100	LOAD –|M(X)|	Transfer –|M(X)| to the accumulator
Unconditional branch	00001101	JUMP M(X,0:19)	Take next instruction from left half of M(X)
	00001110	JUMP M(X,20:39)	Take next instruction from right half of M(X)
Conditional branch	00001111	JUMP + M(X,0:19)	If number in the accumulator is nonnegative, take next instruction from left half of M(X)
	00010000	JUMP + M(X,20:39)	If number in the accumulator is nonnegative, take next instruction from right half of M(X)
Arithmetic	00000101	ADD M(X)	Add M(X) to AC; put the result in AC
	00000111	ADD |M(X)|	Add |M(X)| to AC; put the result in AC
	00000110	SUB M(X)	Subtract M(X) from AC; put the result in AC
	00001000	SUB |M(X)|	Subtract |M(X)| from AC; put the remainder in AC
	00001011	MUL M(X)	Multiply M(X) by MQ; put most significant bits of result in AC, put least significant bits in MQ
	00001100	DIV M(X)	Divide AC by M(X); put the quotient in MQ and the remainder in AC
	00010100	LSH	Multiply accumulator by 2; that is, shift left one bit position
	00010101	RSH	Divide accumulator by 2; that is, shift right one position
Address modify	00010010	STOR M(X,8:19)	Replace left address field at M(X) by 12 rightmost bits of AC
	00010011	STOR M(X,28:39)	Replace right address field at M(X) by 12 rightmost bits

2nd Generation: Transistors

A replica of the first working transistor.

Philco surface-barrier transistor developed and produced in 1953



Assorted discrete transistors

Instead of vacuum tubes, here transistors were used.

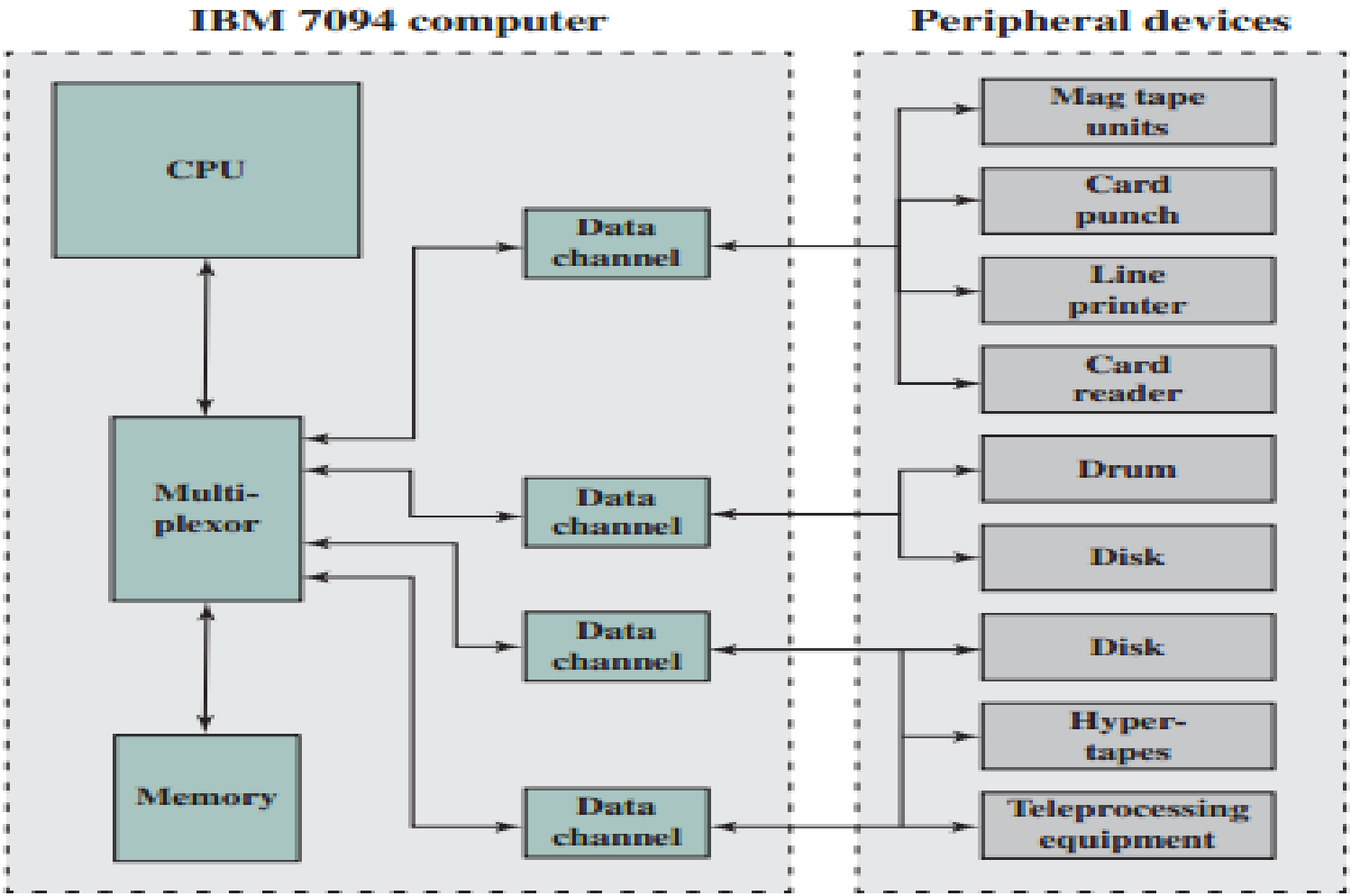
2nd Generation: Main Features

- **Replacement of vacuum tubes by transistors** – smaller, cheaper, less heat generator – all components were then made of **silicon**, *so no wires, metal plates, glass capsule, vacuum*
- More **complex arithmetic and logic units and control units**
- Use **high level programming languages**
- Use of **system software** – OS

System Software – build platform other software
Application Software – allow user to do things

- So many improvements – like **Instruction Buffer Register** – which store adjacent instructions from memory to reduce memory access by about 0.5 times
- **Data channels- refers to** I/O module with its own processor and instruction sets – now CPU is not busy with detail I/O instructions (see in the picture)
- **Multiplexor** – **refers to** central termination point for data channels, CPU, Memory – **schedules access of the memory**

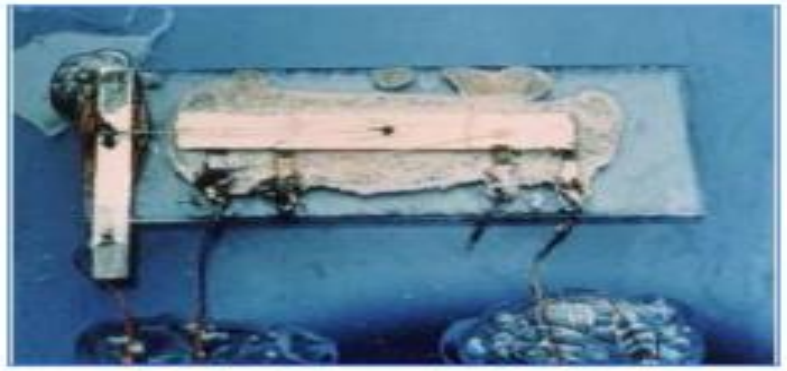
2nd Generation: IBM 7094



3rd Generation: Integrated Circuits

Integrated Circuit based :

A single IC has many transistors, resistors and capacitors along with the associated circuitry. The IC was invented by **Jack Kilby**. This development made computers smaller in size, reliable and efficient.

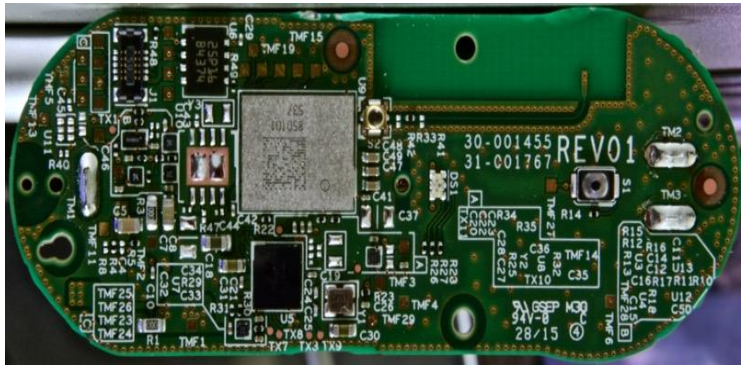


First IC

Hitachi IC

R288-SOUNDGIN-IC

3rd Generation: Why???

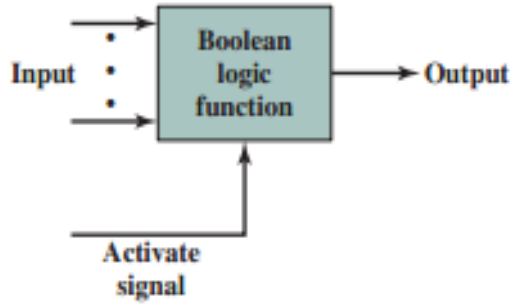


- **Electronic equipment** was composed of **discrete components** – transistors, resistors, capacitors and so on and soldiered or wired onto the circuit board which then installed in computers
- The **entire manufacturing process** from transistors to circuit board was very expensive and cumbersome
- Problems increased when the number of transistors grew to the hundreds of thousands !!!

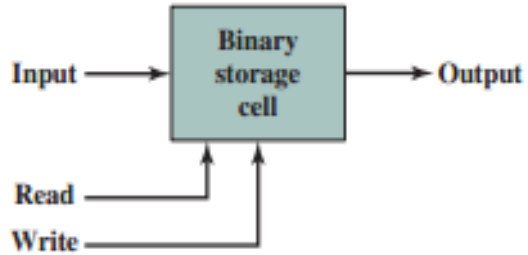
3rd Generation: Digital Electronics (???)

Microelectronics:

- Small electronics
- Gates and memory cell – **fundamental components – made of transistors and capacitors**
- **Gates** – *implement* logical function (AND, OR, …)- control data flow
- **Memory cell** – store 1 bit – in 2 stable states (0,1)
- Interconnection of **the large numbers of these devices** makes a computer
  - **Data storage** – by memory cells
  - **Data Processing** – by gates
  - **Data movement** – by gates through cells
  - **Control** – by gates through cells



(a) Gate

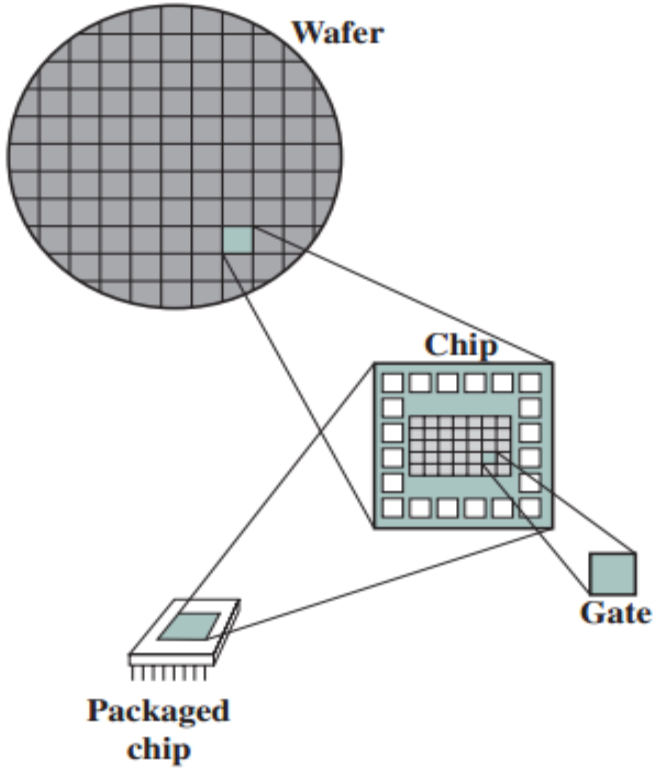


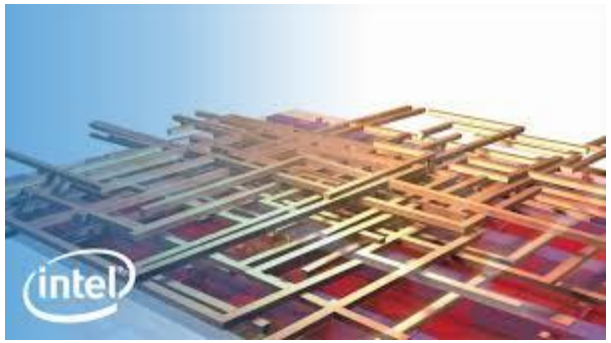
(b) Memory cell

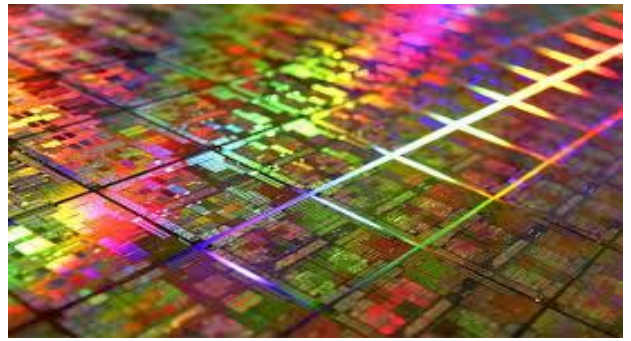
3rd Generation: Integrated Circuits (???)

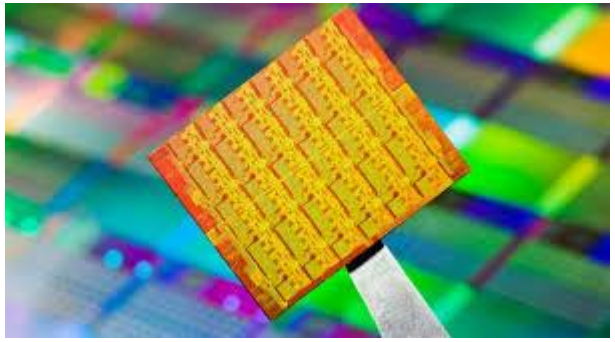
- IC exploits the fact that it **fabricates** all the fundamental components **from silicon (semiconductor)**
- Like fabricating an entire circuit in a tiny piece of silicon rather than assembling discrete components – producing many transistors on a single wafer of silicon – connected through **metallization** to form circuit
- A thin **silicon wafer** divided into **a matrix of small areas**, each a few millimeters square – having **identical circuit pattern** – named as **chips**, having many gates and/or memory cells I/O attachments points
- Chips are **packaged** for protection and **interconnected** on a PCB for complex circuit – **provides pins** for attachment to devices.

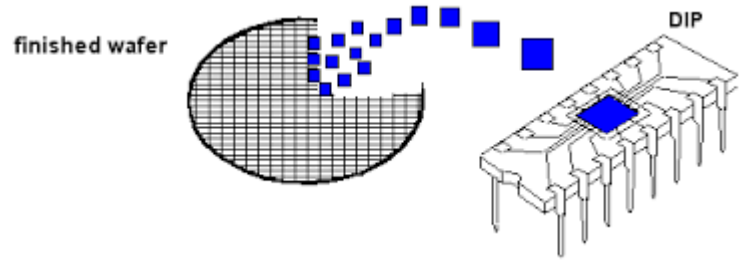
Relationship among Wafer, Chip & Gate











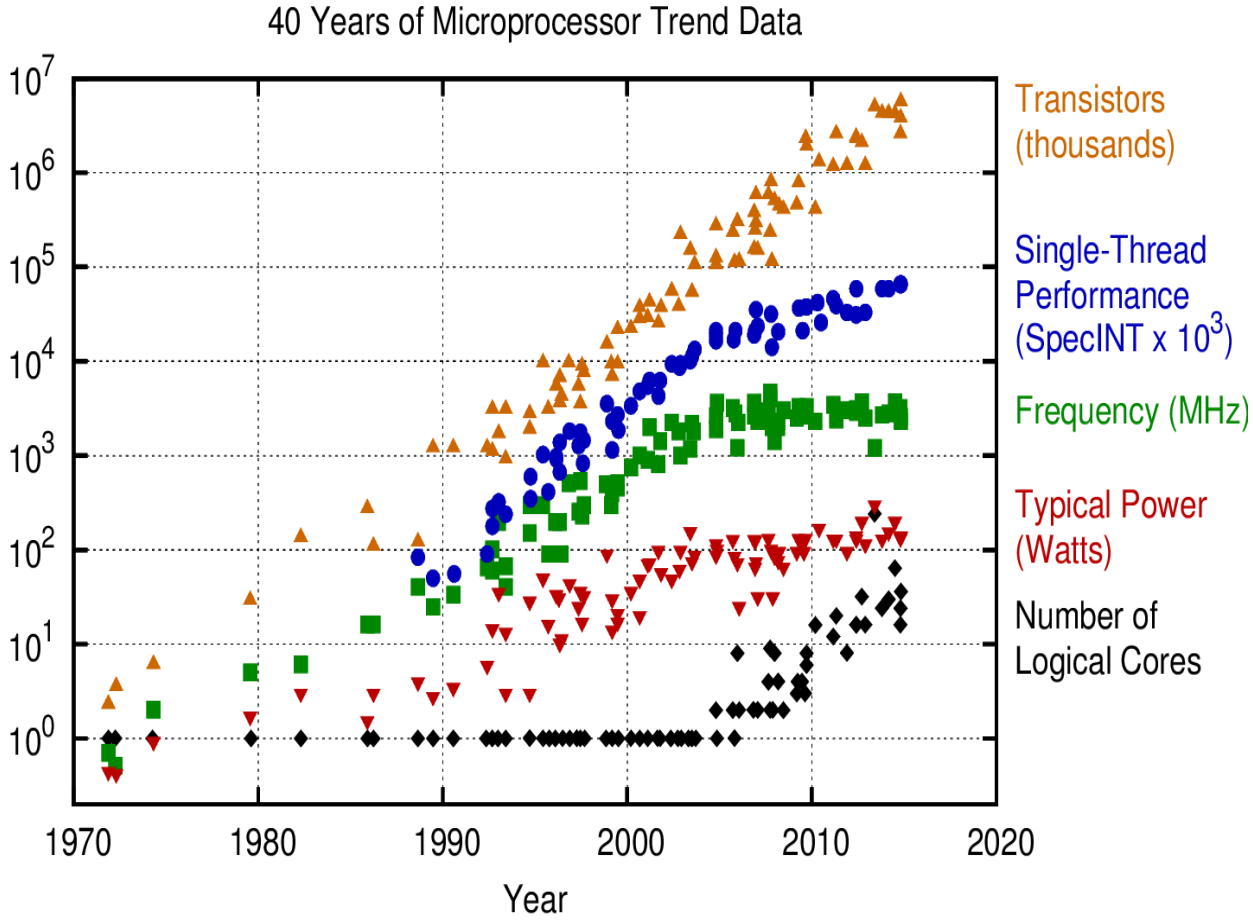
https://www.youtube.com/watch?v=aWVywhzuHnQ

3rd Generation: Integrated Circuits…

- Classification of ICs based on their size:
  - **SSI**: Small scale integration. 3 – 30 gates per chip.
  - **MSI**: Medium scale integration. 30 – 300 gates per chip.
  - **LSI**: Large scale integration. 300 – 3,000 gates per chip.
  - **VLSI**: Very large scale integration. More than 3,000 gates per chip.
  - **ULSI**: Ultra large scale integration. *On the top of others*
- The growth in Density follows the famous **Moore's Law**.
- **Observation of Moore's Law:** The number of transistors on a chip **doubles** every year while the costs are **halved**.
- *But the pace is now slowed to a doubling every 18 months.*

3rd Generation: Consequences of Moore's Law

- The **cost** of computer Logic and memory circuit has fallen at a dramatic rate
- Logic and gates are **placed closer in circuit** – electrical path is shortened – increase operating speed
- Computer becomes **smaller in size**
- **Reduction of power** requirement
- With more circuitry on each chip, **fewer inter chip connections** (more reliable than solder connections)



3rd Generation: IBM SYSTEM/ 360

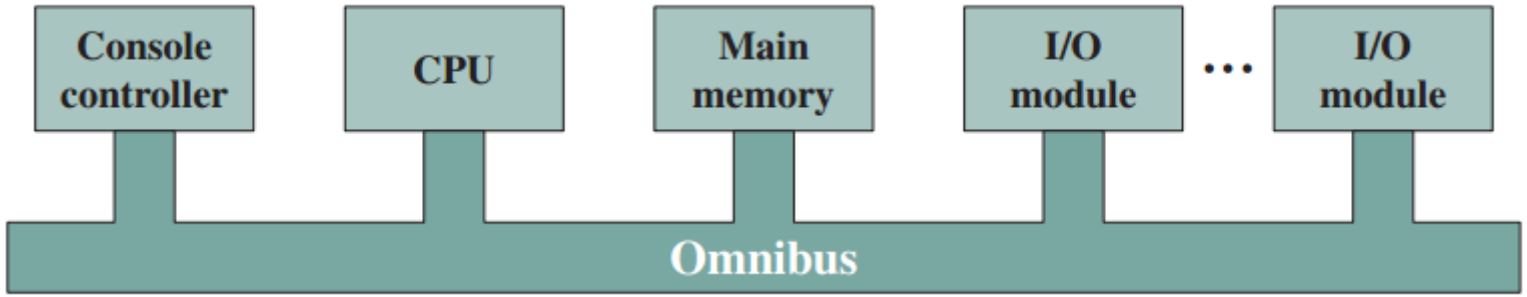
- **Bad News:** the 360 product line was **incompatible** with older IBM machines – to break some constraints and produce system with ICs
- Paid off both financially and technically
- First planned family of computers – members have **differences** only in execution time
- Many of its feature have become **standard** on other large computers

IBM SYSTEM/ 360 family: Characteristics

- **Identical Instruction Set:** Supported by all members of the family
- **Similar Operating System:** Same Basic OS
- **Increasing Speed**: Rate of instruction execution
- **Increasing number of I/O Ports**
- **Increasing Memory Size**
- **Increasing COST (!!!)** : for complexity it supports

3rd Generation: DEC PDP-8

- Built by Digital Equipment Corporation
- **Small in size** that it could be placed on top of a lab bench
- **Cheaper enough** than concurrent IBM System/ 360
- Become universal for its first introduction of **BUS structure.**



Later Generations

With the rapid pace of technology, the **high rate of introduction** of new products, and the importance of software and communications as well as hardware, the classification by generation becomes less clear and less meaningful.

Later Generation: Developments

Semiconductor Memory:

- **IC technology** also used in memory construction
- Earlier it was made of tiny **rings of ferromagnetic materials** – magnetic core – faster but expensive and bulky and use destructive readout (erase stored data)
- **Capacious Semiconductor Memory** – size of a single core – store 256 bits – nondestructive – access time $70X10^{-9}$ Second – but higher cost

Later Generation: Developments…

Microprocessors:

- **Density** of elements of Processor chips increased – fewer chips to construct a processor
- Breakthrough in 1971 – Intel 4004 – first chip containing all components of CPU in a single chip – born of microprocessor – can add and multiply – 4 bit microprocessor
- Marked as the beginning of the evolution of microprocessor
- In 1972, Intel 8008 – first **8 bit single chip** microprocessor
- In 1974, Intel 8080 – first **general purpose** microprocessor
- In 1981, HP and BELL lab – **32 bit single chip** microprocessor

RISC and CISC Architecture Processor

RISC Architecture Processor

CISC Architecture Processor

RISC Architecture Processor: Main Features

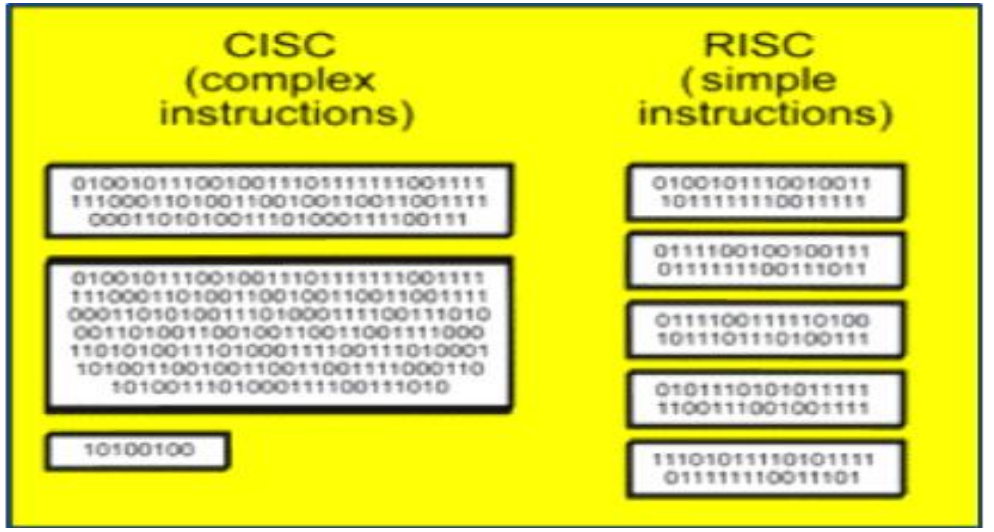
- Represents the **R**educed **I**nstruction **S**et **C**omputer
- Utilizes small and highly **optimized instruction sets (smaller)** – needs **single clock cycle** to be executed – also named as **LOAD/STORE architecture**
- As simplified instructions are used – program code is longer – so **software should be optimized**
- Simple **Addressing modes**, smaller **opcode**, cheaper in **price**, **faster** in operation, **few parameters** in code, **power efficient**
- But **more registers** to reduce memory access
- Simple **compiler** and **hardware** design
- **Pipelining** is easier to be implemented for simple instruction
- **Used** in mobile phones, smart devices, ARM Processor (Section 1.6) – (Advanced RISC Machine)

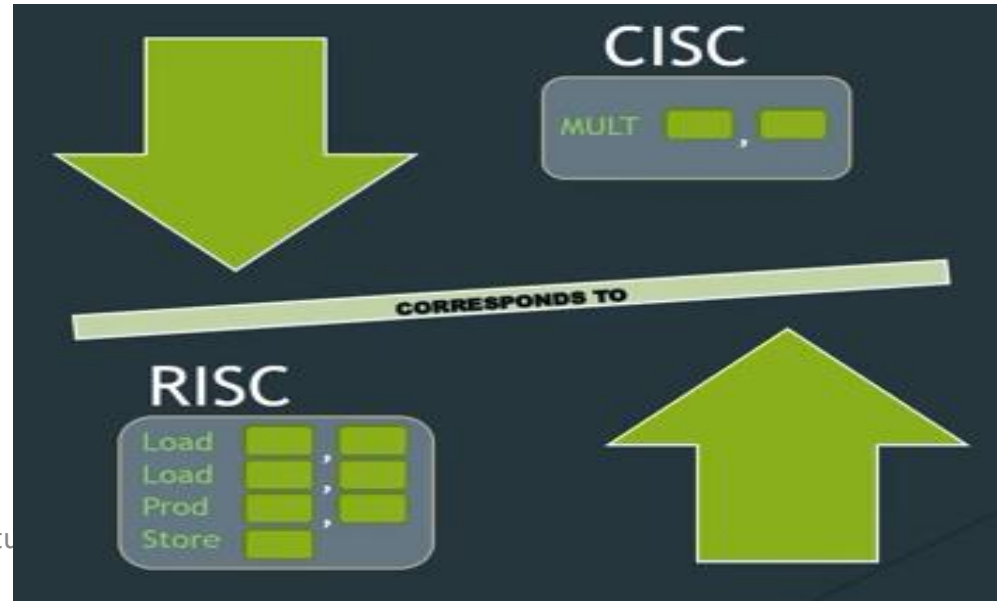
CISC Architecture Processor: Main Features

- **Represents** the **C**omplex **I**nstruction **S**et **C**omputer.
- Main goal – completion of task by using less number of instruction lines – smaller **programming code** but **complex instructions** – **Hardware** can be complex – complex **decoding**
- **Multi clock cycles** required for per instruction execution
- More **Addressing modes**, more **memory access** for operands
- Less **number of registers** in processor
- **Pipelining** is difficult to be implemented for complex instructions
- Support **microprogramming/ micro coding** – low level code –**instructions** are **groups** of microprogram codes and executed accordingly that **defines** how microprocessor execute instructions– **inbuilt** in main memory of the processor – **faster** than memory access
- Used in laptop, general purpose PCs, x86 processor (Section 1.4)

RISC and CISC Architecture Processor

- Both perform **decode and execute** phase in instruction execution
- RISC is highly efficient but has many lines of code whereas CISC has several lines of instructions
- RISC is simple and more cost efficient than CISC (comparing mobile phones with PCs)
- BUT nowadays we use their hybrid

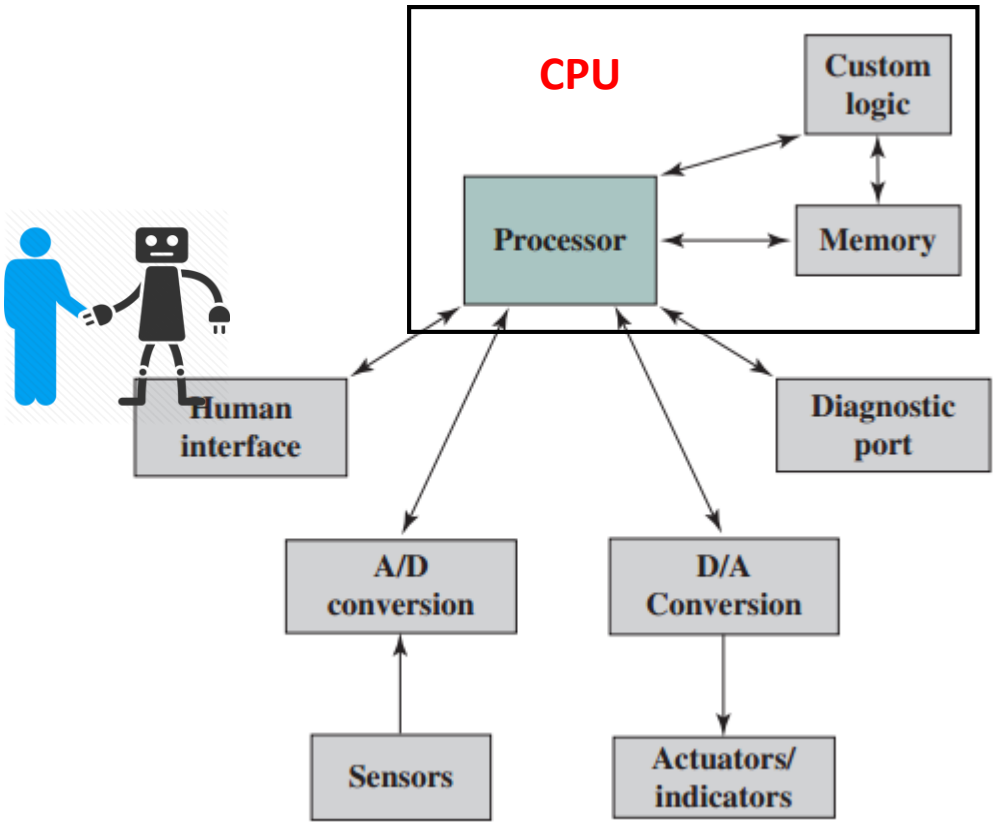




Embedded Systems

- Refers to the **use of electronics and software** within a product – opposite to a general purpose computer.
- Sometimes tightly coupled to the environment – to meet real time constraints

Embedded Systems: System Organization



- Several **Interfaces** for **measurement, manipulation and interaction** (sense, manipulate, communicate) with external world
- **Human interface** to interact with human
- **Diagnostic port** – diagnose the system itself
- **Special hardware** may be used to increase performance
- Application specific software
- **Optimized** energy, code size, execution time, weight, dimensions, cost
- **Embedded operating system** – existing OS (adapted for embedded system) and OS intended solely for embedded use
- **Deeply Embedded System** – subset of embedded system – **use microcontroller rather than microprocessor** – dedicated for a specific purpose

Internet of Things (IoT)

- It refers to **expanding interconnections** of smart devices ranging from appliances to tiny sensors
- The theme is the embedding of short range mobile transceivers into a wide array of gadgets and everyday items –enables new form of communication among people, things and themselves
- Driven by **embedded devices**
- **Internet** support this interconnection through **cloud system**

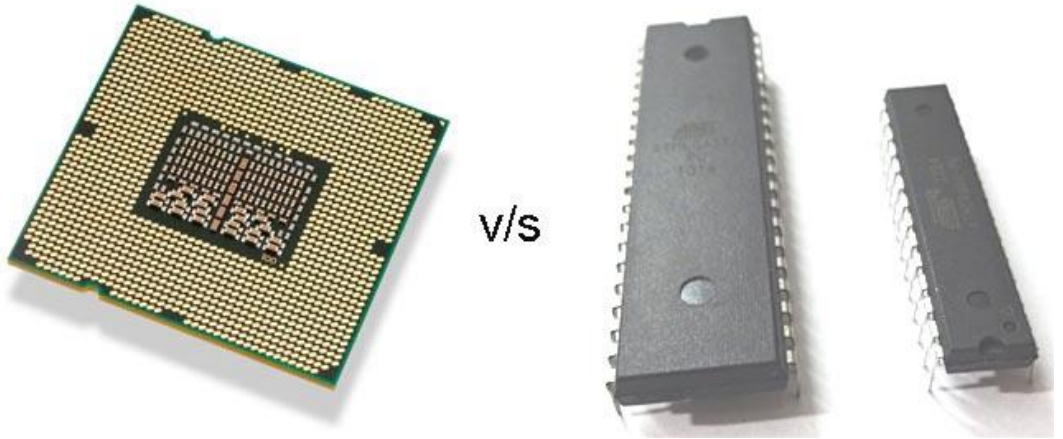
Kuva 1. Internet of Things. Lähde: Huffington Post

Application and Dedicated Processor

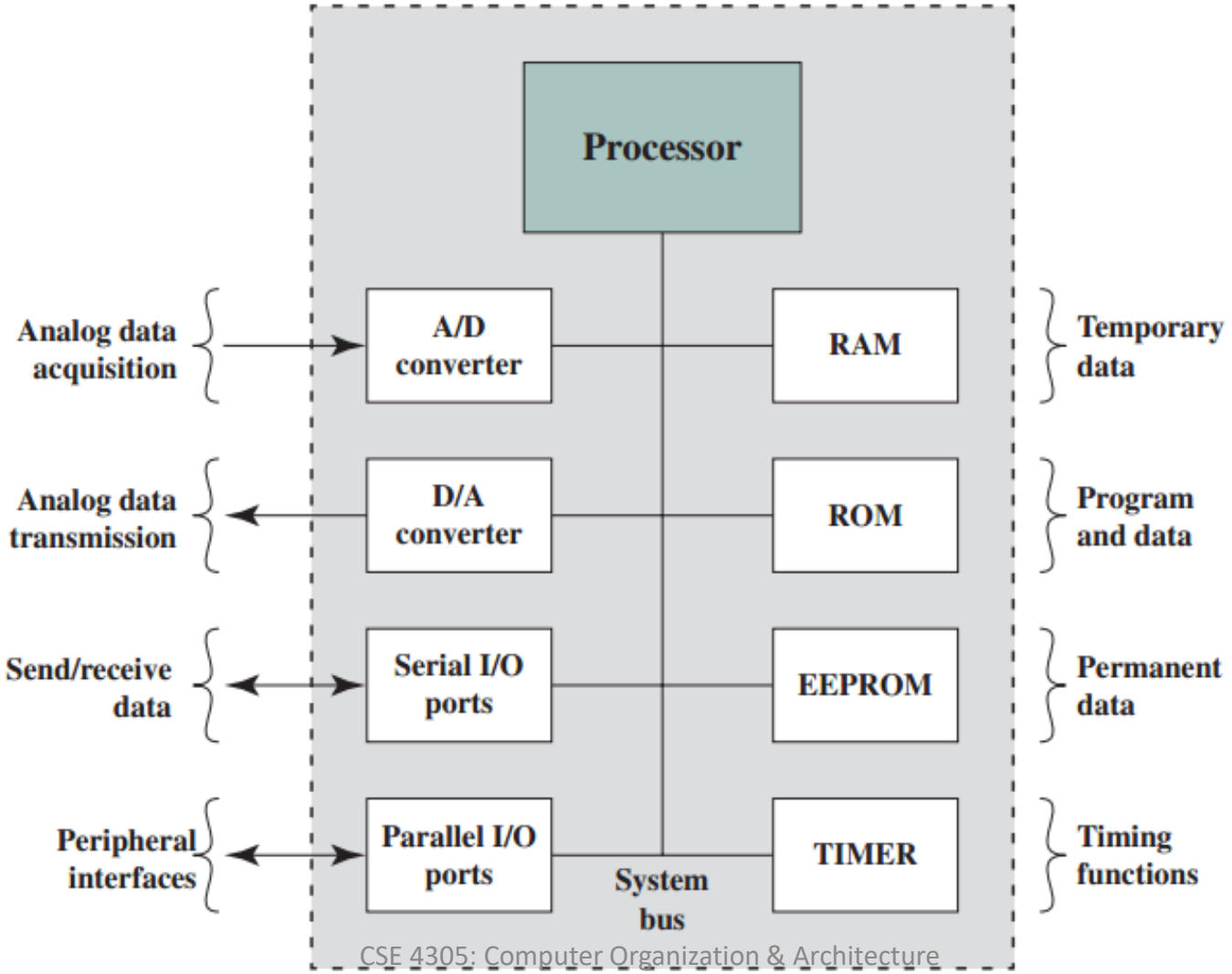
- **Application processor:** able to **execute complex OS** such as Linux, Windows – general purpose in nature – in smartphones
- **Dedicated processor: dedicated** for one or small number of **specific tasks** required by the host device

Microprocessors VS Microcontrollers

- **Microprocessor** includes registers, ALU, Control unit, instruction processing logic – also multiple cores and cache memory
- **Microcontroller** is a single chip containing processor, ROM, RAM, clock, I/O control unit – **computer on a chip**
  - **Slower** than microprocessor – also has smaller area for processing in processor
  - **Not** provide **human interaction**
  - **Programmed** for a specific task
  - **Embedded** in a device



Microcontroller : Block Diagram



Cloud Computing

- **Internet connected infrastructure** – known as enterprise cloud computing – mostly used by large organizations for IT operations
- Single user of PCs and mobile devices also relies on cloud computing – back up, synch, share using personal cloud computing
- Top benefits – **economics of scale, professional network management, professional security management** – attractive to the companies
- Users only **pay for storage capacity and services they need**

Cloud Computing…

Cloud computing: A model for **enabling** ubiquitous, convenient, on-demand **network access** to **a shared pool of configurable computing resources** (e.g., networks, servers, storage, applications, and services) that can be rapidly **provisioned** (temporary) **and released with minimal management effort** or service provider interaction.

- The user, be it company or individual, doesn't have the hassle of setting up a database system, acquiring the hardware they need, doing maintenance, and backing up the data — **all these are part of the cloud service**.

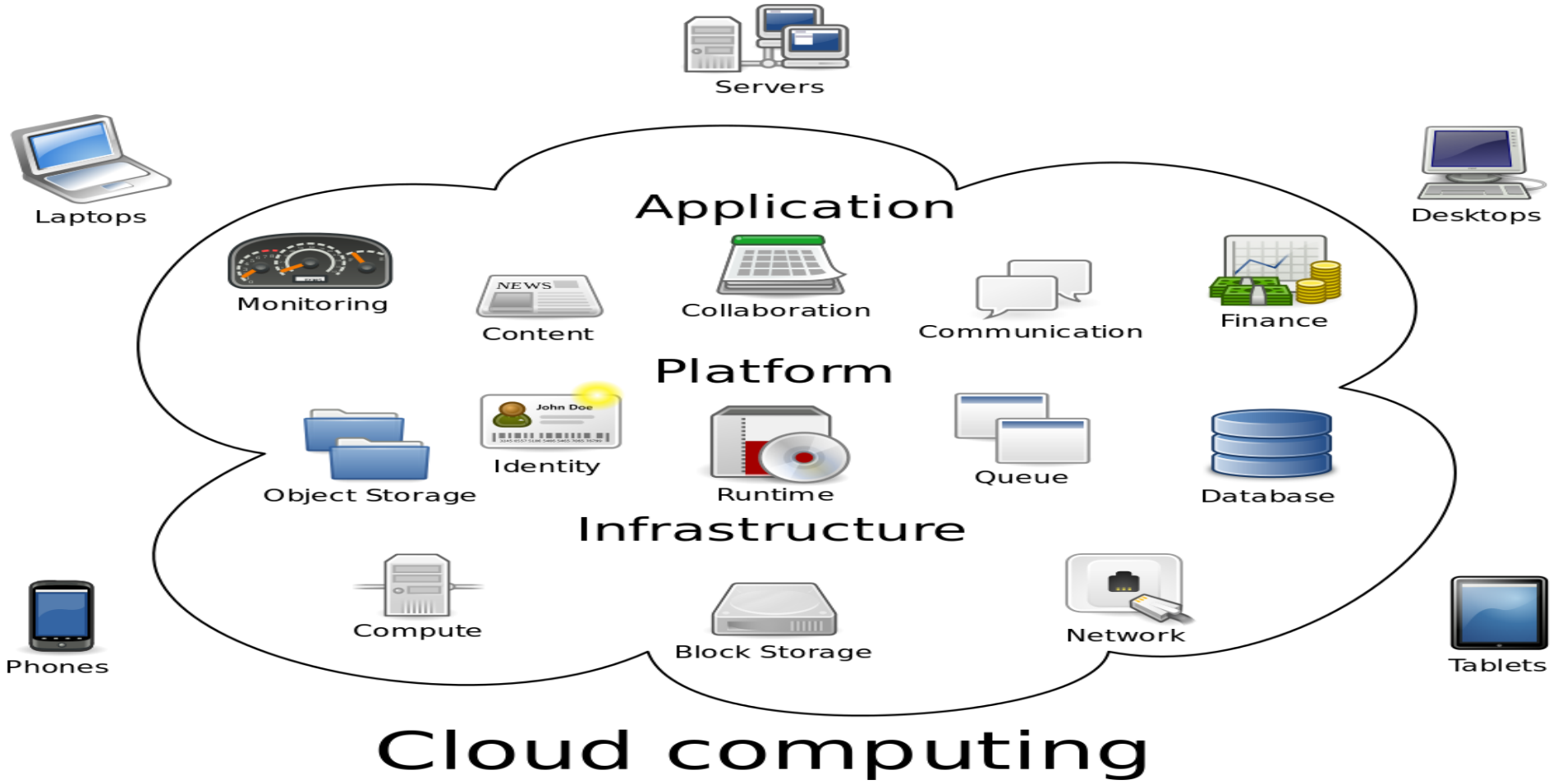
Cloud Computing…

- **Cloud Networking** – **networks and its management** – to enable cloud computing
  - **Internet** is very crucial for all tasks in cloud – **high performance and high reliability** should be ensured between provider and subscribers
  - This INTERNET can be **bypassed** dedicated **private network owned by cloud services** – provides all the services on the behalf real INTERNET – like **access** cloud, **link** with data centers, **use** of firewalls, network **security**
- **Cloud storage** – consisting of **database storage**, **database applications** (controlled cloud servers) – gives access form small business to individuals - without buy, maintain, and manage

Cloud Services

- **Software as a Service** (SaaS) – service **in the form of software** to run and access that software in cloud. Same model of Web services.
- **Platform as a Service** (PaaS) – service **in the form of a platform** on which customer's applications can run. Also some development tools to develop new applications
- **Infrastructure as a Service** (IaaS) – through this service **customers has access to underlying infrastructure** using virtual machine, abstracted hardware, operating systems which are controlled through **API** – Windows AZURE, Amazon ELASTIC

Cloud Services…



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