Islamic University of Technology

Department of Electrical and Electronic Engineering

EEE 4483 – (Digital Electronics and Pulse Technique)

Introduction to VHDL and Modelsim

Introduction

The purpose of this lab is to give a first introduction to the VHDL based design flow for Altera FPGAs.

For code editing `Emacs` text editor will be used. After writing VHDL code for digital circuits we need to verify the program by testbenches. Up to this stage for compilation and to check the timing diagrams will use Modelsim.

Book:

1. Introduction to Logic Circuits & Logic Design with VHDL by *Brock J. LaMeres*

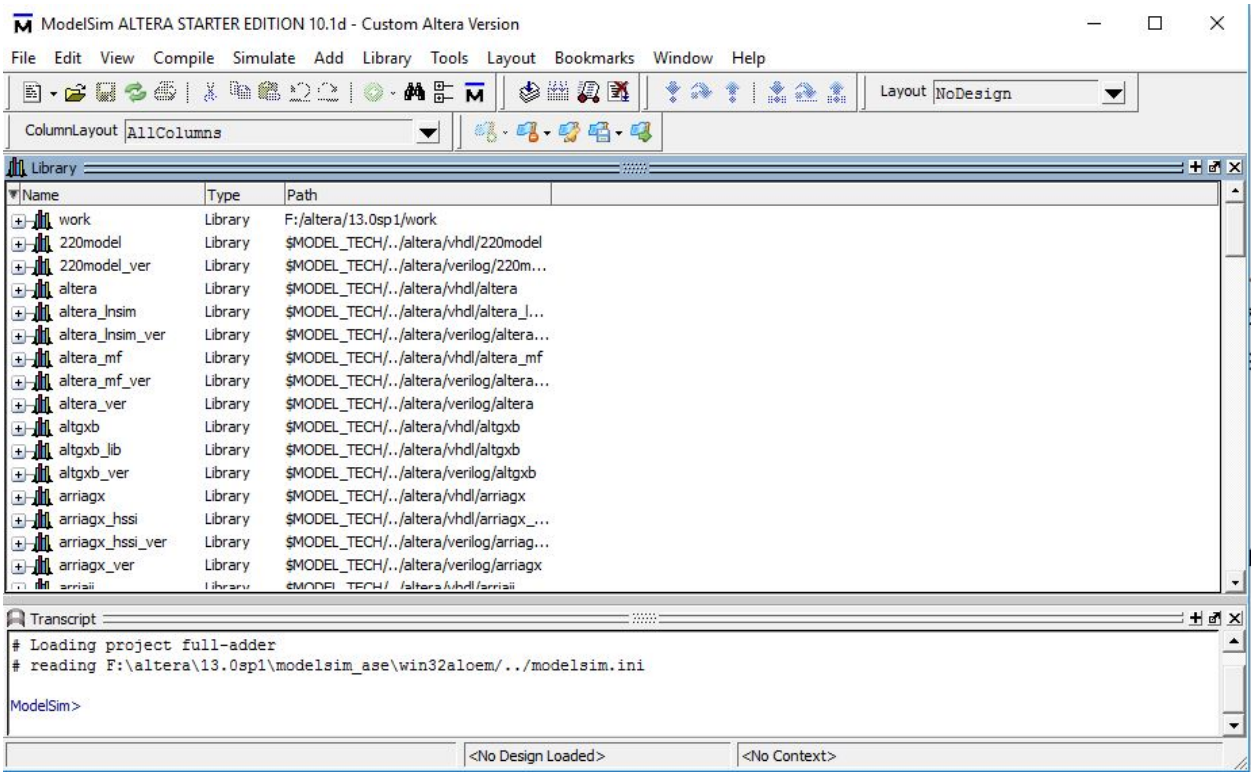
   1st edition (2017)

   Chapter 5 (section - 5.4, 5.5, 5.6, 5.7)

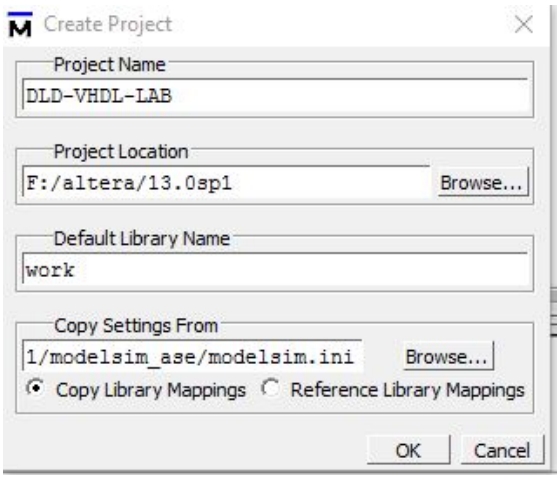
Download Links:

1. Quartus II Web Edition (Free) , includes Quartus II Software and ModelSim-Altera Starter Edition
2. Emacs

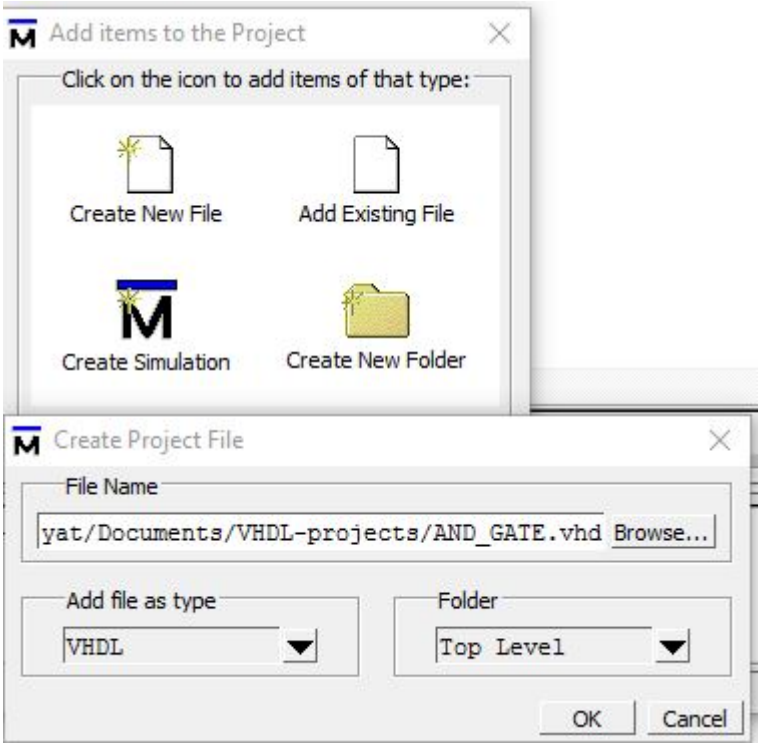
⇨ Steps to run/compile VHDL program in ModelSim:



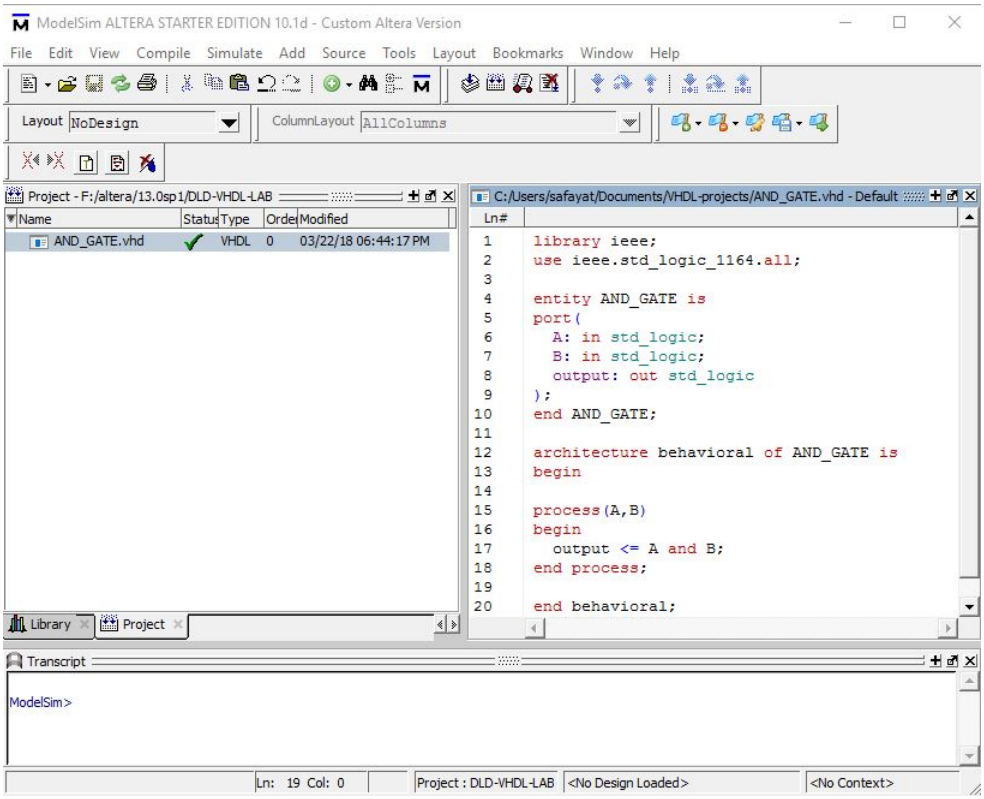
To create a new project in ModelSim : ***`File` → `New` → `Project`.*** The project will be saved in the default `work` library.



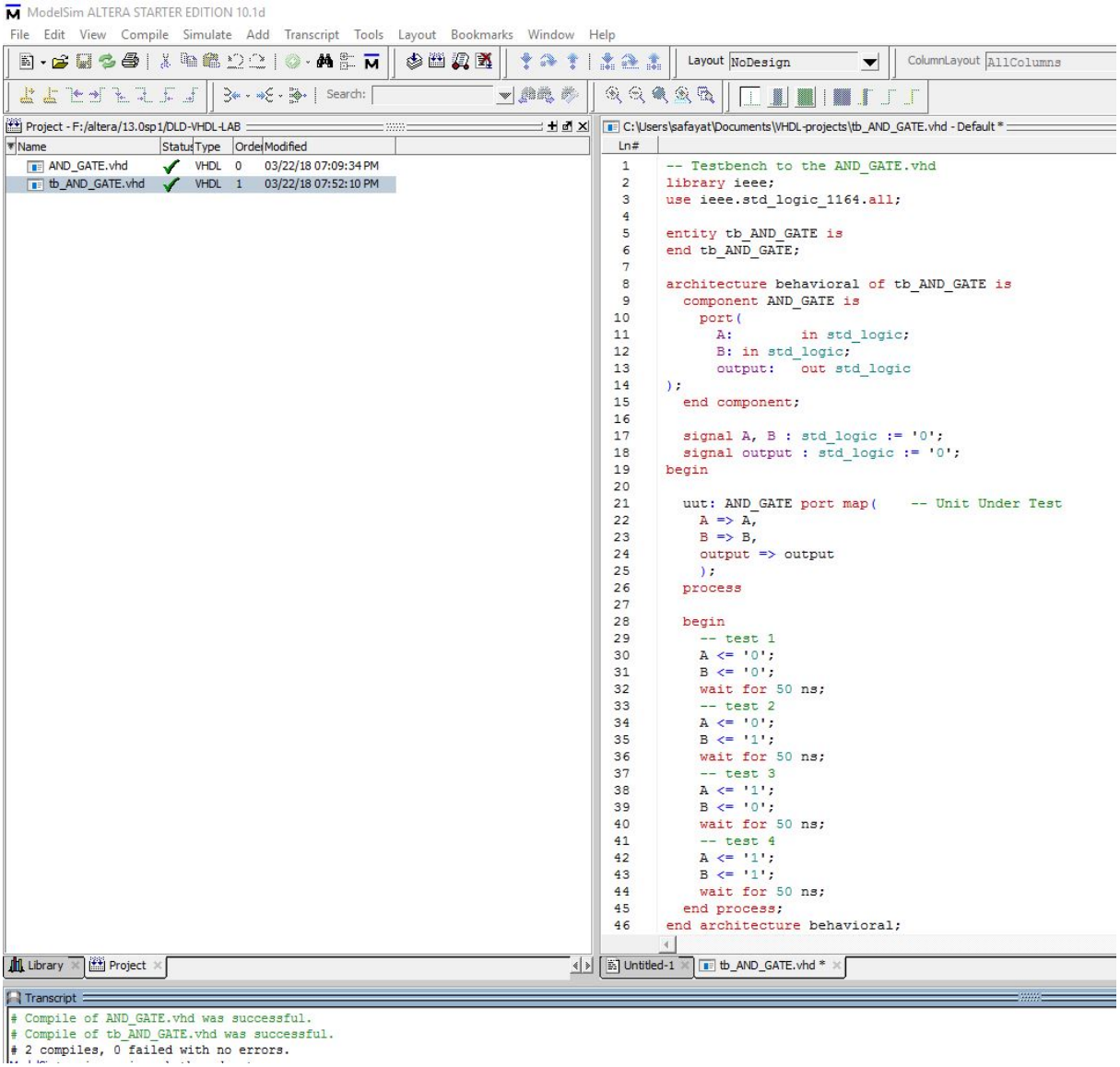
Now click on ***`Create New File`*** and show the appropriate VHDL file (*.vhd) from project directory.



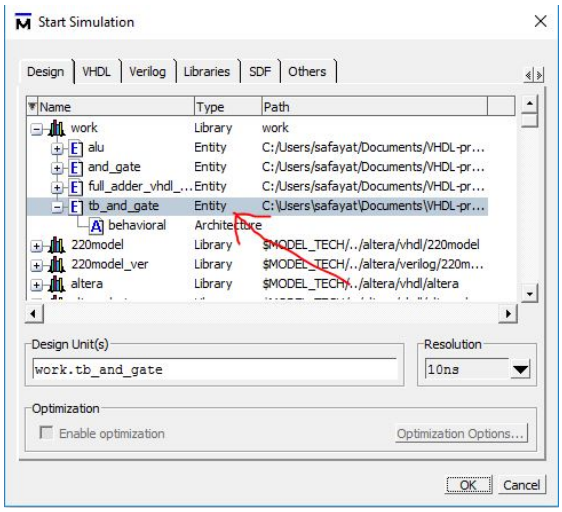
⇨ ***AND_GATE.vhd*** is the main source-code file of the design.



⇨ We need to write a testbench to test the design with various inputs.



⇨ Now we will simulate the testbench and generate the timing diagram. Go to ***Simulate*** → ***Start Simulation***. Set the Resolution as `10ns`. Then proceed by hitting `Ok`.



⇨ A new set of windows will pop up with Objects, Processes, Scope(to see timing diagrams). From the **Add** select ***To Wave*** → ***All items in region***. Next press **F9** or click on **Run.**