80186 Microprocessor

- 80186 contains 8086 processor and several additional functional chips:
  - Clock generator
  - 2 independent DMA channels
  - PIC (Programmable IC)
  - 3 programmable 16-bit timers
- It is more of a microcontroller than a microprocessor
- Used mostly in industrial control applications

Intel 80286: Salient Features

- High performance microprocessor with memory management and protection
  - 80286 is the first member of the family of advanced microprocessors with built-in/on-chip memory management and protection abilities primarily designed for multi-user/multitasking systems
- Available in 12.5MHz, 10MHz & 8MHz clock frequencies

Intel 80286: Salient Features

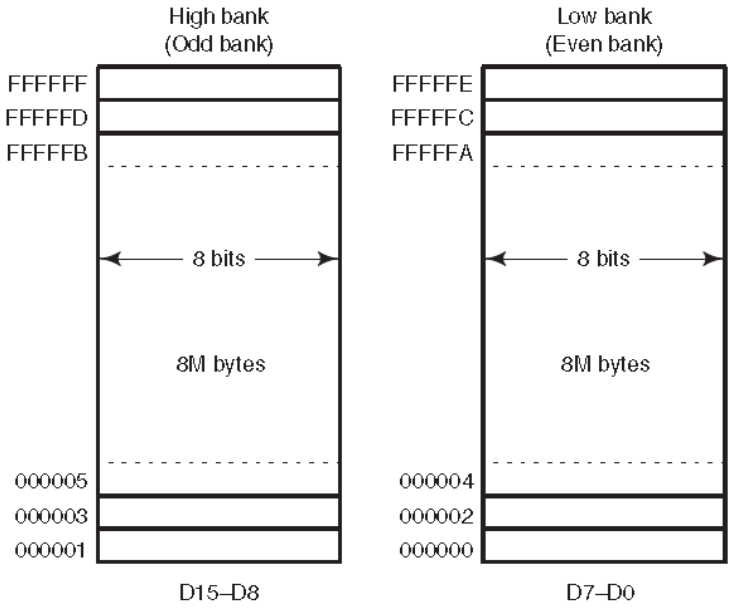
- The 80286 CPU, with its 24-bit address bus is able to address 16MB of physical memory.
- 1GB of virtual memory for each task

Microprocessor	Data bus width	Address bus width	Memory size
8086	16	20	1M
80186	16	20	1M
80286	**16**	**24**	**16M**

Intel 80286: Salient Features

Intel 80286 has 2 operating modes:

- **Real Address Mode :**
  - 80286 is just a fast 8086 - up to 6 times faster
  - All memory management and protection mechanisms are disabled
  - It allows the microprocessor to address only the first 1M byte of memory space.
  - The first 1M byte of memory is called the real memory, conventional memory, or DOS memory system.
  - Windows does not use the real mode.
  - The concept of **Segment** and **Offset** is used.



Intel 80286: Salient Features

Intel 80286 has 2 operating modes:

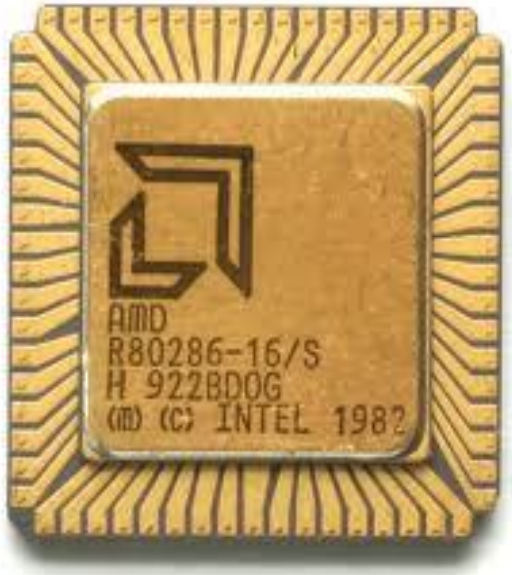
- **Protected Virtual Address Mode**
  - 80286 works with all of its memory management and protection capabilities with the advanced instruction set.
  - It uses all 24 address lines to access upto 16 Mbytes of physical memory and provides upto Gigabyte range virtual memory.
  - **Protected mode** is where Windows operates.

Memory Management Unit

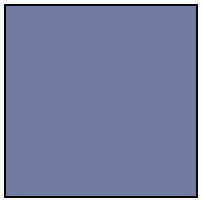
- An 80286 switches to protected mode and start using virtual memory.
- In protected mode, the concept of **Segment** is not used.
- A 80286 virtual address consists of a 16-bit **Selector** and 16-bit **Offset**.
- A memory management unit (MMU) uses 16-bits of selector to access a **Descriptor** for the desired segment in a table of descriptors.
- Each 80286 descriptor describes a 64K-byte memory segment and the 80286 allows 16K descriptors. This (64K × 16K) allows a maximum of 1G bytes of memory to be described for the system.
- The descriptor contains the 24-bit physical address.

Intel 80286: Salient Features

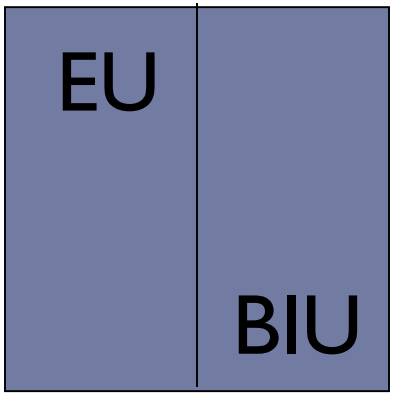
- 80286 includes special instructions to support operating system.
  - for example, one instruction can
    - i) End the current task
    - ii) Save its states
    - iii) Switch to a new task
    - iv) Load its states and
    - v) Begin executing the new task
- Housed in 68-pin package
- 1,34,000 Transistors



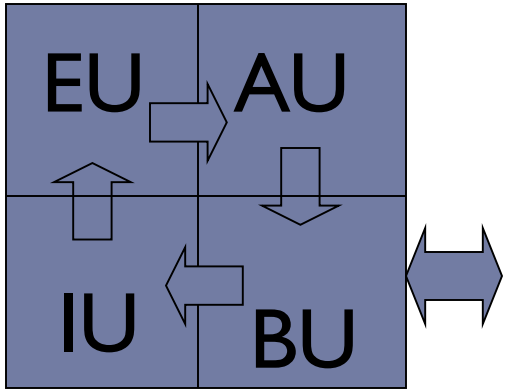
Internal Block Diagram of 80286



8085

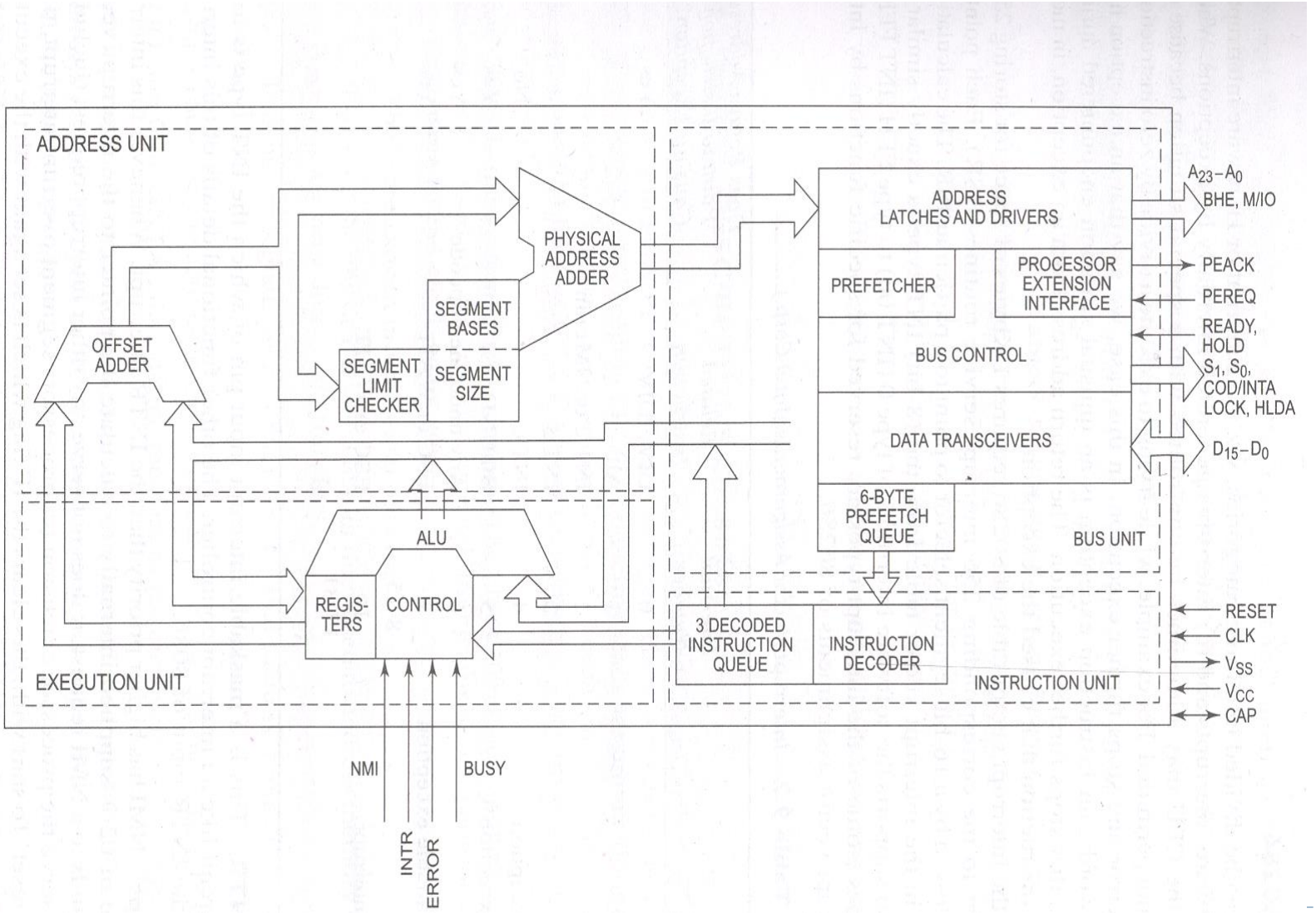


8086



80286

Internal Block Diagram of 80286



Functional Parts of 80286

- Address Unit (AU)
- Bus Unit (BU)
- Instruction Unit (IU)
- Execution Unit (EU)

Address Unit (AU)

- Calculates the physical addresses of the instruction and data that the CPU want to access
- Address lines derived by this unit may be used to address different peripherals.
- Physical address computed by the Address Unit (AU) is handed over to the BUS Unit (BU).

BUS Unit (BU)

- Performs all memory and I/O **read** and **write** operations.
- Take care of communication between CPU and a coprocessor.
- Transmit the physical address over address bus A_0 – A_{23}.
- Pre-fetcher module in the BU performs the task of pre-fetching.
- Bus controller controls the pre-fetcher module.
- Fetched instructions are arranged in a 6 – byte pre-fetch queue.

Instruction Unit (IU)

- IU receives arranged instructions from 6 byte pre-fetch queue.
- Instruction decoder decodes up to 3 pre-fetched instruction and are latched them onto a decoded instruction queue.
- Output of the decoding circuit drives a control circuit in the Execution Unit (EU).

Execution Unit (EU)

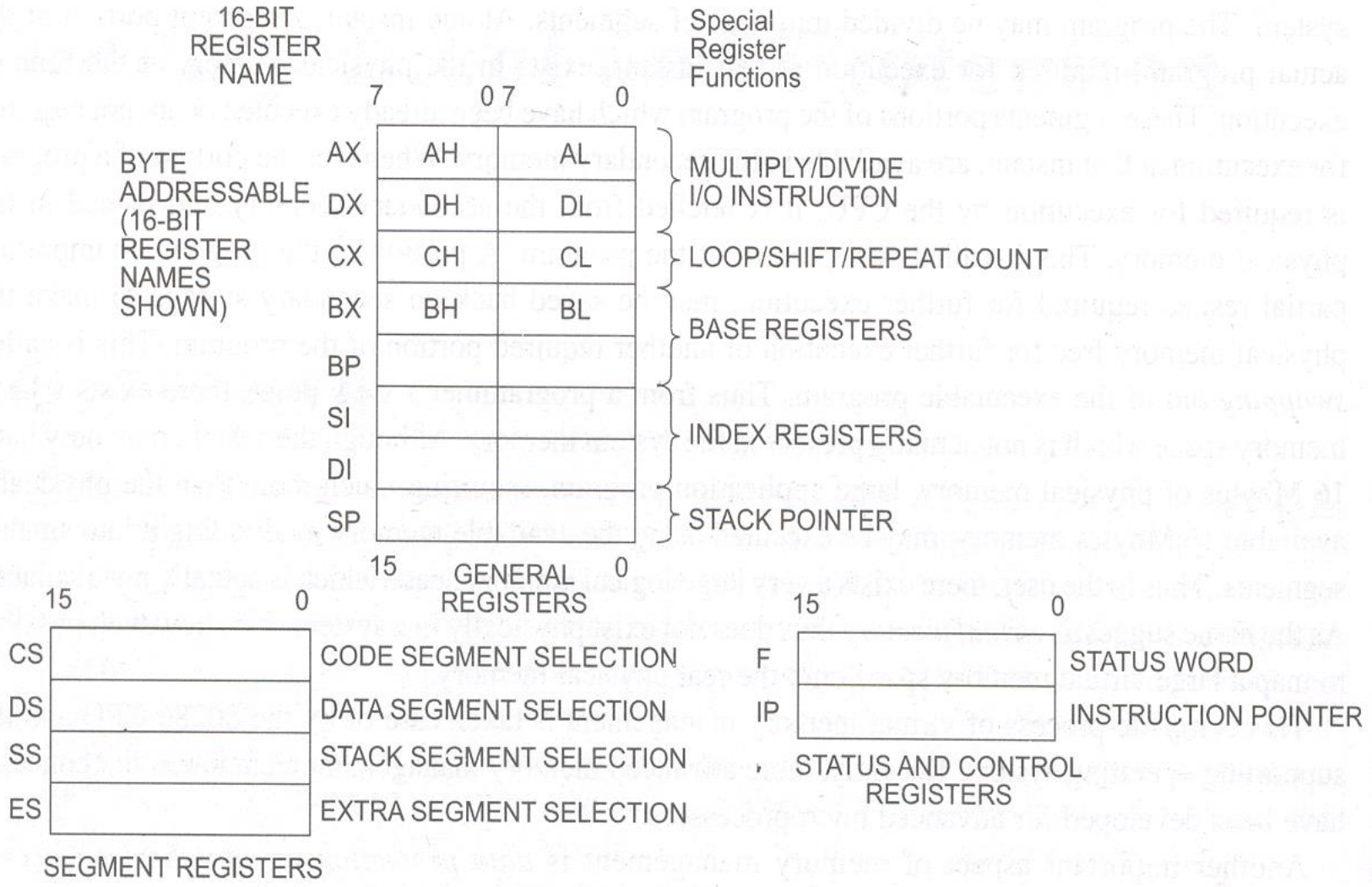
- EU executes the instructions received from the decoded instruction queue sequentially.
- Contains Register Bank.
- Contains one additional special 16-bit register called **Machine status word (MSW)** register **---** lower 4 bits are only used.
- ALU is the heart of Execution Unit (EU).
- After execution ALU sends the result either over data bus or back to the register bank.

Register Organization of 80286

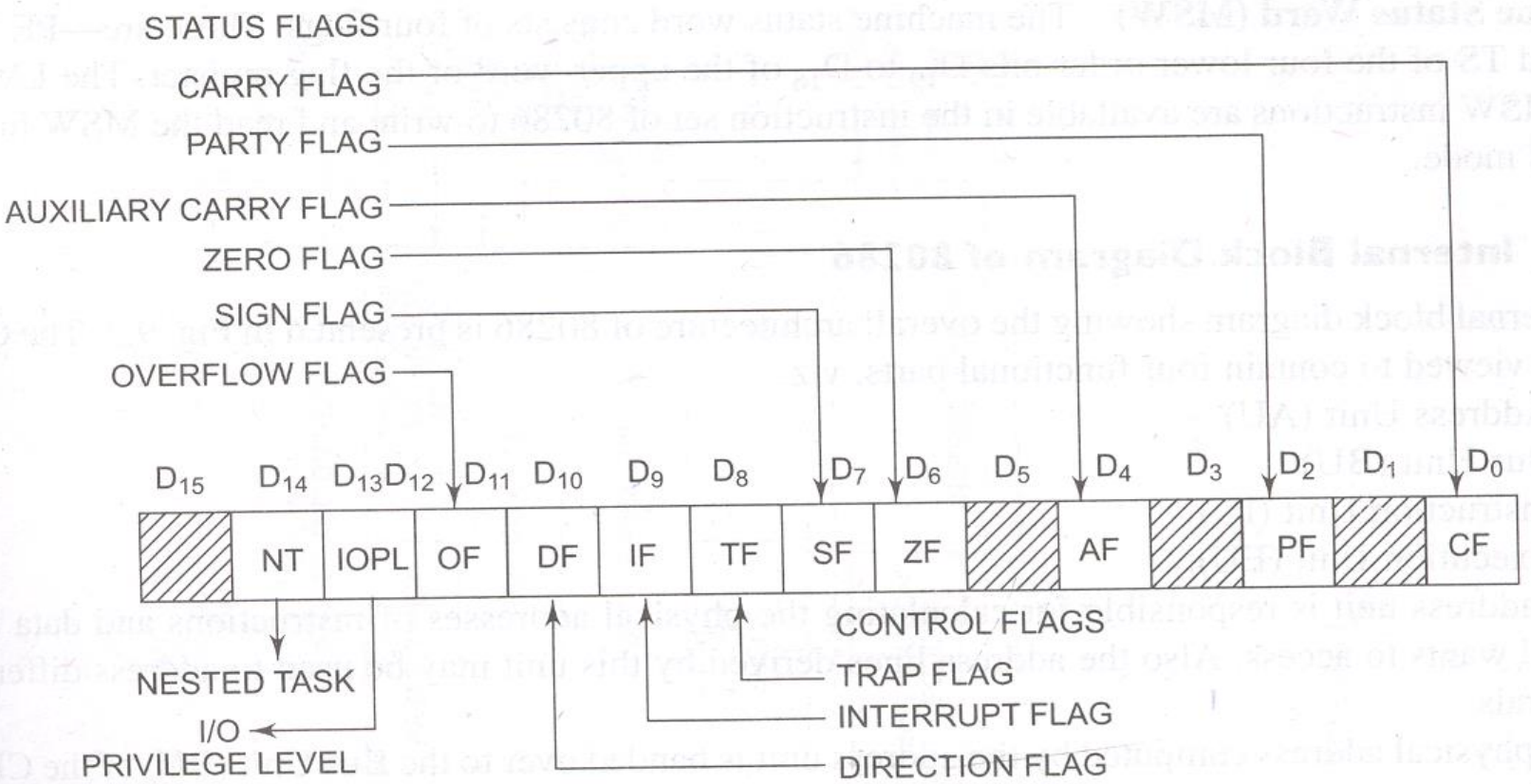
The 80286 CPU contains the same set of registers, as in 8086.

- Eight 16-bit general purpose registers (Data, Base-pointer and Index)
- Four 16 bit segment registers (Segment)
- Status and control register (Flag)
- Instruction pointer (IP)
- Machine Status Word (MSW)

Register Organization of 80286



Only Change in Flag Register



IOPL – Input Output Privilege Level Flags (Bit D_{12} and D_{13})

- IOPL is used in protected mode operation to select the privilege level for I/O devices.
- If the current privilege level is higher or more trusted than the IOPL, I/O is executed without hindrance.
- Note that IPOL 00 is the highest or more trusted and IOPL 11 is the lowest or least trusted.
- If the IOPL value is lower than the current privilege level, an interrupt occurs, causing execution to suspend.

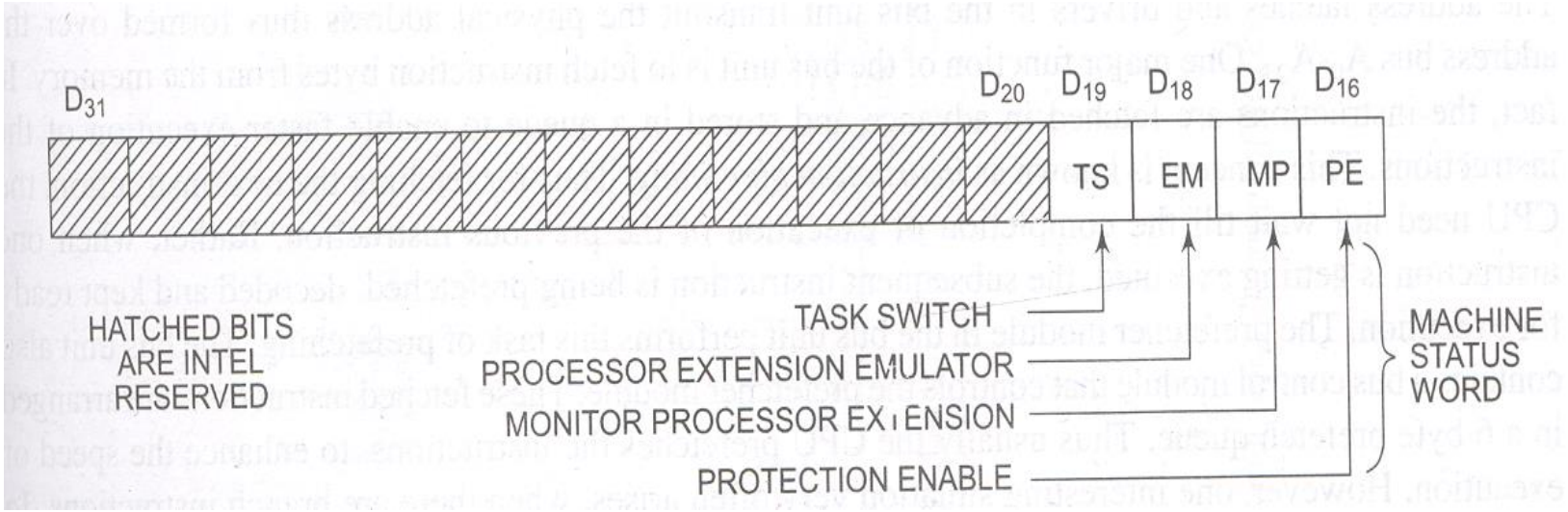
NT – Nested Task Flag (Bit D_{14})

- When NT is set, it indicates that one system task has invoked another through a CALL instruction as opposed to a JMP.
- For multitasking this can be manipulated to have advantage.

Machine Status Word (MSW) Register

- Consist of four flags. These are – **PE**, **MP**, **EM** and **TS**

- **Instructions** are available in the instruction set of 80286 to **write** and **read** the MSW in real address mode.



Machine Status Word (MSW) Register

- PE – Protection Enable
  - Protection enable flag places the 80286 in protected mode, If it is set. This can only be cleared by resetting the CPU.
- MP – Monitor Processor Extension
  - Flag allows WAIT instruction to generate a processor extension (when any Coprocessor is connected or attached).
- EM – Emulate Processor Extension Flag
  - If set , causes a processor extension (Coprocessor) is absent and permits the emulation of processor extension by CPU.
- TS – Task Switch
  - This flag permits the CPU to test whether the current processor extension is for current task or not. As the time progresses, it might be needed to change the current task; to set aside logically the segments that comprise current task and make sub-segment for another task.