

Limitations of 80286

- ▶ 16-bit ALU.
- ▶ 64K segment size for the programs.
- ▶ 1 GB of virtual memory
- ▶ Cannot be easily switched back and forth between **real** and **protected mode**
 - ▶ To come back to the **real mode** from **protected mode**, it is needed to switched off the 80286.

80386 Overcomes 80286 Limitations

- ▶ It has 32 bit ALU.
- ▶ Segment size can be as large as 4GB
 - ▶ A program can have as many as 16K segments
 - ▶ So, a program has access to $4\text{GB} \times 16\text{K} = 64\text{TB}$ of virtual memory
- ▶ 80386 has a ***virtual 86 mode*** which allows easy switching between **real** and **protected modes**.

80386: Salient Features

- ▶ Alternatively referred to as a **386** or the **i386**
- ▶ Intel introduced the first 32-bit chip, 80386, in October 1985 as an upgrade to the 80286 processor
- ▶ Intel stopped producing 386 since September 2007.
- ▶ 386 incorporates 275,000 transistor
- ▶ 386 was capable of performing more than five million instructions every second (**MIPS**)
- ▶ 386 was available in clock speeds between 12 and 40MHz.

Versions of 80386

- ▶ Two versions were commonly available:
 - 1) 80386 DX
 - 2) 80386 SX
- ▶ The original 80386 processor was renamed as 80386DX or 386DX after introducing 386SX.
- ▶ 80386SX was introduced in 1988 as a low cost solution alternative to the original 80386.
- ▶ 80386SX was developed after the DX, for the application that didn't require the full 32-bit capabilities.

Versions of 80386

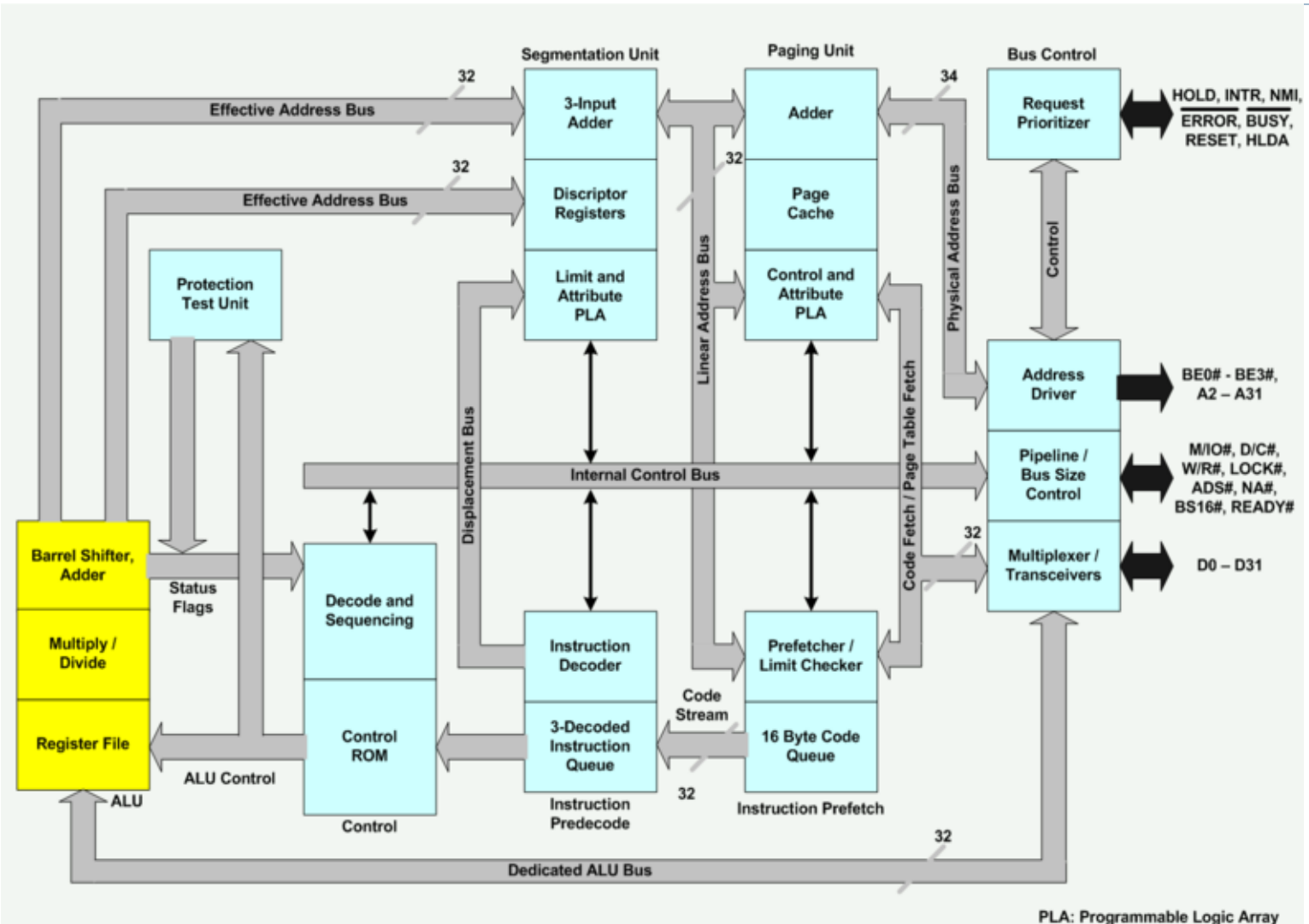
- ▶ It is found in many PCs where it uses the same basic mother board design as the 80286.
- ▶ Most application need less than the 16MB of memory, so the SX is popular and less costly version of the 80386 microprocessor.
- ▶ The 80386SX lacked a math coprocessor but still featured the 32-bit architecture and built-in multitasking.
- ▶ The chip was available in clock speeds of 16MHz, 20MHz, 25MHz, and 33MHz.

80386DX Vs. 80386SX

80386DX	80386SX
32 bit address bus	24 bit address bus
32 bit data bus	16 bit data bus
Packaged in 132 pin	100 pin flat package
Address 4GB of memory	16 MB of memory

- ▶ Both have the same internal architecture.
- ▶ Lower cost package and the ease of interfacing to 8-bit and 16-bit memory and peripherals make SX suitable for use in low cost systems.

Internal Block Diagram of 80386



Architecture of 80386: **Instruction Unit**

- ▶ The Instruction unit decodes the op-code bytes received from the 16-byte **instruction code queue** and arranges them in a 3-instruction decoded instruction queue.
- ▶ After decoding them pass it to the control section for deriving the necessary control signals.
- ▶ The barrel shifter increases the speed of all shift and rotate operations.

Architecture of 80386: **Instruction Unit**

- ▶ The multiply / divide logic implements the **bit-shift-rotate** algorithms to complete the operations in minimum time.
- ▶ Even 32- bit multiplications can be executed within one microsecond by the multiply / divide logic.

Architecture of 80386: **Segmentation Unit**

- ▶ Segmentation unit allows the use of two address components, viz. **segment** and **offset** for relocate ability and sharing of code and data.
- ▶ Segmentation unit allows segments of size 4Gbytes at max.
- ▶ The Segmentation unit provides a 4 level protection mechanism for protecting and isolating the system code and data from those of the application program.

Architecture of 80386: **Paging Unit**

- ▶ The Paging unit organizes the physical memory in terms of pages of 4kbytes size each.
- ▶ Paging unit works under the control of the segmentation unit, i.e. each segment is further divided into pages.
- ▶ The virtual memory is also organizes in terms of segments and pages by the memory management unit.
- ▶ Paging unit converts linear addresses into physical addresses.

Architecture of 80386: **Bus Control Unit**

- ▶ The Bus control unit has a prioritizer to resolve the priority of the various bus requests.
- ▶ This controls the access of the bus.
- ▶ The address driver drives the bus enable and address signal A2 – A31.
- ▶ The pipeline and dynamic bus sizing unit handle the related control signals.
- ▶ The data buffers interface the internal data bus with the system bus.

80386 Data Bus

- ▶ 32-bit data bus
- ▶ D0 through D31 (Data Bus)
- ▶ Bi-Directional

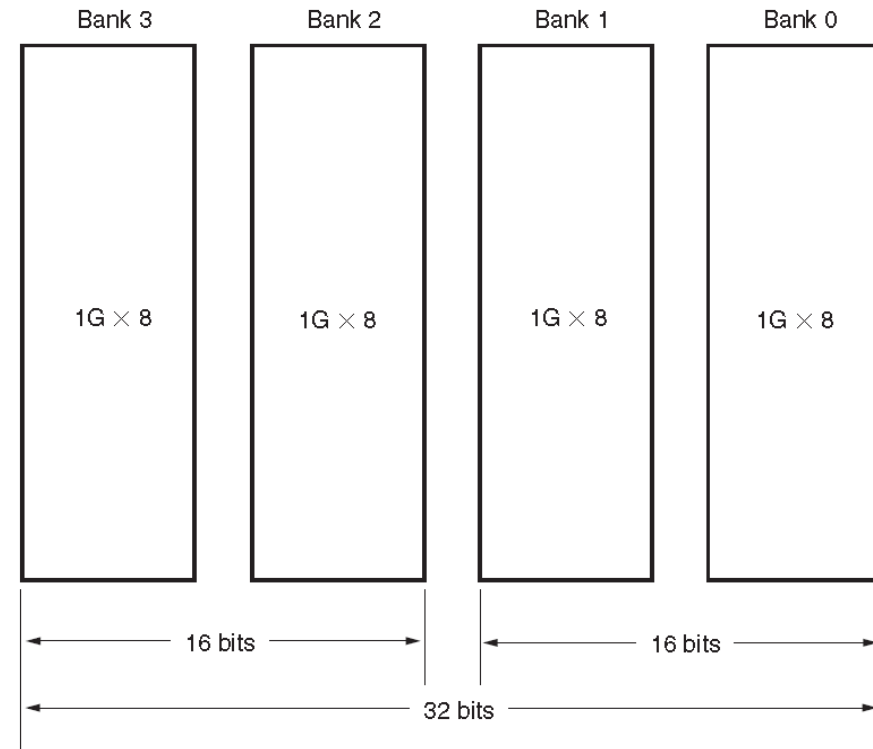
80386 Address Bus

- ▶ Address bus consists of A2 to A31 address lines and BE0 to BE3 byte/bank enable lines
- ▶ No A0 & A1 address lines are available in 386
 - ▶ they are internally decoded to produce BE0 to BE3 signals

80386 Address Bus

▶ **BE0 through BE3**

- ▶ Byte (Bank???) Enable lines
 - ▶ Memory are arranged in 4 Banks
- ▶ BE0-BE3 also allow 80386 to transfer **byte**, **word** and **double word**



Register Organization of 80386

▶ **Segment Descriptor Registers:**

- ▶ This registers are not available for programmers, rather they are internally used to store the descriptor information, like attributes, limit and base addresses of segments.
- ▶ *Six Segment Registers* have corresponding six 73 bit descriptor registers.
- ▶ Each of them contains 32 bit base address and 32 bit base limit and 9 bit attributes.
- ▶ These are automatically loaded when the corresponding segments are loaded with selectors.

Register Organization of 80386

▶ **System Address Registers:**

- ▶ Four special registers are defined to refer to the descriptor tables supported by 80386.
- ▶ The 80386 supports four types of descriptor table, viz.
 - ▶ Global descriptor table (GDT)
 - ▶ Interrupt descriptor table (IDT)
 - ▶ Local descriptor table (LDT) and
 - ▶ Task state segment descriptor (TSS)

Register Organization of 80386

▶ **Control Registers:**

- ▶ The 80386 has three (3) 32 bit control registers CR0, CR2 and CR3.
- ▶ These hold global machine status independent of the executed task.
- ▶ Load and store instructions are available to access different registers of 80386 microprocessor.

Register Organization of 80386

▶ **Debug and Test Registers:**

- ▶ Intel has provide a set of 8 debug registers for hardware debugging.
- ▶ Out of these eight registers DR0 to DR7, two registers DR4 and DR5 are Intel reserved.
- ▶ **The initial four registers DR0 to DR3** store four program controllable breakpoint addresses, while DR6 and DR7 respectively hold breakpoint status and breakpoint control information.
- ▶ **Two more test register** are provided by 80386 for page caching namely test control and test status register.

Register Organization of 80386

▶ **Flag Register:**

- ▶ The Flag register of 80386 is a 32 bit register.
- ▶ Out of the 32 bits, Intel has reserved bits D18 to D31, D5 and D3 and set to 0.
- ▶ While D1 is always set at 1.
- ▶ Two extra new flags are added to the 80286 flag to derive the flag register of 80386.
- ▶ They are VM and RF flags.

Register Organization of 80386

Old flags of 286

31	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RESERVED FOR INTEL				VM	RF	0	NT	IOPL	OF	DF	IF	TF	SF	ZF	0	AF	0	PF	IF	CF

New flags for 386

Register Organization of 80386

- ▶ **VM - Virtual Mode Flag in Flag Register**
- ▶ If this flag is set to 1, the 80386 enters the virtual 8086 mode within the protection mode.
- ▶ When VM bit is 0, 386 operates in protected mode
- ▶ This is to be set only when the 80386 is in protected mode.
- ▶ This bit can be set using IRET instruction or any task switch operation only in the protected mode.

Register Organization of 80386

- ▶ **Resume Flag (RF) in Flag Register**
- ▶ If RF=1, then 80386 ignores debug faults
 - Does not take another exception so that an instruction can be restarted after a normal debug exception.
- ▶ If RF=0, then 80386 takes another debug exception to service debug faults
- ▶ This flag is used with the debug register breakpoints.

Register Organization of 80386

▶ **Resume Flag (RF) in Flag Register**

- ▶ It is checked at the starting of every instruction cycle and if it is set, any debug fault is ignored during the instruction cycle.
- ▶ The RF is automatically reset after successful execution of every instruction, except for IRET and POPF instructions.
- ▶ Also, it is not automatically cleared after the successful execution of JMP, CALL and INT instruction causing a task switch.
- ▶ These instruction are used to set the RF to the value specified by the memory data available at the stack.

80386 Modes of Operation

- ▶ There are 3 modes of operations:
 - ▶ **Real Mode**
 - ▶ Already discussed it in Lecture-10 (80286 MP)
 - ▶ **Protected Mode**
 - ▶ Already discussed it in Lecture-10 (80286 MP) --- same as 80286.
 - ▶ Only difference is in descriptor description (to be discussed in coming lectures)
 - ▶ **Virtual 8086 Mode**
 - ▶ In the 80386, virtual 8086 mode (also called virtual real mode, V86-mode or VM86) **allows the execution of real mode applications that are incapable of running directly** in protected mode while the processor is running a protected mode operating system.
 - Memory Addressing in real mode
 - Interrupt in real mode

Protected Mode

- ▶ Same as 80286
- ▶ Only difference is in
 - ▶ Descriptor's description
 - ▶ Optional use of ***page***
- ▶ If the paging unit is disabled, then linear address produced by segment unit is used as physical address
- ▶ Otherwise the paging unit converts the linear address into page address.
- ▶ The paging mechanism allows handling of large segments of memory in terms of pages of 4Kbyte size.

Virtual 8086 Mode

- ▶ In its protected mode of operation, 386 provides a virtual 8086 operating environment to execute the 8086 programs.
- ▶ The real mode can also be used to execute the 8086 programs along with the capabilities of 386, like protection and a few additional instructions.
- ▶ Once the 386 enters the protected mode from the real mode, it cannot return back to the real mode without a reset operation.

Virtual 8086 Mode

- ▶ Thus, the virtual 8086 mode of operation of 386, offers an advantage of executing 8086 programs while in protected mode.
- ▶ The address forming mechanism in virtual 8086 mode is exactly identical with that of 8086 real mode.
- ▶ In virtual mode, 8086 can address 1Mbytes of physical memory that may be anywhere in the 4Gbytes address space of the protected mode of 386.

Virtual 8086 Mode

- ▶ Like 386 real mode, the addresses in virtual 8086 mode lie within 1Mbytes of memory.
- ▶ In virtual mode, the paging mechanism and protection capabilities are available at the service of the programmers.
- ▶ The 386 supports multiprogramming, hence more than one programmer may be use the CPU at a time.