B.Sc. Engg. / HD CSE 6th Semester — 6 November 2019

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)

Department of Computer Science and Engineering (CSE)

SEMESTER FINAL EXAMINATION — **SUMMER SEMESTER, 2018-2019**

DURATION: 3 Hours — **FULL MARKS: 150**

CSE 4619: Peripherals and Interfacing

Programmable calculators are not allowed. Do not write anything on the question paper.

There are **8 (eight)** questions. Answer any **6 (six)** of them.

Figures in the right margin indicate marks.

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1. a) What is an Embedded System? How does it differ from typical Computer Systems? 10
   b) Differentiate between *Asynchronous*, *Synchronous* and *Isochronous* data transfer. 10
   c) Draw an Embedded Control System Block diagram considering a designer's view. 5

2. a) Write the basic differential features between 8155 and 8255 Programmable Peripheral Interface (PPI). 10
   b) Write short notes on: 10
      i. Daisy-Chain Architecture
      ii. Multi-Level Bus Architecture
   c) List out the implications of being embedded by the embedded systems. 5

3. a) Draw and explain the timing diagrams of 8255 PPI ***mode 0*** and ***mode 1*** signaling. 10
   b) Explain about the handshake signals of 8155 Programmable Peripheral Interface (PPI). 10
   c) In order to connect a Dot-Matrix Display with an 8086 Microprocessor system, how can you interface using a single 8255 PPI? Just draw the interfacing diagram. 5

4. a) How does 8259 PIC can handle 64 Interrupt levels? Explain with necessary diagram. 10
   b) Briefly explain about the operation of Register sets of 8259 PIC. 10
   c) Draw the STACK operation states during an Interrupt. 5

5. a) Draw a block diagram for an 8237 DMA controller. Briefly explain the importance of using HOLD and HOLDA signals. 10
   b) Write a comparative study on *Polling*, *Interrupt* and *DMA* I/O interfacing. 10
   c) "***Memory-Read & I/O Write*** and ***I/O Read & Memory-Write*** signals are used simultaneously for DMA operation" –Explain. 5

6. a) What is CAN bus and why is it called a broadcast type bus? "CAN bus protocol remove $\frac{n(n-1)}{2}$ connections complexity for an embedded system" – explain how? 10
   b) "In CAN, with the bus length increment the transmission speed for data rate decreases" – True/False? Justify your answer. 10
   c) Draw the data frame format of CAN protocol. 5

7. a) "In I^2C bus connections, *master bus* can only be transmitter or transmitter-receiver whereas *slave buses* can only be receiver or receiver-transmitter" – Why? 10

   b) Why does in I^2C bus the Start-End condition and Data-Transition signaling are opposite to each other? Explain. 10

   c) Draw the data formats of I^2C protocol when the Master IC reads and writes to/from Slave IC. 5

8. a) What are UART and USART? Why do we need 8251 UART/USART IC? 10

   b) Write technical specifications on following interfacing techniques: 10

      i. USB
      ii. Firewire
      iii. Infiniband
      iv. Fiber-channel

   c) Differentiate between DVI and HDMI. 5