Lec-11

Programmal → Performed by processing

Polling   Interrupt driven

DMA ─→ i) Overhead to processor (frees the processor of
          D-T   pr mem.)
       ii) Perform co-ordinated by DMA controller.
  Q1   iii) Avoids low speed when moving large amount data
       iv) Avoids bottleneck of having to channel data
                    through processor

       cons → µP is unable to use buses temporarily.

Questions:- i) Faster processing (improvements of DMA)
       ⊛ ii) Block Diagram
         iii) HOLD / HCLA
         iv) Polling vs Interrupt vs DMA I/O
          v) Mem-Read , I/o write I/o Read and M-write
                    used simultaneously
         ⨉ Regist Names of DMA

  Q1 (continued) for typical µp data transfer require
per byte (5-10) µs between RAM and I/O. Inadequate for
     high speed aps. For DMA 1 µs /per byte.

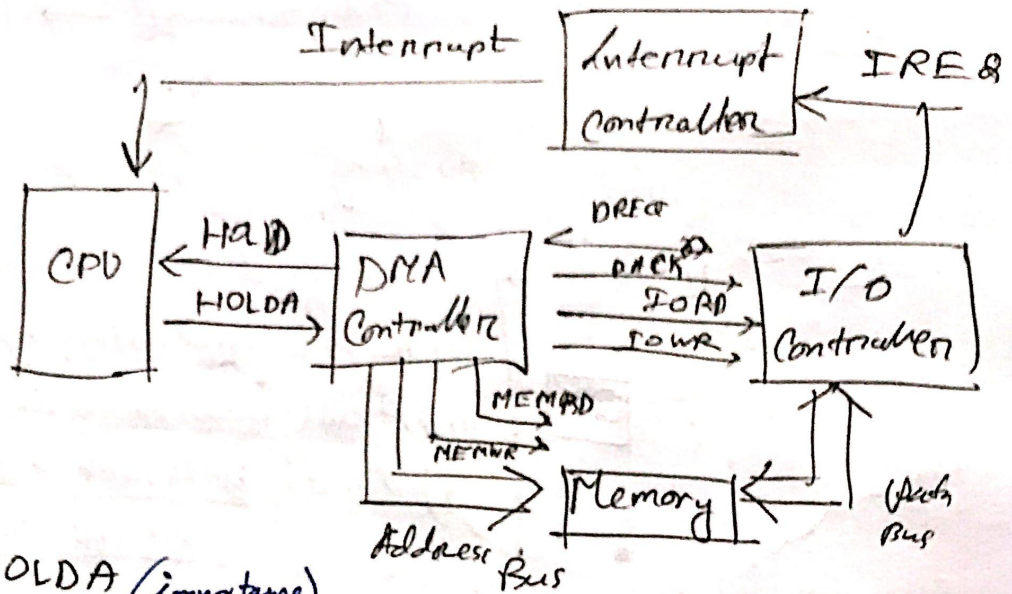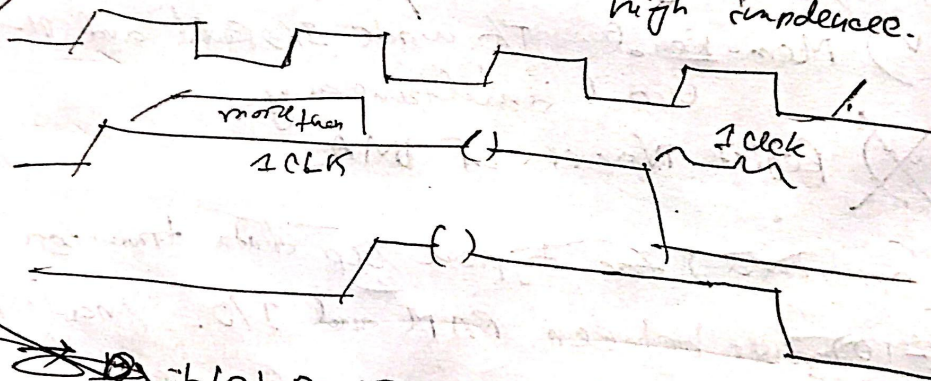| Q4	Polling	Interrupt	DMA
⇒ processor asks I/o device to transfer in a loop.	→ I/o device sends signal to processor if it wants to transfer, otherwise processor will do its work.	D.T between I/o and memory is done directly without aid of processor.
• Inefficient	• Better	• Best for large chunks of data

Q2

Interrupt   Interrupt   IRE8
                             Controller

          Hold
CPU ←————   DMA ————→ DREQ
          HOLDA   Controller ——→ DACK   I/O
     ————————→   ——→ IORD   Controller
                             ——→ IOWR

                        MEMRD
                        MEMWR ——→
                             Memory ←——————
          Address Bus   (Addr
                                          Bus

Q3   HOLD, HOLDA (importance)

HOLD → i) to Request DMA action, HOLD Logic-1 sent by DMA
                                                 controller.
     ii) µp responds - by suspending action.
          — placing data, adress, control bus at
                              high impedence.

          more than
          1 CLK   ( )   1 clock

              ( )

|HOLD   →   HOLD A   → DMA wants bus cycle.

          ii) sends HOLD ACK and grants bus.

Q4

	Advantages	Disadv
Polling	— Fastest Response — Simplest H/w	— Slowest (Speed) — Wasted Command (inefficient) (Efficiency)
Interrupt	— More efficient use of processor time.	— Delay in response time due to interrupt (interrupt latency) — Overhead due to interrupt processing (context switching) — Increased cost and complexity
DMA	— Most efficient, fastest DT Rate — Overhead to Processor, most efficient	— Need DMAC device — Highest Cost and complexity

Points to consider ⟶
- ✳ Response Time
- ✳ Speed
- ✳ Efficiency ⟶
- ✳ Cost and simplicity

H/w
- Interrupt Latency
- Context Switching

Write in this format

	Int	Polling	DMA
Defn:			
Pros:			
Cons:			

$\boxed{Q5}$ Mem-Road ~~#/~~ ~~write~~
fetches the data from memory
and writes in the I/O. [check vid]

Lec-12

a) Fibre Channel → (using Optical Fiber Cables)
- serial, high speed ~~data transfer protocol~~ multiple
  ~~network~~ connect PC to, I/O devices
  network
  Speed - billions of bits/second (Gbps)
       Interconnection of 126 devices only

b) Inti band
- serial ~~connect~~ bus that can ~~does~~ carry
  multiple channel of data

→

→ Network of high speeds links and switches.

	$\downarrow$ R	RF
	Cheaper~~s~~	
	Line of ~~of~~ Sight	No line of Sight
	Short distance	Long distance
	Diode emits infrared signal ~~detects~~	Frequency hopping,
	Infrared transistor	communicate while constantly
	detects signal.	changing transmission frequency

Isochronous is a special type of synchronous

Allows Jitter, ~~periodt~~ internal varies

→ In synchronous commu. the internal is fixed.

High transfer rate, the internal is <u>reduced</u>.

Low transfer rate " " " <u>increared</u>.