Islamic University of Technology

EEE 4483
Digital Electronics & Pulse Techniques

Lecture- 5

Analog-to-Digital Converters
Digital-to-Analog Converters

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555 Timer Syllabus from the Book of Floyd

Digital Fundamentals – Floyd Thomas – Prentice Hall (2007)

Section No. 7-6 (Page No. 404 - 409) (DjVu Page No. 418-424)

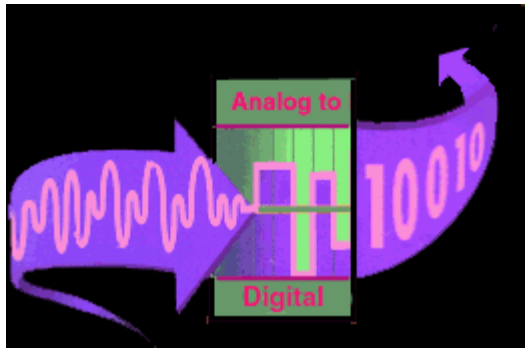
Exercise Problem **29, 30, 31** – (Page No. 420) (DjVu Page No. 435)

Data Converters: Basic Concepts

- Analog signals are continuous, with infinite values in a given range.
- Digital signals have discrete values such as `on/off` or `0/1`.
- Limitations of analog signals
  - Analog signals pick up noise as they are being amplified.
  - Analog signals are difficult to store.
  - Analog systems are more expensive in relation to digital systems.

Data Converters: Basic Concepts

- Advantages of digital systems (signals)
  - Noise can be reduced by converting analog signals in 0s and 1s.
  - Binary signals of `0s/1s` can be easily stored in memory.
  - Technology for fabricating digital systems has become so advanced that they can be produced at low cost.
- The major limitation of a digital system is how accurately it represents the analog signals after conversion.

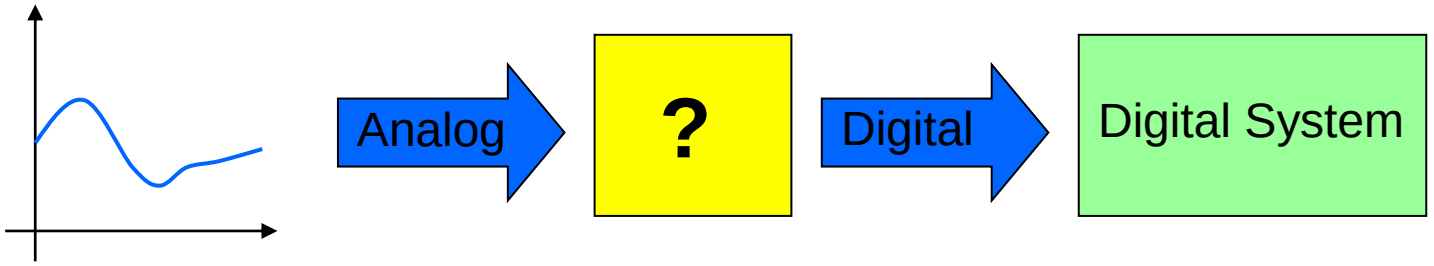


Analog to Digital Conversion

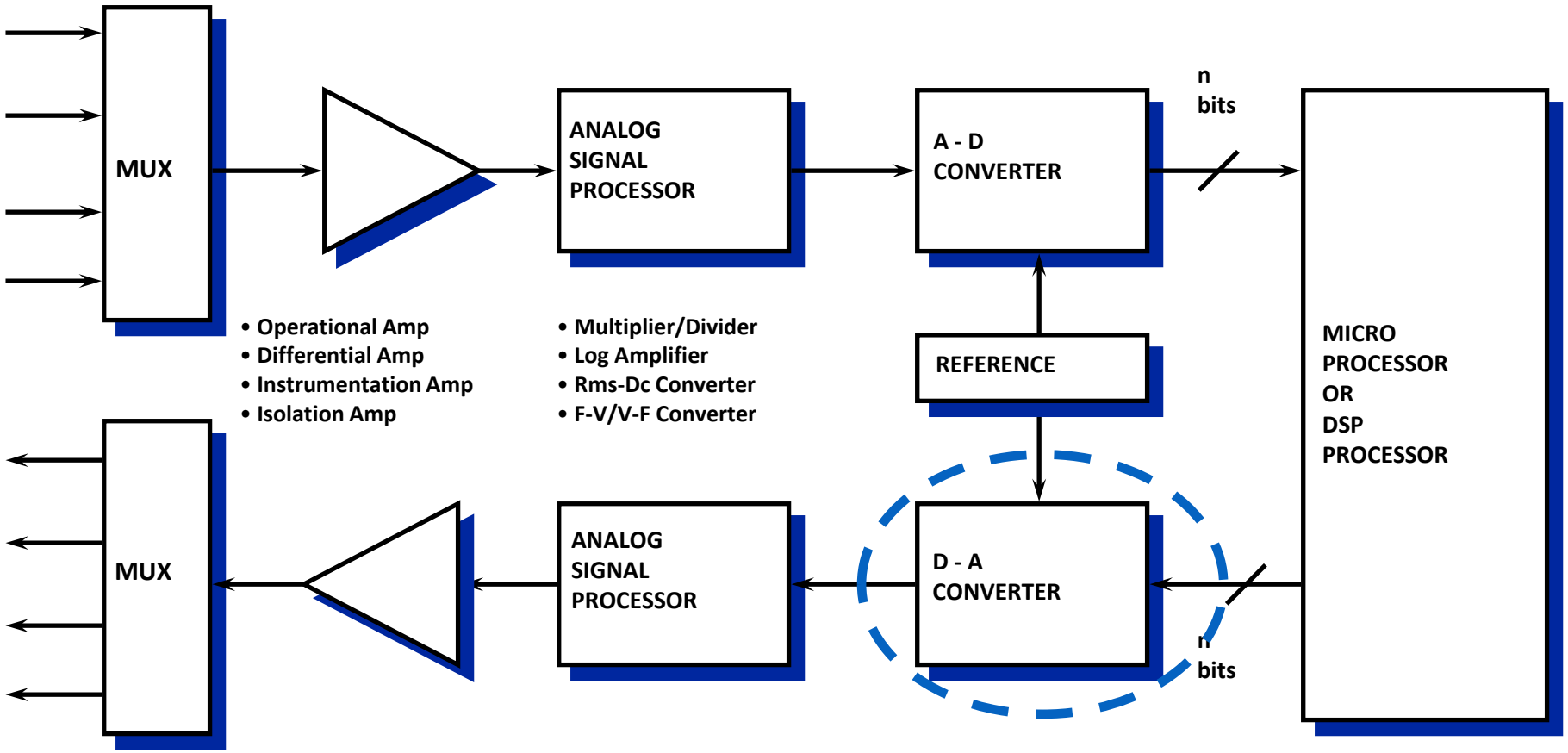
ADC

Analog to Digital Conversion

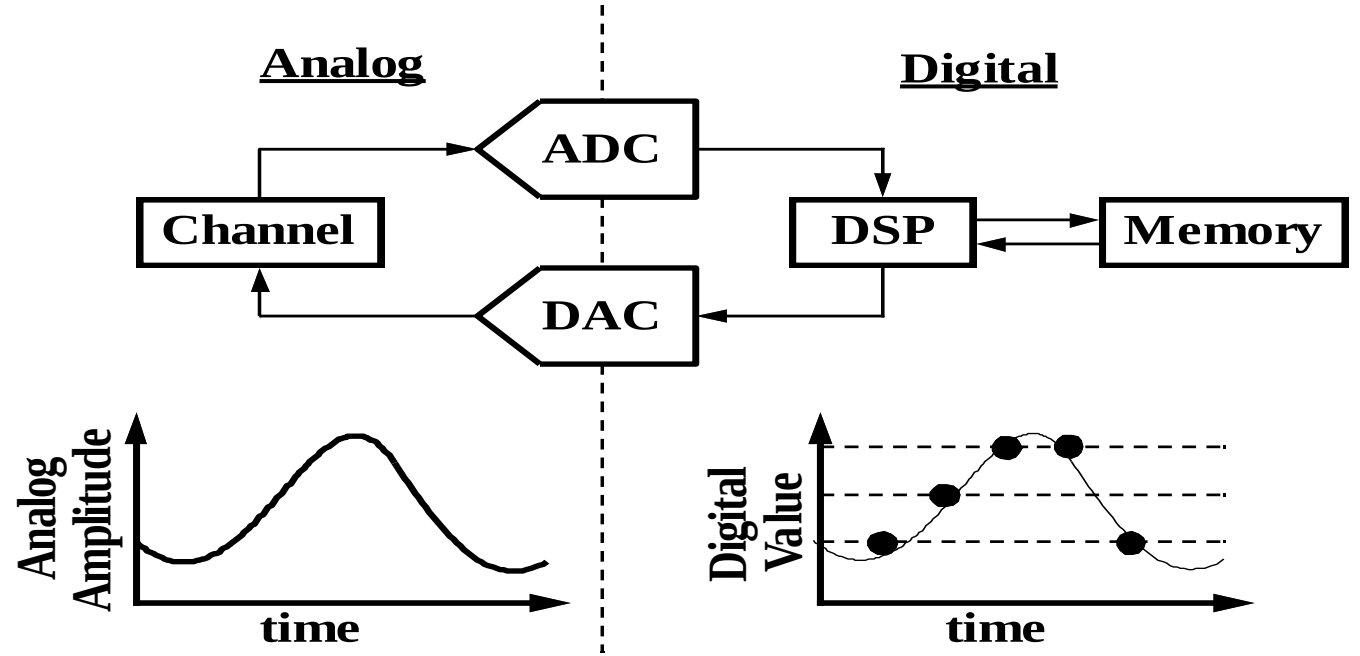
A digital signal is superior to an analog signal because it is more robust to noise and can easily be recovered, corrected and amplified. For this reason, the tendency today is to change an analog signal to digital data. In this section we describe two techniques, pulse code modulation and delta modulation.



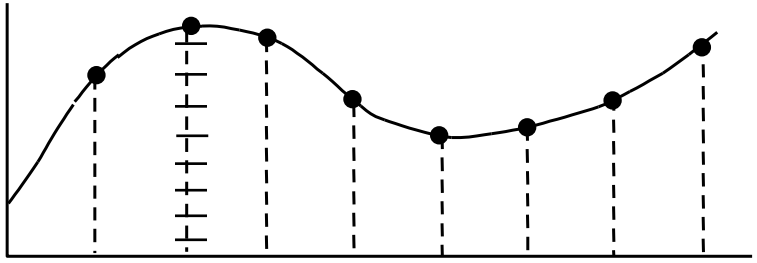
Digital to Analog Converters



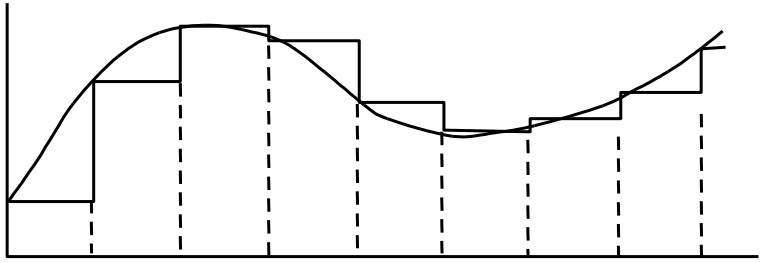
“Real World” Sampled Data Systems Consist Of ADCs and DACs



ADC SAMPLED AND QUANTIZED WAVEFORM

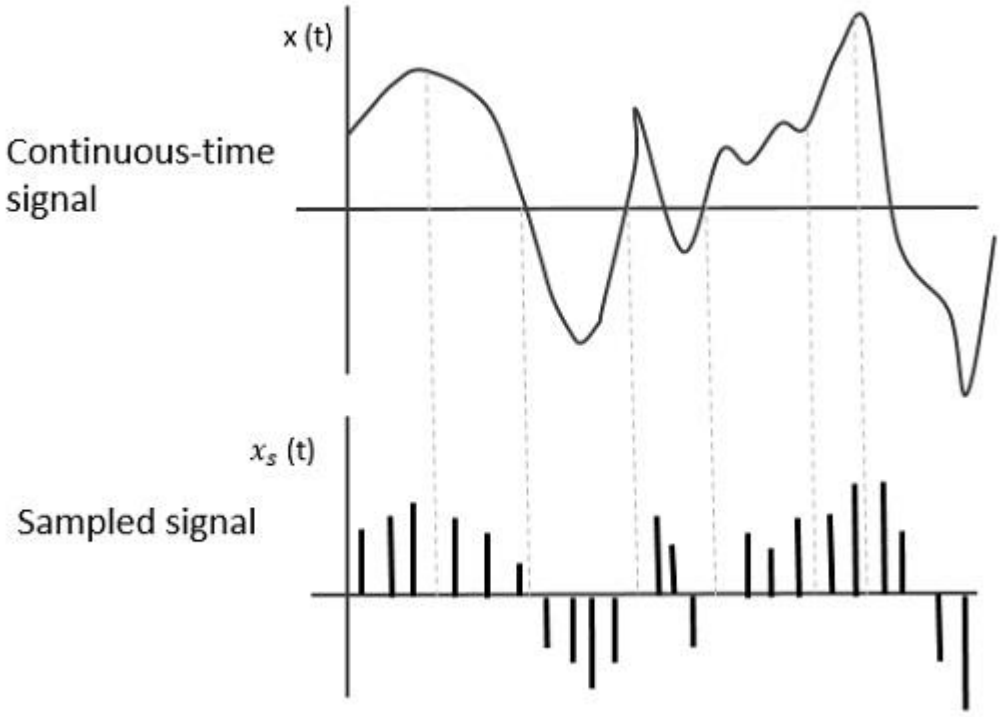


DAC RECONSTRUCTED WAVEFORM



Sampling

An input signal is converted from some continuously varying physical value (e.g. pressure in air, or frequency or wavelength of light), by some electro-mechanical device into a continuously varying electrical signal. This signal has a range of amplitude, and a range of frequencies that can present. This continuously varying electrical signal can then be converted to a *sequence* of digital values, called samples, by some analog to digital conversion circuit.



Nyquist's Sampling theorem

A theorem, developed by H. Nyquist, which states that an analog signal waveform may be uniquely reconstructed, without error, from samples taken at equal time intervals. The sampling rate must be equal to, or greater than, twice the highest frequency component in the analog signal.

A bandlimited signal can be reconstructed exactly if it is sampled at a rate atleast twice the maximum frequency component in it.

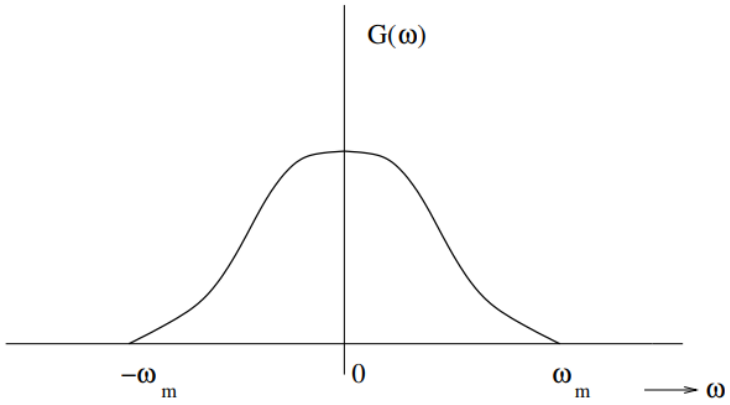
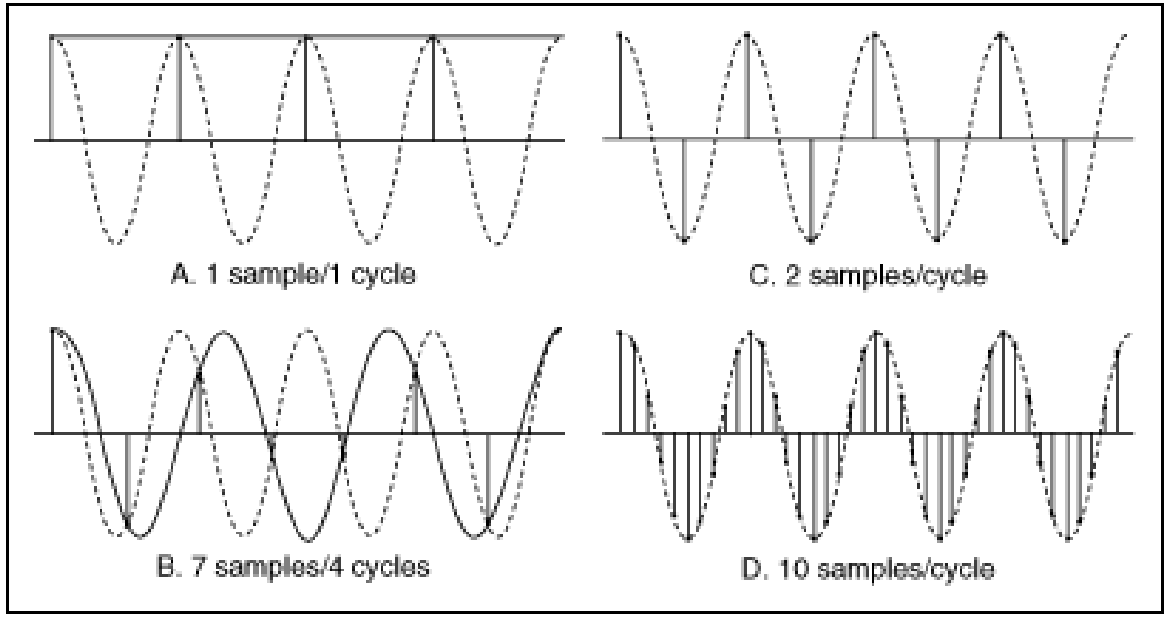


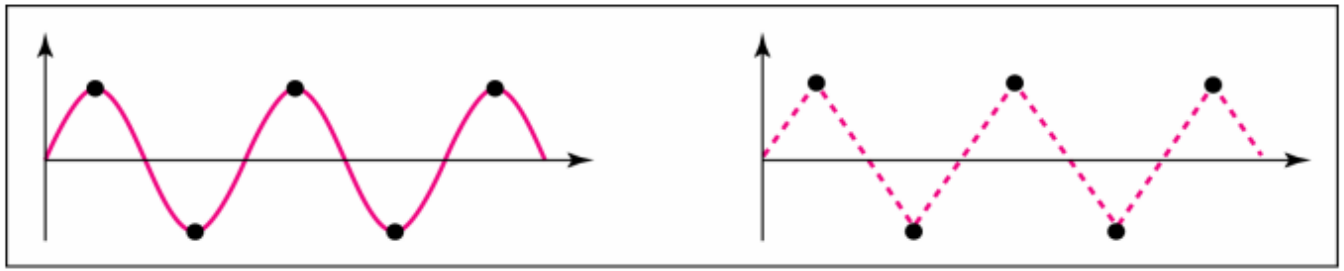
Figure 1: Spectrum of bandlimited signal $g(t)$

The maximum frequency component of g(t) is fm. To recover the signal g(t) exactly from its samples it has to be sampled at a rate $f_s \geq 2f_m$ .The minimum required sampling rate $f_s = 2f_m$ is called Nyquist rate.

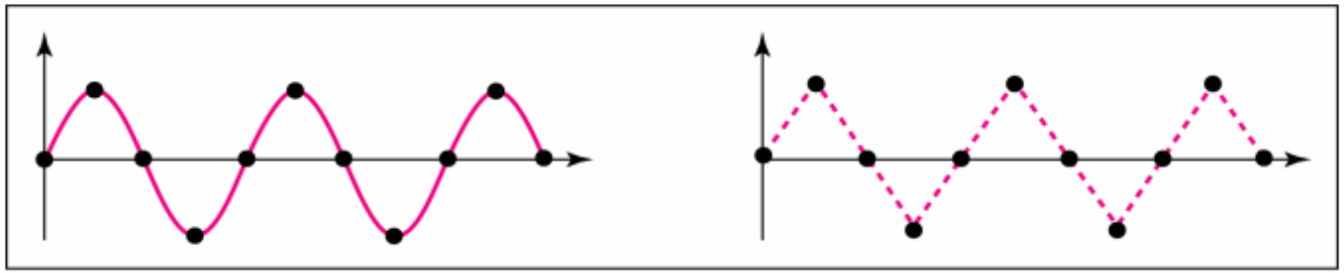
Nyquist's Sampling theorem : continued ..



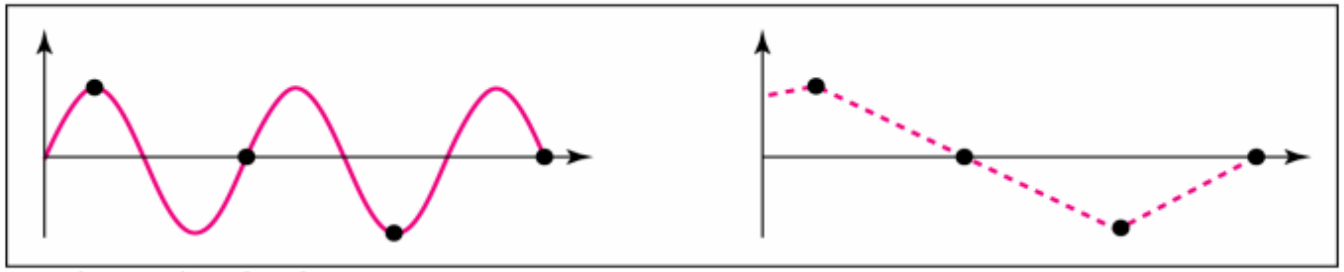
Nyquist's Sampling theorem : continued ..



a. Nyquist rate sampling: $f_s = 2\,f$



b. Oversampling: $f_s = 4\,f$



c. Undersampling: $f_s = f$

Sampling : continued ..

Sampling Rate

To discretize the signals, the gap between the samples should be fixed. That gap can be termed as a sampling period T_S.

Sampling Frequency = $^1/_{T_S} = f_S$

Where,

T_S is the sampling time

f_S is the sampling frequency or the sampling rate

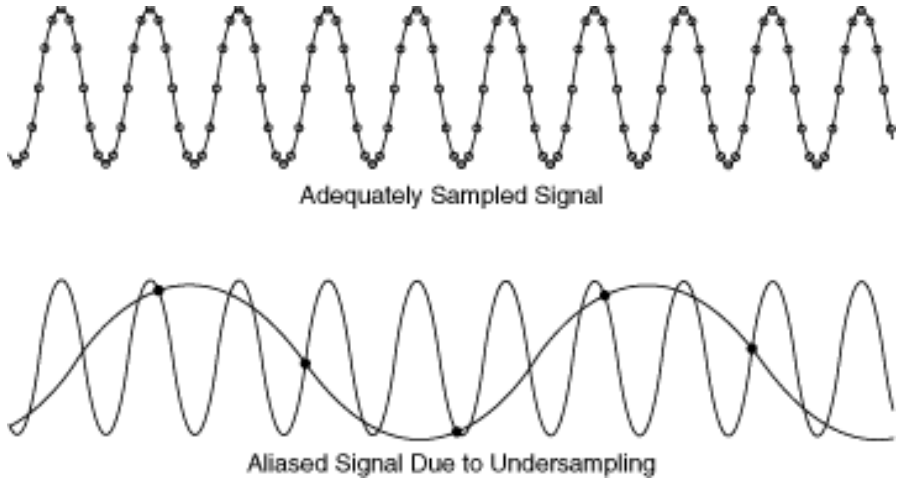
Sampling frequency is the reciprocal of the sampling period. This sampling frequency, can be simply called as Sampling rate. The sampling rate denotes the number of samples taken per second, or for a finite set of values.

For an analog signal to be reconstructed from the digitized signal, the sampling rate should be highly considered. The rate of sampling should be such that the data in the message signal should neither be lost nor it should get over-lapped. Hence, a rate was fixed for this, called as **Nyquist rate**.

Aliasing

Aliasing occurs when a system is measured at an insufficient sampling rate.

An aliased signal provides a poor representation of the analog signal. Aliasing causes a false lower frequency component to appear in the sampled data of a signal. The following figure shows an adequately sampled signal and an undersampled signal.



In the figure, the inadequately sampled signal appears to have a lower frequency than the actual signal—two cycles instead of ten cycles.

Increasing the sampling frequency increases the number of data points acquired in a given time period. Often, a fast sampling frequency provides a better representation of the original signal than a slower sampling frequency.

For a given sampling frequency, the maximum frequency you can accurately represent without aliasing is the **Nyquist frequency.**

Aliasing : continued ..

Analog filtering to reduce aliasing

To reduce the effects of aliasing when sampling analog signals, analog filtering must first be used to reduce the higher frequencies. Data sampled for process control use will typically have a first order analog RC (resistor-capacitor) filter. For a first order analog filter, a filter time constant at least 3 times the sample interval is often appropriate for reducing aliasing in a diagnostic system. The required analog filtering is called an anti-aliasing filter.

- ✓ The anti aliasing filter is a LPF (Low Pass Filter).
- ✓ Its goal is to eliminate, before sampling, all frequencies in the signal that are, at least , above the Nyquist frequency and therefore avoid aliasing.
- ✓ Note that filtering the original signal cause, of course, losing data from the original signal, but it ensures good reconstruction of the filtered signal.

What is Resolution??

Let $n = 2$

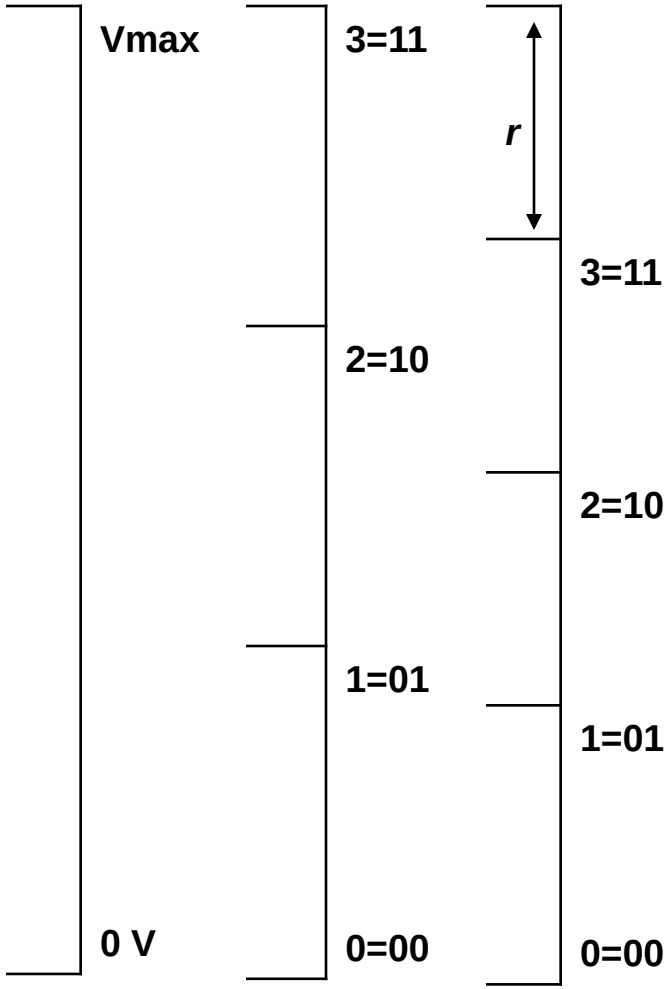
M = $2^n - 1$

3 steps on the digital scale
d_0 = 0 = `0b00 (binary)`
d_{Vmax} = 3 = `0b11 (binary)`

M = 2^n

4 steps on the digital scale
d_0 = 0 = `0b00`
$d_{Vmax - r}$ = 3 = `0b11` (no d_{Vmax})

***r*, resolution**: smallest analog change resulting from changing one bit

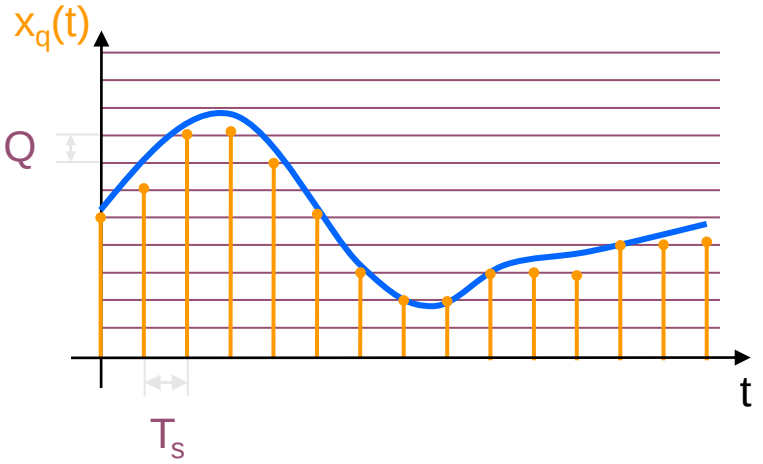


Accuracy

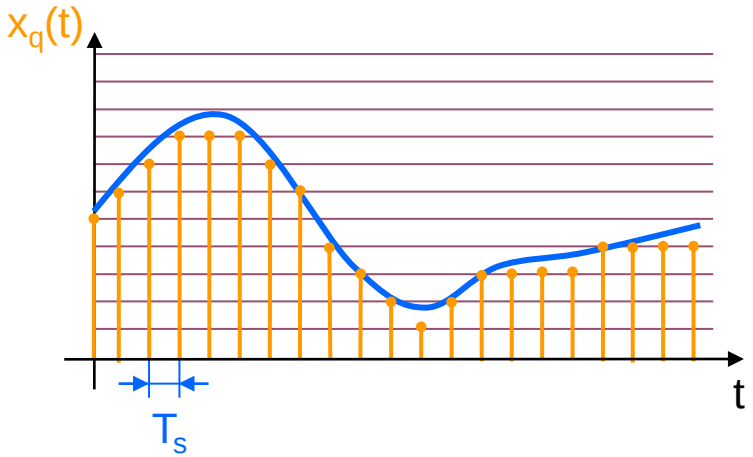
The accuracy of an ADC can be improved by increasing:

- The sampling rate (T_s)
- The resolution (Q)

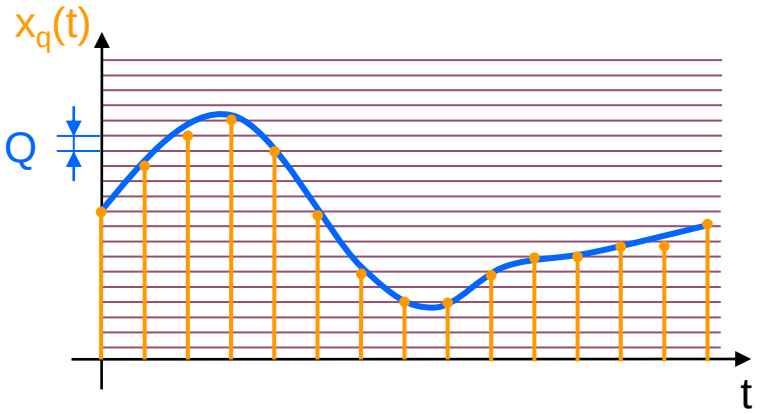
Accuracy : continued..



Higher Sampling rate

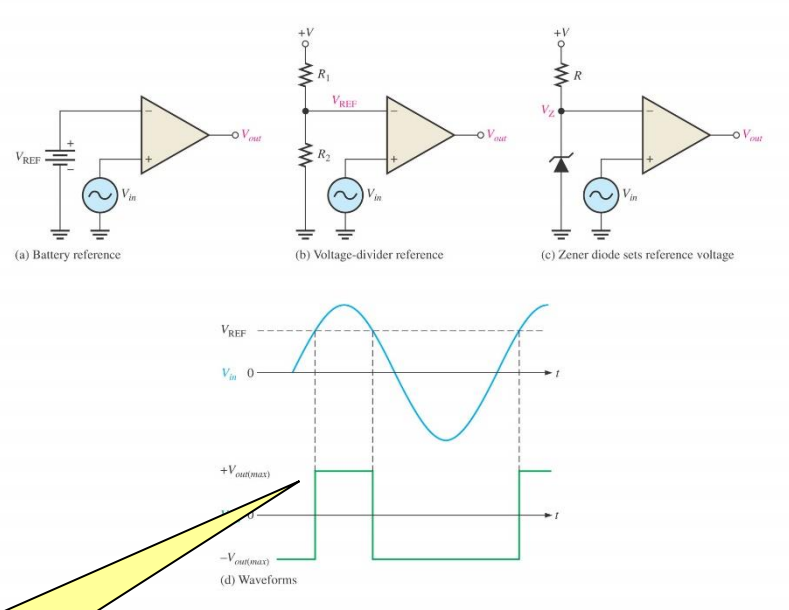


Higher Resolution



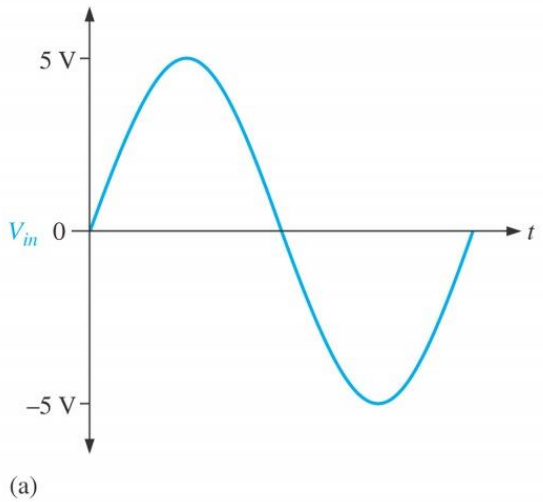
Comparators

- Determines which input is larger
- A small difference between inputs results maximum output voltage (high gain)
- Zero-level detection
- Non-zero-level detection

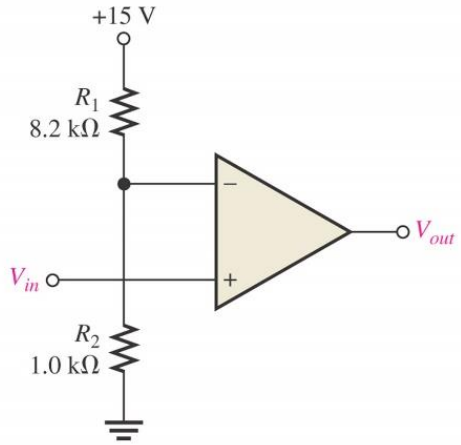


Max and minimum

Comparators : Example

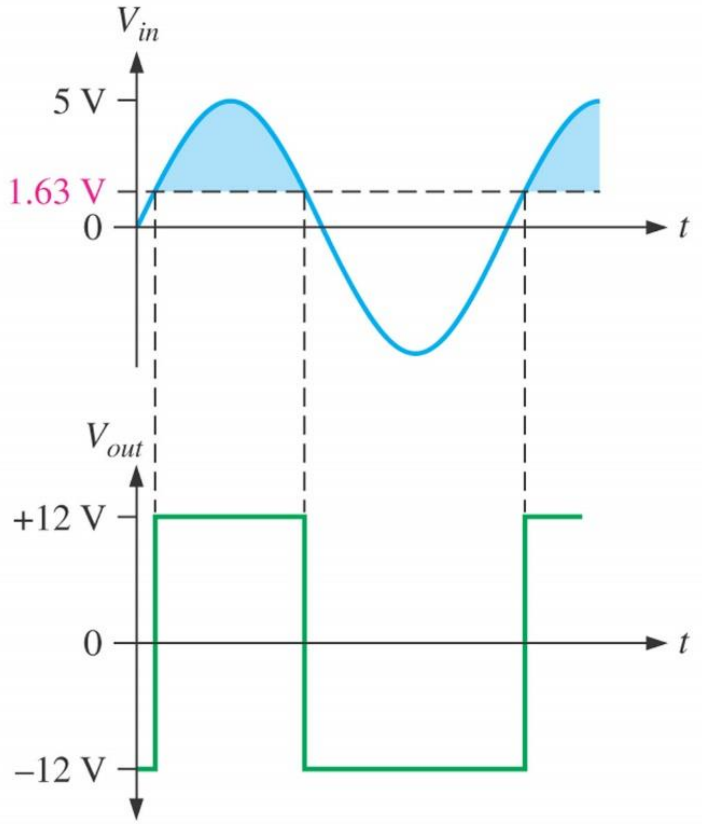


(a)



(b)

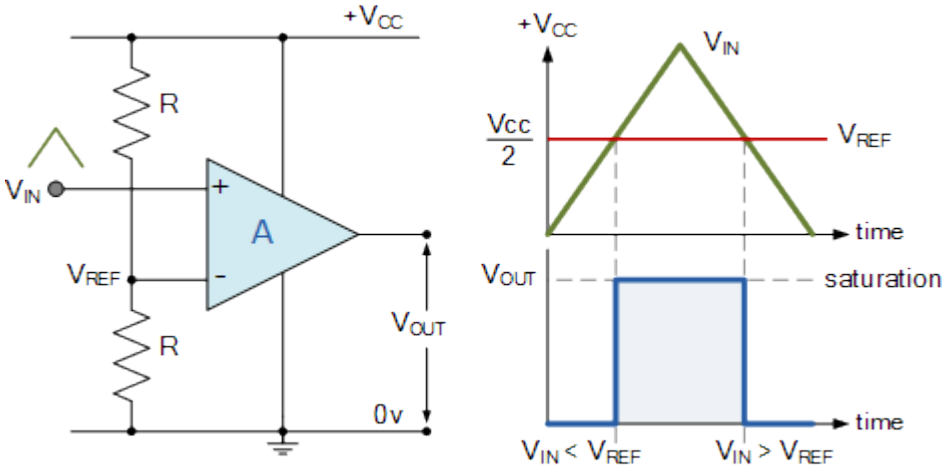
$$V_{ref} = V_{in}(max) \times \frac{R2}{R1 + R2} = 1.63\ V$$



Positive Voltage Comparators : Continued ..

In this non-inverting configuration, the reference voltage is connected to the inverting input of the operational amplifier with the input signal connected to the non-inverting input. To keep things simple, we have assumed that the two resistors forming the potential divider network are equal and: R1 = R2 = R. This will produce a fixed reference voltage which is one half that of the supply voltage, that is $V_{CC}/2$, while the input voltage is variable from zero to the supply voltage.

When V_{IN} is greater than V_{REF}, the op-amp comparators output will saturate towards the positive supply rail, V_{CC}. When V_{IN} is less than V_{REF} the op-amp comparators output will change state and saturate at the negative supply rail, 0v as shown

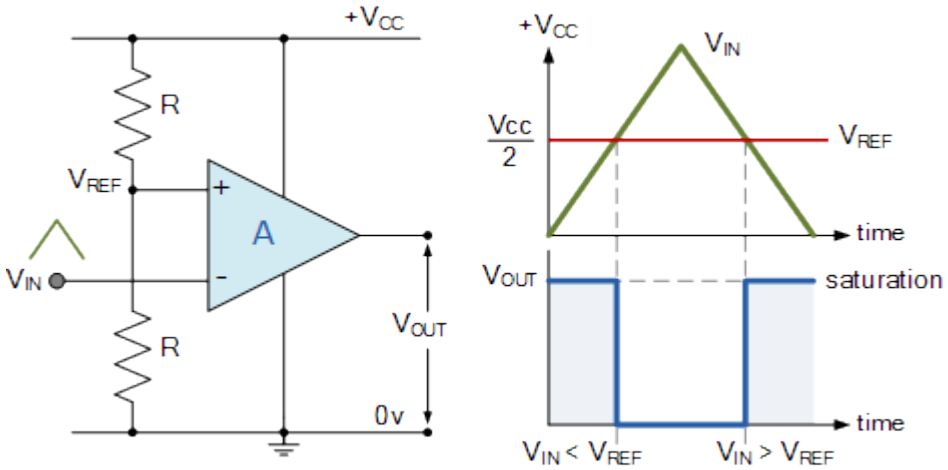


Negative Voltage Comparators : Continued ..

The basic configuration for the negative voltage comparator, also known as an inverting comparator circuit detects when the input signal, V_{IN} is BELOW or more negative than the reference voltage, V_{REF} producing an output at V_{OUT} which is HIGH as shown.

In the inverting configuration, the reference voltage is connected to the non-inverting input of the operational amplifier while the input signal is connected to the inverting input. Then when V_{IN} is less than V_{REF} the Op-amp comparators output will saturate towards the positive supply rail, V_{CC}.

Likewise the reverse is true, when V_{IN} is greater than V_{REF}, the op-amp comparators output will change state and saturate towards the negative supply rail, $0V$.



PCM

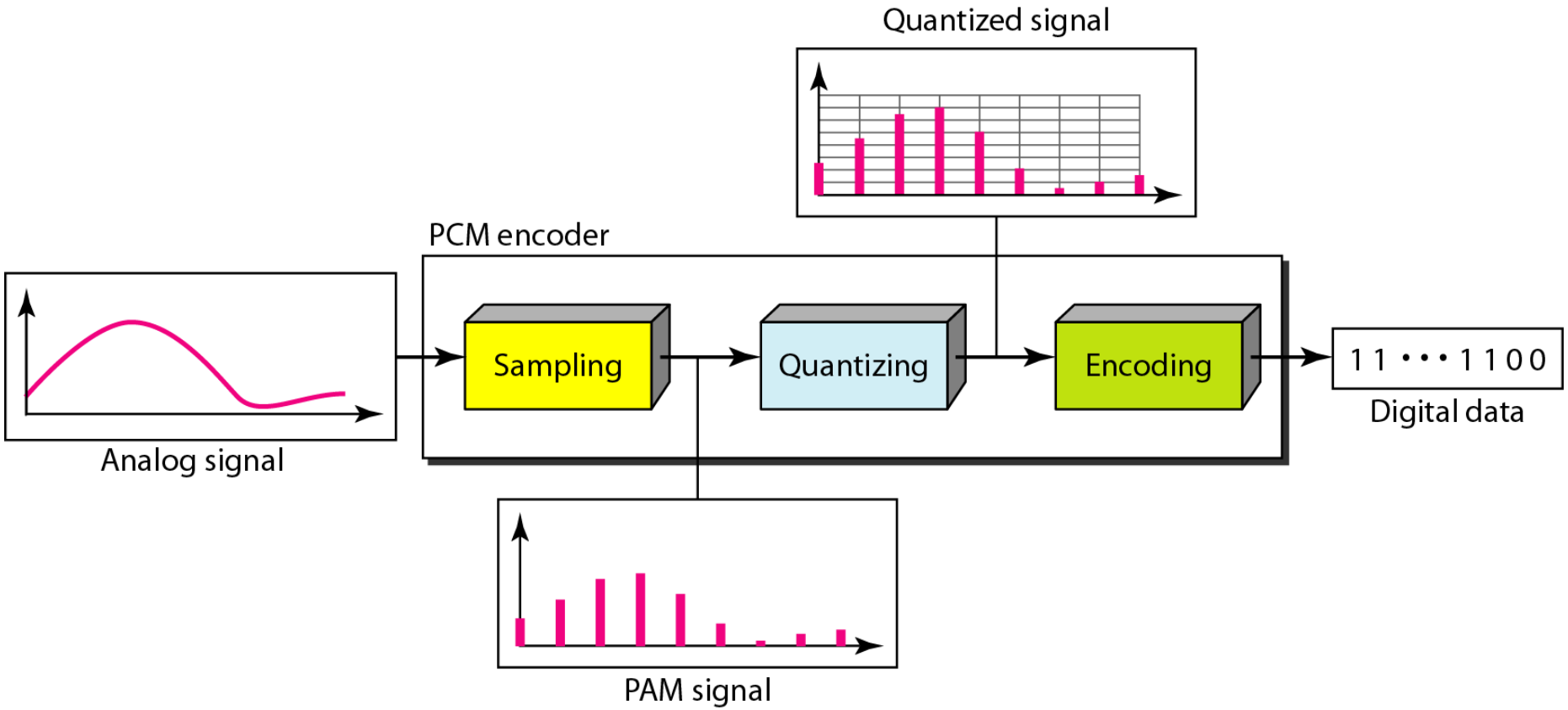
Pulse code modulation (PCM) is a digital representation of an analog signal that takes samples of the amplitude of the analog signal at regular intervals. The sampled analog data is changed to, and then represented by, binary data. PCM requires a very accurate clock. The number of samples per second, ranging from 8,000 to 192,000, is usually several times the maximum frequency of the analog waveform in Hertz (Hz), or cycles per second, which ranges from 8 to 192 KHz.

PCM consists of three steps to digitize an analog signal:

1. Sampling
2. Quantization
3. Binary encoding

- Before we sample, we have to filter the signal to limit the maximum frequency of the signal as it affects the sampling rate.
- Filtering should ensure that we do not distort the signal, ie remove high frequency components that affect the signal shape.

Components of PCM Encoder

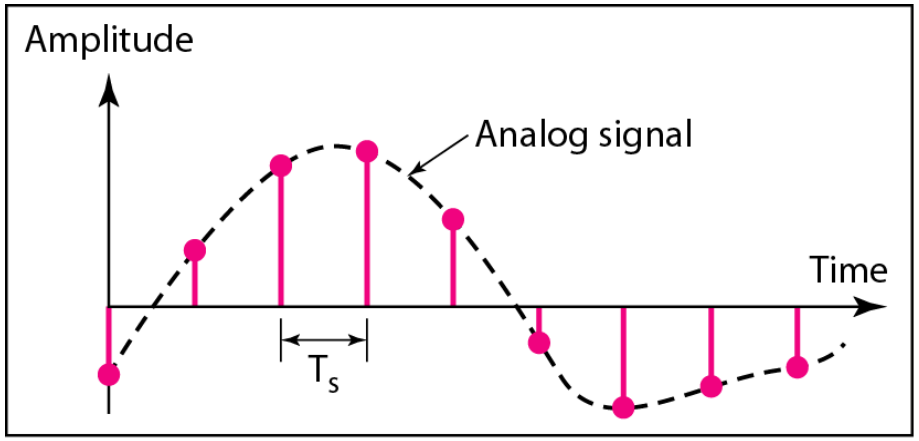


PCM Sampling Methods

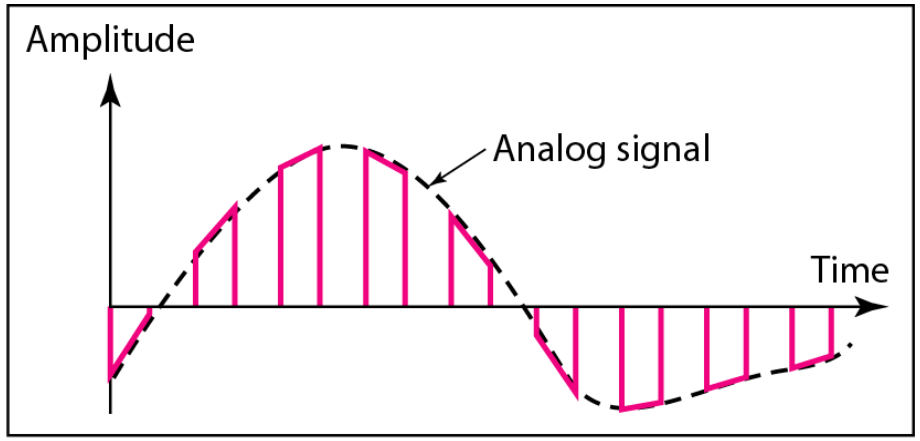
There are 3 sampling methods:

- **Ideal** - an impulse at each sampling instant
- **Natural** - a pulse of short width with varying amplitude
- **Flattop** - sample and hold, like natural but with single amplitude value

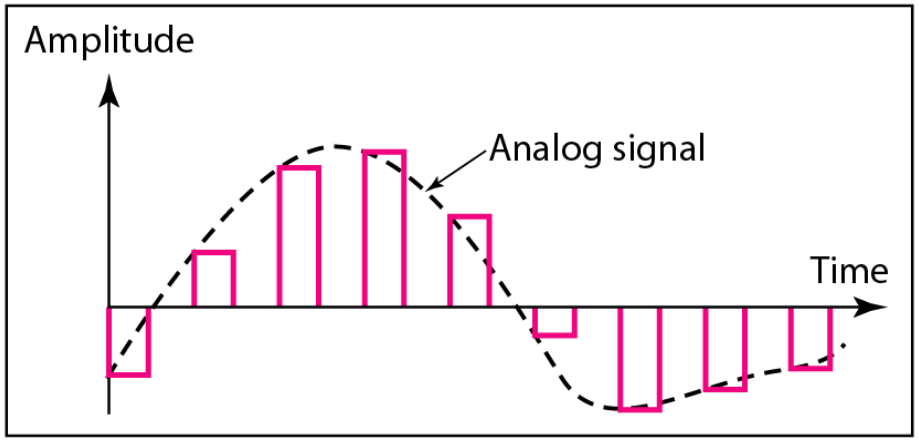
Three different methods for PCM



a. Ideal sampling



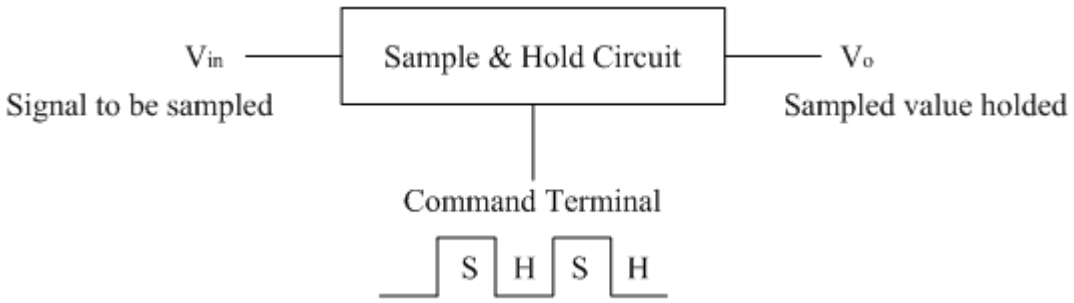
b. Natural sampling

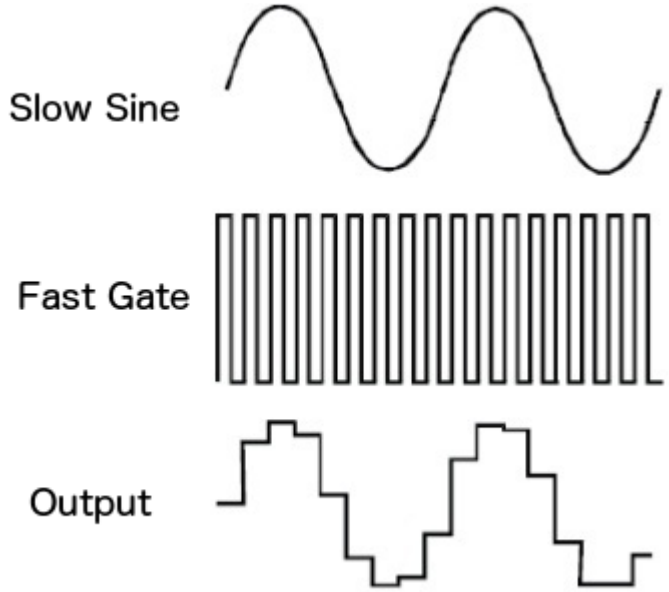


c. Flat-top sampling

Sample and Hold (S/H) Circuit

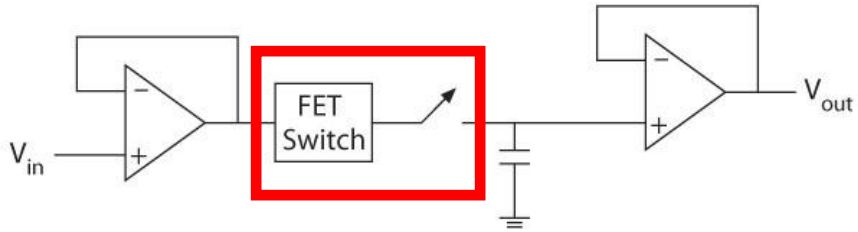
Sample & Hold Circuit is used to sample the given input signal and to hold the sampled value. Sample and hold circuit is used to sample an analog signal for a short interval of time in the range of `1` to `10 µs` and to hold on its last sampled value until the input signal is sampled again. The holding period may be from a few milliseconds to several seconds.





Sample and Hold Circuit : Continued ..

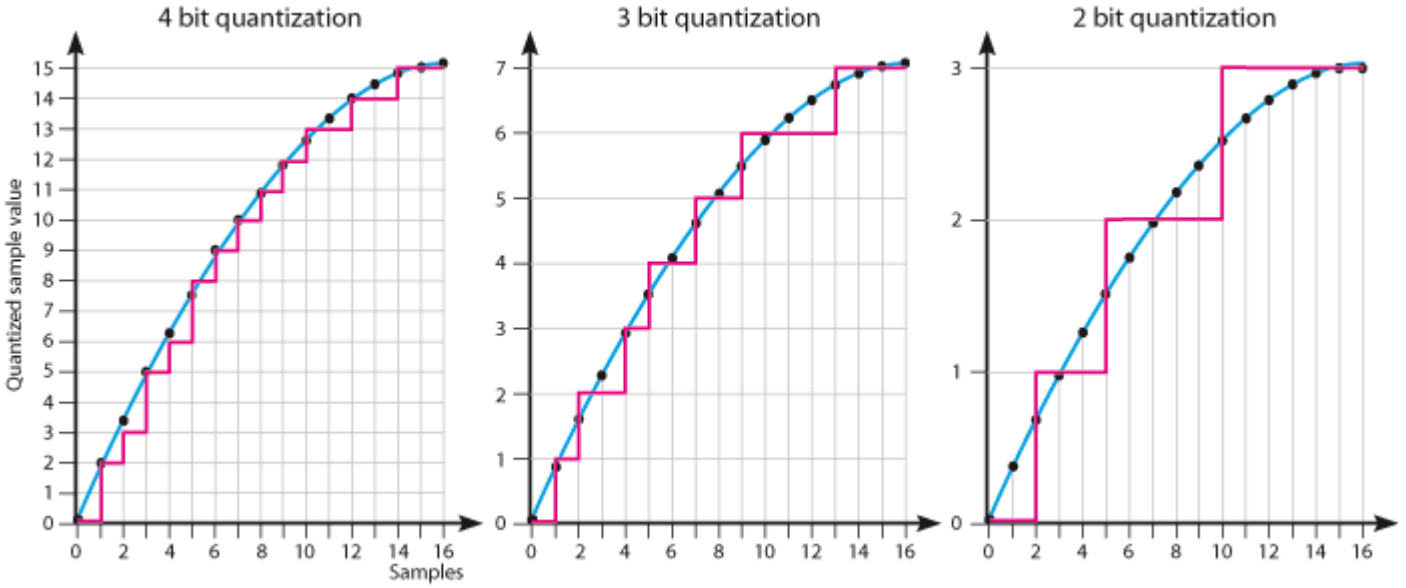
- If the input voltage to an A/D converter is variable, the digital output is likely to be unreliable and unstable. Therefore, the varying voltage source is connected to the ADC through a sample and hold circuit.



- Basic Operation:
  - When the switch is connected, it samples the input voltage.
  - When the switch is open, it holds the sampled voltage by charging the capacitor.
  - Acquisition time: time to charge the capacitor after the switch is open and settle the output.

Quantization

There are two factors which determine the accuracy with which the digital sequence of values captures the original continuous signal: the maximum rate at which we sample, and the number of bits used in each sample. This latter value is known as the quantization level.



This graph represents sampling and quantization. The blue curve is the input analog waveform, the black dots are the samples, and the red curve is the quantized output. The result is one n-bit number per sample.

Quantization: continued ..

- Sampling results in a series of pulses of varying amplitude values ranging between two limits: a `min` and a `max`.
- The amplitude values are infinite between the two limits.
- We need to map the *infinite* amplitude values onto a finite set of known values.
- This is achieved by dividing the distance between `min` and `max` into `L` zones, each of height Δ.

$$\Delta = (\text{max} - \text{min})/L$$

Quantization Levels

- The midpoint of each zone is assigned a value from `0` to `L-1` (resulting in L values)
- Each sample falling in a zone is then approximated to the value of the midpoint.

Quantization Zones

- Assume we have a voltage signal with amplitudes V_{min}=-20V and V_{max}=+20V.
- We want to use L = 8 quantization levels.
- Zone width Δ = (20 - -20)/8 = 5
- The 8 zones are: -20 to -15, -15 to -10, -10 to -5, -5 to 0, 0 to +5, +5 to +10, +10 to +15, +15 to +20
- The midpoints are: -17.5, -12.5, -7.5, -2.5, 2.5, 7.5, 12.5, 17.5

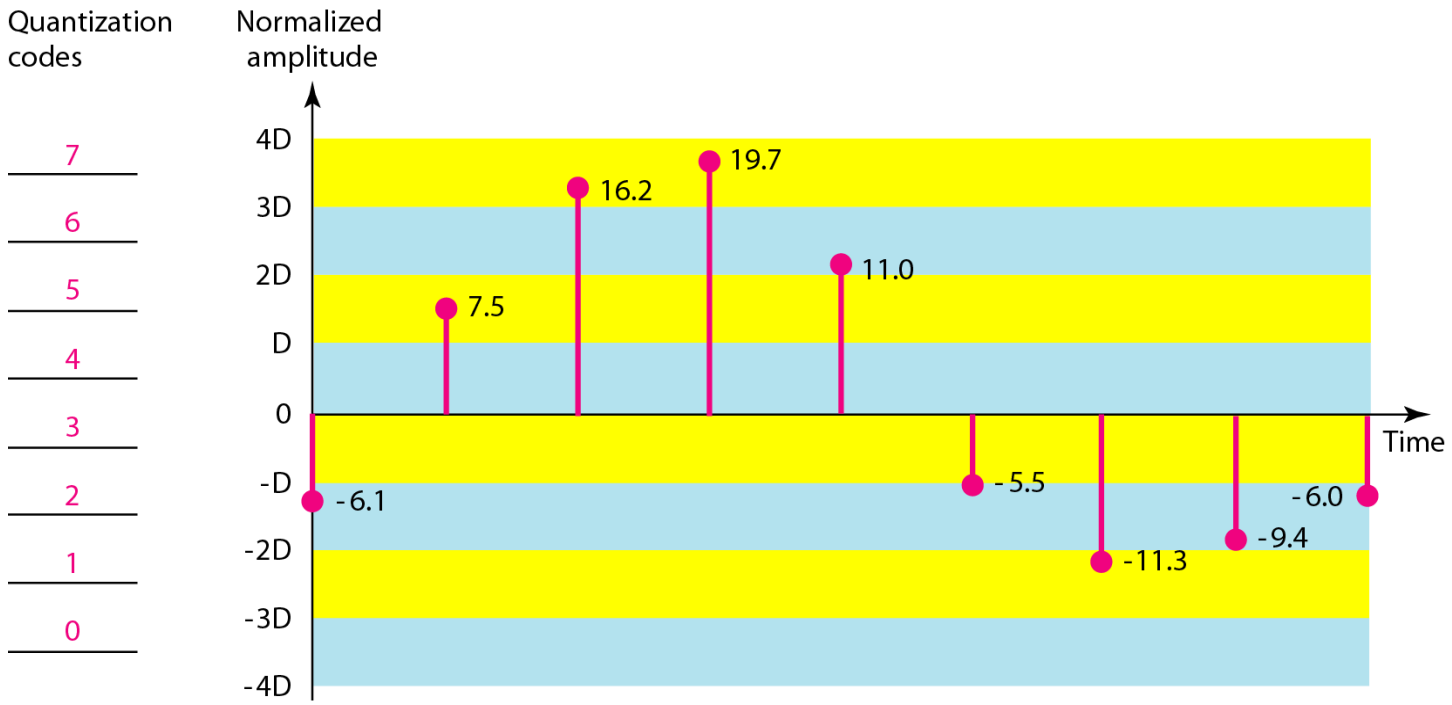
Assigning Codes to Zones

- Each zone is then assigned a binary code.
- The number of bits required to encode the zones, or the number of bits per sample as it is commonly referred to, is obtained as follows:

$$n_b = \log_2 L$$

- Given our example, $n_b = 3$
- The 8 zone (or level) codes are therefore: 000, 001, 010, 011, 100, 101, 110, and 111
- Assigning codes to zones:
  - 000 will refer to zone -20 to -15
  - 001 to zone -15 to -10, etc.

Quantization and Encoding of a sampled signal



Normalized PAM values	-1.22	1.50	3.24	3.94	2.20	-1.10	-2.26	-1.88	-1.20
Normalized quantized values	-1.50	1.50	3.50	3.50	2.50	-1.50	-2.50	-1.50	-1.50
Normalized error	-0.38	0	+0.26	-0.44	+0.30	-0.40	-0.24	+0.38	-0.30
Quantization code	2	5	7	7	6	2	1	2	2
Encoded words	010	101	111	111	110	010	001	010	010

A/D Examples

- Example 1
  - Assumes the input analog voltage is changing between 0–5 V.
  - Using a 3-bit A/D converter draw the output as the input signal ramps from 0 to 5 V.
  - Calculate the resolution.
  - What is the maximum possible voltage out? (this is called the full-scale output)
  - If the output is 10000000, what is the input?
- Example 2
  - Assumes the input analog voltage is changing between –5 to 5 V; using a 10-bit A/D converter.
  - Calculate the number of quantization levels.
  - Calculate the voltage resolution.

A/D Examples : Continued ..

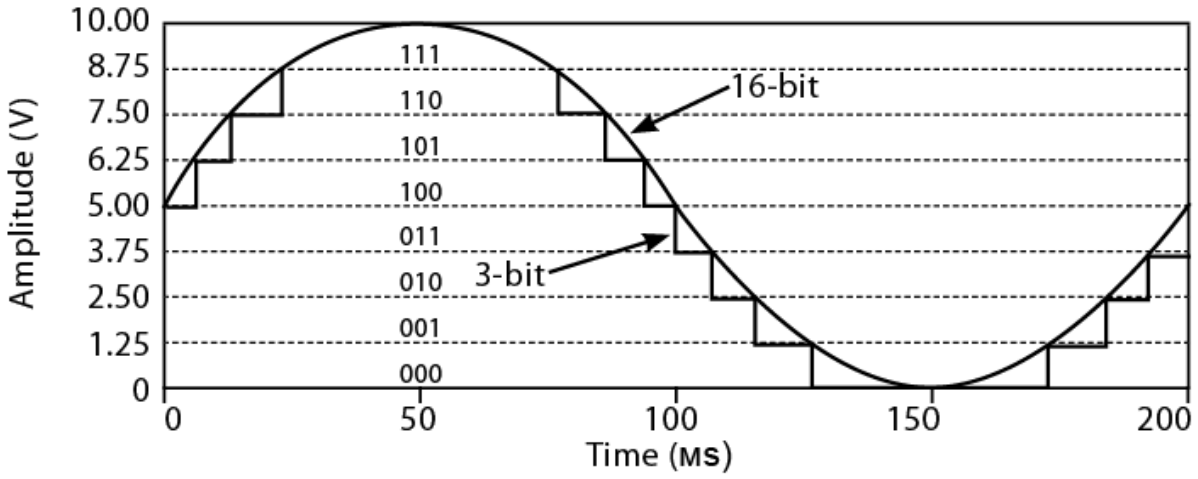
- Example 1
  - Assumes the input analog voltage is changing between 0-5 V.
  - Using a 3-bit A/D converter draw the output as the input signal ramps from 0 to 5V.
  - Calculate the resolution. 5- Resolution
  - What is the maximum possible voltage out? (this is called the full-scale output) 1 / 2^8 = 19.53 mV
  - If the output is 1000 0000, what is the input? MaxVolt / 2 = 2.5
- Example 2
  - Assumes the input analog voltage is changing between -5 to 5 V; using a 10-bit A/D converter.
  - Calculate the number of quantization levels. 2^10
  - Calculate the voltage resolution. 5-(-5)/1024 = 9.76 mV

Quantization Error

- When a signal is quantized, we introduce an error - the coded signal is an approximation of the actual amplitude value.
- The difference between actual and coded value (midpoint) is referred to as the quantization error.
- The more zones, the smaller Δ which results in smaller errors.
- BUT, the more zones the more bits required to encode the samples  higher bit rate

Quantization Error: Continued..

Quantization error is the difference between the analog signal and the closest available digital value at each sampling instant from the A/D converter. Quantization error also introduces noise, called quantization noise, to the sample signal. The higher the resolution of the A/D converter, the lower the quantization error and the smaller the quantization noise. The relationship between resolution (in bits) and quantization noise for an ideal A/D converter can be expressed as Signal to Noise `(S/N)= -20*log (1/2^n)` where n is the resolution of the A/D converter in bits. S/N is the signal to noise and is expressed in `dB`. This relationship can also be approximated as `S/N = 6*n`. Typical `S/N` ratios for ideal A/D converters are `96dB` for `16` bits, `72dB` for `12` bits, and `48dB` for `8` bits.



Quantization Error: Continued..

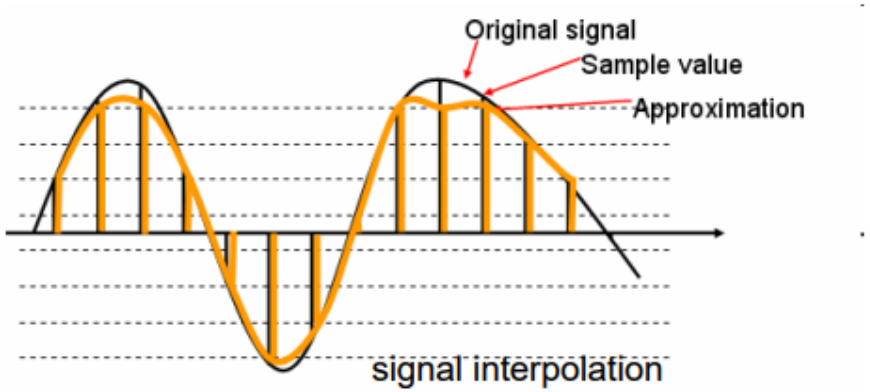
Quantization Error – **by quantizing the PAM signal, the original signal is now only approximated & cannot be 100% recovered**

- **effect known as quantizing error or quantizing noise**
- **SNR ratio due to quantizing noise can be expressed as**

$$\text{SNR [dB]} \approx 6m + 1.76 \text{ [dB]}$$

bits per sample

- **every additional bit used in quantizer will increase SNR by 6 [dB]**
  - **# of quantization levels ↑ ⇒ higher SNR ⇒ better (received) signal quality**



ADC Types

Can be classified in several groups:

- Flash ADC
- Sigma-delta ADC
- Dual slope converter
- Successive approximation converter

We will study Flash ADC and Successive Approximation converter!!

Flash:

- uses multiple comparators in parallel.
- The known signal is connected to one side of the comparator and the analog signal to be converted to the other side of the comparator.
- The output of the comparators provides the digital value.
- This is a high-speed, high cost converter.

Successive Approximation converter: Includes a D/A (digital to analog) converter and a comparator. An internal analog signal is generated by turning on successive bits in the D/A converter.

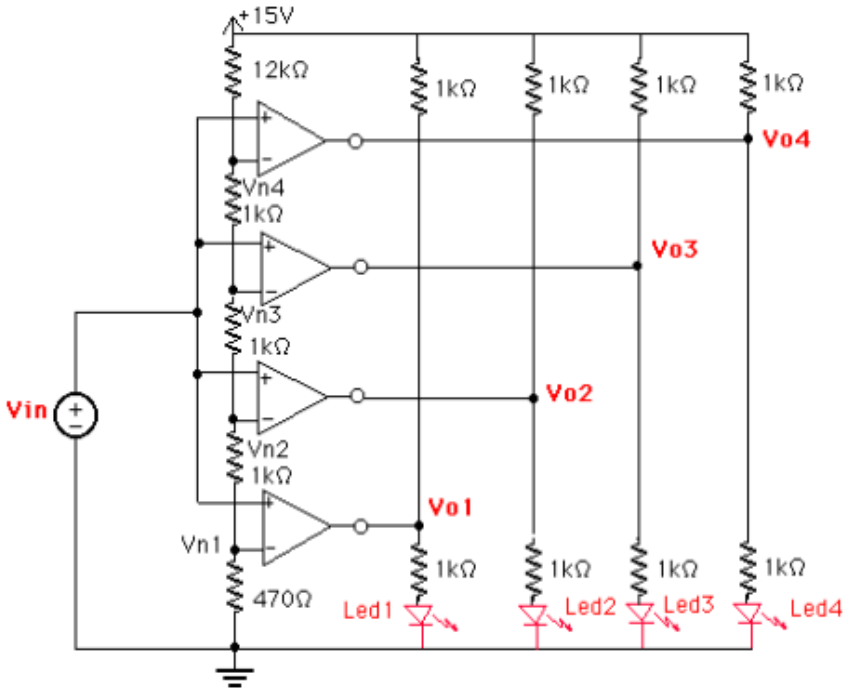
The SAR ADC does the following things for each sample:

- The analog signal is sampled and held.
- For each bit, the SAR logic outputs a binary code to the DAC that is dependent on the current bit under scrutiny and the previous bits
  already approximated. The comparator is used to determine the state of the current bit.
- Once all bits have been approximated, the digital approximation is output at the end of the conversion (EOC).

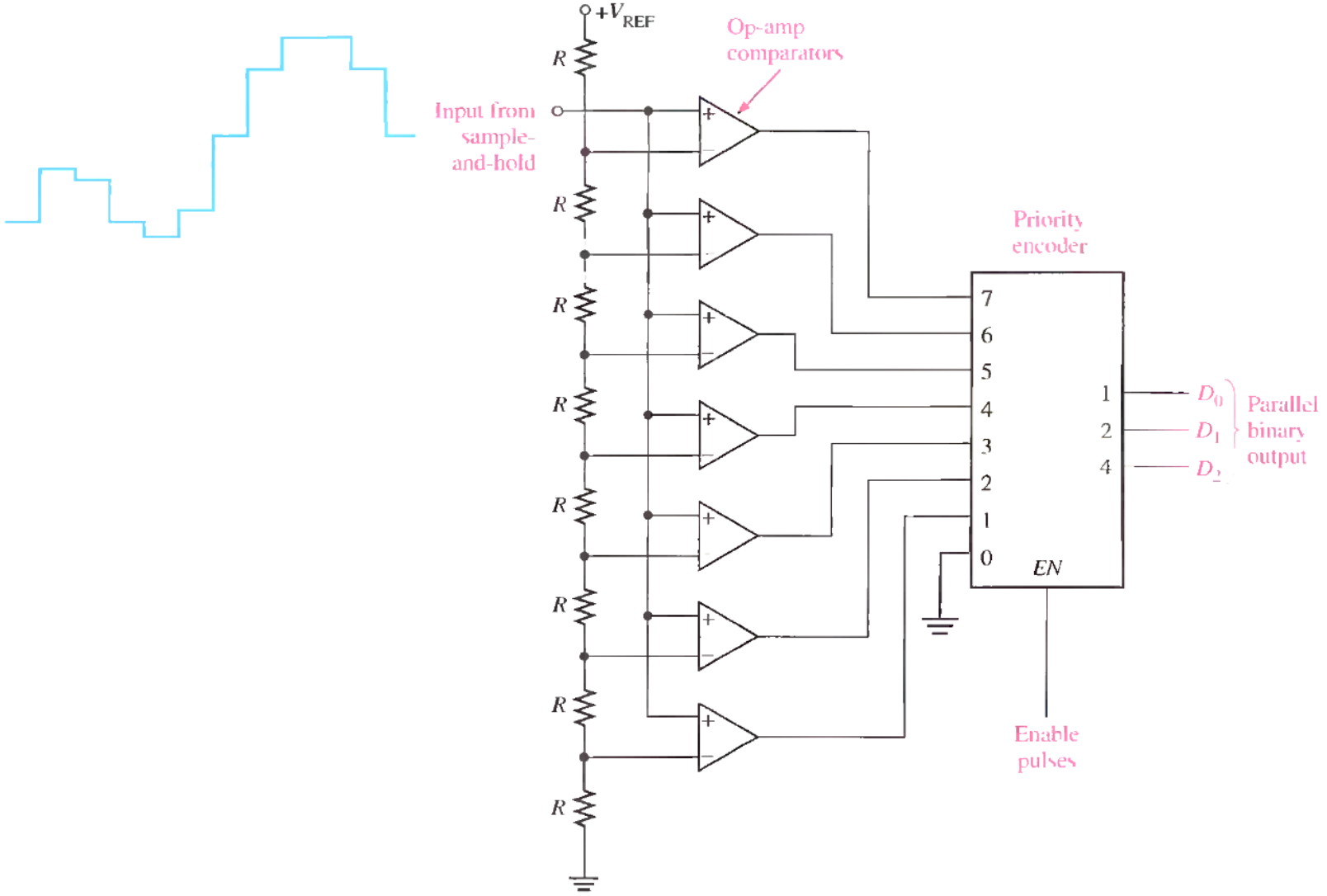
A/D Conversion: Flash

Watch on:

- Flash Converter
  - The circuit consists of 4 comparators whose inverting inputs are connected to a voltage divider.
  - A comparator is basically an operational amplifier used without feedback.
  - The outputs of the comparators correspond to a digital word.
  - When the input rises above `Vn1` , the first comparator will switch to a high output voltage causing the LED to light up, indicating a (`0001`).
  - For larger input voltages the output of other comparators will switch high as well. For large input voltages (above Vn3) all comparators will be high corresponding to (`1111`) digital output.



3-bit Flash ADC



Flash ADC : continued ..

Advantages	Disadvantages
• Very fast	• Needs many parts (255 comparators for 8-bit ADC) • Lower resolution • Expensive • Large power consumption

A/D Conversion: Successive Approximation

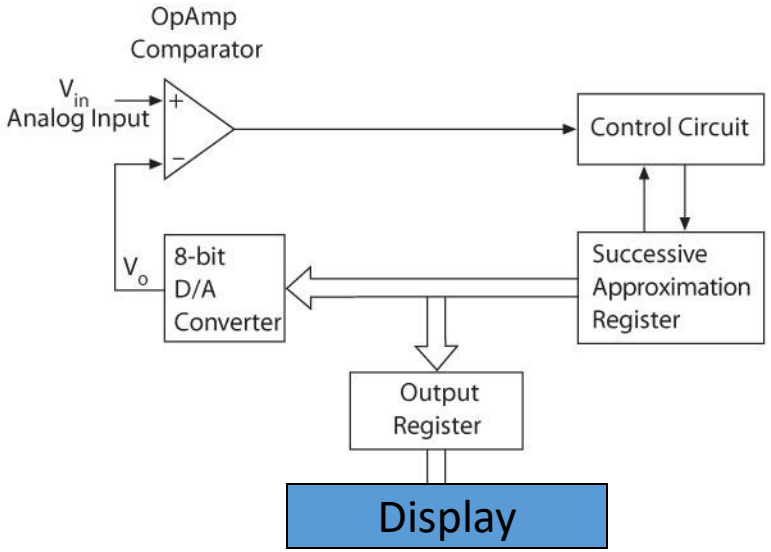
Successive Approximation type ADC is the most widely used and popular ADC method. The conversion time is maintained constant in successive approximation type ADC, and is proportional to the number of bits in the digital output, unlike the counter and continuous type A/D converters. The basic principle of this type of A/D converter is that the unknown analog input voltage is approximated against an n-bit digital value by trying one bit at a time, beginning with the MSB. The principle of successive approximation process for a 4-bit conversion. This type of ADC operates by successively dividing the voltage range by half.

Watch on:

YouTube

A/D Conversion: Successive Approximation

- The SAR (successive approximation register) begins by turning on the MSB Bit7.
- V_o of the D/A converter is compared with the analog input voltage V_{in} in the comparator.
- If analog voltage is less than the digital voltage, Bit7 is turned off and Bit6 is turned on.
- If analog voltage is greater than the digital voltage, Bit7 is kept on and Bit6 is turned on.
- The process of turning bit on/off is continued until Bit0.
- Now the 8-bit input to the D/A converter represents the digital equivalent of the analog signal V_{in}.



Bit 7 is set: b7=1
If Va < Vd → b7=0; b6=1
If Va > Vd → b7=1; b6=1
…..
If Va < Vd → b7=0; …b0=1
If Va > Vd → b7=1; … b0=1
Done

A/D and D/A Syllabus from the Book of Floyd

Digital Fundamentals – Floyd Thomas – Prentice Hall (2007)

Chapter – 13 (Page No. 744 - 757) (DjVu Page No. starting 759)

Digital to Analog Conversion (Page No. 768 - 775)

Self Study : Sigma-Delta Analog-to-Digital Converter (Page 758)

Digital to Analogue Conversion

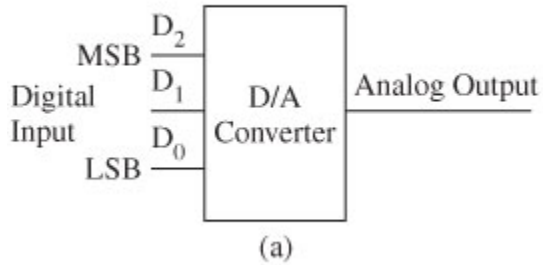
DAC

Digital to Analog (D/A, DAC) Conversion

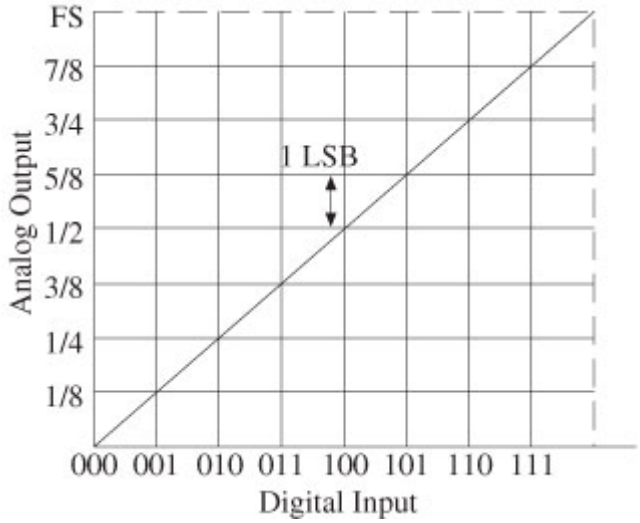
- Converting discrete signals into discrete analog values that represent the magnitude of the input signal compared to a standard or reference voltage
  - The output of the DAC is discrete analog steps.
  - By increasing the resolution (number of bits), the step size is reduced, and the output approximates a continuous analog signal.

Digital to Analog Conversion : continued

- The resolution of a DAC is defined in terms of bits—the same way as in ADC.
- The values of LSB, MSB, and full-scale voltages calculated the same way as in the ADC.
- The largest input signal `111` is equivalent of `7/8` of the full-scale analog value.

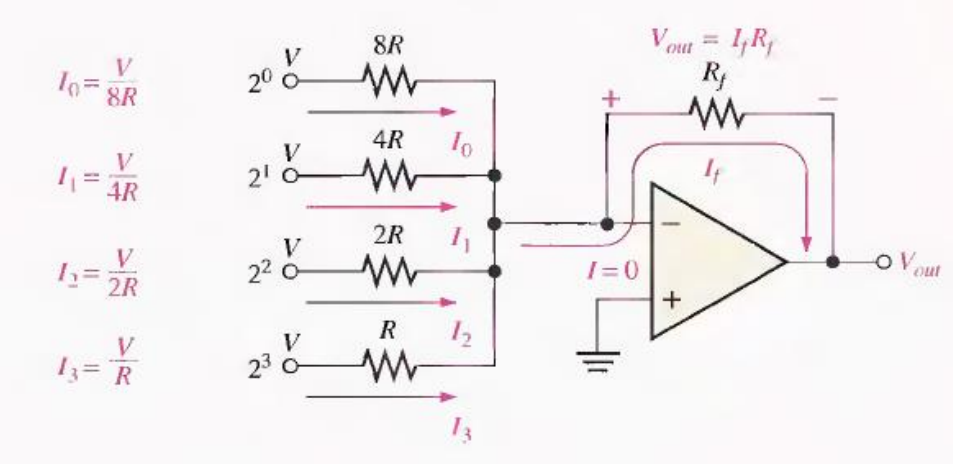


(a)



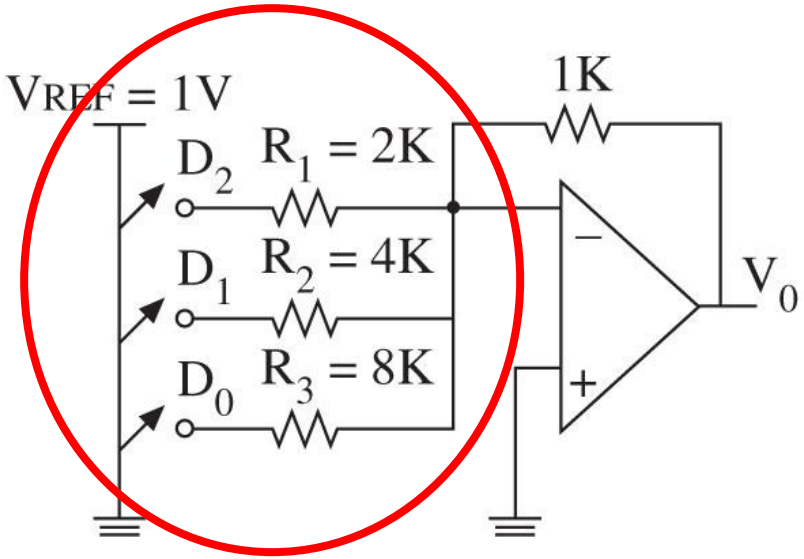
D/A Converter Circuits

- Can be designed using an operational amplifier and appropriate combination of resistors
- Resistors connected to data bits are in binary weighted proportion, and each is twice the value of the previous one.
- Each input signal can be connected to the op amp by turning on its switch to the reference voltage that represents logic 1.
  - If the switch is off, the input signal is logic 0.



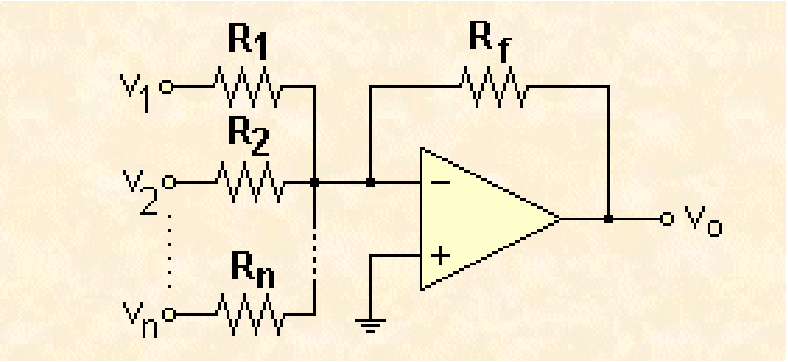
Binary Weighted DAC

- 3-bit D/A Converter Circuit



Summing amplifier

- R/2R Ladder Network for D/A Converter



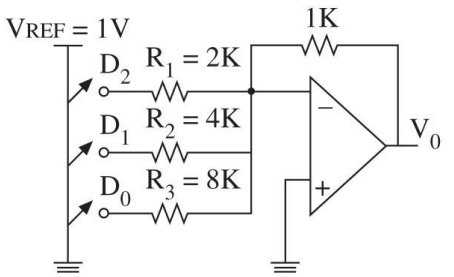
The transfer function of the summing amplifier :

vo = -(v1/R1 + v2/R2 + … + vn/Rn)Rf

Thus if all input resistors are equal, the output is a scaled sum of all inputs.

If they are different, the output is a weighted linear sum of all inputs.

Binary Weighted DAC : continued..



- If the reference voltage is 1 V, and if all switches are connected, the output current can be calculated as follows:

- Output voltage

$$I_o = I_T = I_1 + I_2 + I_3 = \frac{V_{REF}}{R_1} + \frac{V_{REF}}{R_2} + \frac{V_{REF}}{R_3} = \frac{V_{REF}}{1k}\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8}\right) = 0.875\,mA$$

$$V_O = -R_f I_T = -(1k) \times (0.875\ mA) = -0.875\ V = \left| 7/8\ V \right|$$

Note that the output will be inverted!

Disadvantages of Binary Weighted DAC

(i) One disadvantage of this DAC is that N inputs require N binary-weighted resistor values.

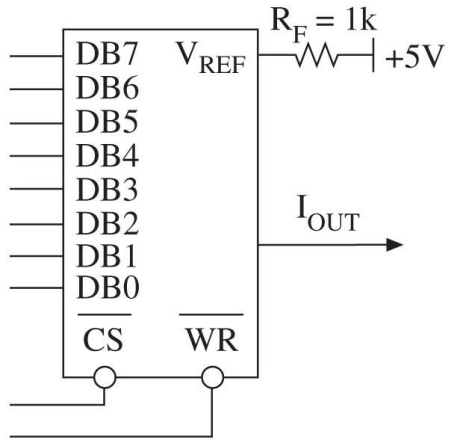
(ii) Another is that the circuit can require very accurate resistors, as the DAC would require that the error in each resistor be less than the smallest resistor value. This type requires large range of resistors with necessary high precision for low resistors. For an N-bit DAC, this means an error of less than 1 part in 2^N for the largest resistor, 1 part in 2^{N-1} for the next largest, and so on.

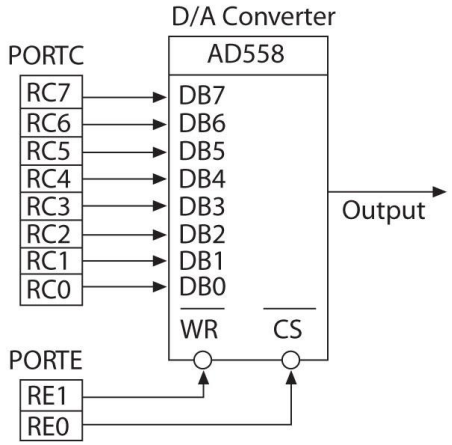
(iii) Requires low switch resistances in transistors.

(iv) Can be expensive. Hence resolution is limited to 8-bit size.

D/A Converter as Integrated Circuits

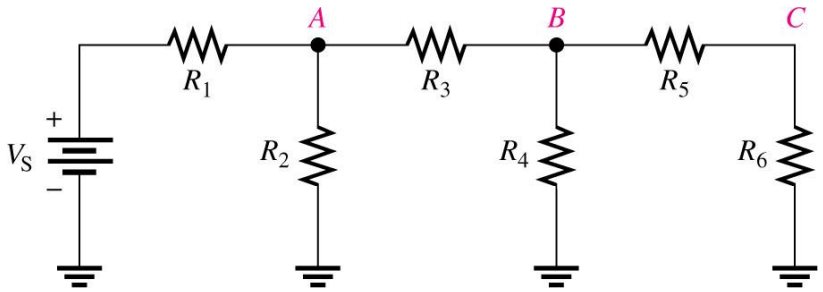
- D/A converters are available commercially as integrated circuits
- Can be classified in three categories.
  - Current output, voltage output, and multiplying type
    - Current output DAC provides the current I_O as output signal
    - Voltage output D/A converts I_O into voltage internally by using an op amp and provides the voltage as output signal
    - In multiplying DAC, the output is product of the input voltage and the reference source V_{REF}.
  - Conceptually, all three types are similar

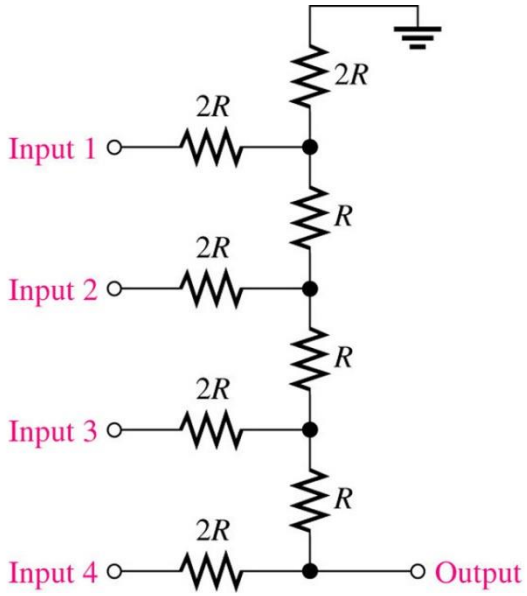




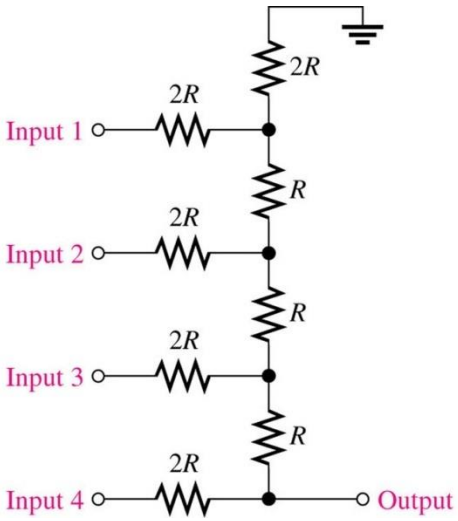
Analysis of a Ladder Network

- A resistive ladder network is a special type of series-parallel circuit.
- One form of ladder network is commonly used to scale down voltages to certain weighted values for digital-to-analog conversion
  - Called R/2R Ladder Network
- To find total resistance of a ladder network, start at the point farthest from the source and reduce the resistance in steps.



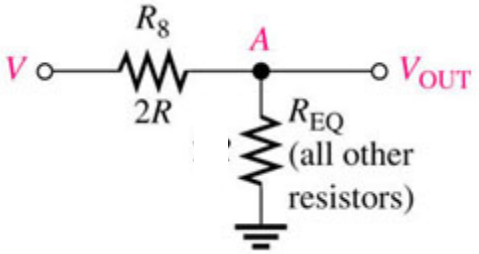


The R-2R Ladder Network

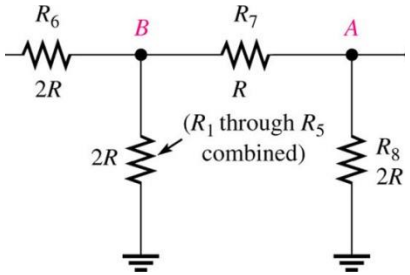


Used for Digital-to-analog converter!

Only Input 4 is HIGH



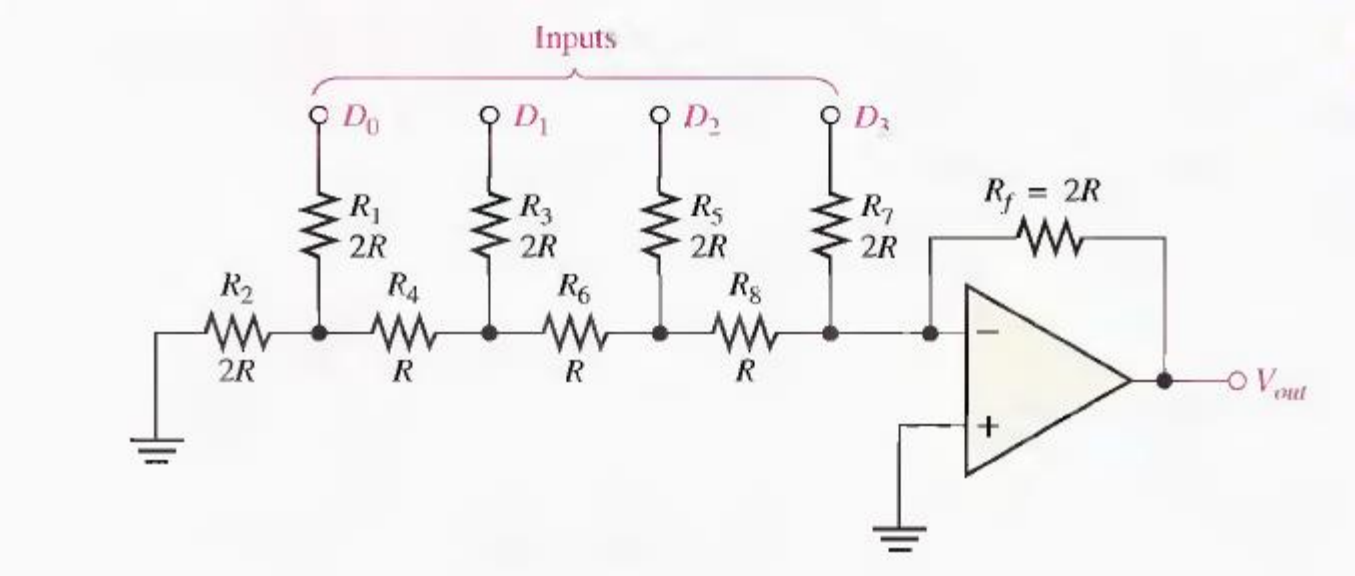
Only Input 3 is HIGH



The R/2R Ladder Network : continuing from previous slide

To overcome huge range of resistor used in weighted resistor D/A converter, R/2R ladder D/A converter is introduced.

Suppose we have to design 8-bit weighted register D/A converter then we need the resistance value $\mathbf{2^0R+2^1R+....+2^7R}$. So the largest resistor corresponding to bit b_8 is 128 times the value of the smallest resistor correspond to b_1. But in case of R/2R ladder D/A converter, Resistors of only two value (R and 2R) are used.



The R-2R Ladder Network : continuing from previous slide

Advantages:

- Only two resistor values are used in R-2R ladder type.
- It does not need as precision resistors as Binary weighted DACs.
- It is cheap and easy to manufacture.

Disadvantages:

- It has slower conversion rate.

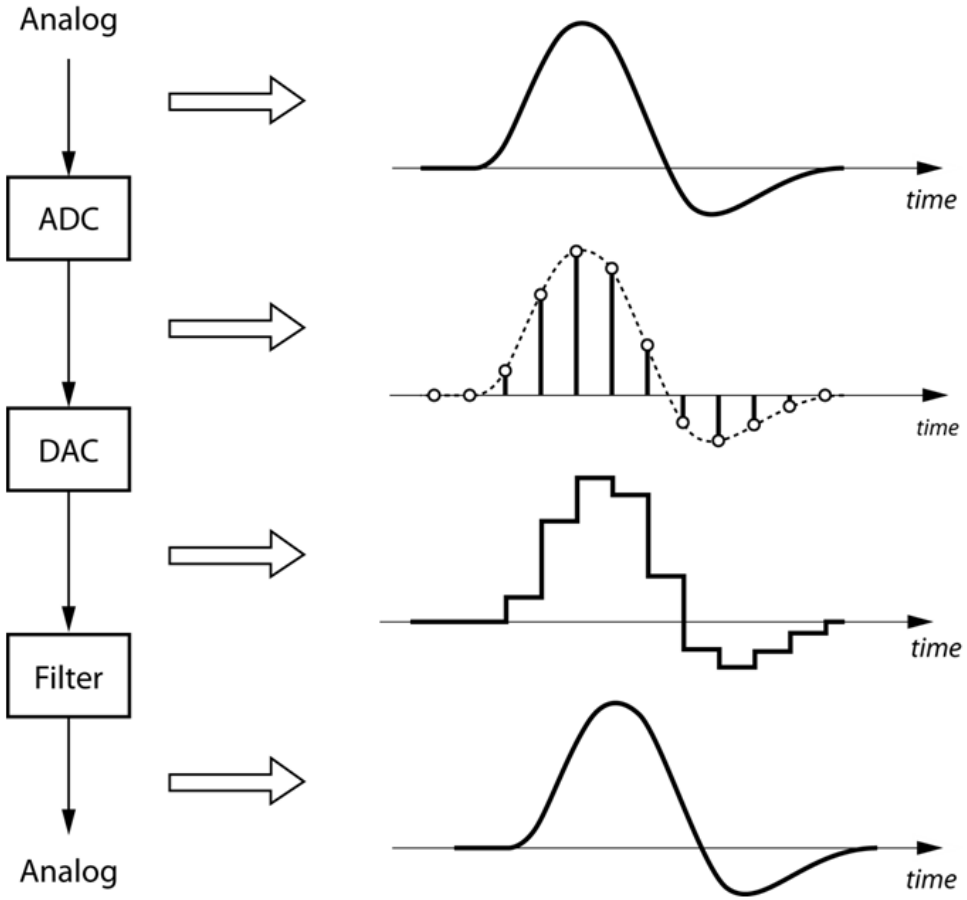
For N bit DAC:

- Number of different levels = 2^N
- Number of Steps = $2^N - 1$

Resolution or step size of DAC = Analog output/Number of steps = $Va/(2^N - 1)$

% Resolution = (Step Size/Full scale output) x 100 %

The Reconstruction Filter



In sound application that some weird sound is acceptable (not intended at DSP level). Lets say I make up some sound using 8-bit microcontroller. We can just use R-2R Ladder to generate analog output from normal digital output pin. The output will not smooth at all but it is acceptable

The ADC (Analog-to-digital converter) and the DAC (Digital-to-analog converter are the gateways between the real analog world of electrons and the digital binary world; While it is possible that some converters are controllable via firmware/software and thus conceptually are upgradeable, it fundamentally imperative that some sort of hardware exist that realize the electrical conversion, either by sampling and quantization (ADC) or reconstruction.

So the DAC quality is all about how well the reconstruction from curve 3 to curve 4 is carried out. Both hardware and the controlling software/firmware has influence here, but in the end the hardware sets the limit to what can be achieved, and what is controllable with software and what is not varies greatly with different DAC hardware. Thus it is not possible to give a general answer to your question - it depends on the hardware.