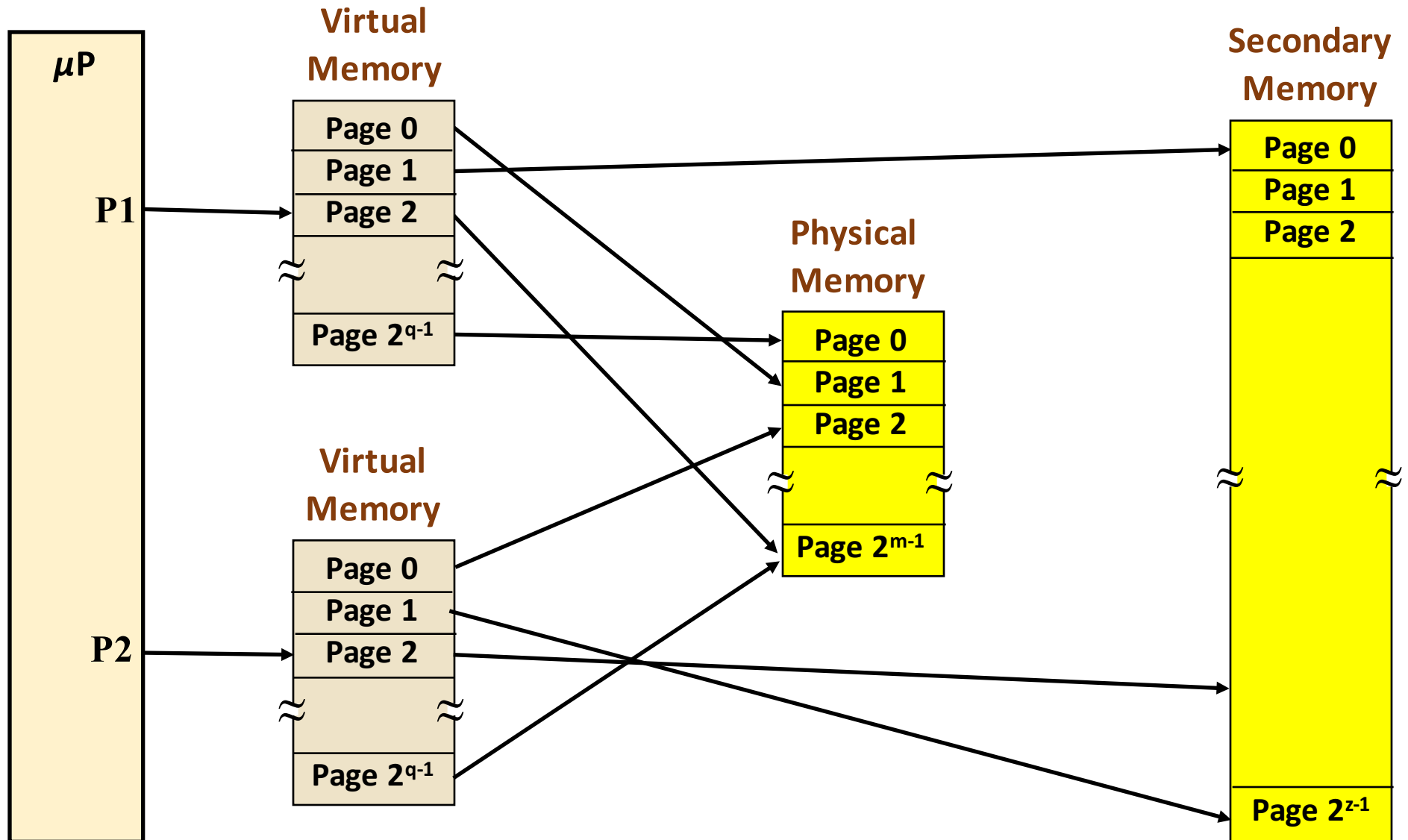


Virtual Memory

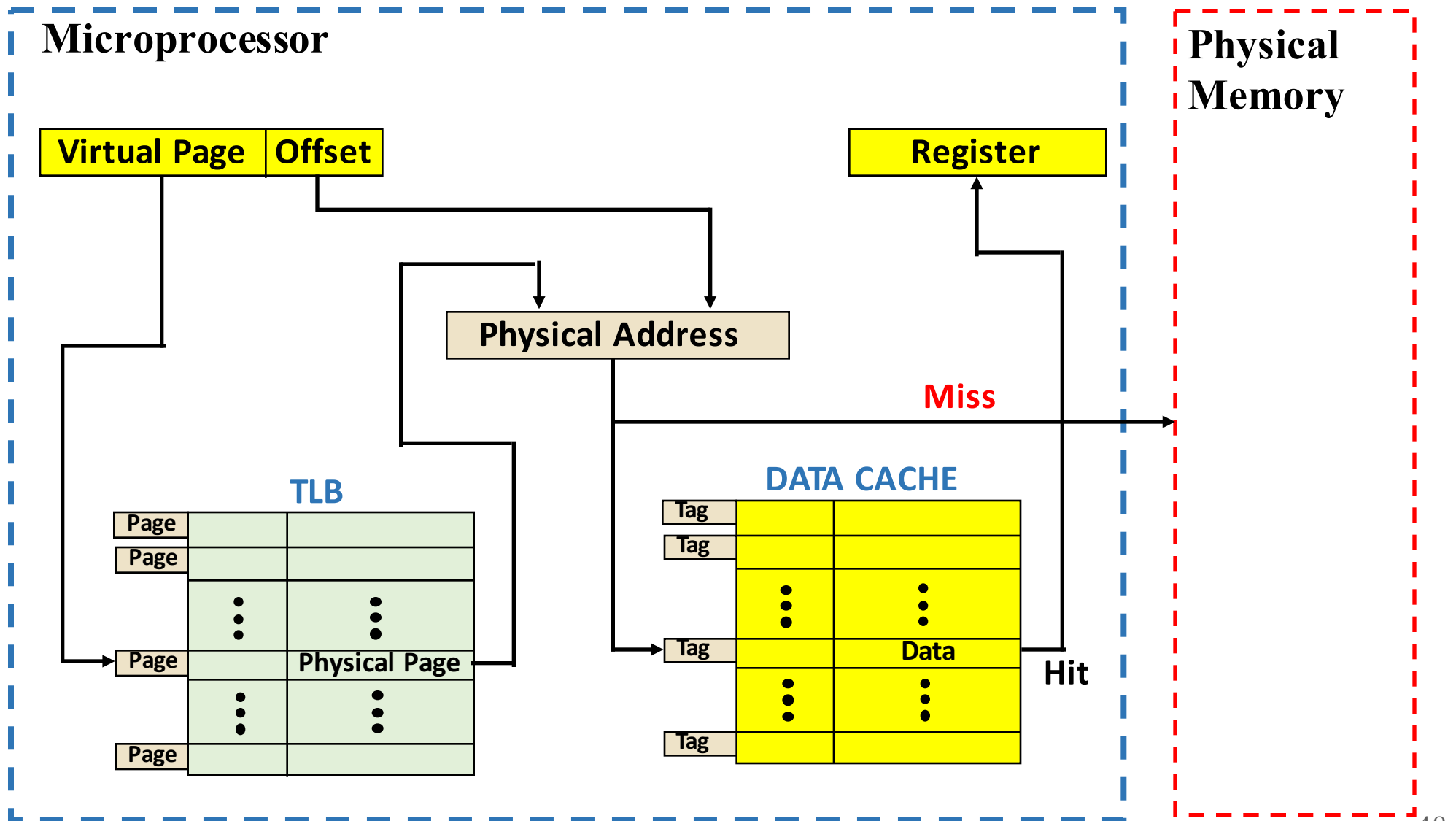
Caches on Virtual Memory Systems



Caches on Virtual Memory Systems

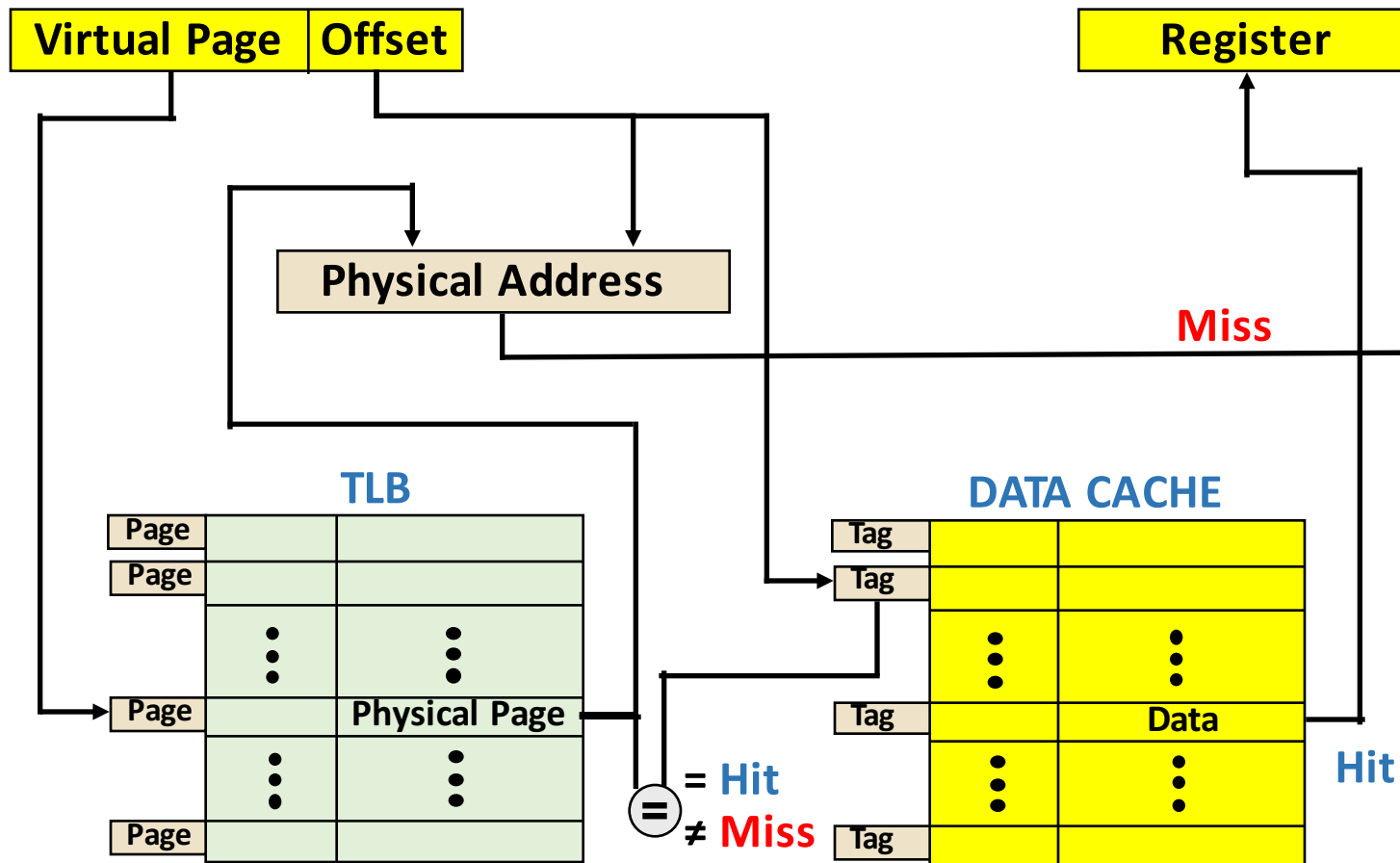
- Physical Cache
 - *Use physical addresses*
 - *Total memory access can be a minimum of two cycles if a TLB produces the physical address*
- Virtually Indexed, Physically Tagged (VIPT) Cache
 - *Uses offset of virtual address as index*
 - *Uses physical address tags (physical pages)*
 - *Needs TLB to validate physical page*
 - *Total memory access can be a minimum of one cycle*

Physical Caches on Virtual Memory Systems



Virtually Indexed, Physically Tagged (VIPT) Caches on Virtual Memory Systems

Microprocessor



Physical Memory

Lesson Outcomes

- Understand the organization of virtual memory systems.
- Understand the process of virtual to physical address translation.
- Know how the operating system intervenes in a virtual memory system, in particular on a page fault.
- Know how multi-level page tables accomplish address translation.
- Know how address translation is accomplished on virtual memory systems that use segmentation.
- Understand how caches are integrated on a virtual memory system.