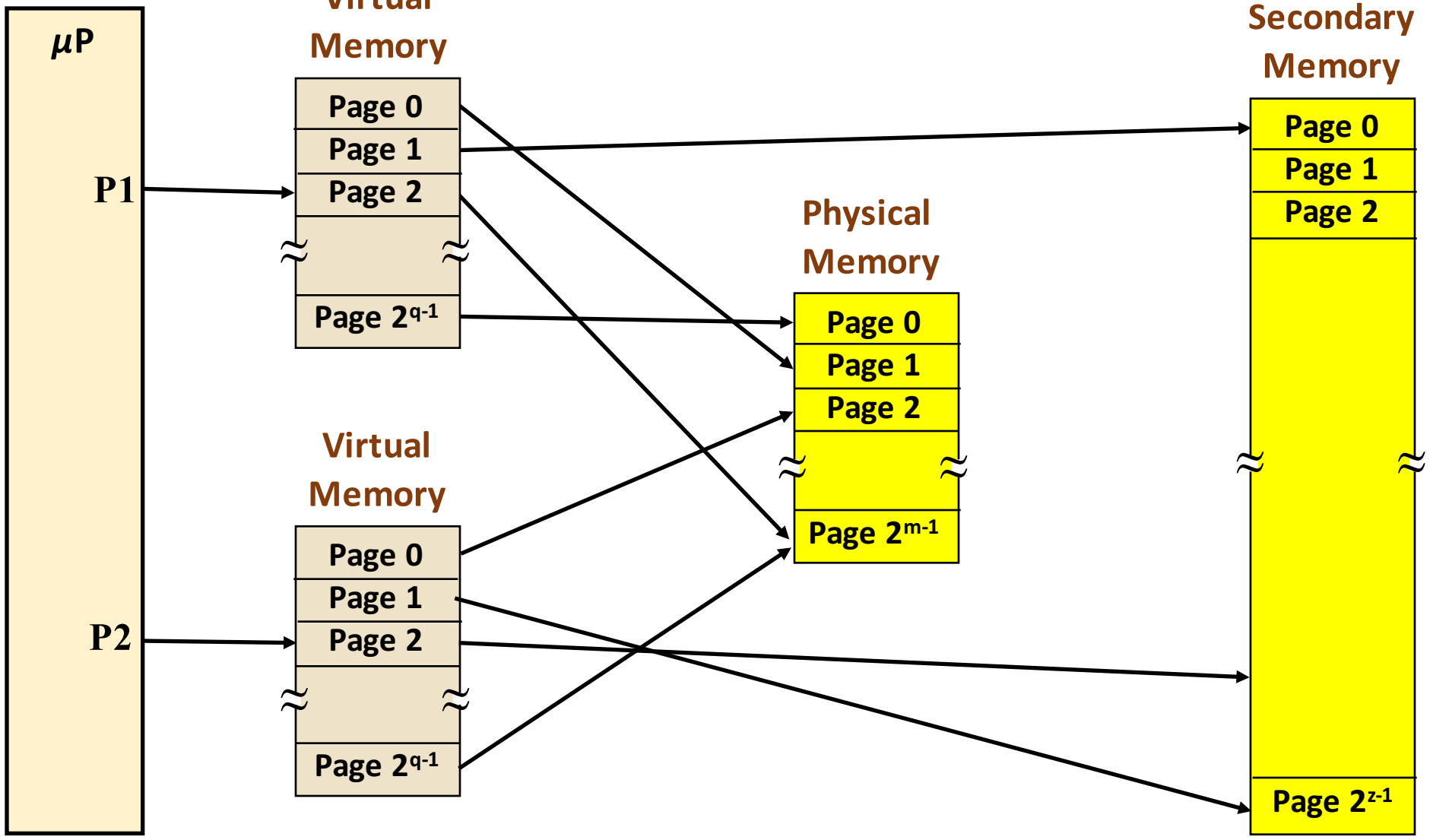
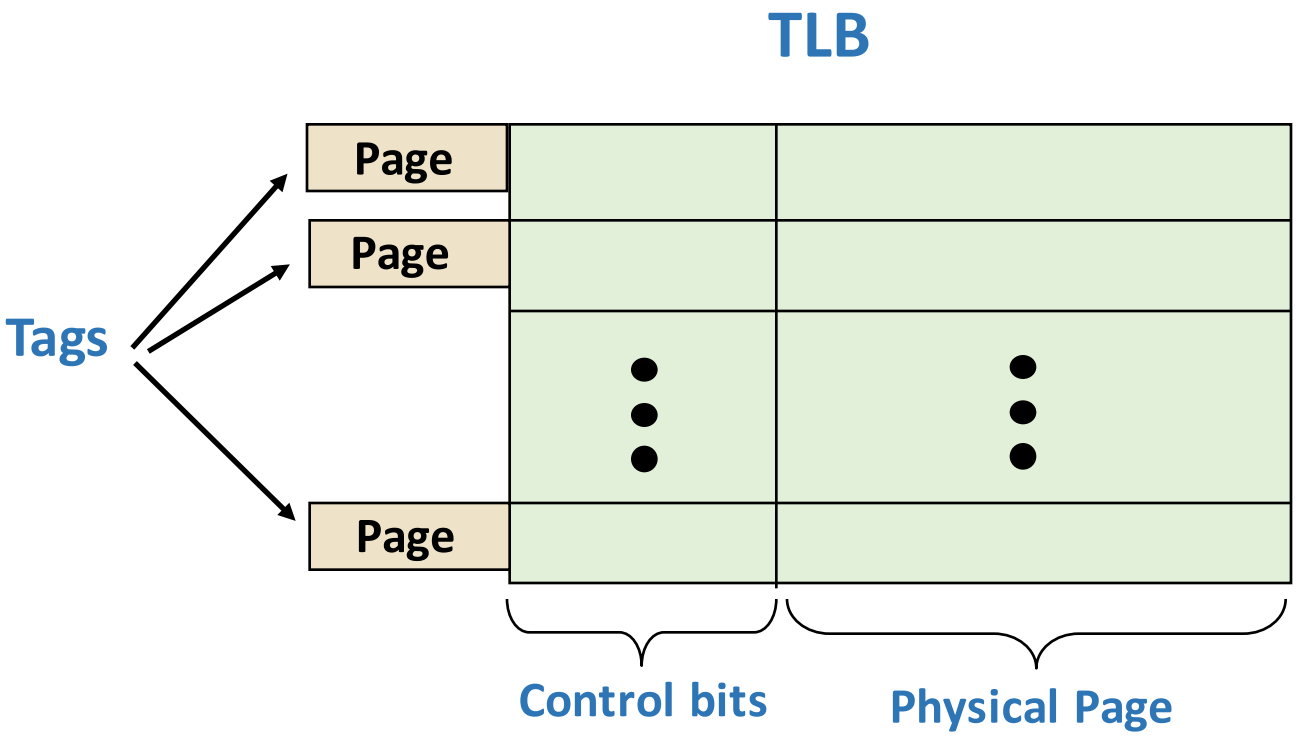
Virtual Memory
Reducing Translation Time



Reducing Memory Translation Time

- A CPU access to memory involves two memory access on a virtual memory system, one to the page table and one to the desired memory location in physical memory.
- On the best scenario (a hit on a cache) each access may take one cycle.
- The access time could be reduced by incorporating a mechanism that can construct the physical address without having to access the page table in physical memory.
- A small fully associative cache of virtual to physical page translations could do the job.
- Such cache is known as a Translation Lookaside Buffer (TLB).

Translation Lookaside Buffer (TLB)



- Tags are virtual page numbers
- Resides in the microprocessor

Translation Misses

- When an address translation results in a miss, the translation is made using the page table in physical memory.
- The resulting translation is placed on the TLB using a cache replacement algorithm.
- If the virtual page is not in physical memory, then a page fault is generated.

Address Translation with TLB