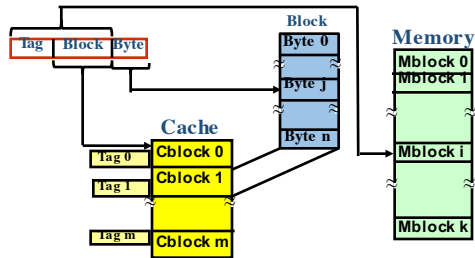# Caches: Replacement Algorithms

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On this Lesson

- Algorithms for block replacement on misses
  - *First-in first-out (FIFO)*
  - *Least recently used (LRU)*
  - *Optimum*
- Mapping memory addresses to memory blocks
- Allocation of a sequence of memory blocks into the cache
- Determine hits and misses for a sequence of memory accesses

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Cache Miss

When the location being accessed by the CPU is not in the cache

- *A replacement algorithm is used to choose a cache block (a victim) to place the block of memory where the location being accessed is saved*
- *If the victim block has been written to, it must be placed back on its corresponding block of memory*
- *The block of memory holding the location being accessed is placed in the cache victim block spot.*

Replacement Algorithms

- **Direct-Mapped:**
  - *Direct-mapped caches have an inherent replacement algorithm (the victim is always the block specified by the block field of the address).*
- **Fully Associative or Bock-Set Associative:**
  - ***First-In-First-Out (FIFO)*** *– Replaces the first block that got into the cache (the oldest block)*
  - ***Least Recently Used (LRU)*** *– Replaces the block with the most time without being accessed*
  - ***Optimum*** *– Replaces the block that will spend the most time without being accessed (used only for performance comparison since it cannot be implemented)*

Determining Memory Blocks Corresponding to Memory Accesses

- For any cache configuration the memory block is specified by the most significant bits of the address excluding the bits of the Byte field
  - Tag|Block – *Direct mapped cache*
  - Tag|Set – *Block-set associative cache*
  - Tag – *Fully associative cache*

- Alternatively, the memory block can be determined with a div operation:
  - *Memory Block = (Memory Address)* ***div*** *(Number of Bytes per Block)*

Determining Memory Blocks Corresponding to Memory Accesses: Examples

Blocks of 4 bytes

Memory Address	128	233	28	163
Memory Block	32	58	7	40

Blocks of 8 bytes

Memory Address	128	233	28	163
Memory Block	16	29	3	20

Blocks of 16 bytes

Memory Address	128	233	28	163
Memory Block	8	14	1	10

Allocation of Memory Blocks on the Cache

- Direct mapped cache
  - Block specified by Block field of address
  - Alternatively:
    Block = (memory block) **mod** (number of cache blocks)

- Fully associative cache
  - Any block (determined by replacement algorithm)

- Block-set associative cache
  - Any block (determined by replacement algorithm) within the set specified by Set field of the Address
  - Alternatively:
    Set = (memory block) **mod** (number of cache sets)

7

Example of Block Replacement on Direct-Mapped Cache

- Architectural memory of 2^{32} bytes
- 4-block cache, 8 bytes per block
- Sequence of memory accesses
  10, 22, 27, 33, 17, 41, 52, 20, 60, 67, 23, 39, 75, 18

- Use div operation to determine corresponding memory blocks:
  Memory Block = (Memory Address)/8

- Use Block field of address or mod operation to determine cache blocks for direct mapped caches:
  Cache Block = (Memory Block) % 4

Memory Address	10	22	27	33	17	41	52	20	60	67	23	39	75	18
Memory Block	1	2	3	4	2	5	6	2	7	8	2	4	9	2
Cache Block	1	2	3	0	2	1	2	2	3	0	2	0	1	2

8

Example of Block Replacement on Direct-Mapped Cache

Mem. Address	10	22	27	33	17	41	52	20	60	67	23	39	75	18
Memory Block	1	2	3	4	2	5	6	2	7	8	2	4	9	2
Cache Block	1	2	3	0	2	1	2	2	3	0	2	0	1	2

Cache block 0				4	4	4	4	4	4	8	8	4	4	4
Cache block 1	1	1	1	1	1	5	5	5	5	5	5	5	9	9
Cache block 2		2	2	2	2	2	6	2	2	2	2	2	2	2
Cache block 3			3	3	3	3	3	3	7	7	7	7	7	7

■ Hit

9

Example of Block Replacement on Fully Associative Cache

- Architectural memory of 2^{32} bytes
- 4-block cache, 8 bytes per block
- Sequence of memory accesses
  10, 22, 27, 33, 17, 41, 52, 20, 60, 67, 23, 39, 75, 18

- Use div operation to determine corresponding memory blocks:
  Memory Block = (Memory Address)/8

Memory Address	10	22	27	33	17	41	52	20	60	67	23	39	75	18
Memory Block	1	2	3	4	2	5	6	2	7	8	2	4	9	2

10

Example of FIFO Block Replacement on Fully Associative Cache

Mem. Address	10	22	27	33	17	41	52	20	60	67	23	39	75	18
Memory Block	1	2	3	4	2	5	6	2	7	8	2	4	9	2

FIFO	1	2	3	4	2	5	6	2	7	8	2	4	9	2	Youngest
		1	2	3	4	2	5	6	2	7	8	2	4	9	
			1	2	2	3	4	5	6	2	7	2	8	4	
				1	1	2	3	4	5	6	6	2	7	8	Oldest

■ Hit

11

Example of LRU Block Replacement on Fully Associative Cache

Mem. Address	10	22	27	33	17	41	52	20	60	67	23	39	75	18
Memory Block	1	2	3	4	2	5	6	2	7	8	2	4	9	2

LRU	1	2	3	4	2	5	6	2	7	8	2	4	9	2	MRU
		1	2	3	4	2	5	6	2	7	8	2	4	9	
			1	2	3	4	2	5	6	2	7	8	2	4	
				1	1	3	4	2	5	6	6	7	8	8	LRU

■ Hit

12

2

Example of Optimum Block Replacement on Fully Associative Cache

Mem. Address	10	22	27	33	17	41	52	20	60	67	23	39	75	18
Memory Block	1	2	3	4	2	5	6	2	7	8	2	4	9	2

Optimum														
	1	2	2	2	2	2	2	2	2	2	2	2	2	2
		1	3	4	4	4	4	4	4	4	4	4	4	4
			1	3	3	5	6	6	7	8	8	8	8	9	9
				1	1	3	5	5	6	7	7	7	7	8	8

■ Hit

13

Replacement Algorithms Comparison: 4-block Cache

Mem. Address	10	22	27	33	17	41	52	20	60	67	23	39	75	18
Memory Block	1	2	3	4	2	5	6	2	7	8	2	4	9	2

FIFO														
	1	2	3	4	4	5	6	2	7	8	8	4	9	2
		1	2	3	4	5	6	2	7	7	8	4	9	
			1	2	2	3	4	5	6	6	2	7	8	
				1	1	2	3	4	5	6	6	2	7	8

LRU														
	1	2	3	4	2	5	6	2	7	8	2	4	9	2
		1	2	3	4	2	5	6	2	7	8	2	4	
			1	2	3	4	2	5	6	2	7	8		
				1	1	3	4	5	6	6	7	8		

Hit ■

D-Mapped														
				4	4	4	4	4	4	8	4	4		
	1	1	1	1	1	5	5	5	5	5	5	9	9	
	2	2	2	2	2	6	2	2	2	2	2	2		
		3	3	3	3	3	7	7	7	7	7			

Optimum														
	1	2	2	2	2	2	2	2	2	2	2	2	2	2
		1	3	4	4	4	4	4	4	4	4	4	4	
			1	3	3	5	6	6	7	8	8	8	9	9
				1	1	3	5	5	6	7	7	7	8	8

Example of Block Replacement on Block-Set Associative Cache

- *Architectural memory of 2^{32} bytes*
- *4-block cache, 8 bytes per block, 2-way (two blocks per set)*
- *Sequence of memory accesses:*
  10, 22, 27, 33, 17, 41, 52, 20, 60, 67, 23, 39, 75, 18

- Use div operation to determine corresponding memory blocks:

  Memory Block = (Memory Address)/8

- Use set field of address or mod operation to determine cache blocks for direct mapped caches:

  Cache Block = (Memory Block) % 2

Memory Address	10	22	27	33	17	41	52	20	60	67	23	39	75	18
Memory Block	1	2	3	4	2	5	6	2	7	8	2	4	9	2
Cache Set	1	0	1	0	0	1	0	0	1	0	0	0	1	0

15

Example of FIFO Block Replacement on Block-Set Associative Cache

Mem. Address	10	22	27	33	17	41	52	20	60	67	23	39	75	18
Memory Block	1	2	3	4	2	5	6	2	7	8	2	4	9	2
Cache Set	1	0	1	0	0	1	0	0	1	0	0	0	1	0

Set 0		2	2	4	4	4	6	2	2	8	8	4	4	2	Youngest
			2	2	2	4	6	6	2	2	8	8	4	Oldest
Set 1	1	1	3	3	3	5	5	5	7	7	7	9	9	Youngest
			1	1	3	3	3	5	5	5	7	7	7	Oldest

■ Hit

16

Example of LRU Block Replacement on Block-Set Associative Cache

Mem. Address	10	22	27	33	17	41	52	20	60	67	23	39	75	18
Memory Block	1	2	3	4	2	5	6	2	7	8	2	4	9	2
Cache Set	1	0	1	0	0	1	0	0	1	0	0	0	1	0

Set 0		2	2	4	2	2	6	2	2	8	2	4	4	2	MRU
			2	2	4	4	2	6	6	2	8	2	2	4	LRU
Set 1	1	1	3	3	3	5	5	5	7	7	7	9	9	MRU
			1	1	3	3	3	5	5	5	7	7	7	LRU

■ Hit

17

Lesson Outcomes

- Understand the FIFO and LRU replacement algorithm

- Know how to map CPU memory addresses to memory blocks

- Know how to determine hits and misses for a sequence of CPU memory access for any cache configurations

18