Digital Circuit Laboratory

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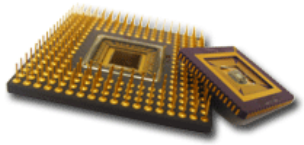
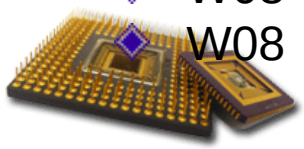
Goals

- Learn the digital circuit design (i.e., logical design) in Verilog
  - Combinational circuit
  - Synchronous sequential circuit
  - Input and output circuit and protocol
- Practice hardware description language: Verilog
- Practice EDA Tools for the FPGA Design



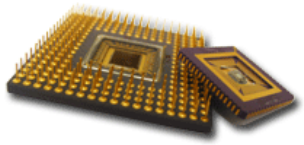
Syllabus (1/2)

- W01 09/02(一) Not need to go to class
- W01 09/06(五) Mat 1: Introduction to Vivado and Lab 1: Sequential Multiplier
- W02 09/09(一) TAs meet all students.
- W02 09/13(五) Mat 2: Introduction to Verilog and Lab 2: Matrix Multiplication Simulation
- W03 09/16(一) Lab 1 Demo Check
- W03 09/20(五) Mat 2: Introduction to Verilog and Lab 3: Simple ALU Simulation
- W04 09/23(一) Lab 2 Demo Check
- W04 09/27(五) Mat 2: Introduction to Verilog and Lab 4: Push Button and LED Control
- W05 09/30(一) Lab 3 Demo Check
- W05 10/04(五) Mat 3: Introduction to FPGAs and Lab 5: Character LCD Control
- W06 10/07(一) Lab 4 Demo Check
- W06 10/11(五) Lab 6: UART Communications
- W07 10/14(一) Lab 5 Demo Check
- W07 10/18(五) Lab 7: Matrix Multiplication Circuit for Real
- W08 10/21(一) Lab 6 Demo Check
- W08 10/25(五) Experiment Time



Syllabus (2/2)

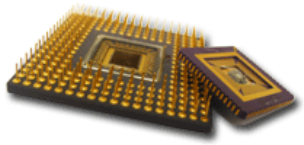
- W09 10/28(一) Online Test
- W09 11/01(五) Lab 8: SD Card Reader Circuit
- W10 11/04(一) Lab 7 Demo Check and Review Test
- W10 11/08(五) Lab 9: Password Cracking
- W11 11/11(一) Lab 8 Demo Check
- W11 11/15(五) Lab 10: VGA Graphic Display
- W12 11/18(一) Lab 9 Demo Check
- W12 11/22(五) Final Project Topics
- W13 11/25(一) Lab 10 Demo Check
- W13 11/29(五) Experiment Time
- W14 12/02(一) Experiment Time
- W14 12/06(五) Experiment Time
- W15 12/09(一) Experiment Time
- W15 12/13(五) Experiment Time
- W16 12/16(一) Experiment Time
- W16 12/20(五) Final Project and Demo (End of Class)



Recommended Books

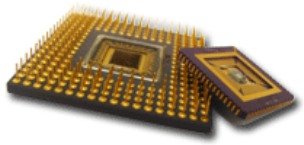
- Logic Design:
  - M. Morris Mano, Michael D. Ciletti, Digital Design, Sixth Edition, Pearson Education, 2019.
  - Charles H. Roth, Jr., Larry L. Kinney, Eugene B. John, Fundamentals of Logic Design, 2021.
  - Randy Katz, Gaetano Borriello, Contemporary Logic Design, Pearson Education, 2005.

- Verilog: there are plenty of good Verilog books and on-line resources.
  - Peter J. Ashenden, Digital Design: An Embedded Systems Approach Using Verilog, Morgan Kaufmann Publishers, 2008.
  - Pong P. Chu, FPGA Prototyping by Verilog Examples: Xilinx Spartan-3 version, J. Wiley & Sons, 2008.
  - M. B. Lin. Digital System Designs and Practices, Wiley, 2008.



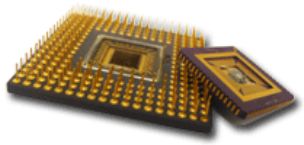
Staff and Evaluation

- Instructor:
  - Prof. Lan-Da Van (范倫達), EC419, #54815, ldvan@cs.nycu.edu.tw
- Website: http://viplab.cs.nycu.edu.tw/course/DCL2024_Fall.php
- Grades
  - 10 Labs 50%
  - 1 Online Test 20%
  - 1 Final Project 30%
- Lecture Location and Time:
  - EC122 (工三館122教室), Friday 10:10AM – 12:00noon
- Lab Location and Time:
  - EC220 (工三館220教室), Monday, 18:30PM~21:30PM
- Office hours
  - TA Office Hour:
    - 吳承芶: vickwu0329@gmail.com、鄭鈞瀚、陳祁鎔、程琪薰、邱晨恩、沈陽明、盧珮芸、黃芷嫻
    - Teacher Office Hour: EC-419, Friday: 8:00AM~10:00AM.



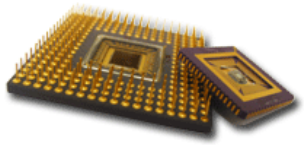
Lab Regulations

- Lab is individual lab NOT team lab.
- Each Lab has 10 days for practice/working at least.
- At the due date, you will be asked to submit your file(s) to E3 by 6:00pm. If any delay happens for submission from your side, this lab grade will also be zero. That means no delay and no extension is available!!!
- The TA will ask you some questions if needed for each lab. Your answer will be part of grade.
- Please do NOT copy.
- If TA finds out the (part) answer you show is copied from others, the lab grade will be zero.



Online Test Regulations

- Online test is individual exam NOT team exam.
- You can take one USB flash disk to store the necessary data but you have to back up to the PC you used before the test. During the test, no internet and no outsourcing data.
- The TA will ask you some questions if needed for each online test. Your answer will be part of grade.
- Please do NOT copy.
- If TA finds out the (part) answer you show is copied from others, the test will be zero.



Final Project Regulations

- Final project is team work within 4 people at most.
- Please list every member task and weighting.
- Please do NOT copy code or others from other teams.
- No extension is available!!! If exceeding the due date, this final project grade will be zero.
- The TA will ask you some questions if needed for the final project. Your answer will be part of grade.