Q1. Consider a program segment below: [1+1+2+2=6]

| Labels | Instruction Counter | Instruction/Data |
|---|---|---|
| | 100 | Load X |
| | 101 | MOV R1 |
| | 102 | Load Y |
| | 103 | Add R1 |
| | 104 | Store Z |
| | 105 | Halt |
| X: | 106 | 23H |
| Y: | 107 | E9H |
| Z: | 108 | 0000 |

a) Draw the symbol table.

| | |
|---|---|
| X | 106 |
| Y | 107 |
| Z | 108 |

b) What is the addressing mode used in instruction "Load X"

Direct

c) If PC-relative addressing was to be used in place of "X", what would be the offset?

PC is at 101, X refers to 106; Offset=5

d) What value is stored at Z?

Sum of 23H and E9H = 0CH

00100011
11101001
Sum: 00001100 (=0CH)
Carry: 1

Q2. You are on the design team for a new processor. The clock of the processor runs at 200 MHz. The following table gives instruction count and number of cycles the instructions take for the different classes of instructions for a benchmark program. For this problem, we assume that the processor only executes one instruction at a time. [6]

| **Instruction type** | **Count** | **Cycles** |
|---|---|---|
| Load/Store | 30 | 6 |
| Arithmetic | 50 | 4 |
| Others | 20 | 3 |

a) What is the MIPS processor speed for the benchmark?

Total no. of clock cycles = 30*6+50*4+20*3=440
Total no. of instructions=30+50+20=100
100 instructions need 440 clock cycles = 440/(200*$10^6$) seconds

Therefore, in 1 second, we can execute 200*$10^6$*100/440 instructions
=45.45*$10^6$ instructions

MIPS = 45.45

b) The compiler expert says that if you double the number of registers, then the compiler will generate code that requires only half the number of Loads & Stores. What will be the CPI?

CPI = Total clock cycles/Total no. of instructions
= (15*6+50*4+20*3)/(15+50+20)
=350/85 = 4.1

Q3. In the following expression, what is the state of any two PSW bits (which are being affected by the operation). Assume that machine is of 8-bits. [4]
1010 1101 + 1110 1111

Sum is 10011100 with a carry/overflow
Therefore affected PSW bits are: carry/overflow, Sign, Parity, Auxiliary carry

**Q4. Consider the following expression:**

**X = A + ( B * (( C + ( D * E ))/ F ))**

**a) Write a program to compute the value of this expression for the following machines with only the specified instructions available: [3+3=6]**

**Machine 1: Push M, Pop M, Add, Sub, Mul, Div**

**Machine 2: Load M, Store M, Add M, Sub M, Mul M, Div M**

**Here, M is a 16-bit memory address. The opcode is of 8-bits and instruction length is multiple of 4 bits.**

**b) How many bits does each machine need to compute X? [2]**

**Reverse polish notation -** A B C D E * + F / * +

| | Machine 1 | | Machine 2 | |
|---|---|---|---|---|
| | Push A | 24 = 16+8 | Load D | 24 |
| | Push B | 24 | Mul E | 24 |
| | Push C | 24 | Add C | 24 |
| | Push D | 24 | Div F | 24 |
| | Push E | 24 | Mul B | 24 |
| | Mul | 8 | Add A | 24 |
| **Ans a)** | Add | 8 | Store X | 24 |
| | Push F | 24 | | |

| | | | | |
|---|---|---|---|---|
| | Div<br>Mul<br>Add | 8<br>8<br>8 | | |
| **Ans b)** | Total bits | 184 bits | | 168 bits |

**Q5. Explain briefly:** **[2*2=4]**

a) **One morning, the queen bee of a beehive calls all her worker bees and tells them that today's assignment is to collect marigold nectar. The workers then fly off in different directions looking for marigold. Should it be treated as SIMD or MIMD system? Explain.**

**SIMD.**

b) **A computation is highly sequential (i.e. each step depends on the preceding step). Would an array processor or a pipeline processor be more appropriate for this? Explain.**

**Pipeline Processor.**

Q6. Copute the following expression using IEEE-754 single-precision floating point format [6]

$-6.5_{10} + 11.25_{10}$

| Decimal No. | Sign | Exponent | Mantissa |
|---|---|---|---|
| -6.5 | = 1 | 10000001 | 1010000 00000000 00000000 |
| 11.25 | = 0 | 10000010 | 01101000000000000000000 |
| --- | | | |
| 4.75 | = 0 | 10000001 | 0011000 00000000 00000000 |

Q7. Write the micro-sequence for the instruction "**Branch_if_S=0, M"** for a three-bus organization, where **M** is a memory address available in register R5 and **S** is the sign flag. [6]

1. $PC_{outB}$ , R=B, $MAR_{in}$, Read, IncPC
2. WMFC
3. If S=1, End
4. $R5_{outB}$, R=B, $PC_{in}$, End