COA – QUIZ 1

Year 2020 – Y19 Batch

Q. Consider the addition of -7 and +3, determine which of the following condition code flags are set:

(a) Carry (C)

(b) Overflow (V)

(c) Zero (Z)

(d) Sign (N)

Q. Consider the following program segment used to execute on a hypothetical processor.

Instruction	Size (word)
I_1	2
I_2	1
I_3	1
I_4	2

Assume that program is stored in the byte addressable memory with start address of 200 and word size is 32-bits. During the execution of instruction I_3 what could be the value present in program counter (PC)?

(a) 2016

(b) 2012

(c) 2015

(d) 2017

Q. ----------addressing mode is an efficient way to access linear array elements

(a) Register Addressing Mode

(b) Auto indexed Addressing Mode

(c) Immediate Addressing Mode

(d) Indirect Addressing Mode

Q. If a computer system has 612 no. of instruction then how many bits are required to represent opcode field of an instruction format?

(a) 9 bits

(b) 10 bits

(c) 8 bits

(d) 7 bits

Q. Examine the following statements:

I: RISC supports variable length of instruction

II: A compiler has to do lot of work in RISC style.

III: In RISC style, instruction-decoding logic is complex

which of the following is TRUE about RISC Computer?

(a) I, II and II are true

(b) I, II and II are false

(c) I, III are false but II is true

(d) I, II are true but III is false

Q. Instruction decode (ID) unit:

(a) determines total number of operations

(b) identifies type of operation

(c) specifies addressing mode

(d) none

Q. In which addressing mode, the address field of instruction gives the address of memory location where the effective address is stored.

a) Displacement Addressing Mode

b) Immediate Mode

c) Direct Addressing Mode

d) Indirect Addressing Mode

Q. Task of linker is/are

I: translate source code into object code

II: combine all object module to a complete image

III: resolve external & internal references

(a) I & II

(b) II & III

(c) I & III

(d) I, II & III

Q. Mark the false statement for Assembler Directives:

I: An instruction that will be executed when the object program is run

II: It does not appear in the object program

(a) Only I

(b) Only II

(c) Both false

(d) None

Q. The smallest integer that can be represented by a 9-bit number in 2's complement form is:

(a) -255

(b) -256

(c) -127

(d) 0

Q. Consider a machine supports 2-address instructions, a 24-bit instruction is placed in a word-addressable memory consisting of 128 words. The number of possible operations is?

(a) 1024

(b) 512

(c) 128

(d) 2048

Q. Result of subtraction of -5 from -7 in the 2's-complement system:

(a) 1 1 1 0

(b) 1010

(c) 1101

(d) 1011

Q. Example of Immediate addressing mode:

(a) Add R2,R1

(b) Add R2, #5

(c) Add R2, 100(R3)

(d) Add R5, (R2+R3)

Q. To resolve the forward reference problem in assembly process, we use :

a) Loader
b) Two-pass assembler
c) Op-Assembler
d) Debugger

Q. How many address bits are required to represent 256 G memory:

a) 38bits
b) 18bits

c) 48 bits

d) 8bits

Q. Array processor is an example of:

a) SISD Architecture

b) MIMD Architecture

c) SIMD Architecture

d) MISD Architecture

Q. ----------Register is used to hold the currently fetched instruction to decode

a) Memory Buffer Register

b) Memory Address Register

c) Instruction Register

d) Program Counter

Q. Status of memory is given below.

word 100 contains 300

word 200 contains 400

word 300 contains 600

word 400 contains 700

Which of the following instruction is used to load 600 into the accumulator?

(a) load immediate 300

(b) load indirect 400

(c) load immediate 100

(d) load indirect 100

Q. For the instruction MOVE R3, R7, how many times will the memory be accessed?

a) 0

b) 1

c) 2

d) 3

Q. In the instruction LOAD R3, 100(R1), what will be the effective memory address from where the operand is fetched? Assume, R1 currently holds 2500 and R3 holds 3000. Also instruction is present at memory address 1000.

a) 1000

b) 2500

c) 2600

d) 3000