LNMIIT
The LNM Institute of Information Technology

Electronics and Communication Engineering Department
The LNMIIT, JAIPUR
Digital Circuits and Systems (Endterm Exam)

Date: 05/12/2017

Time: 180 Minutes | Maximum Marks: 100

Student's roll number: | Student's name:

Important Notes: *This question paper consists of* ***two*** *sections having six questions in each, that is, total twelve questions.* ***Five*** *questions from each section are required to be answered. All questions carry equal marks.*

Section I

1. A 10-bit binary data 0011101101 is received, check using even parity Hamming code *i*). if received data is correct, *ii*). if there is an error determine the bit position and determine the corrected code and the uncoded message. Leftmost is the starting bit. [05]

Total bits = 10 = 4 parity bits + 6 ~~data~~ message bits

P_1	P_2	M_0	P_4	M_1	M_2	M_3	P_8	M_4	M_5
0	0	1	1	1	0	1	1	0	1

(1)

Check if data received correctly:-

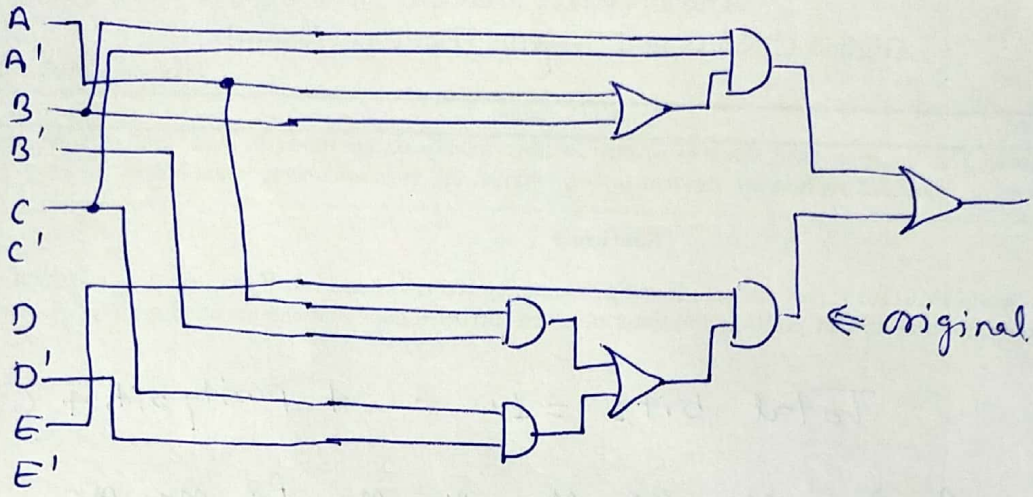
Check for $P_1 \Rightarrow 0\ 1\ 1\ 1\ 0 = 1$ (To make it even)
" " $P_2 \Rightarrow 0\ 1\ 0\ 1\ 1 = 1$ } Shows error in received data
" " $P_4 \Rightarrow 1\ 1\ 0\ 1 = 1$
" " $P_8 = 1\ 0\ 1 = 0$

(2)

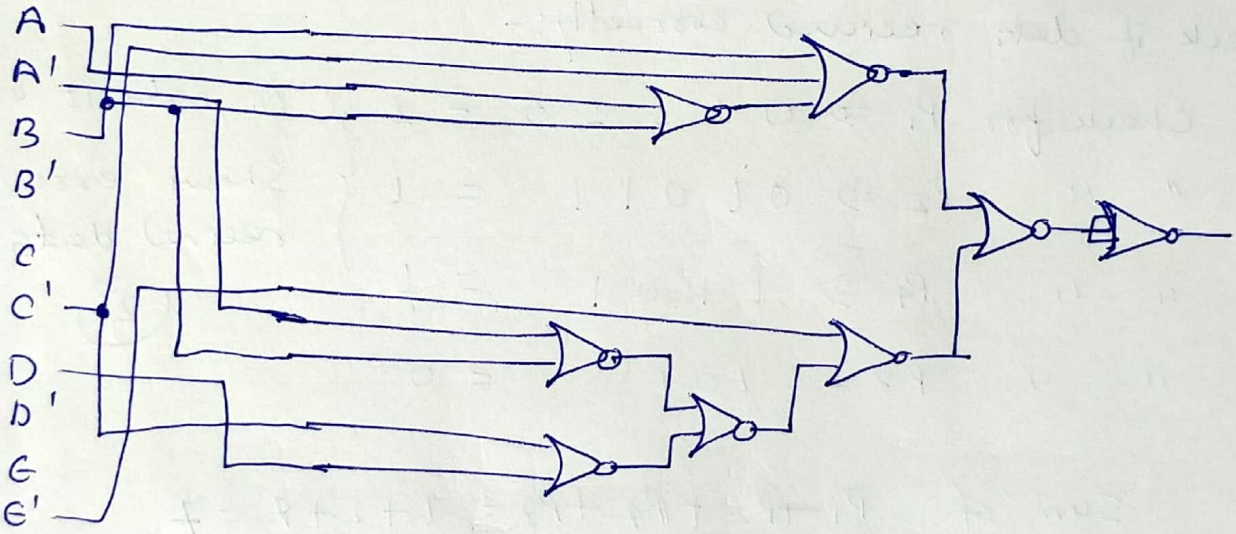
Sum of $P_1 + P_2 + P_4 + P_8 = 1 + 2 + 8 = 7$
bit position from left 7 has error i.e. $m_3 = 1 \to 0$

Correct code is :- 0011100101 (1)
and uncoded message - 110001 (1)

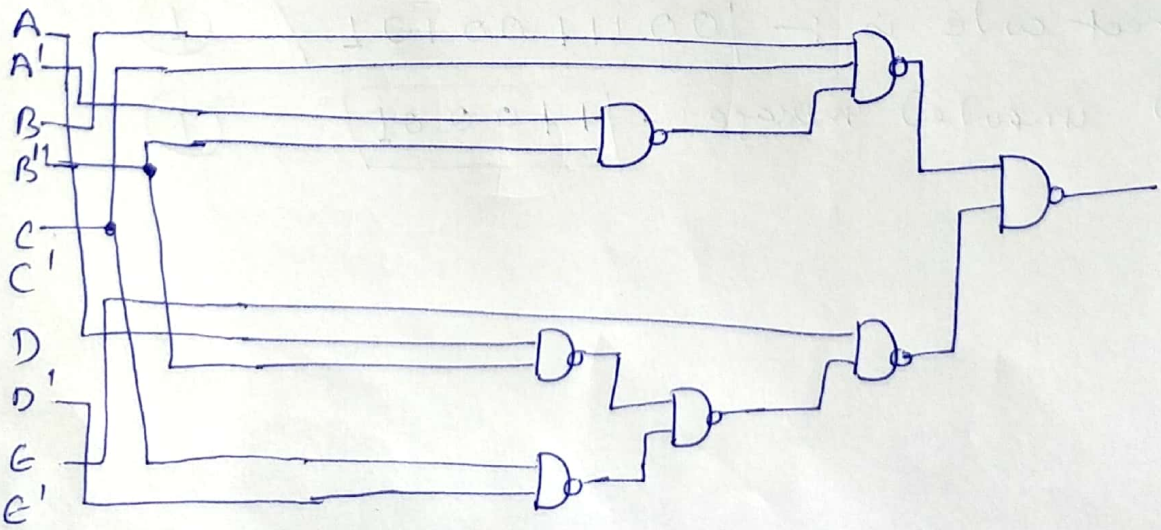
2. Draw the multi-level NOR and multi-level NAND circuits for the expression: $(AB' + CD')E + BC(A + B)$. [05]



NOR implementation:-



NAND implementation:-



3. Show that the dual of the EX-NOR is equal to EX-OR and show also, using truth table, that a positive logic NAND gate is a negative logic NOR gate. [05]

Dual of EX-NOR :-

assuming inputs x & y, then

EX-NOR $\Rightarrow$ $x \odot y = x.y + x'y'$ (2)

dual of it :- $= (x+y).(x'+y') = xx' + xy' + x'y + yy'$

$= xy' + x'y = x \oplus y$ = EX-OR

Assuming a truth table for a gate having two i/ps x & y and o/p z :-

x	y	z
L	L	H
L	H	H
H	L	H
H	H	L ↑ (1)

Positive logic for this table

x	y	z
0	0	1 → H
0	1	1 → H
1	0	1 → H
1	1	0 → L (1)

This is a NAND gate o/p (+ve logic)

-ve logic for this table

x	y	z
1	1	0 → H
1	0	0 → H
0	1	0 → H
0	0	1 → L (1)

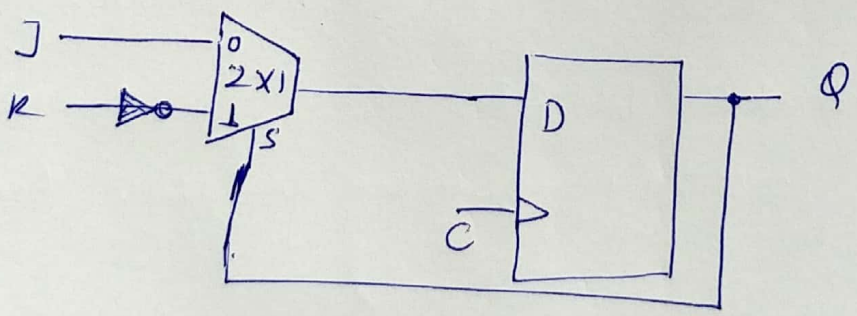
This is a NOR gate o/p (-ve logic)

=

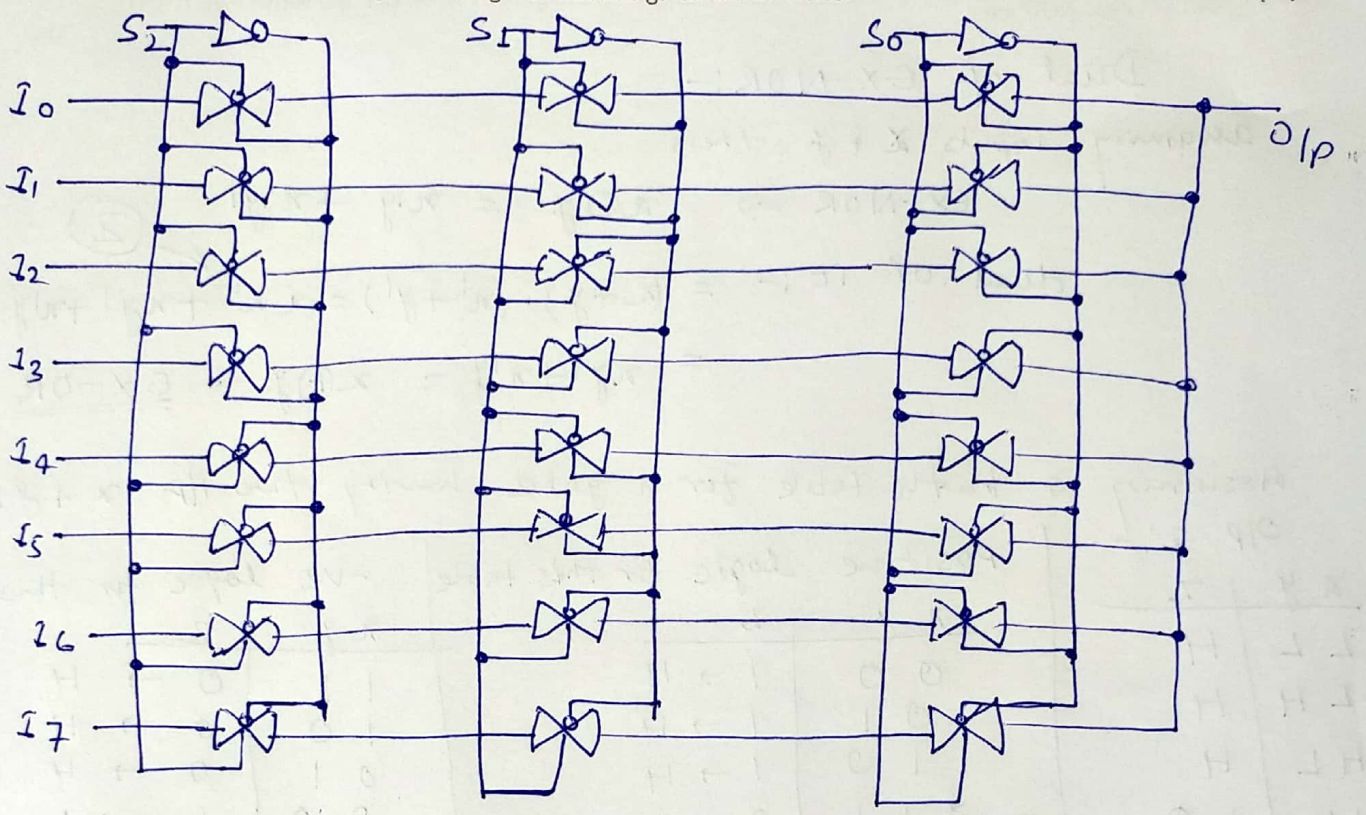
4. Construct a JK flip-flop using a D flip-flop a two-to-one line multiplexer and an inverter. [05]

Relationship bet^n D & JK $\Rightarrow$ $D = JQ' + K'Q$

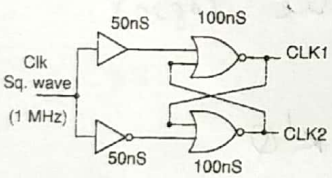
to implement this :-



5. Construct an eight-to-one line multiplexer using transmission gates and inverters. [05]



6. Find the output timing diagram for the circuit shown in the following figure: [05]



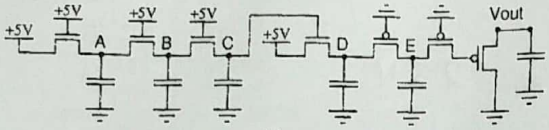
Non-overlaping clock pulses :-

Student's roll number: **Student's name:**

Important Notes: *This question paper consists of* ***two*** *sections having six questions in each, that is, total twelve questions.* ***Five*** *questions from each section are required to be answered. All questions carry equal marks.*

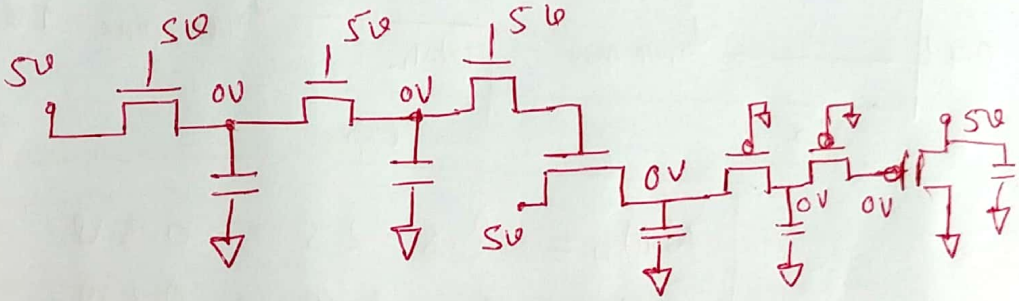
Section II

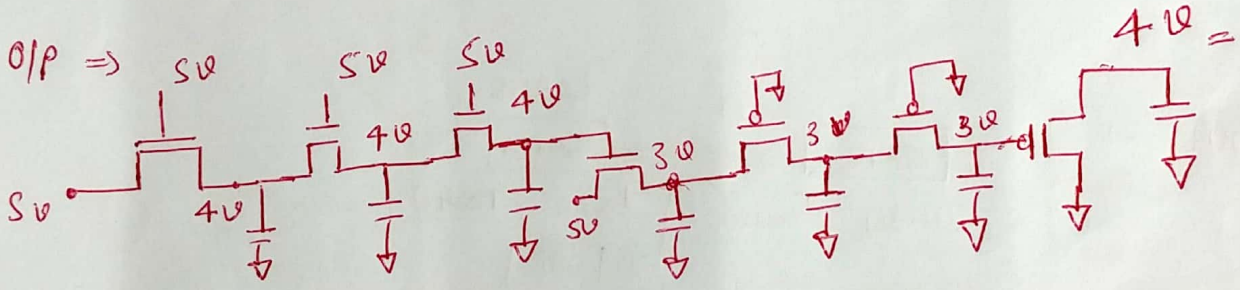
1. Find the output voltage V_{out} under steady state for the circuit shown in the following figure, where all nodes are discharged to 0V, except the output node V_{out} which is pre-charged at 5 Volts ($|V_{th,p}| = V_{th,p} = 1V$). [05]



(a)

initial Condition:

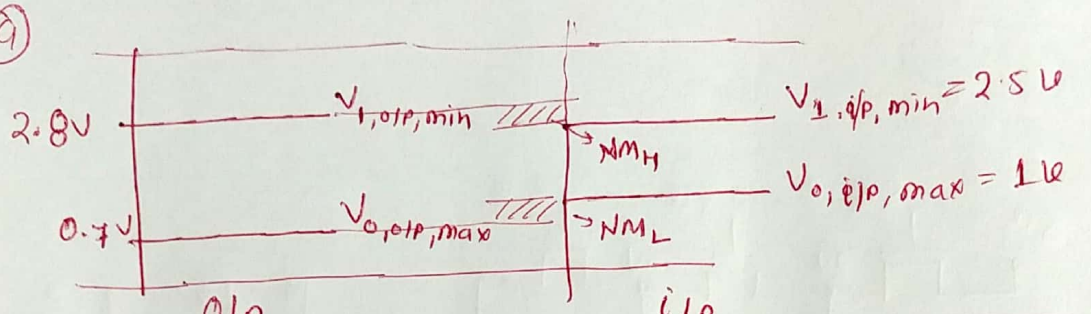




O/P = 4V Ans

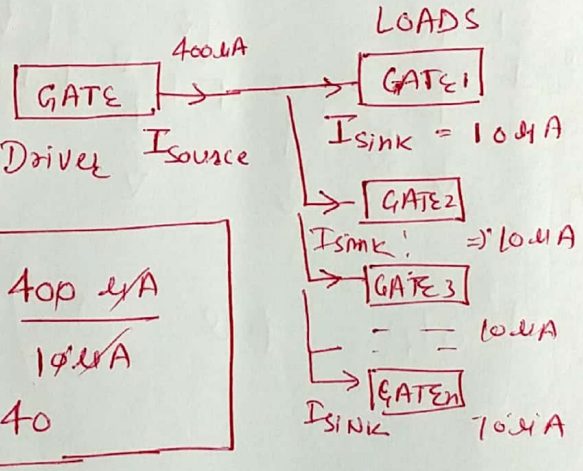
2. (a) Find **Fanout** (input and output) and **Noise Margin** (upper and lower) for TTL series logic gates with following ratings:
Max. voltage for logic '0' at i/p = $V_{IL,max}$ = 2.5 V, Max. voltage for logic '0' at o/p = $V_{OL,max}$ = 2.8 V,
Min. voltage for logic '1' at i/p = $V_{IL,min}$ = 1 V, Min. voltage for logic '1' at o/p = $V_{OL,min}$ = 0.7 V
Max. sourcing current from the i/p of a logic gate=0.1 mA,
Max. sinking current into the i/p of a logic gate=10 μA,
Max. sourcing current from the o/p of a logic gate = 400 μA,
Max. sinking current into the o/p of a logic gate = 8 mA. [05]

(a)



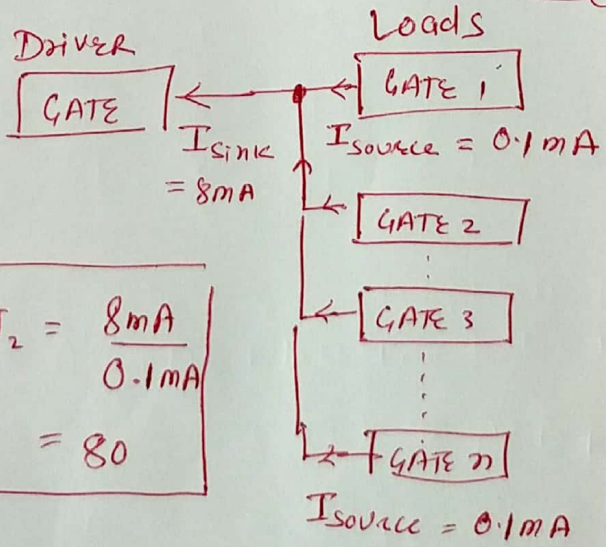
$NM_H = 2.8 - 2.5 = 0.3\ V$
$NM_L = 1 - 0.7 = 0.3\ V$ Ans.

(b) fanout :→



Any

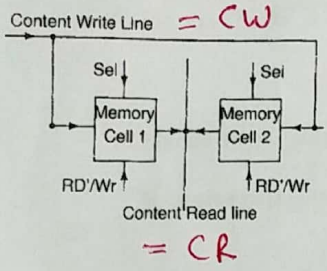
$FANOUT_1 = \frac{40\mu A}{10\mu A} = 40$

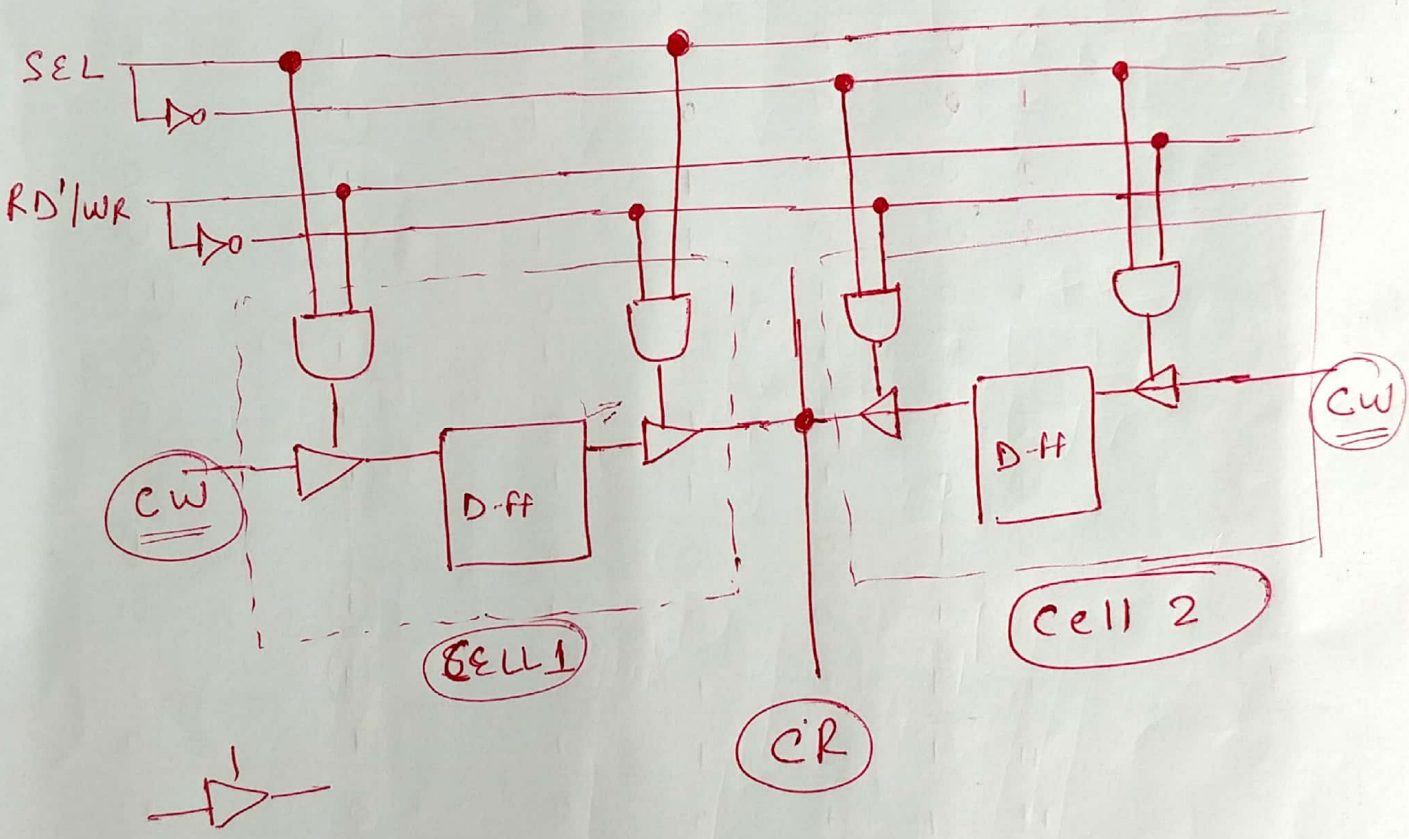


Any

$FANOUT_2 = \frac{8mA}{0.1mA} = 80$

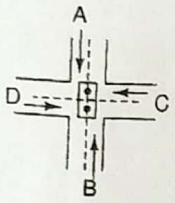
3. Design a memory cell for circuit shown in the following figure with following functions: - The memory cell 1 should select when Sel = '1', The memory cell 2 should select when Sel = '0'.
Operation: When a memory cell is selected, with RD'/WR = '0' the content of the respective memory cell must transfer to the "Content Read Line", and when RD'//WR = '1' the content of the "Content Write Line" transferred into the respective memory cell.
Use logic gates and D-FFs to implement the memory cell. [05]

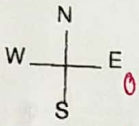




tristate Buffer

4. The following figure shows the intersection of a main highway with a secondary access road. Vehicle detection sensors are placed along lanes C and D (main road) and lanes A and B (access road). These sensor outputs are low (0) when no vehicle is present and High (1) when a vehicle is present. The intersection traffic light is to be controlled according to the following logic:
(1). The east-west (E-W) traffic light will be green whenever **both** lanes C and D are occupied.
(2). The E-W light will be green whenever **either** C or D is occupied **but** lanes A and B are not **both** occupied.
(3). The north-south (N-S) light will be green whenever **both** lanes A and B are occupied **but** C and D are not **both** occupied.
(4). The N-S will also be green when **either** A or B is occupied while C and D are **both** vacant.
(5). The E-W light will be green when **no** vehicle are present.
Using the sensor outputs A, B, C, and D as inputs, design a logic circuit to control the traffic light. There should be two outputs, N-S and E-W, that go high when the corresponding light is to be green.
*** **use your rough sheets for analysis and write ONLY the truth table and Boolean expression of outputs N-S and E-W as a function of A, B, C, and D in main answer sheet.** [05]





	A	B	C	D	E-W	N-S
0	0	0	0	0	1	0
1	0	0	0	1	1	0
2	0	0	1	0	1	0
3	0	0	1	1	1	0
4	0	1	0	0	0	1
5	0	1	0	1	1	0
6	0	1	1	0	1	0
7	0	1	1	1	1	0
8	1	0	0	0	0	1
9	1	0	0	1	1	0
10	1	0	1	0	1	0
11	1	0	1	1	1	0
12	1	1	0	0	0	1
13	1	1	0	1	0	1
14	1	1	1	0	X	1
15	1	1	1	1	1	0

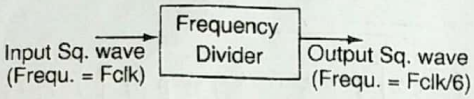
$E\text{-}W = \Sigma(0,1,2,3,5,6,7,9,10,11,15)$
$= A'B' + A'D + B'D + A'C + B'C + CD$

$N\text{-}S = \Sigma(4,8,12,13,14) = AB\bar{D} + ABC' + AC'D' + BC'D'$

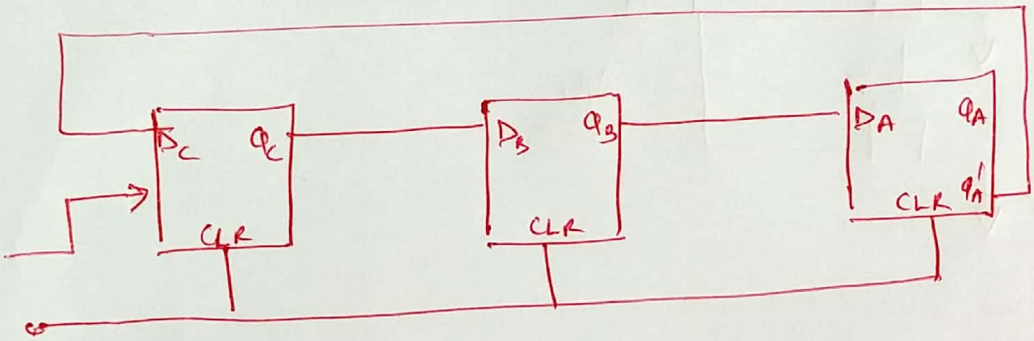
E-W OR N-S = '1' for "Verification"

5. Design a circuit (for the following figure) with input a square wave signal with fundamental frequency f_{clk} that produces another square wave signal with fundamental frequency $f_{clk}/6$ as output. [05]

Hint: A square wave signal has 50% duty cycle.



Johnson Counter with 3 Stages



CLR ⇒ "is must"

000
100
110
111
011
001
000
100

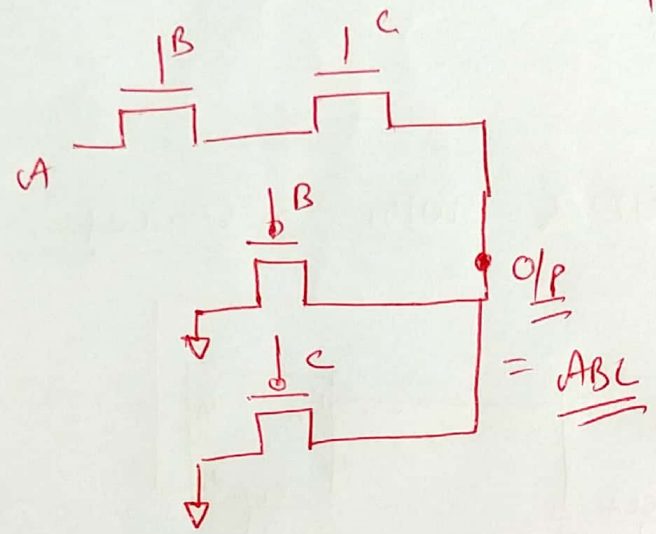
Repeat

6. Design expression Y = [A′BC + B′C + C′]′ with (a) Minimum number of MOS transistors (use PMOS and/or NMOS to implement) (b) Static CMOS logic. [05]

$Y = ABC$

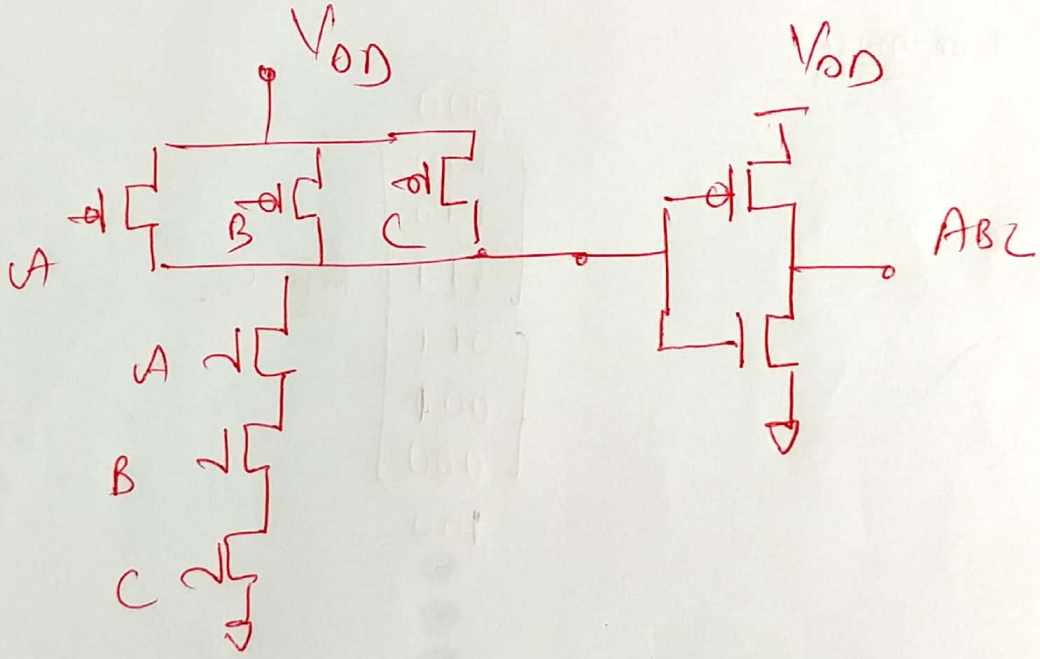
(after Simplification)

(a)



"4 transistors"

(b)



"8 transistors"