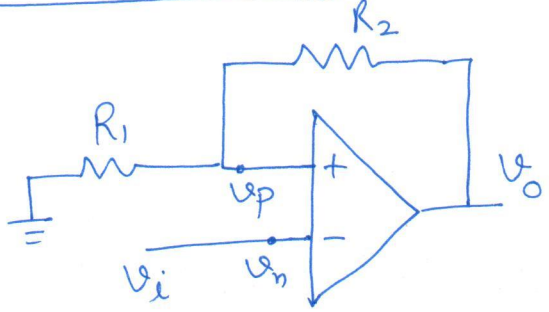
ELECTRONICS - I
END TERM SOLUTIONS.

1) If $v_o = +V_{cc} = +10V$.



$v_i = v_n = v_p$

KCL at v_p.

$$\frac{v_p - 0}{R_1} + \frac{v_p - 10}{R_2} = 0$$

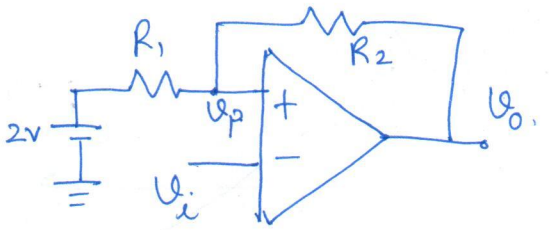
$$v_p\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = \frac{10}{R_2} \Rightarrow v_p = \frac{10R_1}{R_1 + R_2}$$

$$\Rightarrow v_i = \frac{10 \times 2}{6} = \frac{10}{3} V$$

(2)

Similarly for $v_o = -V_{cc} = -10V$ $\quad v_i = -\frac{10}{3} V$

For $v_o = 10V = +V_{cc}$.



KCL at v_p.

$$\frac{v_p - 2}{R_1} + \frac{v_p - 10}{R_2} = 0$$

$$v_p\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = \frac{2}{R_1} + \frac{10}{R_2}$$

$$\Rightarrow v_p = v_i = \left(\frac{2}{R_1} + \frac{10}{R_2}\right)\frac{R_1 R_2}{R_1 + R_2} = \left(\frac{2}{2} + \frac{10}{4}\right)\frac{8}{6}$$

$$= +\frac{14}{3} V$$

for $v_o = -10V$.

$$\frac{v_p - 2}{R_1} + \frac{v_p + 10}{R_2} = 0 \Rightarrow$$

(3)

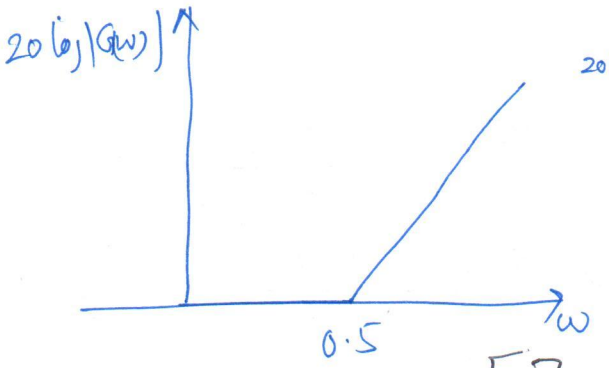
$$v_p\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = \frac{2}{R_1} - \frac{10}{R_2} \Rightarrow v_p = \left(\frac{2}{2} - \frac{10}{4}\right) \times \frac{2 \times 4}{2+4}$$

$$= -\frac{6}{3} = -2V$$

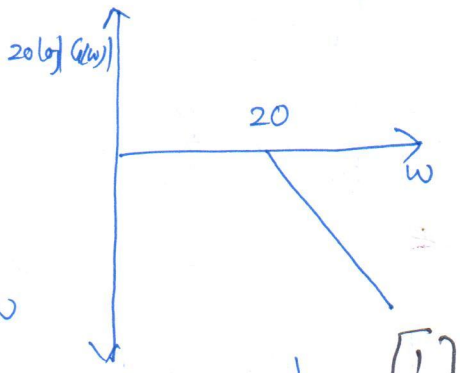
2) $$\frac{2000(jw+0.5)}{jw(jw+10)(jw+50)} = \frac{2000 \times \frac{1}{2}\left(\frac{jw}{0.5}+1\right)}{jw\times 10\left(\frac{jw}{10}+1\right)\times 50\left(\frac{jw}{50}+1\right)}$$

$$= \frac{2\left(\frac{jw}{0.5}+1\right)}{jw\left(\frac{jw}{10}+1\right)\left(\frac{jw}{50}+1\right)}$$

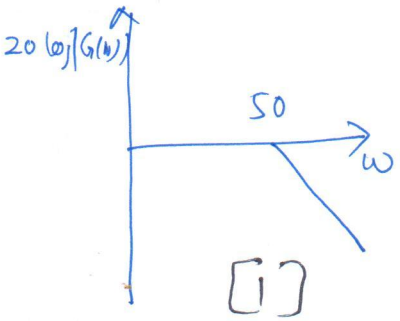
∴ Individual plots are.



$G(jw) = \left(\frac{jw}{0.5}+1\right)$ [1]

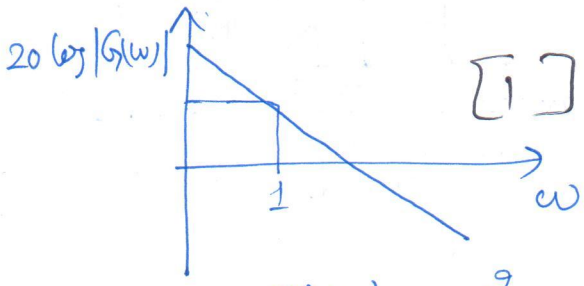


$G(jw) = \frac{1}{\left(\frac{jw}{10}+1\right)}$ [1]



[1]

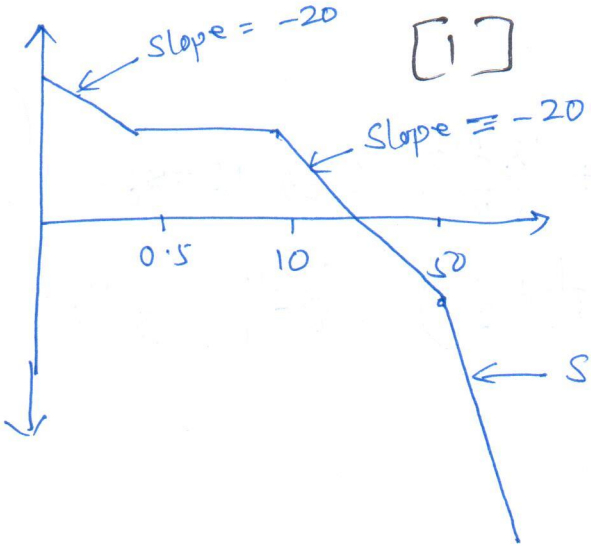
$G(jw) = \frac{1}{\left(\frac{jw}{50}+1\right)}$



[1]

$G(jw) = \frac{2}{jw}$.

∴ Total Graph.



[1]

3) Delay of flip flop = $T_{prop} + T_{setup} + T_{hold}$.

∴ Min delay of FF = 4 + 5 + 1 = 10 ns

Max " " " = 7 + 5 + 1 = 13 ns.

Delay of logic gate = T_{prop}.

∴ Min delay of gate = 2 ns, Max delay = 6 ns.

In path from A to V, output is dependent of P and Q.

∴ Total of 3 gates and 2 FF. [1]

Hex gate ! and FF C1 are in parallel. So the component with larger delay would be considered.

∴ T_{A-V} min = 2×10 + 3×2 = 26 ns

T_{A-V} max = 2×13 + 3×6 = 44 ns] [1]

Similarly for B to V. 2 FF and 3 gates. [1]

T_{B-V} min = 2×10 + 3×2 = 26 ns

T_{B-V} max = 2×13 + 3×6 = 44 ns.] [1]

For max clock frequency, we need minimum delay.

∴ $f_{max} = \frac{1}{T_{min}} = \frac{1}{26ns}$ = 38.46 MHz. [1].

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4) $v_p = \left(\frac{R/3}{R+\frac{R}{3}}\right)v_2 + \left(\frac{R/3}{R+\frac{R}{3}}\right)v_4 + \left(\frac{R/3}{R+\frac{R}{3}}\right)v_6$

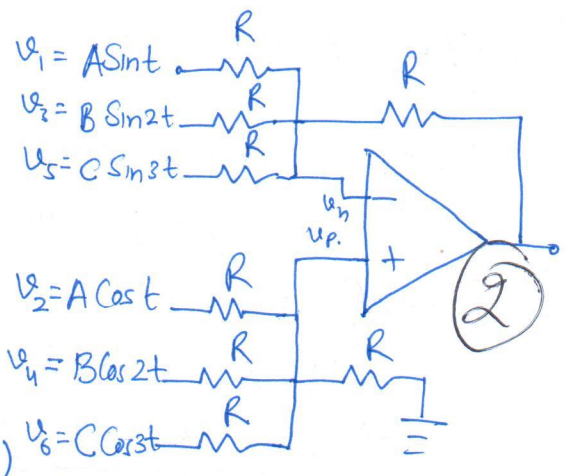
$= \frac{1}{4}(v_2 + v_4 + v_6)$ (3)

KCL at v_n = and put $v_p = v_n$

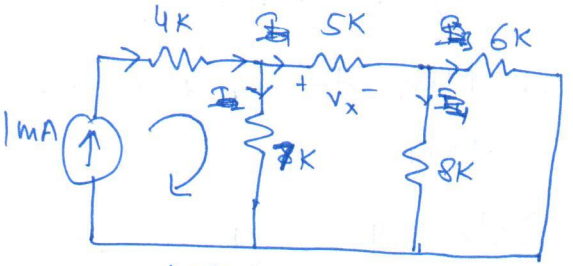
$\frac{v_p - v_1}{R} + \frac{v_p - v_3}{R} + \frac{v_p - v_5}{R} + \frac{v_p - v_0}{R} = 0$

$v_0 = 4v_p - (v_1 + v_3 + v_5)$

$= (v_2 - v_1) + (v_4 - v_3) + (v_6 - v_5)$



5) Considering only 1mA source.



$I_8 = 1mA$

KVL in loop 1

$4 \times 1 + 7(1 - I_2) = 0$ — (i)

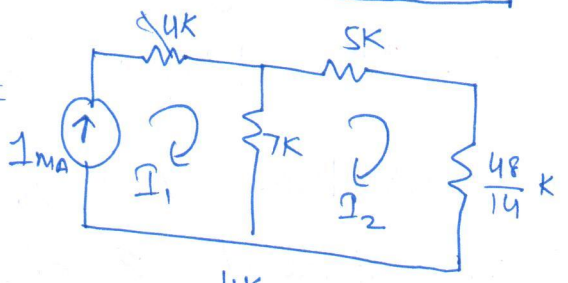
KVL in loop 2.

$5I_2 + \frac{48}{14} I_2 + 7(I_2 - I_1) = 0$ — (ii)

$4 + 7 - 7I_2 = 0$

$I_2 = \frac{11}{7}$ mA

=



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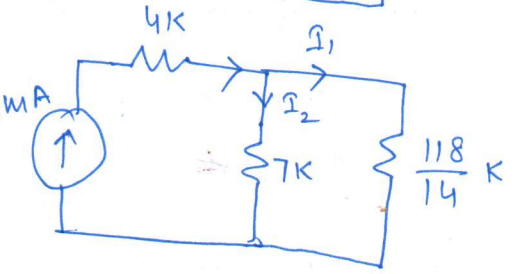
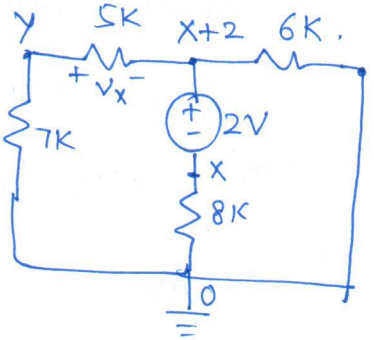


$I_1 = 1mA \times \frac{7K}{7K + \frac{118}{14}K} = \frac{7 \times 14}{216} = 0.45$ mA

$\therefore$ $V_{x_1} = I_1 \times 5k\Omega = 2.26$ V ✓

⟹ Considering only 2V source.



KCL at X.

$\frac{X-0}{8} + \frac{X+2-0}{6} + \frac{X+2-Y}{5} = 0$

$15X + 20X + 40 + 24X + 48 - 24Y = 0$

$59X - 24Y = -88$ — (i)

KCL at Y.

$\frac{0-Y}{7} + \frac{X+2-Y}{5} = 0$

$-5Y + 7X + 14 - 7Y = 0$

$7X - 12Y = -14$ — (ii)

(i) − 2(ii) ⇒

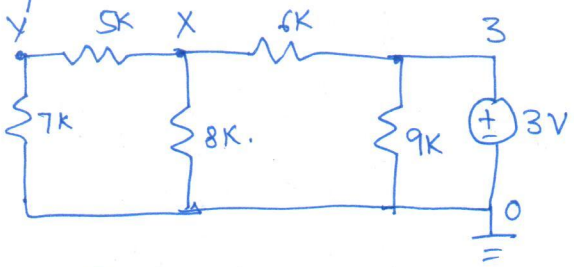
$45X = -60 \Rightarrow X = -\frac{4}{3}$ ✓

$\Rightarrow Y = \frac{7x - \frac{4}{3} + 14}{12} = \frac{14}{36}$ $\therefore V_X = Y - (X+2)$

$\frac{14}{36} + \frac{4}{3} - 2 = \frac{-10}{36}$

$(V_{x_2} = -0.277\,V)$

Considering only 3V source.



KCL at X: $\frac{X-3}{6} + \frac{X-0}{8} + \frac{X-Y}{5} = 0$

$20X - 60 + 15X + 24X - 24Y = 0$

$59X - 24Y = 60$ — (I)

KCL at Y: $\frac{0-Y}{7} + \frac{X-Y}{5} = 0$

$-5Y + 7X - 7Y = 0$

$7X - 12Y = 0$ — (II)

(I) − 2(II) ⇒ $45X = 60 \Rightarrow X = \frac{4}{3}$

$Y = \frac{7 \times \frac{4}{3}}{12} = \frac{28}{36} \quad \frac{7}{9}$.

$\therefore V_{X_3} = Y - X = \frac{7}{9} - \frac{4}{3} = \frac{7-12}{9} = \frac{-5}{9}$

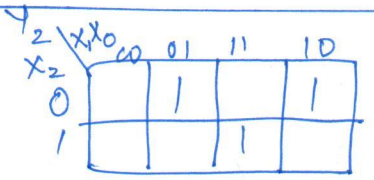
(2) $= -0.55$ V.

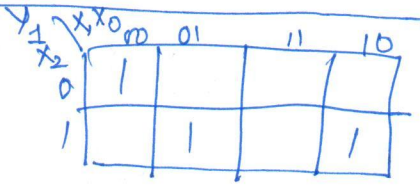
$\therefore$ Total $V_X = 2.26 - 0.277 - 0.55 = 1.42$ V.

6)

$X_2 X_1 X_0$	$Y_2 Y_1 Y_0$
0 0 0	0 1 1
0 0 1	1 0 0
0 1 0	1 0 1
0 1 1	0 0 0
1 0 0	0 0 1
1 0 1	0 1 0
1 1 0	0 1 1
1 1 1	1 0 0

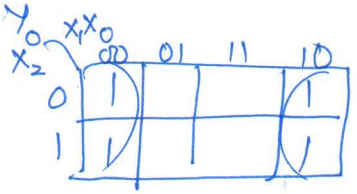
(2)





$Y_2 = \bar{X}_2 \bar{X}_1 X_0 + \bar{X}_2 X_1 \bar{X}_0 + X_2 X_1 X_0$

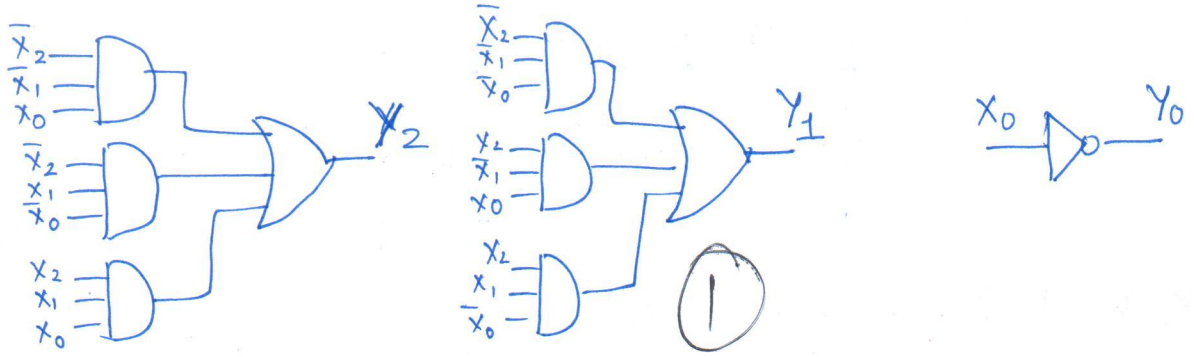
$Y_1 = \bar{X}_2 \bar{X}_1 \bar{X}_0 + X_2 \bar{X}_1 X_0 + X_2 X_1 \bar{X}_0$



$Y_0 = \bar{X}_0$

(2)

∴ Combinational ckt is

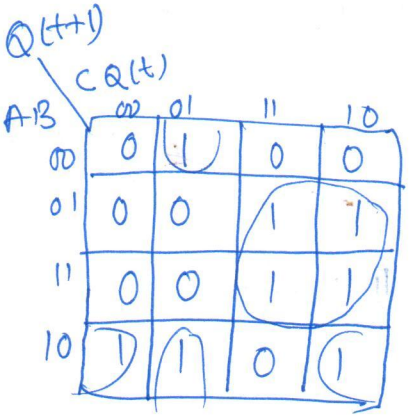


(1)

7) In charecteristics table 3 input variables A, B, C along with Q(t) would decide Q(t+1).

A	B	C	Q(t)	Q(t+1)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

(2)



$$Q(t+1) = BC + A\bar{B}\,\overline{Q(t)} + \bar{B}\bar{C}\,Q(t)$$

(1)

Excitation Table.

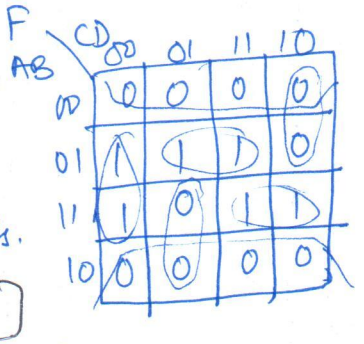
Q(t)	Q(t+1)	A	B	C
0	0	x	x	x
0	1	x	x	x
1	0	x	x	x
1	1	x	x	x

(2)

8)

$f = AB(C+D') + A'B(C'+D)$

$= ABC + ABD' + A'BC' + A'BD$



∴ SoP [1]

$f = B\bar{C}\bar{D} + \bar{A}BD + ABC$

or any other with only 3 products.

PoS [1]

$= F = (B)(\bar{A}+C+\bar{D})(A+\bar{C}+D)$ [1]

∴ SoP will be implemented using 3 AND + 1 OR. [1]

∴ PoS " " " " 2 OR & 1 AND.

∴ PoS would be better solution. [1]

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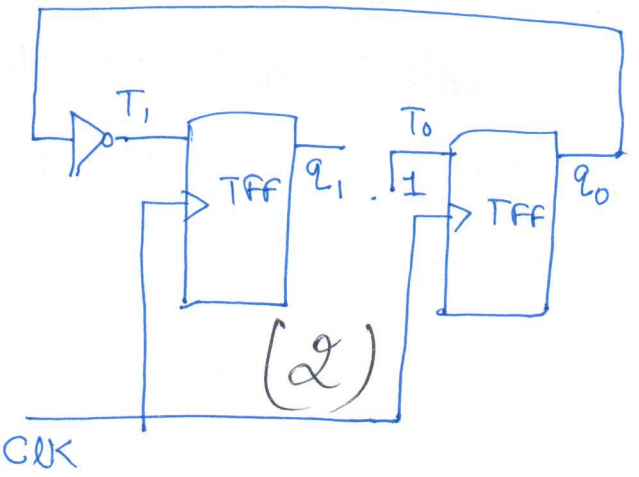
9)

$q_1 q_0$	$Q_1 Q_0$	$T_1 T_0$
0 0	1 1	1 1
0 1	0 0	0 1
1 0	0 1	1 1
1 1	1 0	0 1

(3)

∴ $T_0 = 1$

$T_1 = \bar{q}_0$



(2)

10)

$X_3 X_2 X_1 X_0$	With Shift = 1 $Y_3 Y_2 Y_1 Y_0$	With Shift = 0 $Y_3 Y_2 Y_1 Y_0$
0 0 0 0	0 0 0 0	0 0 0 0
0 0 0 1	0 0 1 0	0 0 0 1
0 0 1 0	0 1 0 0	0 0 1 0
0 0 1 1	0 1 1 0	0 0 1 1
0 1 0 0	1 0 0 0	0 1 0 0
0 1 0 1	1 0 1 0	0 1 0 1
0 1 1 0	1 1 0 0	0 1 1 0
0 1 1 1	1 1 1 0	0 1 1 1
1 0 0 0	0 0 0 0	1 0 0 0
1 0 0 1	0 0 1 0	1 0 0 1
1 0 1 0	0 1 0 0	1 0 1 0
1 0 1 1	0 1 1 0	1 0 1 1
1 1 0 0	1 0 0 0	1 1 0 0
1 1 0 1	1 0 1 0	1 1 0 1
1 1 1 0	1 1 0 0	1 1 1 0
1 1 1 1	1 1 1 0	1 1 1 1

[2] [1]

∴ The circuit doesn't do anything if Shift = 0.

and It shift X towards left by 1 bit by replacing LSB with 0 and excluding the overflown MSB.

[2]

∴ It is a left shifter.