LNMIIT
The LNM Institute of Information Technology

Digital Circuits and Systems

Mid Semester Exam-1

Date: 23rd August 2014 Time: 60 Minutes Max Marks. 30

Notes: All questions are compulsory. Marks of each question are mention against it.
Assumptions made should be written clearly.

1: Analyze the circuit given in figure 1. P and Q are inputs from two sensors which provide logic value 1 when the path is intercepted by an object. Provide the truth table for O/P in terms of P and Q. Make one general statement about the usability of the circuit. **[5]**

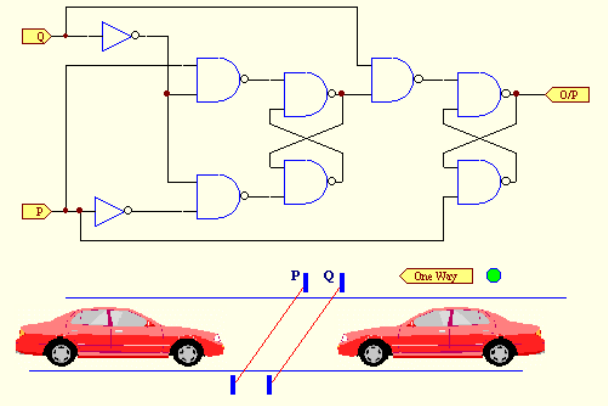

Figure 1

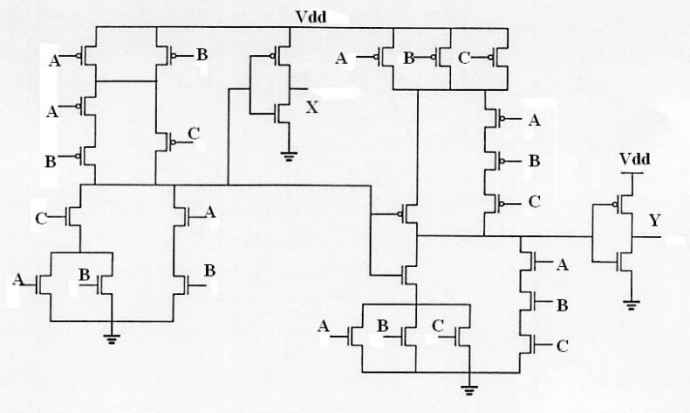

Figure 2

2: Implement the function Z = F (A, B, C) = ∑m (0, 1, 5, 6) using only one PFET and multiple NFETs. **[5]**

3: Consider the following system description.

Input: x(t) ϵ {0,1}
Output: z(t) ϵ {0,1}
Function: $z(t) = \begin{cases} 1 \ if \ x(t-4,t) = 11011 \\ 0 : Otherwise \end{cases}$

If input sequence from t=0 to t=15 is 0011011011101011 Then what is the output sequence. **[5]**

4: Analyze the circuit given in figure2. Provide the switching expressions for X and Y. Make one general statement about the usability of the circuit in real world. **[5]**

5: Design a CMOS circuit that implements the complement of F (A, B, C) = ∑m (1, 2, 4, 7). (Hint: You can always explore the possibility of cascading simple gates here). **[5]**

6: Describe a four-bit combinational circuit that works as a 2's complementer using binary specification. (The output generates the 2's complement of the input binary number.) **[5]**