LNMIIT
The LNM Institute of Information Technology

Electronics I
End Term Exam

Date: 17th November 2015 **Time: 180 Minutes** **Max Marks. 50**

Notes: Start every solution on fresh page.
Highlight your answers by inboxing or underlining them.
Assumptions made should be written clearly.

1. An Inverting Schmitt Trigger is shown in Figure 1. The output voltage can either be $+V_{CC}$ = 10V or $-V_{CC}$ = -10V. Find the value of switching thresholds V_{IL} and V_{IH} for the circuit if, R_2= 4kΩ and R_1 = 2k.Ω. Consider the circuit in figure 2 with same values of R_1 and R_2 and V_1 = 2V. Find the value of switching thresholds V_{IL} and V_{IH} for the circuit. **[5]**

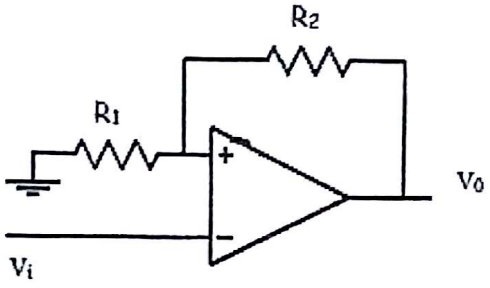

Figure 1

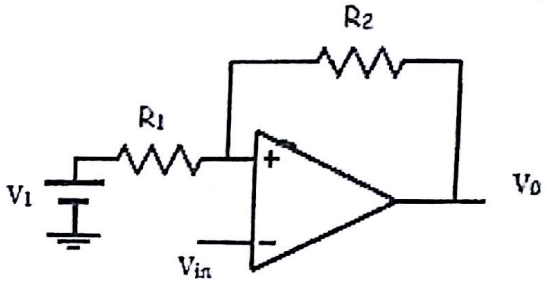

Figure 2

2. Plot the magnitude Bode plot for the system with transfer function

$$G(s) = \frac{2000(jw+0.5)}{jw(jw+10)(jw+50)}$$ **[5]**

3. In the circuit shown in figure 3, the setup and hold times of the flipflops are 5 ns and 1 ns respectively. The propagation delay of the flipflops (C1 can represent any flip flop) may vary between 4 and 7 ns while the propagation delay of the gates(& and ! can be any logic gate) may vary between 2 and 6 ns. Calculate the minimum and the maximum propagation delay T_{A-V} ~~and~~ and T_{B-V}. Hence calculate the maximum frequency of the clock, C. **[5]**

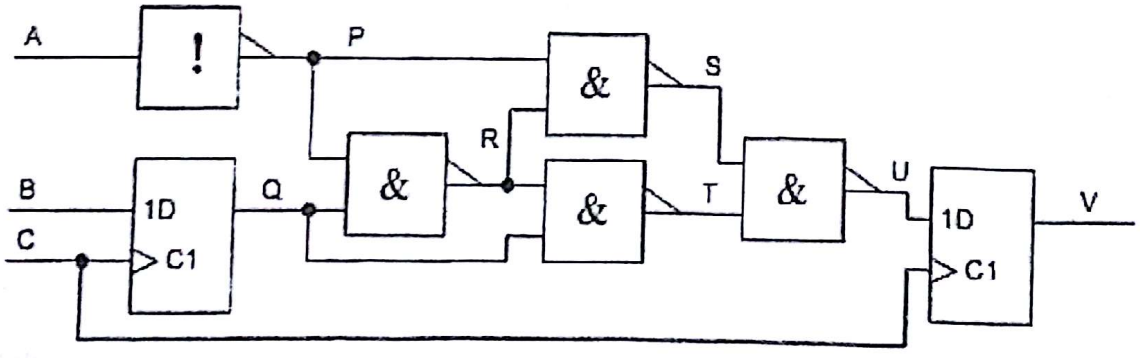

Figure 3

4. You are provided with various input signals like, ASint, BSin2t, CSin3t, ACost, BCos2t and CCos3t. Design a circuit whose output is A(Sint-Cost) + B(Sin2t-Cos2t) + C (Sin3t-Cos3t) **[5]**

5. Find out the value of Vx in figure 4 using Superposition theorem. [5]

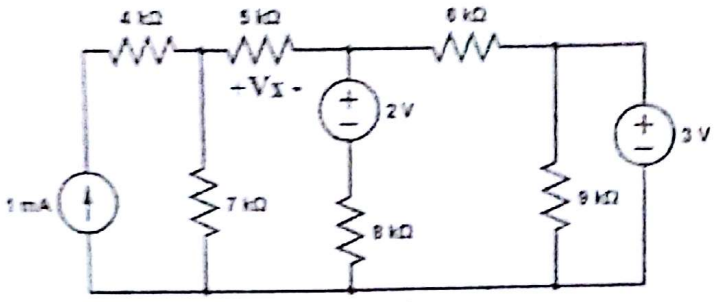

Figure 4

6. X is an integer with values from 0 to 7. Y = (X + 3) modulus 6. Design a combinational circuit that converts every value of X to corresponding value of Y. [5]

7. A new flip flop is designed with following description. It has 3 inputs A, B and C and output is Q. It holds the output if all inputs are 0 and flips the current output if all the inputs are 1. If the number of 1's in inputs are 1, then it resets the output to 0 and sets the output to 1 if the number of 1s are 2. Write down the characteristic table, characteristic function and excitation table for this flip flop. [5]

8. Simplify the expression F = AB(C + D') + A'B(C' + D) using a K-map. Write down the optimized SoP and PoS for F. Neglecting NOT gates in the design, which expression (SoP or PoS) can be implemented with less number of logic gates? [5]

9. Design a 2 bit down counter using T flip flops and logic gates. [5]

10. Observe the circuit given in Figure 5. Consider Shift ='1', then write down the truth table expressing the relation of X with Y. Write down another similar truth table when Shift = '0'. Looking at the output patterns of both the Truth tables and what can you say about the behaviour of the circuit? [5]

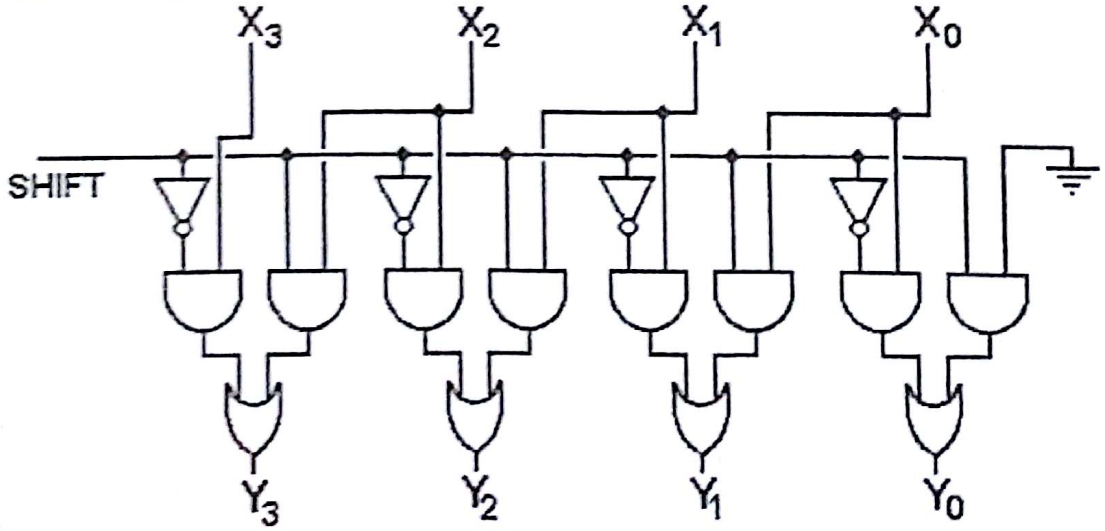

Figure 5