Date: 27th November, 2018 **Time:** 3 hours Max. Marks (Part - A): **10**
Max. Marks (Part - B): **50**

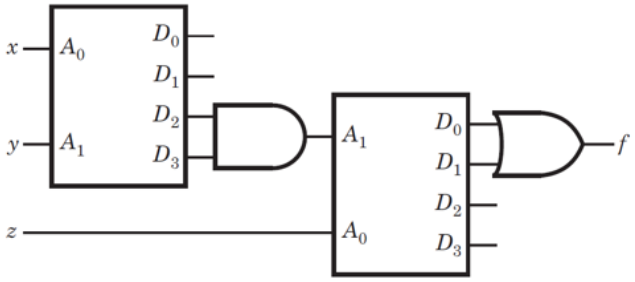
Instructions:

1. *This question paper has total **6** pages, including this page.*
2. *This question paper consists of **Part A** (10 marks) and **Part B** (50 marks). There is no negative marking.*
3. *Part - A has 8 multiple choice questions. **All questions are compulsory.***
4. *Part - B has 6 questions of 10 marks each. **Attempt any 5 questions.***
5. *Start each answer on a fresh page and **highlight** your answers.*

Part - A (Quiz 4)

NO credit will be given if answer is not correct for Part - A

MCQ 1) A logic circuit consists of two 2X4 decoders as shown below: **[2]**



The outputs of the decoders are as follows:
$D_0 = 1$ when $A_0 = 0, A_1 = 0$ $D_1 = 1$ when $A_0 = 1, A_1 = 0$
$D_2 = 1$ when $A_0 = 0, A_1 = 1$ $D_3 = 1$ when $A_0 = 1, A_1 = 1$
The value of f(x,y,z) is:
[A] 0 **[B]** z **[C]** $\overline{z}$ **[D]** 1

Solution: D

MCQ 2) What is one disadvantage of an S-R flip-flop? **[1]**
[A] It has no enable input. **[B]** It has an invalid state.
[C] It has no clock input. **[D]** Possibility of race-around condition when both inputs are high.

Solution: B

MCQ 3) A group of 4 bits is known as **[1]**
[A] a nibble **[B]** a byte **[C]** a q-bit **[D]** a quad

Solution: A

MCQ 4) Let $(A2C)_{16} = (X)_8$. Then X is given by: **[1]**
[A] 7054 **[B]** 6054 **[C]** 5154 **[D]** 5054

Solution: D

MCQ 5) How many NOR gates are required to realise a AND gate? **[1]**

[A] 2 **[B]** 3 **[C]** 4 **[D]** 5

Solution: B

MCQ 6) How many select lines are contained in a multiplexer with 1024 inputs and one output? **[1]**

[A] 512 **[B]** 258 **[C]** 64 **[D]** 10

Solution: D

MCQ 7) If functions *W, X, Y* and *Z* are as follows: **[2]**

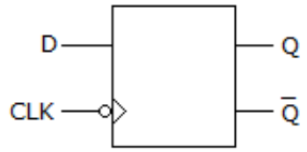
$$W = R + \overline{P}Q + \overline{R}S$$
$$X = PQ\overline{R}\,\overline{S} + \overline{P}\,\overline{Q}\,\overline{R}\,\overline{S} + P\overline{Q}\,\overline{R}\,\overline{S}$$
$$Y = RS + \overline{PR + P\overline{Q} + \overline{P}\,\overline{Q}}$$
$$Z = R + S + \overline{PQ + \overline{P}\,\overline{Q}\,\overline{R} + P\overline{Q}\,\overline{S}}$$

Then

[A] $W = Z, X = \overline{Z}$ **[B]** $W = Z, X = Y$ **[C]** $W = Y$ **[D]** $W = Y = \overline{Z}$

Solution: A

MCQ 8) The symbols on the flip-flop shown below indicate: **[1]**



[A] triggering takes place on the negative-going edge of the CLK pulse
[B] triggering takes place on the positive-going edge of the CLK pulse
[C] triggering can take place anytime during the HIGH level of the CLK waveform
[D] triggering can take place anytime during the LOW level of the CLK waveform

Solution: A

Part - B (Main Exam)

Q1) a) A series resonant circuit has ***L = 1mH*** and ***C = 10μF***. Calculate the value of ***R*** required if the bandwidth ***BW = 15.9 Hz***. 74/9 **[2]**

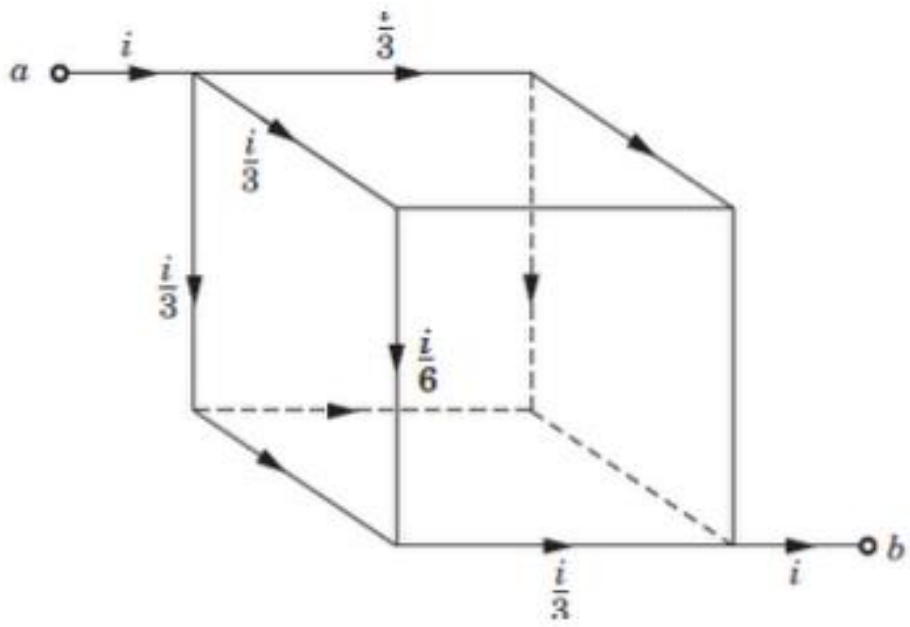
Solution:

$$\text{BW} = \frac{R}{L}$$ 1

$$\Rightarrow \quad \frac{R}{1\times 10^{-3}} = 15.9 \times 2\pi = 0.1\Omega$$ 1

b) Twelve ***6Ω*** resistors are placed along each edge of a cube. Calculate the equivalent resistance between any two diagonally opposite corner points. **[2]**

Solution:



From the above image, due to symmetry and all resistances being same (6 ohm), current *i* will split as shown above.

Total current between 2 diagonally opposite edges will be –

$i_{eq} = i/3 + i/6 + i/3 = 5i/6$

$V = i_{eq}R = 5i/6 \times 6 = 5i$

Veq = Req x I

Req = 5Ω

NO partial credit

Note: Students who have correctly and fully solved the problem assuming Req for face diagonal instead of body diagonal, will get full credit.

c) For the circuit given below, find i_1:

[3]

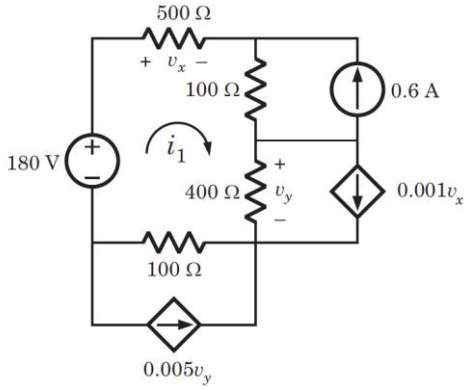


Figure 1.c

Solution:

$$v_x = 500i_1$$

1.5

$$v_y = 400(i_1 - 0.001v_x) = 400\,(i_1 - 0.5i_1) = 200i_1$$

$$180 = 500i_1 + 100(i_1 - 0.6) + 200i_1 + 100(i_1 + 0.005v_y)$$

$$180 = 900i_1 - 60 + 100 \times 0.005 \times 200i_1$$

1.5

$$i_1 = 0.12 \text{ A}$$

d) For the circuit given below, find $i(t)$:

[3]

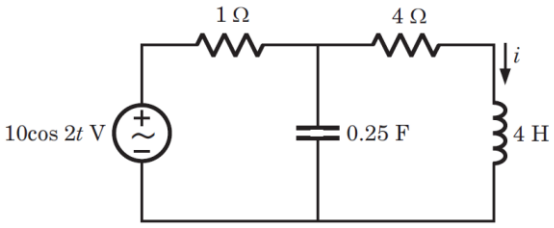


Figure 1.d

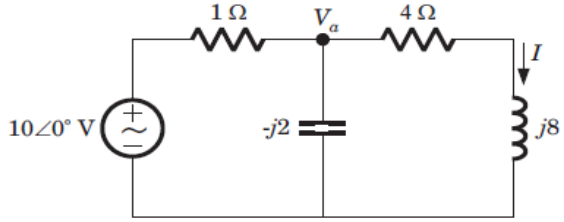
Solution:

$$V_a = \frac{\frac{10\angle 0}{1}}{\frac{1}{1} + \frac{1}{-j2} + \frac{1}{4 + j8}} = \frac{10\angle 0}{1.05 + j0.4} \text{ V}$$

1.5

$$I = \frac{V_a}{4 + j8} = \frac{10\angle 0}{1 + j10} = 1\angle -84.23 \text{ A}$$

1.5



$$i(t) = \cos\,(2t - 84.23°) \text{ A}$$

Q2) a) Calculate the Thevenin's equivalent resistance R_{Th} for the following circuit: **[3]**

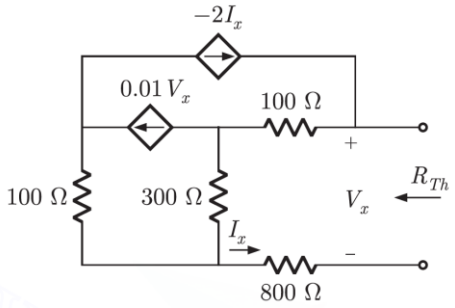
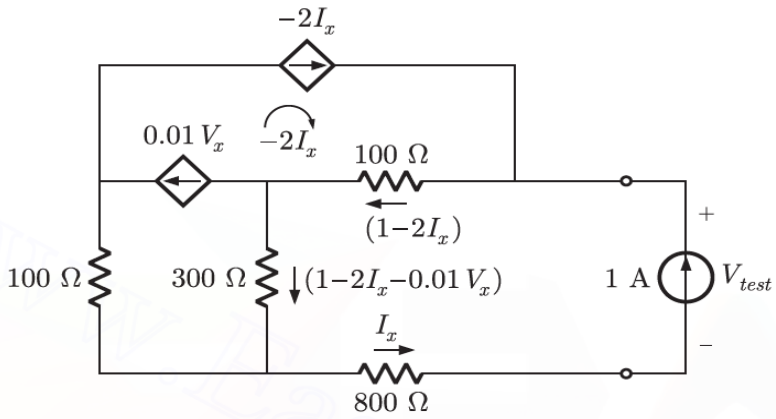


Figure 2.a

Solution:

Writing currents into 100 Ω and 300 Ω resistors by using KCL as shown in figure.



$$I_x = 1 \text{ A},\ V_x = V_{test}$$

Writing mesh equation for bottom right mesh.

$$V_{test} = 100(1 - 2I_x) + 300(1 - 2I_x - 0.01\,V_x) + 800 = 100 \text{ V}$$ 1.5

$$R_{Th} = \frac{V_{test}}{1} = 100\,\Omega$$ 1.5

b) For the network shown below: **[2]**

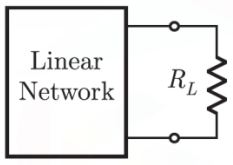


Figure 2.b

R_L	10 kΩ	30 kΩ
P	3.6 mW	4.8 mW

Table 2.b

The power absorbed by load resistor R_L is shown in the table 2.b above. At what value of R_L would the power absorbed be maximum?

Solution:

For $R_L = 10\,\text{k}\Omega$, $V_{ab1} = \sqrt{10\text{k} \times 3.6\text{m}} = 6$ V

For $R_L = 30\,\text{k}\Omega$, $V_{ab2} = \sqrt{30\text{k} \times 4.8\text{m}} = 12$ V

$$V_{ab1} = \frac{10}{10 + R_{Th}} V_{Th} = 6 \quad \ldots(\text{i})$$

$$V_{ab2} = \frac{30}{30 + R_{Th}} V_{Th} = 12 \quad \ldots(\text{ii})$$

Dividing equation (i) and (ii), we get $R_{Th} = 30\,\text{k}\Omega$. Maximum power will be transferred when $R_L = R_{Th} = 30\,\text{k}\Omega$.

1

1

c) In the following second order circuit, the switch is moved from position a to b at t = 0. Find $i_L(t)$ for t > 0. **[3]**

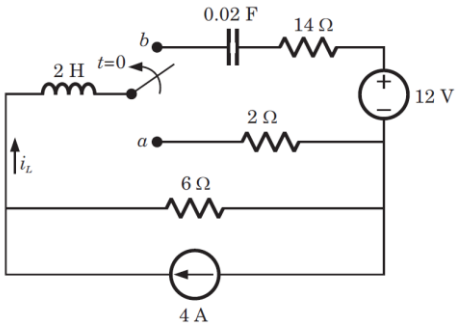


Figure 2.c

Solution:

$$v_C(0) = 0, \qquad i_L(0) = \frac{4 \times 6}{6 + 2} = 3$$

$$0.02 \frac{dv_C(0)}{dt} = i_L(0) = 3 \quad \Rightarrow \quad \frac{dv_C(0)}{dt} = 150$$

$$\alpha = \frac{6 + 14}{2 \times 2} = 5, \qquad \omega_o = \frac{1}{\sqrt{2 \times 0.02}} = 5$$

1

$\alpha = \omega_o$ critically damped

1

$$v(t) = 12 + (A + Bt)e^{-5t}$$

$$0 = 12 + A, \quad 150 = -5A + B \quad \Rightarrow \quad A = -12, \quad B = 90$$

$$v(t) = 12 + (90t - 12)e^{-5t}$$

$$i_L(t) = 0.02(-5)\, e^{-5t}(90t - 12) + 0.02(90)e^{-5t} = (3 - 9t)e^{-5t}$$

1

d) Calculate R_{eq}:

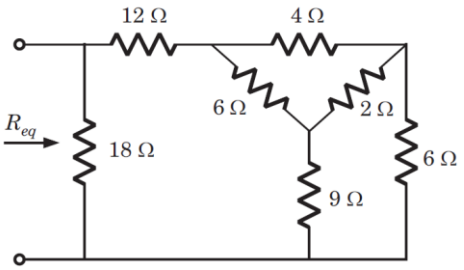
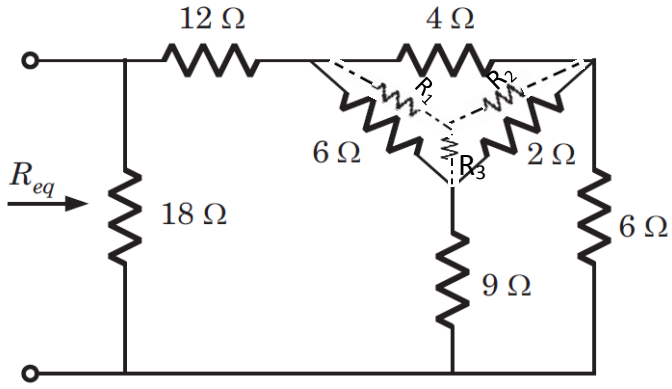


Figure 2.d

[2]

Solution:

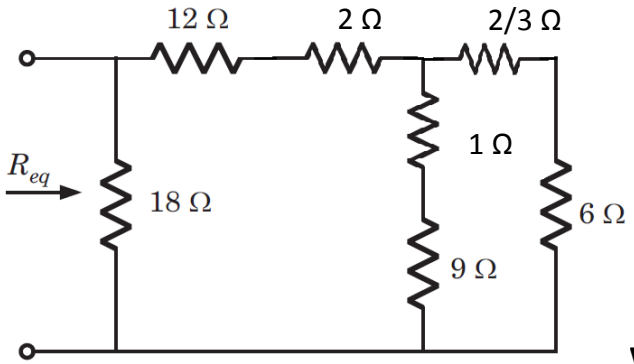


Converting Delta to Star –

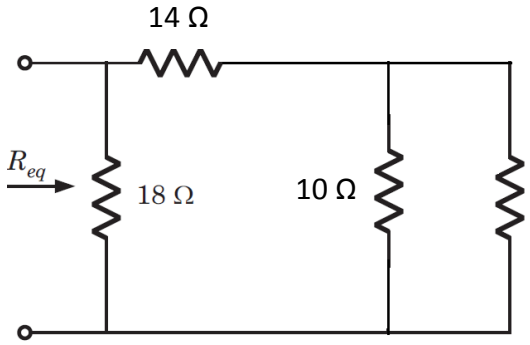
R_1 = 24/12 = 2

R_2 = 8/12 = 2/3

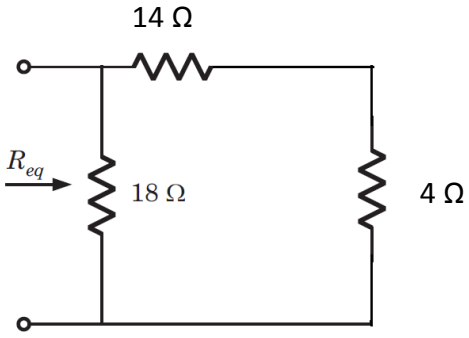
R_3 = 12/12 = 1



which equals to :



which equals to :



= 9Ω

NO partial credit

Q3) a) For the following circuit, derive the expression for transfer function ***H(ω)*** : **[2]**

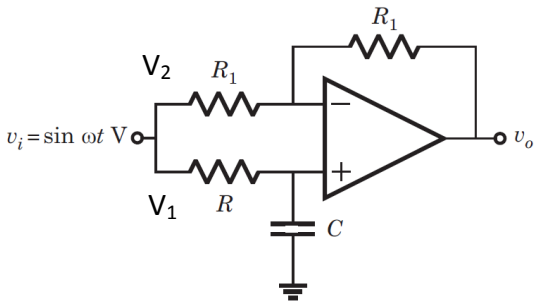


Figure 3.a

Solution:

Applying Superposition theorem:

$$v_0 = \frac{v_1 \frac{1}{j\omega C}}{R+\frac{1}{j\omega C}} \left[1 + \frac{R_1}{R_1}\right] + v_2[-1]$$ 1

But, $v_2 = v_1$

$$v_0 = v_1[\frac{2}{1 + j\omega RC} - 1]$$

$$\frac{v_0}{v_1} = \frac{2 - 1 - j\omega RC}{1 + j\omega RC}$$

$$\frac{v_0}{v_1} = \frac{1-j\omega RC}{1+j\omega RC}$$

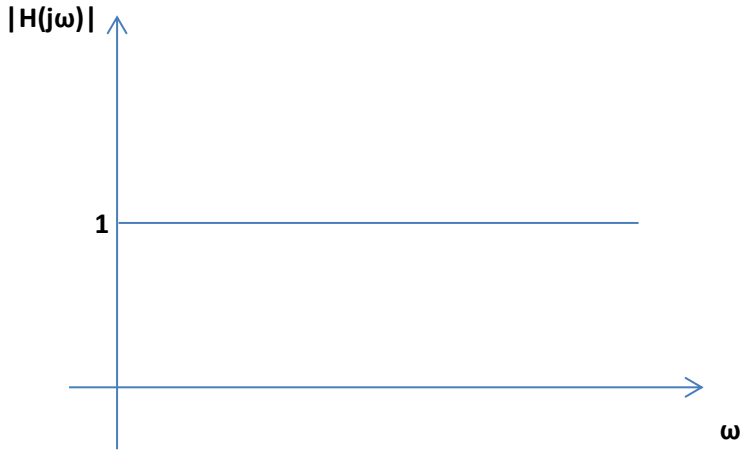
= H(ω) 1

b) Draw the Gain plot for ***H(ω)*** obtained in Q3 a. **[2]**

Solution:

$$\frac{v_o}{v_i} = H(j\omega) = \frac{1 - j\omega RC}{1 + j\omega RC}, \quad |H(j\omega)| = \frac{\sqrt{1 + (\omega RC)^2}}{\sqrt{1 + (\omega RC)^2}} = 1$$

1



1

c) For the opamp circuit given below, derive the expression for differential gain, G = $\frac{V_o}{V_2 - V_1}$. **[3]**

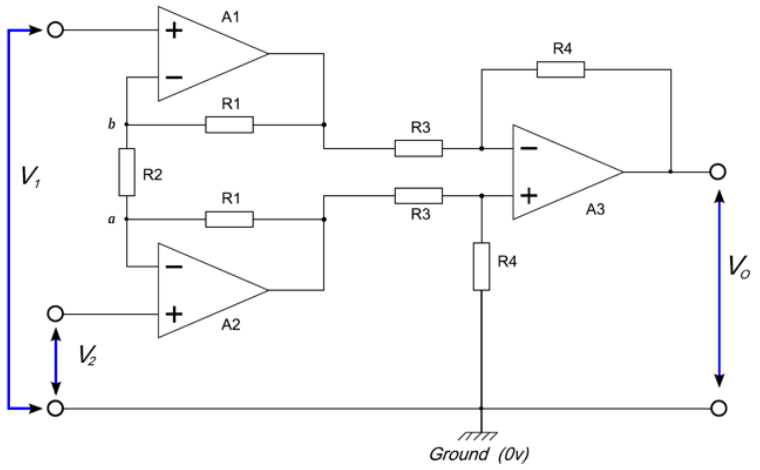


Figure 3.c

Solution: Derivation of Instrumentation Amplifier.

$$\frac{R_4}{R_3}\left[1 + \frac{2R_1}{R_2}\right]$$

2

1 mark will be given based on attempt

d) For the circuit given below: **[3]**

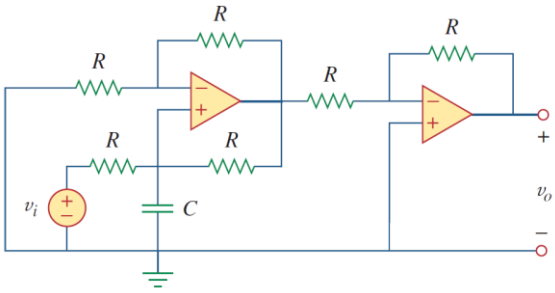


Figure 3.d.i

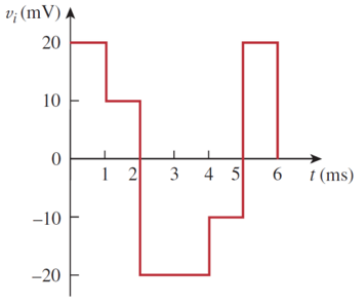
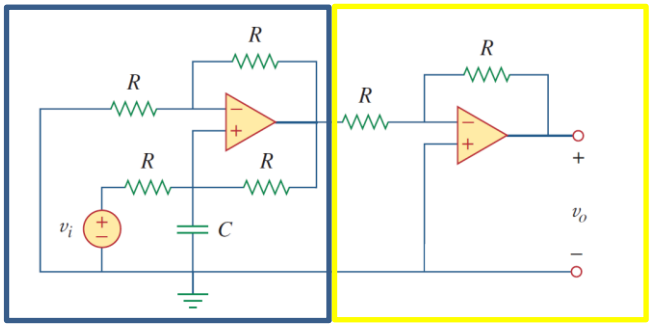


Figure 3.d.ii

Draw the output $v_o(t)$ waveform for the input $v_i(t)$ given above, if ***R = 4MΩ*** and ***C = 2μF***.

Solution:



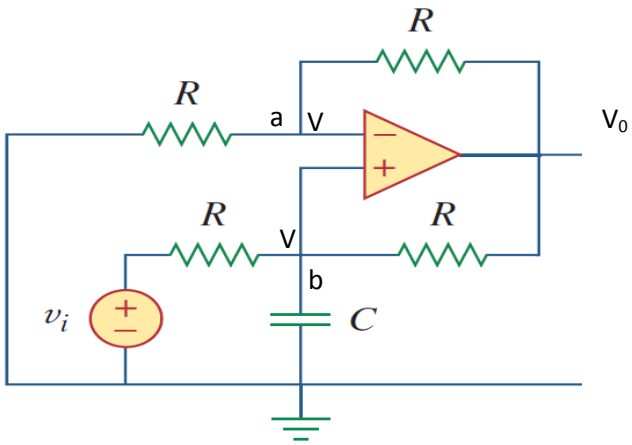
Stage 1 Stage 2

Stage 2 is unity gain Inverting amplifier.

Let, $V_a = V_b = V$

At node a, $\frac{0-V}{R} = \frac{V-V_0}{R}$

$V = V_0/2$ ------- (i)



Stage 1 : At node b,

$$\frac{V_i - V}{R} = \frac{V - V_0}{R} + C\frac{dV}{dt}$$

$$V_i = 2V - V_0 + RC\frac{dV}{dt} \qquad \text{--------- (ii)}$$

Combining (i) and (ii)

$$V_i = V_0 - V_0 + \frac{RC}{2}\frac{dV_0}{dt}$$

Or, $V_0 = \frac{2}{RC}\int V_i dt$

Thus, Stage 1 is functioning like a non-inverting integrator.

Stage 1 is cascaded with Stage 2, thus, the complete circuit functions as an inverting integrator.

Therefore, $V_0 = -\frac{2}{RC}\int V_i dt$ 1

Waveform representation:

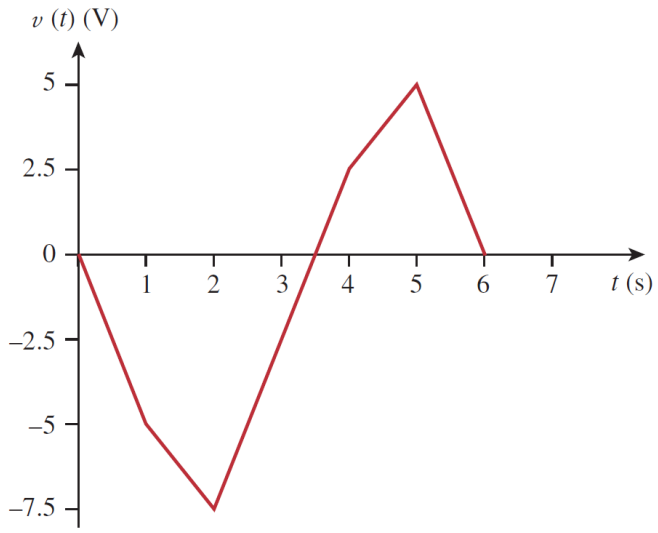
$$V_0 = -\frac{2}{RC}\int V_i dt = -\frac{1}{4}\int V_i dt$$

For 0 < t < 1, $V_i = 20$, $V_0 = -\frac{1}{4}\int_0^t 20dt = -5t\ mV$

For 1 < t < 2, $V_i = 10$, $V_0 = -\frac{1}{4}\int_1^t 10dt + V(1) = -2.5t - 2.5\ mV$ 1

Similarly, continue for other timestamps.

Thus, $V_0(t)$ is represented as:



1

Q4) a) For the opamp amplifier circuit below, calculate the value of ***R*** so that the closed loop gain $A_v = v_o/v_i = -10$.

[2]

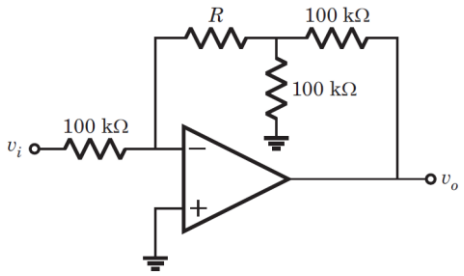
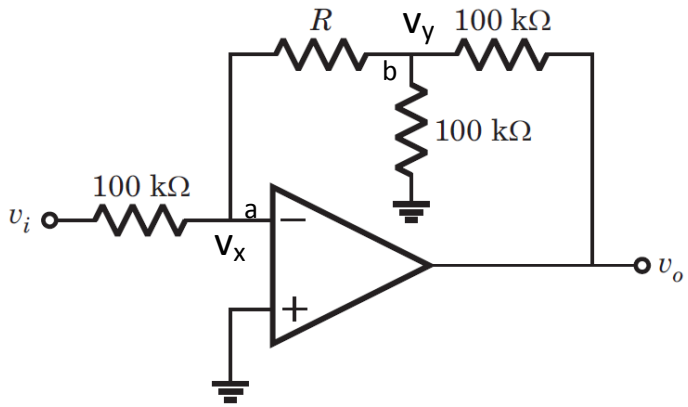


Figure 4.a

Solution:



Using virtual short, $V_x = 0$

Applying KCL at node a,

$$\frac{V_x - V_i}{100K} = \frac{V_y - V_x}{R} \Rightarrow \frac{-V_i}{100K} = \frac{V_y}{R} \quad \text{------ (i)}$$

Nodal analysis at node b,

$$\frac{V_y - V_x}{R} + \frac{V_y}{100K} + \frac{V_y - V_0}{100K} = 0 \quad \text{As } v_x = 0;$$

$$\frac{100K}{R}V_y + V_y + V_y - V_0 = 0 \Rightarrow V_0 = (2 + \frac{100K}{R})V_y \quad \text{------- (ii)}$$

1

Taking ratios of eq. i and ii

$$\frac{V_0}{V_i}(-100K) = \frac{(2 + \frac{100K}{R})V_y}{\frac{V_y}{R}}$$

$$\frac{V_0}{V_i}(-100K) = 2R + 100K$$

But, $V_0/V_i = -10$ (from given question)

∴ 1000 K = 2R +100K

⇨ 2R = 900 kΩ

⇨ **R = 450 kΩ**

1

b) Derive the transfer function ***H(ω)*** for the following circuit. Identify the type of filter. **[3]**

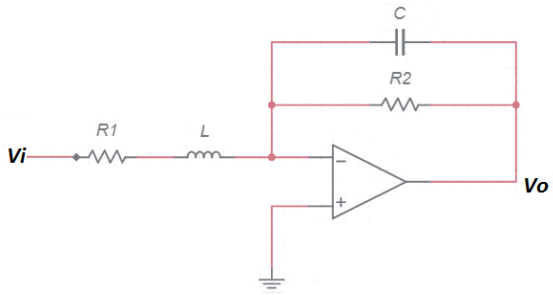


Figure 4.b

Solution:

$H(\omega) = V_0/V_i = -R_f/R_i$ as this is inverting mode

$$R_f = R_2 || \frac{1}{j\omega C} = \frac{R_2}{j\omega C(R_2 + \frac{1}{j\omega C})} = \frac{R_2}{1 + j\omega R_2 C}$$

$R_i = R_1 + j\omega L$

$$H(\omega) = -\frac{R_2}{(1+j\omega R_2 C)(R_1+j\omega L)} = \frac{-R_2}{R_1}\left[\frac{1}{(1+j\omega\frac{L}{R_1})(1+j\omega R_2 C)}\right]$$

2

At ω=0, $|H(\omega)| = -R_2/R_1$ ------ passband or DC gain

At ω = infinite, $|H(\omega)| = 0$

Filter behaves as a low-pass filter

1

c) Design a 4-bit BCD to Excess – 3 (XS-3) code converter. Use sum of products (minterms) format. **[3]**

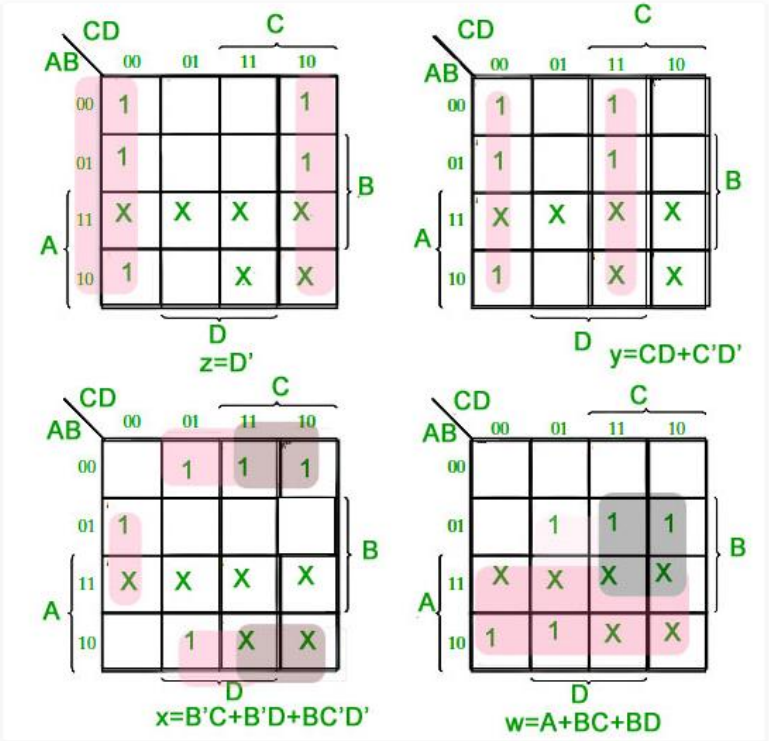
Solution:

Let $A, B, C, and\ D$ be the bits representing the binary numbers, where D is the LSB and A is the MSB, and Let $w, x, y, and\ z$ be the bits representing XS-3 code of the binary numbers, where z is the LSB and w is the MSB. The truth table for the conversion is given below. The X's mark don't care conditions.

BCD(8421)				Excess-3			
A	B	C	D	w	x	y	z
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	X	X	X	X
1	0	1	1	X	X	X	X
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

1

To find the corresponding digital circuit, we will use the K-Map technique for each of the Excess-3 code bits as output with all of the bits of the BCD number as input.

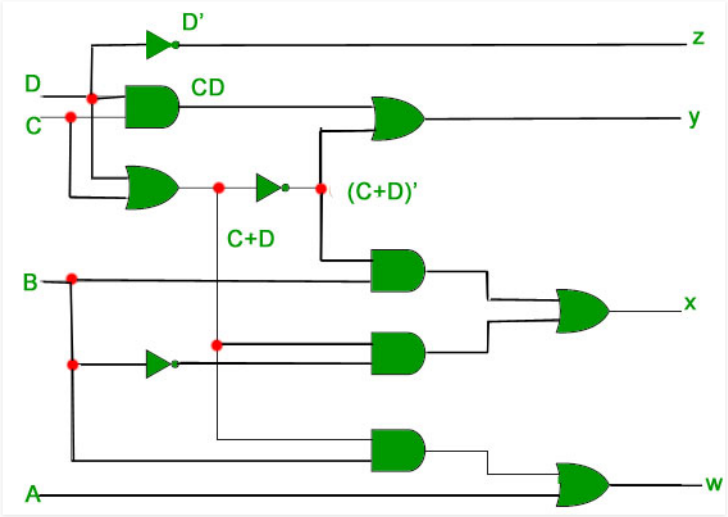


1.5

Corresponding minimized Boolean expressions for Excess-3 code bits –

$$w = A + BC + BD$$
$$x = B'C + B'D + BC'D'$$
$$y = CD + C'D'$$
$$z = D'$$

The corresponding digital circuit-



0.5

d) Verify if the Boolean expression $(A + \overline{B})(\overline{A} + B) = \overline{AB} + AB$ is true, using truth tables. **[2]**

Solution:

A	B	$\overline{A}$	$\overline{B}$	$(A + \overline{B})$	$(\overline{A} + B)$	$(A + \overline{B})(\overline{A} + B)$	AB	$\overline{AB}$	$\overline{AB} + AB$
0	0	1	1	1	1	1	0	1	1
0	1	1	0	0	1	0	0	1	1
1	0	0	1	1	0	0	0	1	1
1	1	0	0	1	1	1	1	0	1

Since, LHS ≠ RHS, the given Boolean expression is FALSE.

No partial credit

Q5) a) A lawn sprinkling system is controlled automatically by certain combinations of the following variables: 112 **[3]**

- Season (S = 1 if summer, S = 0 otherwise)
- Moisture content of soil (M = 1 if high, M = 0 if low)
- Outside temperature (T = 1 if high, T = 0 if low)
- Outside humidity (H = 1 if high, H = 0 if low)

The sprinkler should be turned on under any of the following conditions:

- The moisture content is low in winter.
- Temperature is high and moisture content is low in summer.
- Temperature and humidity both are high in summer.
- Temperature and moisture content both are low in summer.
- Temperature is high and humidity is low.

Use a K-map to find the simplest logic expression (both sum of products [minterm] and product of sums [maxterm]) involving variables S, M ,T, H for turning on the sprinkler system. Draw the logic circuit using only NAND gates.

Solution:

The given circumstances 1,2,3,4 and 5 are expressed in terms of the defined variables S,M,T and H as $\bar{M}\,\bar{S}, T\overline{M}S, THS, \overline{T}\,\overline{M}\,S$ and $T\overline{H}$, respectively.

The Boolean expression is

$$\bar{S}\,\overline{M} + S\overline{M}T + STH + S\overline{M}\,\overline{T} + T\overline{H}$$

= 0 0 X X + 1 0 1 X + 1 X 1 1 + 1 0 0 X + X X 1 0 **1**

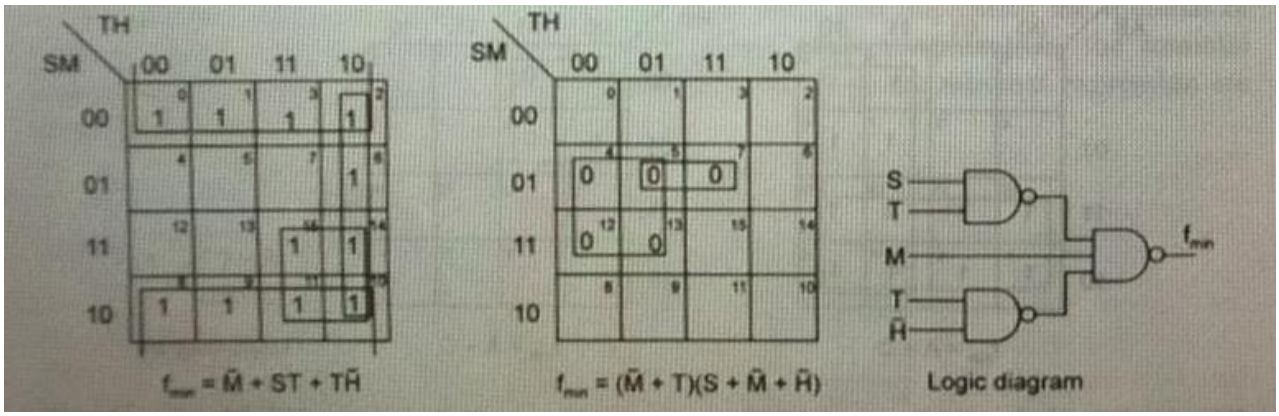
The expression in terms of minterms and maxterms are

$$\sum m\,(0, 1, 2, 3, 6, 8, 9, 10, 11, 14, 15)$$

$$\Pi\, M(4, 5, 7, 12, 13)$$

0.5

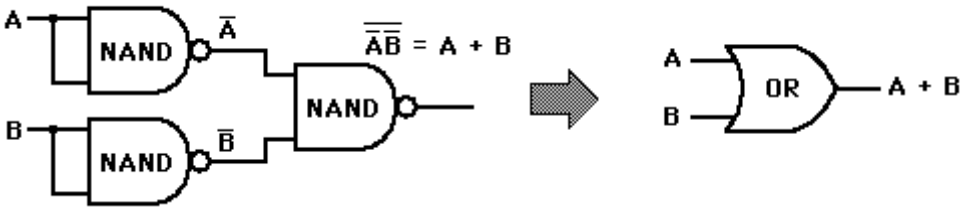
Both the SOP and POS forms give same minimum.



1.5

b) Implement an OR gate using NAND gates **[2]**

Solution:



NO partial credit

c) Solve the following problems: **[5]**

- Convert $(163.875)_{10}$ to binary
- Perform subtraction 100-110000 using 2's compliment method.
- Convert $(110101.101010)_2$ to octal.
- Convert $(3A9E.B0D)_{16}$ to binary.
- In what radix (base) number system will $\sqrt{41} = 5$?

Solution:

NO partial credit, 1 mark each

- $(163.875)_{10} = (10100011.111)_2$
- 100-110000 = 1010100
  Since there is no carry and MSB is 1, it's a negative number. Taking 2's compliment and putting a minus sign, we get -0101100 = -44
- $(110101.101010)_2 = (65.52)_8$
- $(3A9E.B0D)_{16} = (11101010011110.101100001101)_2$
- Radix will be 6

Q6) a) Implement a J-K latch using NAND gates. Write its truth-table and explain any issue with the J-K latch using timing diagram. Suggest any two solutions to solve the issue. **[2]**

Solution:
Circuit – 0.5 marks
Truth table – 0.5 marks
Race around condition using time diagram – 0.5 marks
Solutions (use edge triggered or master-slave) – 0.5 marks

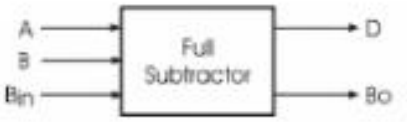
b) Implement a master-slave JK flip-flop using only NAND gates. Write its truth table and draw timing diagram showing at least 6 clock pulses. **[3]**

Solution:
Circuit – 1 mark
Truth table – 0.5 marks
Timing diagram – 1.5 marks

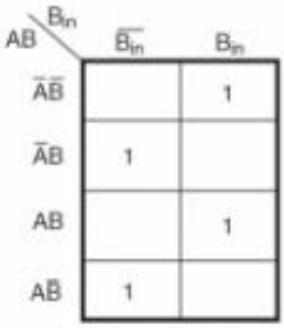
c) Implement a full subtractor using only 2-input NOR gates. **[3]**

Solution:

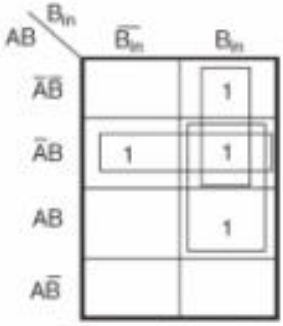
Minuend (A)	Subtrahend (B)	Borrow In (B_{in})	Difference (D)	Borrow Out (B_O)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



1



$$D = \overline{A}.\overline{B}.B_{in} + \overline{A}.B.\overline{B_{in}} + A.\overline{B}.\overline{B_{in}} + A.B.B_{in}$$

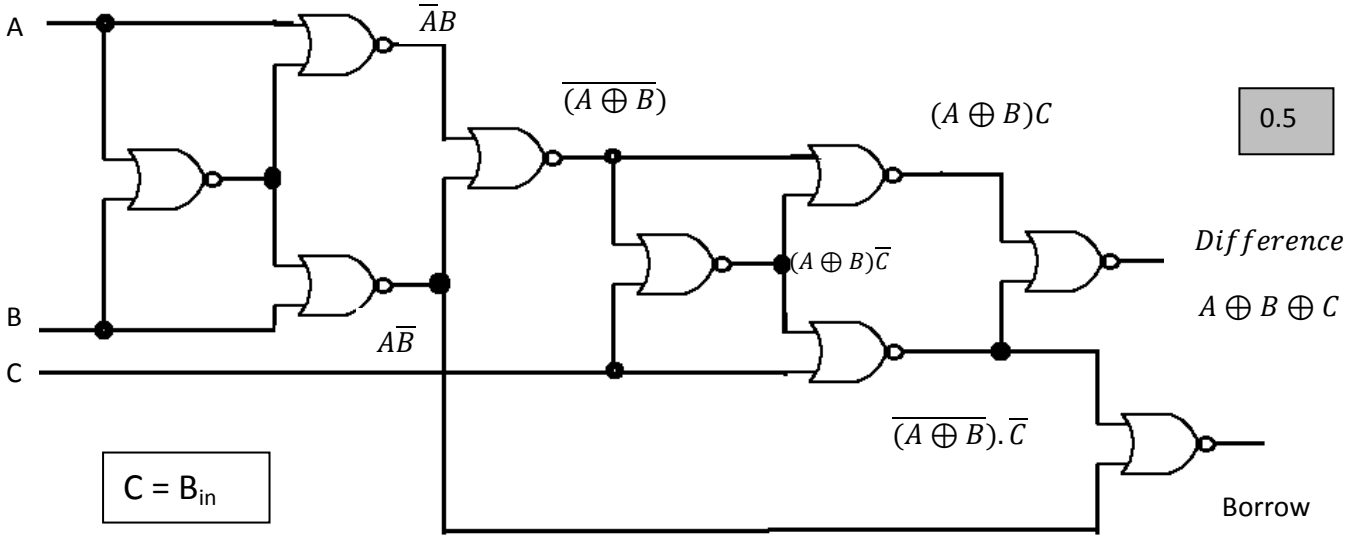


$$B_o = \overline{A}B + \overline{A}.B_{in} + B.B_{in}$$

1.5

Solving further for D :-

$$D = \left(A\overline{B} + \overline{A}B\right).\overline{B_{in}} + \left(\overline{A}B + AB\right).B_{in}$$
$$= (A \oplus B).\overline{B_{in}} + \left(\overline{A} + B\right)(A + \overline{B}).B_{in}$$
$$= (A \oplus B).\overline{B_{in}} + \left(\overline{A\overline{B}}\,.\,\overline{\overline{A}B}\right).B_{in}$$
$$= (A \oplus B).\overline{B_{in}} + \left(\overline{A\overline{B} + \overline{A}B}\right).B_{in}$$
$$= (A \oplus B).\overline{B_{in}} + \left(\overline{A \oplus B}\right).B_{in}$$
$$= (A \oplus B \oplus B_{in})$$



0.5

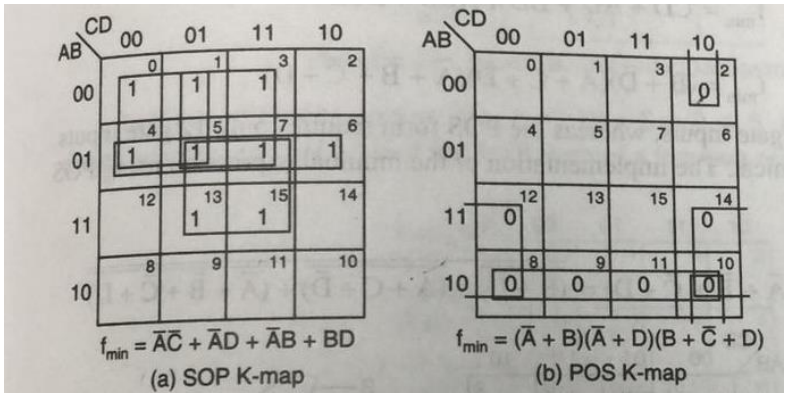
Note: Students who have cascaded 2 half subtractors will also get full credit provided only NOR gates are used.

d) For the expression f = Π M(2,8,9,10,11,12,14), implement the minimal (reduced) expression using only NOR gates. **[2]**

Solution:

The given expression in the SOP form is f = ∑ m (0,1,3,4,5,6,7,13,15).

K-map for SOP form, POS form, their reductions and reduced expressions are shown below :



1

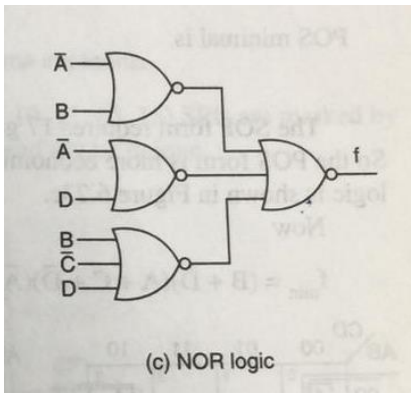
It is more economical to implement POS form, which use 10 NOR gates, over SOP form (uses 12 NOR gates).

Reduced POS expression:

$$f_{min} = (\bar{A} + B)(\bar{A} + D)(B + \bar{C} + D) = \overline{\overline{(\bar{A} + B)} + \overline{(\bar{A} + D)} + \overline{(B + \bar{C} + D)}}$$

0.5

NOR gate implementation:



(c) NOR logic

0.5

END