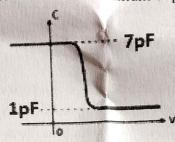
The LNM Institute of Information Technology, Jaipur

Department of Electronics and Communication Engineering Modeling and Simulation of MOS Transistor (ECE4181)

End Term

		Maximum	
Time:	180 Minutes Date: 5/12	2/2019	the
	ctions: All the Questions are Compulsory. Please paper, consisting of 2 printed pages.	had that there must be 5 questions if	1 the
Instru	ctions: All the Questions are Compulsory. Please	check that	
	paper, consisting of 2 printed pages.		
01.0)	Draw and explain the MOS structure		[1]
Q.1: a)	i Three-terminal MOS structure in flat-hand Co	ondition, with $V_{CB} = 0$.	[1]
			[1]
	iii. The structure of (ii) with a positive V_{CB} , wh	ich reduces electron concentration	1-9
			[1]
	iv. The structure of (iii) with further increase	sed V _{GB} , which restores electron	
	concentration at the curtage to the level in (1)		[2]
	v. Plot the conduction energy band edge vs	horizontal position along a fine	121
	adjacent to the surface for the situation (i)	(1) (111) and (1V).	[1+1+1+1]
b)	For a three terminal MOS structure plot	various quantities given belog.	
	characterizing the structure vs Vcp and VG	c. (a) Surface potential, (a)	
	conscitonce to the rest of the structure per unit a	rea: (c) logarium of myordion	
	abarga magnitude per unit area: (d) inversion la	ver charge magintude per unit all	
	Plot for Von=0 and for a Von of a given positi	ve value. Where VCB is the voltage	
	source between the n+ region (added to the bas	ic MOS two terminal structure) and	
	substrate region.		[2]
Q.2: a)	Explain Body effect in MOSFET.	f voltage in a MOSFET with body	[2]
b)	Explain and find the expression for pinch of	voltage in a wost E1 with 3023	[2]
	effect. Draw the inversion layer charge vs V _{CB} (chann	el to body hias) for different gate to	
c)		of to body blus for different game	
	body voltage. Calculate the change in threshold voltage due to	to an applied source to body voltage	[4]
d)	Calculate the change in threshold voltage due $V_{CB}=1$ V. Consider an n-channel silicon MC	OSEFT at $T = 300 \text{ K}$ Assume the	
	$V_{CB}=1$ V. Consider an n-chainlet smooth WC substrate is doped to $N_a=3 \times 10^{16}$ cm ⁻³ and assistance.	ume the oxide is silicon dioxide with	
	substrate is doped to Na= 3 x 10 cm and assi	unic the oxide is smoon diomide with	
	a thickness of t_{ox} = 500 Angstrom. [Assume n_i =1.5 x 10 ¹⁰ cm ⁻³ , the relative p	permittivities of Si and SiOn are 11.7	
	[Assume $n_i=1.5 \times 10^{10} \text{ cm}^3$, the relative r_i	/cml	
	and 3.9 respectively and $\varepsilon_0 = 8.85 \times 10^{-14} \text{ F}$	Cin	
	· MOCCET	2 Darius and find the expression for	[1+3]
Q.3: a)	Why velocity saturation occurs in MOSFET	Derive and tind the expression for	
	: 1logity caturation		「フエフブ
b)	Briefly describes channel-length modulation	and now it affects wides to the	
	voltage characteristics.		[2]
c)	Write short notes on Hot carrier effects in a	Short channel MOSFET	

a) The figure shows the high frequency capacitance-voltage (C-V) characteristics of Q.4: [2+2] MOS capacitor having an area of 1x10⁻⁴ cm². Assume that the permittivity of Silicon and SiO₂ are 1x10⁻¹² and 3.5 x 10⁻¹³ F/cm respectively. Find the gate oxide thickness in the MOS capacitor. Find the maximum depletion width in Silicon.



b) Briefly explain about different oxide-semiconductor interface charges in a MOS capacitor.

[1+1+1+1]

c) Calculate the flat-band voltage for an MOS capacitor with a p-type semiconductor substrate.

[2]

- Consider an MOS structure with a p-type semiconductor substrate doped to $N_a=10^{16}$ cm⁻³, a silicon dioxide insulator with a thickness of $t_{ox}=500$ Angstrom and an n+ polysilicon gate. Given interface trapped Charge $Q_0=10^{11}$ electronic charges per cm². Assume ϵ_{ox} = 3.9 for SiO₂, work function difference ϕ_{ms} = -1.1V.
- Consider a uniformly doped GaAs pn junction at T= 300 K. The junction capacitance at zero bias is C_J (0) and the junction capacitance with a 10 V reverse Q.5: a) bias voltage is C_J (10). The ratio of the capacitance is $C_J(0) / C_J(10) = 3.13$

[3]

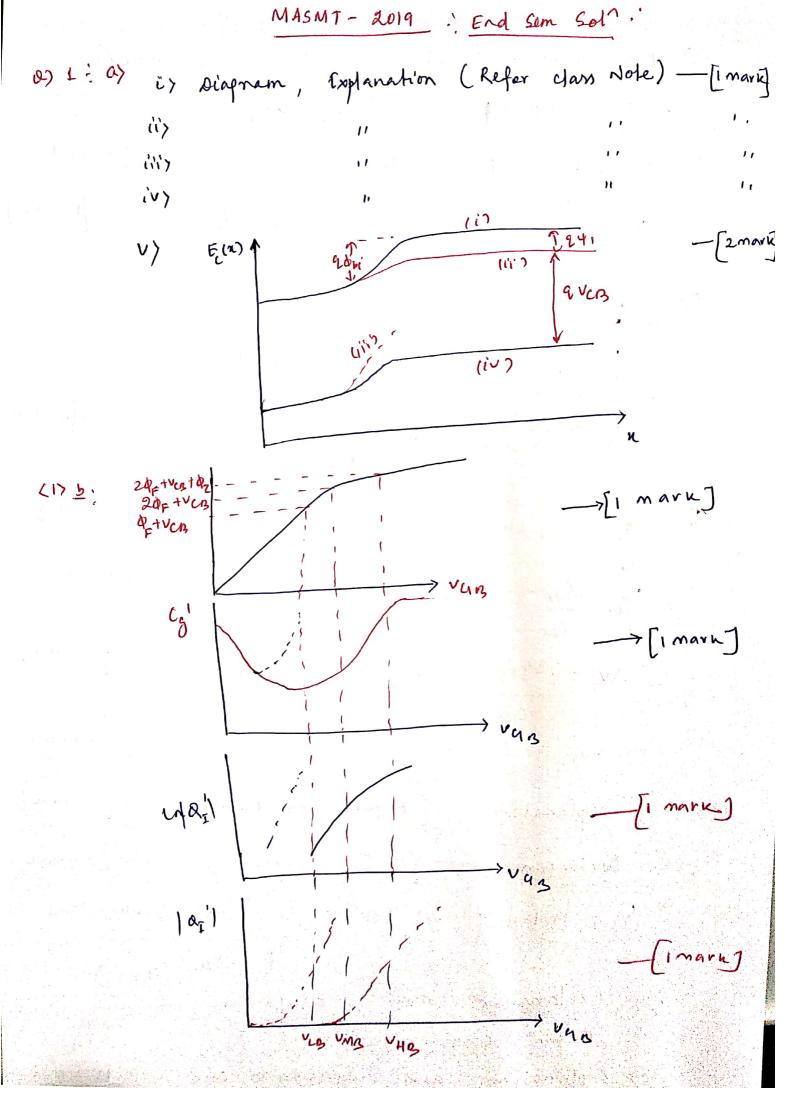
Also under reverse bias, the space charge width in to the p region is 0.2 of the total space charge width. Determine Built in potential (V_{bi}) and find N_d/N_a .

Why Punch through occurs in MOSFET and what is its effect on drain current b)

[3]

Explain the concept of drain induced barrier lowering in a short channel device. c)

[4]



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0)2: a) Dingram, Explanation _____ [2 maru] VCB↑, > \Q_[] \$ for fixed Uqc by Explanation (Refer class Note) — [mark] Vp = (-1/2 + / 1/4 + V4g - VFB) - Po V 431 < V432 < V43, -> (2m u/K) $P_{FP} = v_t \ln \left(\frac{Na}{Ni} \right) = 0.376 V$ $Cox = \frac{c_{ox}}{t_{ox}} = 6.9 \times 10^{8} \text{ F/cm}^{2}$ $\Delta v_{T} = \sqrt{29 \varepsilon_{S} N_{a}} \left[\sqrt{29 \rho} + v_{SB} - \sqrt{29 \rho} \right] - \left[1 \text{ mark} \right]$ 4U1 = 0.66V ______[1 maru] a) 3: a> Explanation - [Refer class Note] -[mark] Derivotin — [3 mark] IDEN including vel. Sat = IDEN, not Counting Usat by Explanation and diagram (4 morns)

Refer class Now.

C) Explanation and diagram and Effects - Company

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6)
$$1 = \frac{1}{(a) - C_{0x}} = \frac{C_{max}}{t_{0x}} = \frac{E_{0x}}{t_{0x}} = 7 PF$$

=) $\frac{3 \cdot 5}{t_{0x}} \times \frac{10^{13}}{t_{0x}} = \frac{7}{4} PF$

=) $\frac{1}{C_{min}} = \frac{1}{C_{0x}} + \frac{1}{C_{dep}}$

=) $\frac{1}{11PF} = \frac{1}{7} + \frac{1}{11PF}$

=) $\frac{1}{11PF} = \frac{1}{7} + \frac{1}{$

5) a.
$$\frac{C_{j}(0)}{C_{j}(0)} = 3.13 = \left(\frac{V_{bi} + V_{R}}{V_{bi}}\right)^{1/2}$$

for $V_{R} = 10V$, M_{R} find

$$(3.13)^{2}V_{bi} = V_{bi} + 10$$

$$=) V_{bi} = 1.14V$$

$$\frac{X_{P}}{X_{P}} = 0.2 M = 0.2(X_{A} + X_{P})$$

$$\frac{X_{P}}{X_{P}} = 0.25 = \frac{N_{d}}{N_{A}}$$

$$\frac{X_{P}}{X_{P}} = 0.25 = \frac{N$$