Packet based commnuication

BIDIRECTIONAL LVDS

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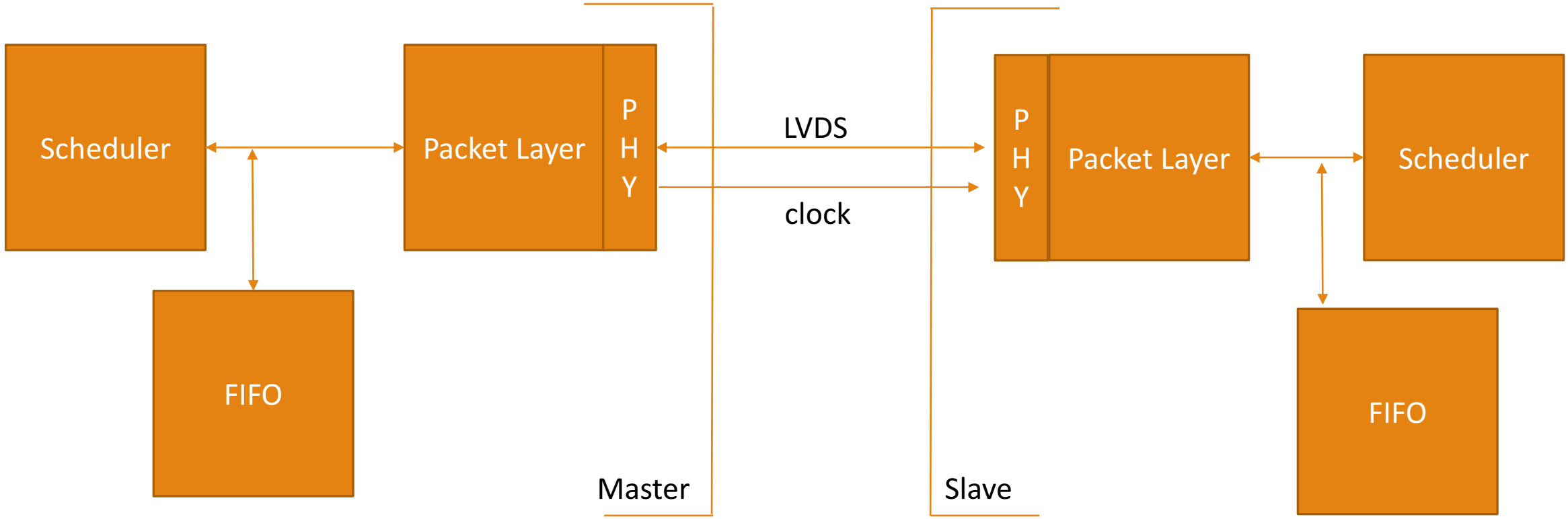
Aim

Aim of the project is to design a packet based bidirectional protocol over single LVDS link that can fully utilize the available band width based on priority based task scheduling.

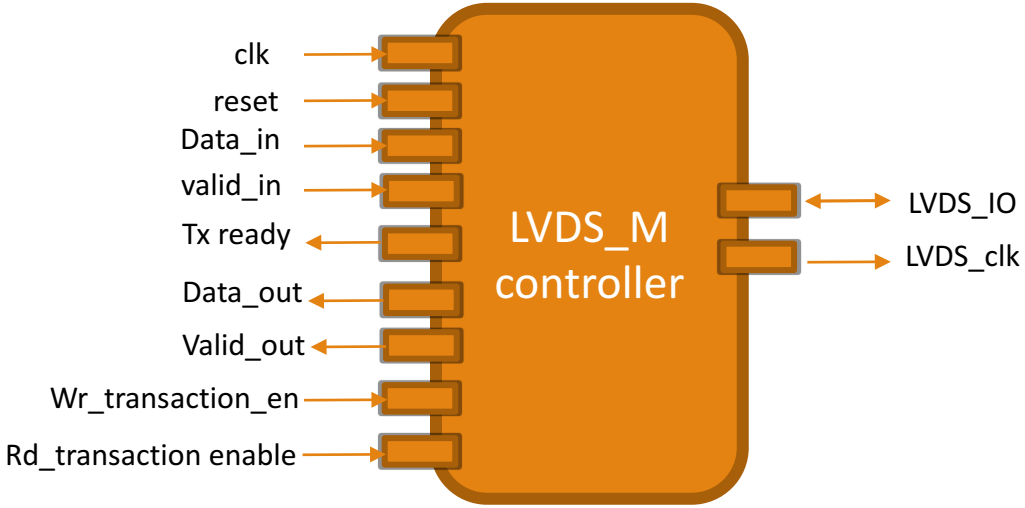
RTL structure



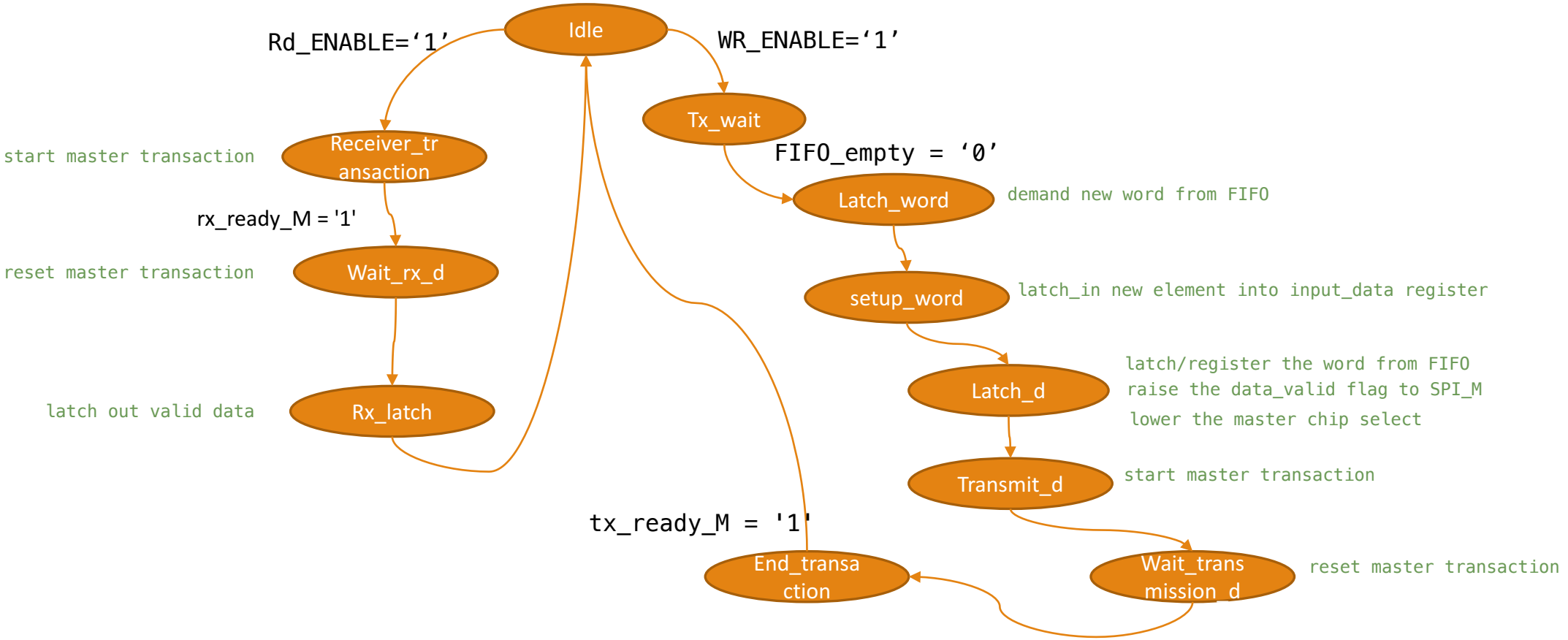
RTL structure

- The scheduler accepts user commands including address as well as bursts size. Based on the priority of the service, a specific FIFO is used to store the data of corresponding service (address).
- The scheduler then redirects specific command as well as FIFO link to the packet layer which parses the command to generate the required packets. First packet transferred over the LVDS link is command packet which specifies IO address as well as burst size. Then based on the command either data is written to the LVDS link or is read from it. The schedulers on both the master as well as slave sides ensures that there is no bus contention.
- The physical layer acts as bidirectional SERDES. The master PHY produces both clock and data while slave PHY produces/receives data on the clock provided by master.

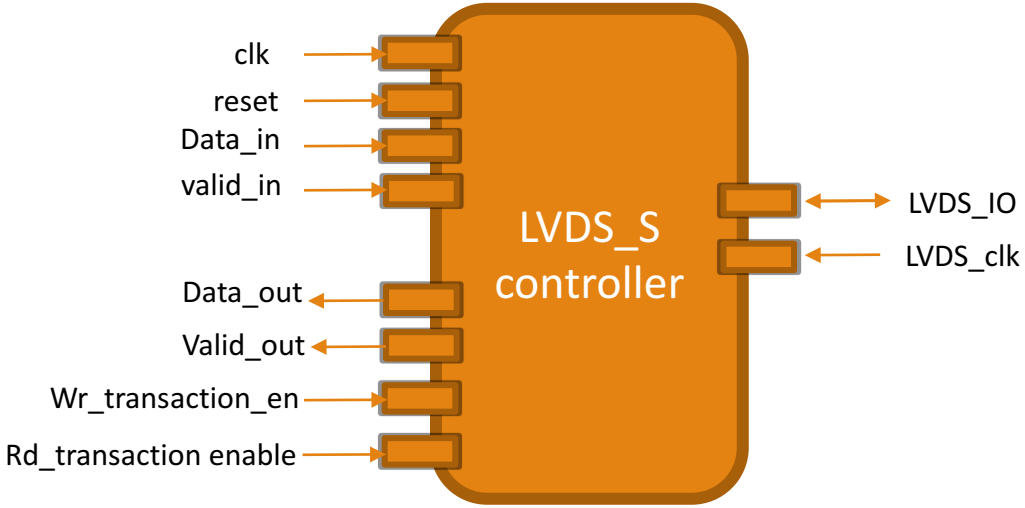
Master LVDS-PHY SERDES



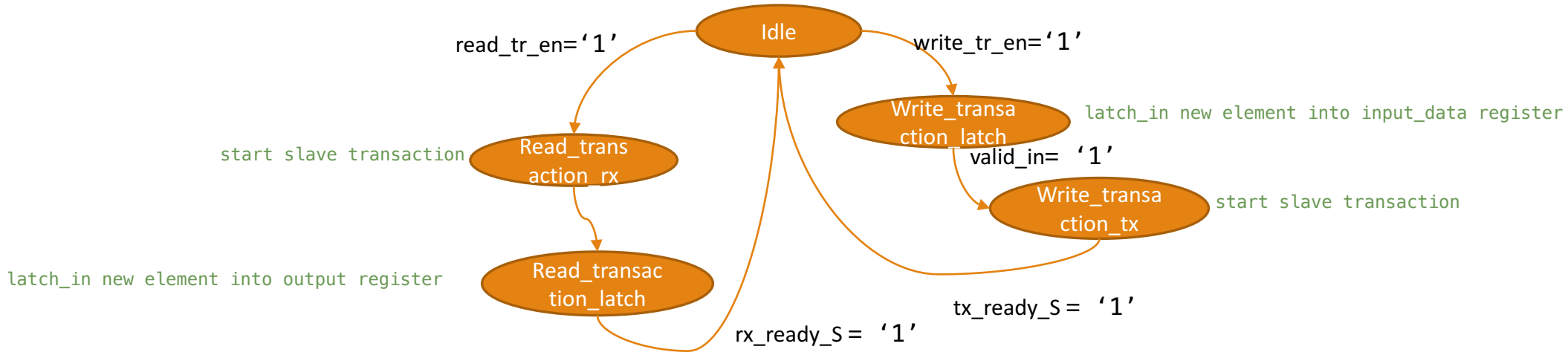
Master LVDS-PHY SERDES

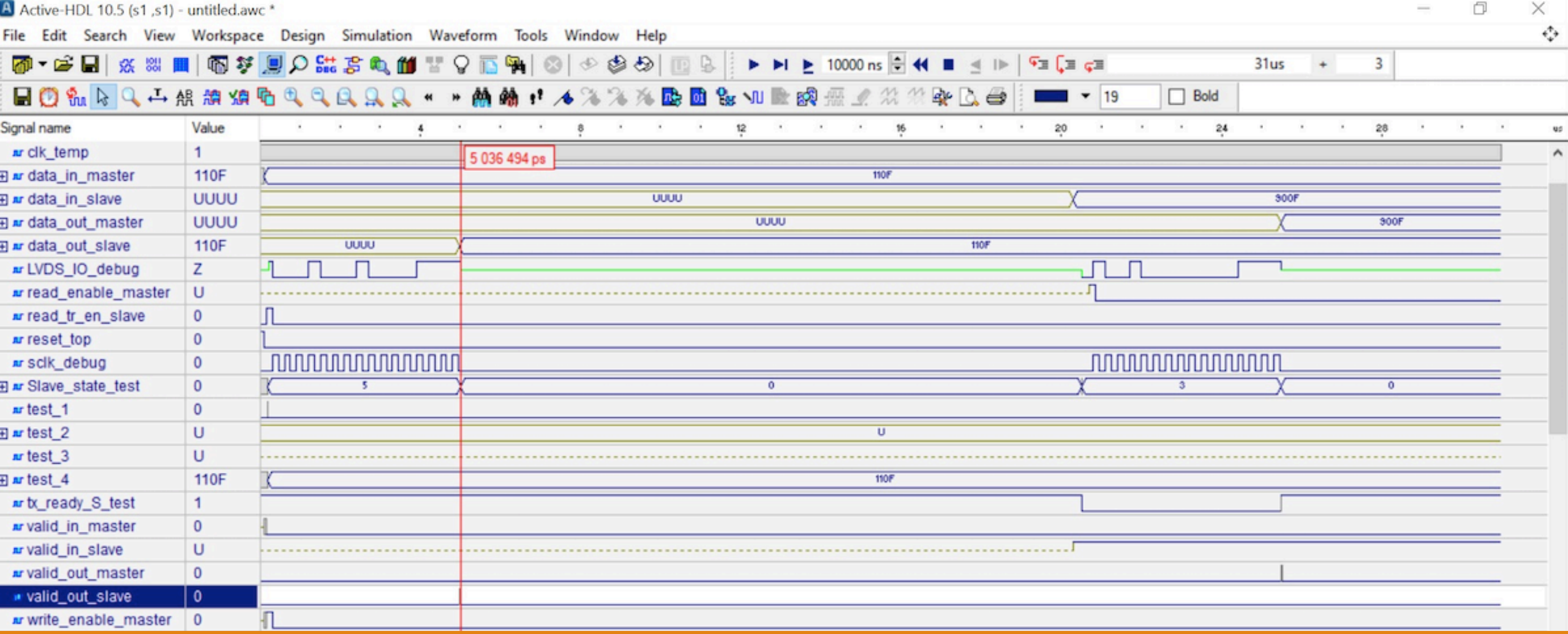


Slave LVDS-PHY SERDES



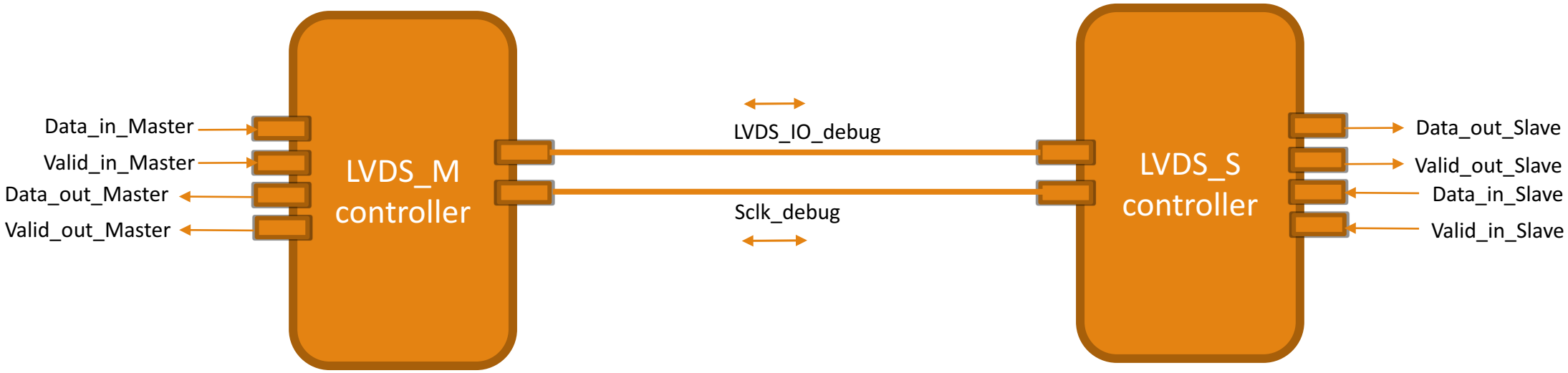
Slave LVDS-PHY SERDES



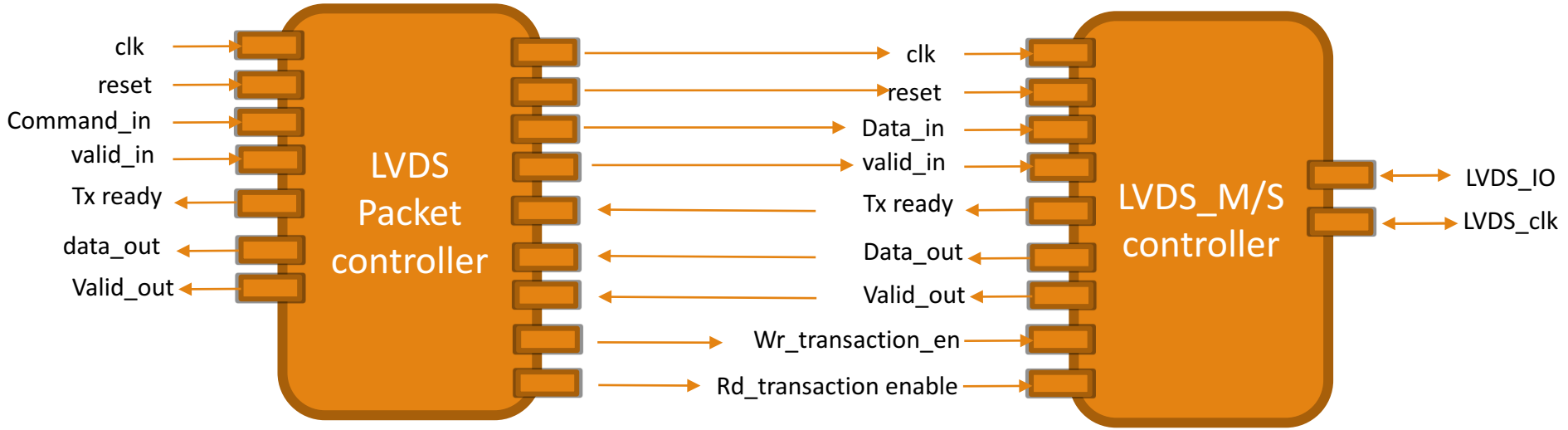


VHDL Test Simulations

VHDL Testbench

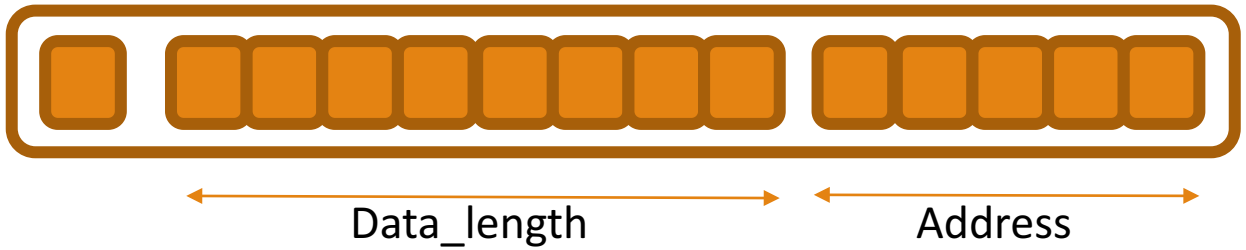


Packet layer master/slave



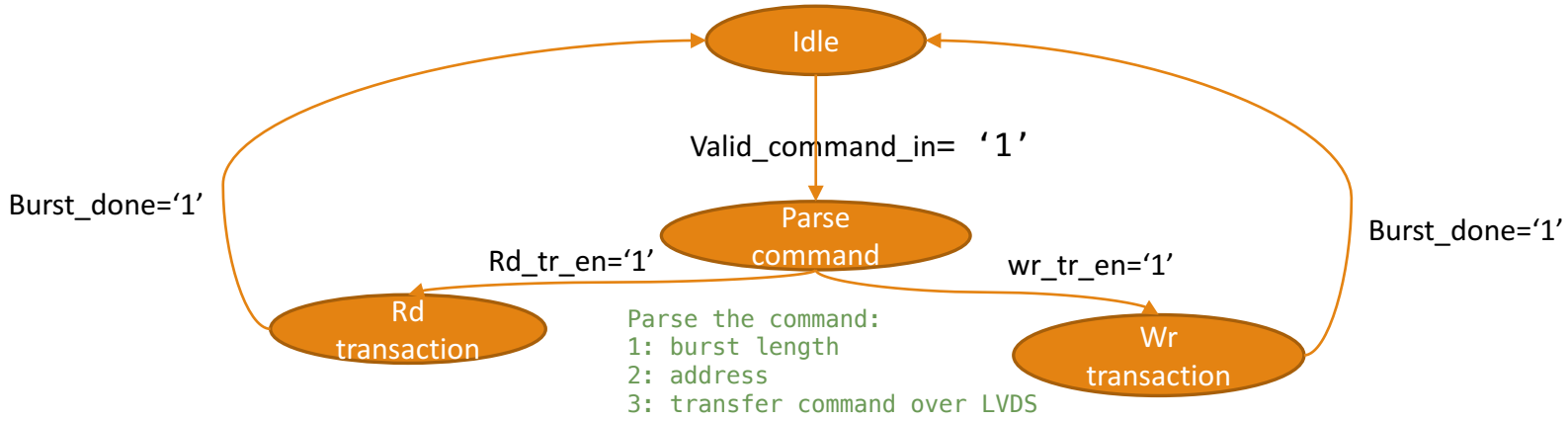
Command_layout (vector- 21 bits)

Read/write command



Example: read x bytes from 0xaabb
write x bytes to 0xaabb

Packet controller FSM



Deliverables first evaluation

- LVDS PHY implementation
- Packet layer implementation
- Testbench validation
- SPI based transaction establishment via the designed LVDS link. (testbench)