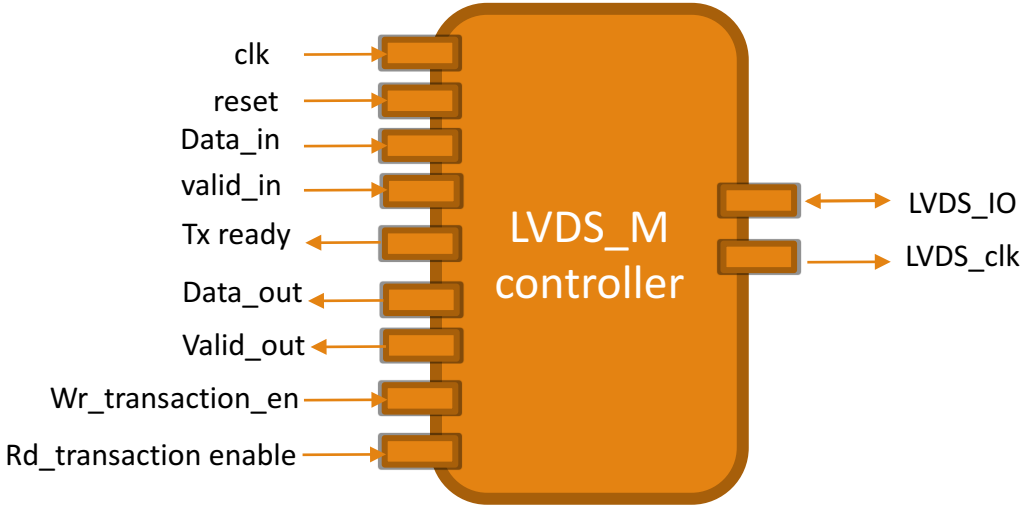
Physical Layer Design

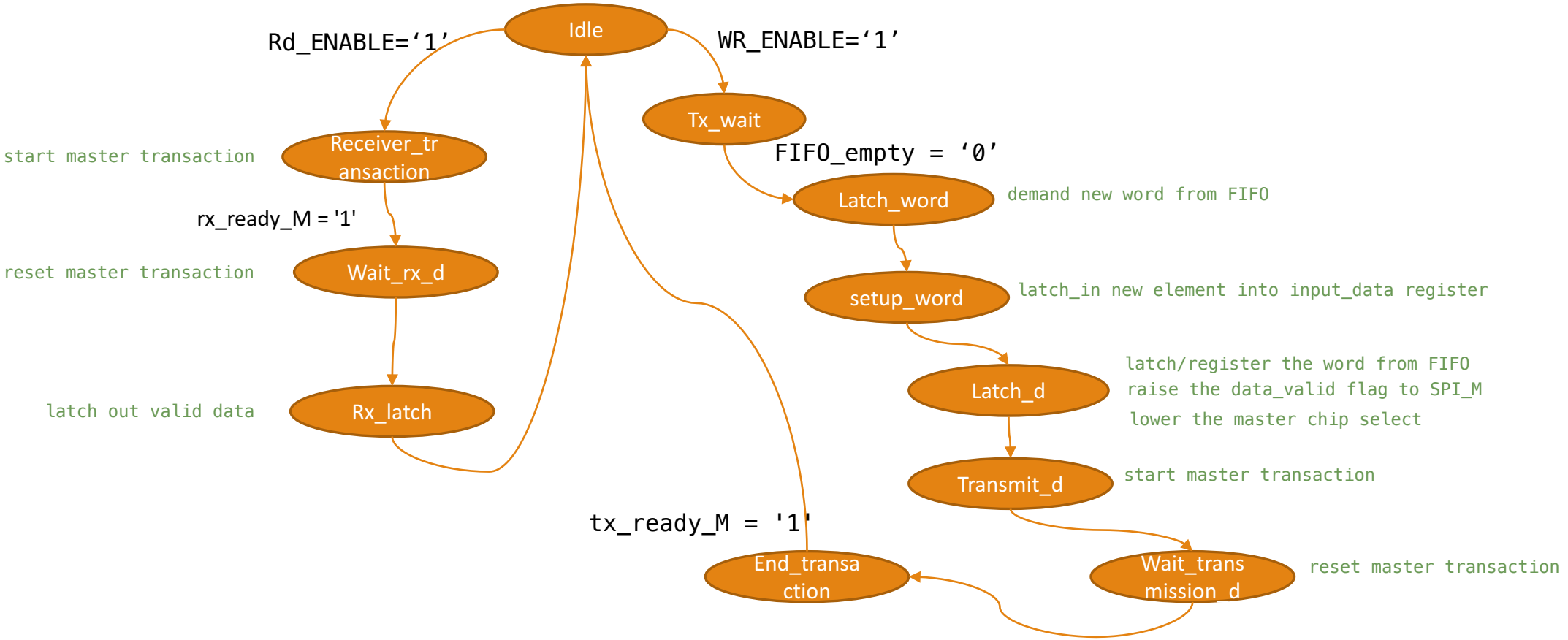
BIDIRECTIONAL LVDS

APOORVA ARORA

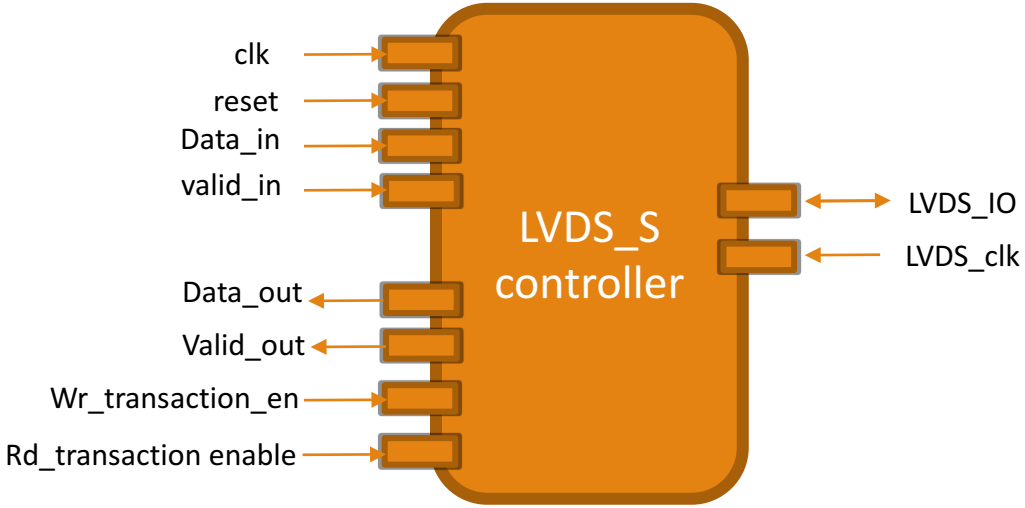
Master LVDS-PHY SERDES



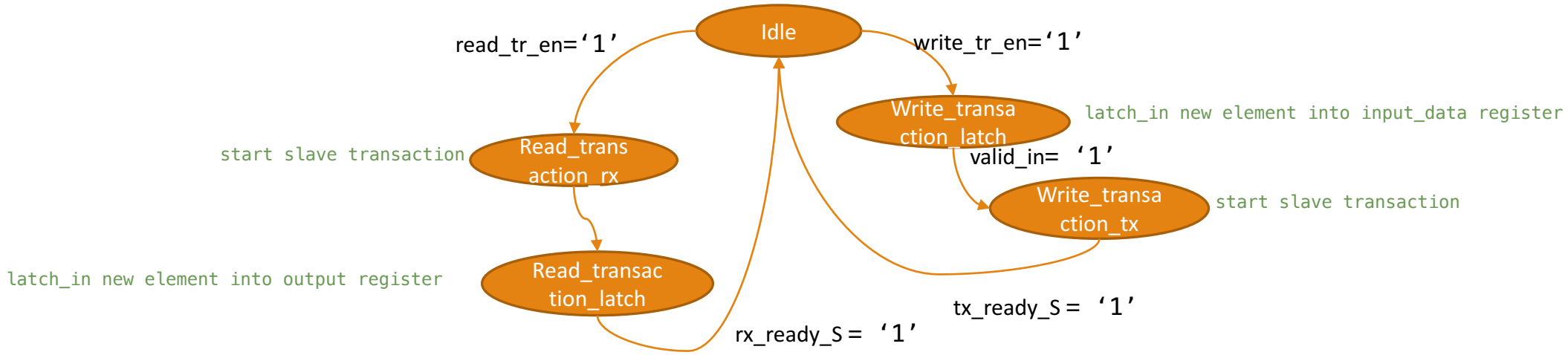
Master LVDS-PHY SERDES

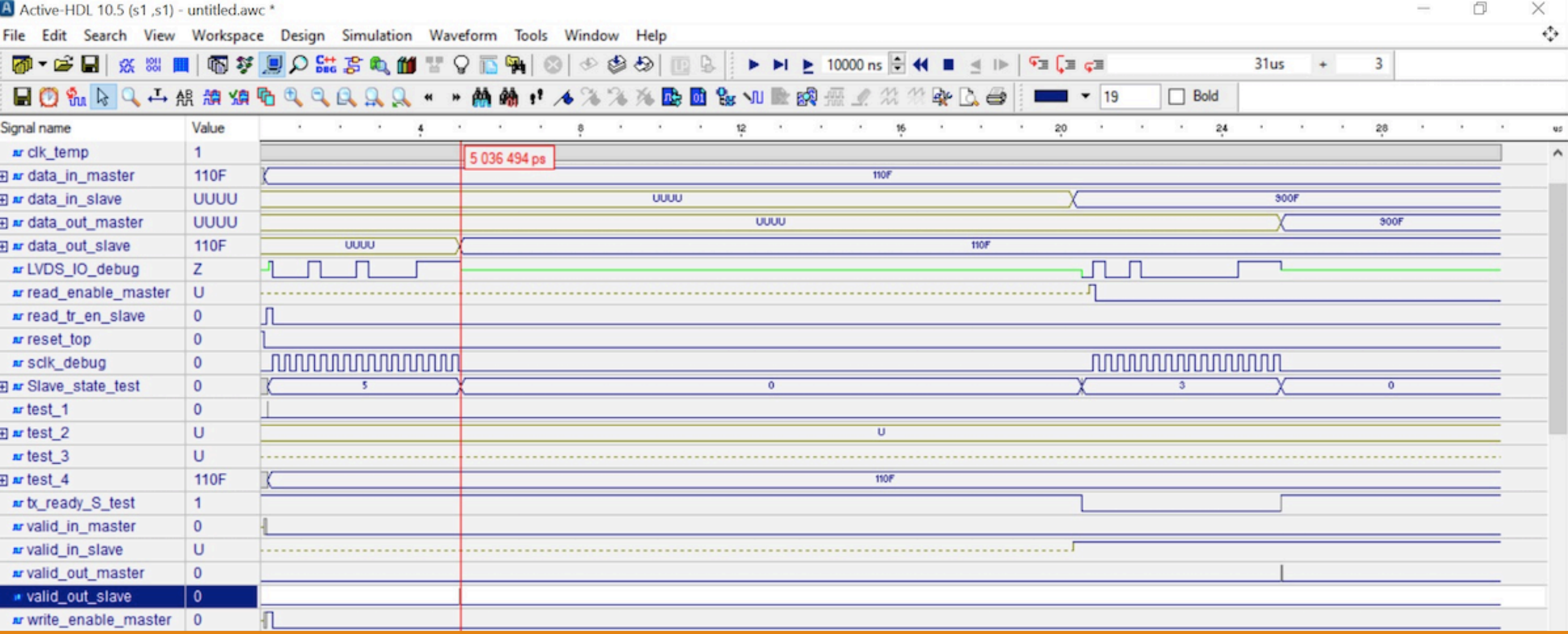


Slave LVDS-PHY SERDES



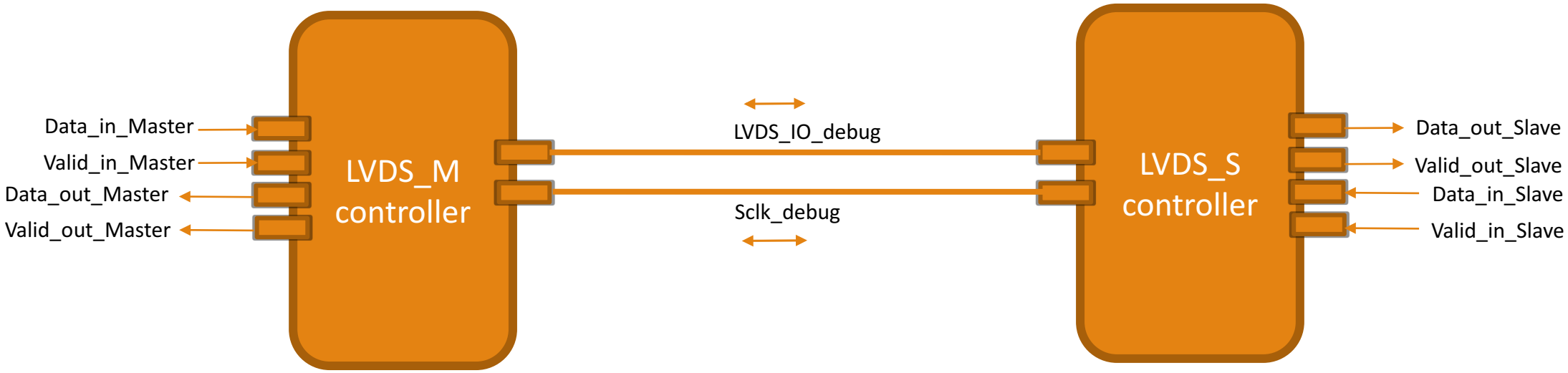
Slave LVDS-PHY SERDES



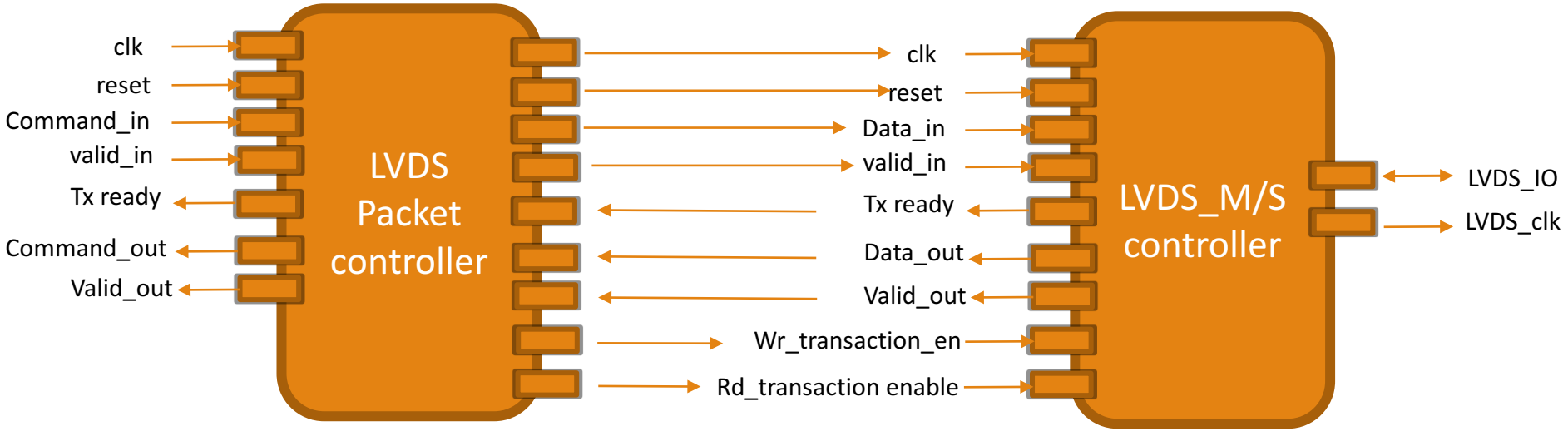


VHDL Test Simulations

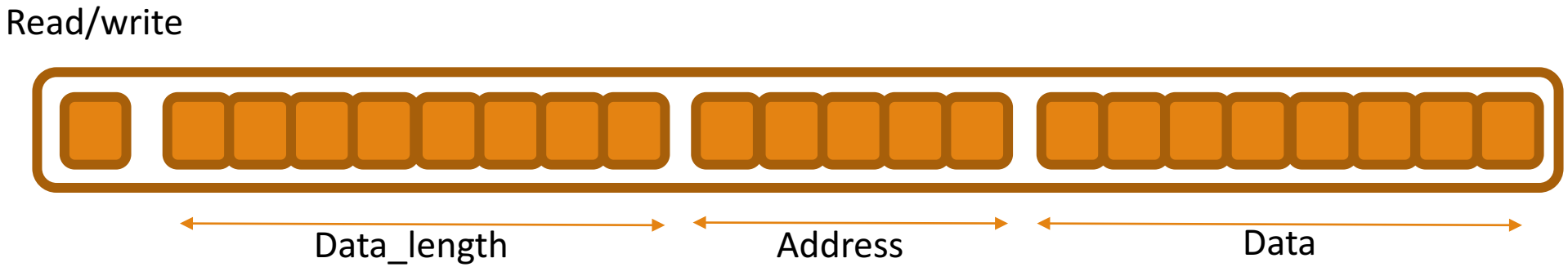
VHDL Testbench



Packet layer



Command_layout (vector- 21 bits)



Packet controller FSM write channel