Indian Institute of Technology, Bhubaneswar
School of Electrical Sciences
Digital Electronic Circuits (EC2L004)

Date: March 1, 2023

Spring Mid-Semester Examination 2023

Time: 2 hours Maximum Marks:60

Instructions

1. This question paper contains 10 questions and 4 printed pages. Answer all the questions.
2. Draw the truth tables, and logic diagrams as clearly as possible.
3. If you make any assumptions, mention them clearly.
4. Be precise and answer to the point. "Keep it short, and simple".

Wish you all the best

1. Simplify the following Boolean functions by first finding the essential prime implicants. Supplement sheet contains the *Karnaugh* maps, use them.
   (a) $F_1(w,x,y,z) = \Sigma(0,1,4,5,6,7,9,11,14,15)$ [2]
   (b) $F_2(A,B,C,D) = \Sigma(0,1,3,7,8,9,10,13,15)$ [2]
   (c) $F_3(w,x,y,z) = \Sigma(0,1,2,4,5,6,7,10,15)$ [2]
2. Simplify the Boolean function [6]
   $f(A,B,C,D) = \Sigma m(1,3,4,5,10,12,13,15)$ using Quine-McCluskey method. Use the supplement sheet to solve this question, it will save your time.
3. Construct the adder for 2-digit decimal numbers represented in BCD code. Use 4-bit binary adders as building blocks and logic gates. Draw the circuit schematic. [6]
4. Consider an 8-bit ripple-carry adder built using eight full-adders. Each full adder is built using a two-level sum-of-products circuit for the carry-out and a 3-input XOR gate for the sum. In this adder assume that the

Question 4 continues on the next page...

delay through a gate is:

Gate delay $= 1 + 0.1 \times$(#Inputs-1) ns,
where # Inputs is the number of inputs to the gate.

Using this equation, the delay through an inverter is equal to 1 ns, the delay through a 2-input gate (any type) is 1.1 ns, and so on.

(a) What is the critical path delay in the ripple-carry adder? (Recall: the critical path is the longest (slowest) path in the circuit.) Give your answer in ns. [2]

(b) Consider next a carry lookahead adder, as discussed in class. If you can use gates of any size (number of inputs), what is the critical path delay in the 8-bit carry lookahead adder? [2]

(c) Now assume that you can use gates with a fanin of no more than four inputs. What is the critical path delay for the carry lookahead adder in this case? [2]

5. Design a four-bit combinational 2's complementer circuit. (The output generates the 2's complement of the input binary number.) Show that the circuit can be constructed with exclusive-OR gates. Can you predict what the output functions are for a five-bit 2's complementer? Supplement sheet contains the truth-table and Karnaugh maps, please use them. [6]

6. (a) If the data-select inputs to the multiplexer in Figure 1(a) are sequenced as shown by the wave-forms in Figure 1(b), determine the output waveform with the following data inputs: $D_0 = 0, D_1 = 1, D_2 = 1, D_3 = 0$. [2]

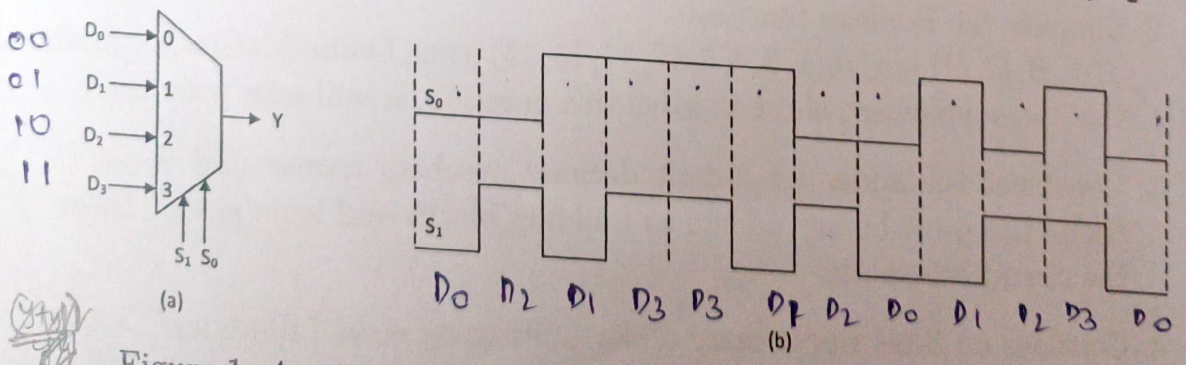


Figure 1: 4×1 multiplexer and timing diagram of its select signals.

Question 6 continues on the next page...

(b) Sketch the output of D-Latch and D-Flip-Flop if the following "D"and "Clk" inputs shown in Figure 2 are applied to "D"and "En/Clk"pins of the latch and flip-flop. Please consider the latch as positive-level sensitive latch and the flip-flop as positive-edge triggered flip-flop. [2]

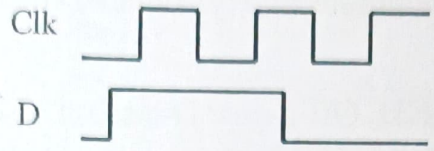


Figure 2: Input waveforms for both D-Latch and D-Flip-Flop.

7. Implement the function [4]

$$f(w_1, w_2, w_3, w_4, w_5) = w_1'w_2'w_4'w_5' + w_1w_2 + w_1w_3 + w_1w_4 + w_3w_4w_5$$

by using a 4×1 multiplexer and as few other gates as possible. Assume that only the uncomplemented inputs w_1, w_2, w_3, w_4, and w_5 are available.

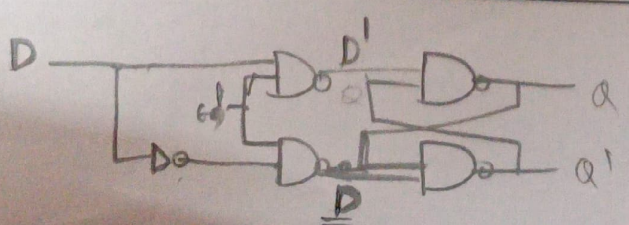
8. This question is about building a digital circuit that will add three 4-bit numbers, X, Y, and Z. The individual bits of these three numbers will be represented as X_i, Y_i, and Z_i. To illustrate this clearly, the addition of three 4-bit numbers would be written on papers as follows:
Recall the design of a Full Adder (FA) building block described in class

	x_3	x_2	x_1	x_0
+	y_3	y_2	y_1	y_0
+	z_3	z_2	z_1	z_0
s_5	s_4	s_3	s_2	s_1	s_0

which is used as a building block to create an adder that adds two N-bit numbers. You will design the complete circuit in two steps, part (a) and (b) below.

(a) Using only FA building blocks give the design of a new building block that performs the function needed to implement the box surrounding x_2, y_2, z_2, and s_2, (shown above). You will call this building block TNFA and use it in part (b) below. It computes the sum bit S_i, corresponding to the three inputs X_i, Y_i, and Z_i and any other inputs and outputs that are necessary in the context of the full adder. [4]

Question 8 continues on the next page...



(b) Using the building block of part (a), the TNFA, and any other logic gates you deem necessary give the design of the three 4-bit number adder (which produces a 6-bit sum, $s_5 \ldots s_0$). Your answer should show all the inputs (i.e. all X_i, Y_i and Z_i, $i = 0 \ldots 3$ and any carry inputs) and outputs necessary to make the complete adder function correctly. [4]

9. Implement NOT, AND, OR gates, D-latch, D-Flip-Flop using only 2×1 multiplexers. Please consider a positive-level sensitive latch and positive-edge triggered flip-flop while implementing. [4]

10. Design a combinational circuit whose input A is a vector of 7-bits and its output Z is a 3-bit vector which counts the number of "1"s present in the input. For instance, $A = 1001001$ or $A = 1010100$ both will results in $Z = 011$, indicating that both input vectors have three numbers of "1"s. *Please note that you have to use only full-adders while building this circuit.* [10]