2023 Digital IC Design Homework 3

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| --- | --- | --- | --- | --- | --- |
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| **Simulation Result** | | | | | |
| Functional simulation | | 23 | | Gate-level simulation | Score |
|  | | | | (your gate-level sim result) | |
| **Synthesis Result** | | | | | |
| Total logic elements | | |  | | |
| Total memory bits | | |  | | |
| Embedded multiplier 9-bit elements | | |  | | |
| Total cycle used | | |  | | |
| Clock width | | |  | | |
| (your flow summary) | | | | | |
| **Description of your design** | | | | | |
| 分成三個always區塊寫成FSM形式。 | | | | | |

*Scoring = Area cost \* Timing cost*

*Area cost = Total logic elements + Total memory bits + 9\*Embedded multipliers 9-bit elements*

*Timing cost = Total cycle used \* Clock width*

**\* Total logic elements must not exceed 1500.**