2024 Digital IC Design

Homework 3: matrix multiplier

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| **Simulation Result** | | | | | | | | | |
| Functional simulation | 100 | | Gate-level simulation | 100 | Clock  width | | 25(ns) | Gate-level simulation time | 177275 (ns) |
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| **Synthesis Result** | | | | | | | | | |
| Total logic elements | | | | | | 912/55856 | | | |
| Total memory bit | | | | | | 0/2396160 | | | |
| Embedded multiplier 9-bit element | | | | | | 1/308 | | | |
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| **Description of your design** | | | | | | | | | |
| FSM有五個狀態：DATA\_IN1, DATA\_IN2, MULTIPLY, OUT, WAIT。DATA\_IN1讀取in\_data，將第一個矩陣存入mat1，size1會儲存矩陣的行列大小；DATA\_IN2讀取in\_data，將第二個矩陣存入mat2，size2會儲存矩陣的行列大小，並在讀完所有值之後(也就是row\_end訊號為1)將busy設為1；MULTIPLY會先判斷是否能執行矩陣乘法，如果可以的話運算輸出矩陣的值，因為Verilog使用迴圈通常會消耗大量硬體資源，所以使用x,y,z三個counter運算，當矩陣不能運算或者運算完成時，done設為1；OUT將valid設為1，輸出運算過後矩陣的值；WAIT將所有變數的值初始化為0。當row\_end訊號為1時，DATA\_IN1和DATA\_IN2會進入到下一個狀態，當done為1時，MULTIPLY會進入到OUT，當運算過後矩陣的所有值全部輸出之後或者is\_legal為0時，OUT會進入到WAIT，WAIT在下一個cycle就會進入到DATA\_IN1。 | | | | | | | | | |

*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (Total cycle used\*clock width)*